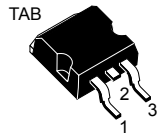
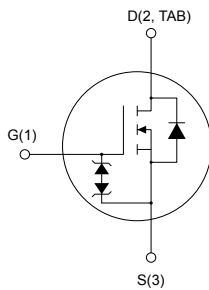


N-channel 600 V, 0.108 Ω typ., 26 A MDmesh M2 Power MOSFET in a D²PAK package


D²PAK


AM01476v1_tab


Product status link
[STB33N60M2](#)
Product summary

Order code	STB33N60M2
Marking	33N60M2
Package	D ² PAK
Packing	Tape and reel

Features

Order code	V_{DS} @ T_J max.	$R_{DS(on)}$ max.	I_D
STB33N60M2	650 V	0.125 Ω	26 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters, resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	26	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	16	A
$I_{DM}^{(1)}$	Drain current (pulsed)	104	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		

- Pulse width is limited by safe operating area.
- $I_{SD} \leq 26\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
- $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.66	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^{\circ}\text{C}/\text{W}$

- When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	450	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 13\text{ A}$		0.108	0.125	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1781	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{rss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	135	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	5.2	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 26\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	45.5	-	nC
Q_{gs}	Gate-source charge		-	9.9	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 13\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	16	-	ns
t_r	Rise time		-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	109	-	ns
t_f	Fall time		-	9	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		26	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		104	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 26\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	375		ns
Q_{rr}	Reverse recovery charge		-	5.6		μC
I_{RRM}	Reverse recovery current		-	30		A
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	478		ns
Q_{rr}	Reverse recovery charge		-	7.7		μC
I_{RRM}	Reverse recovery current		-	32.5		A

1. Pulse width is limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

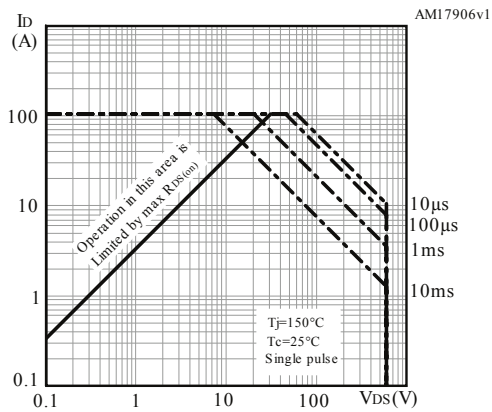
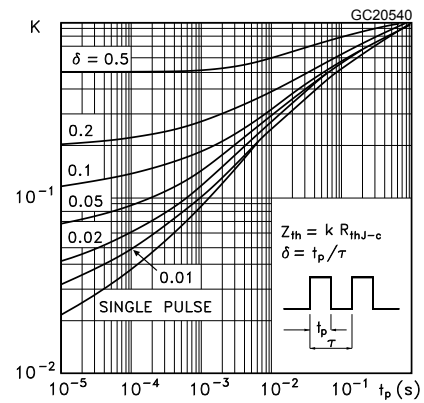
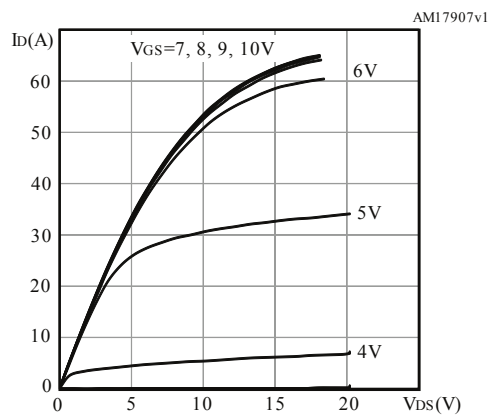
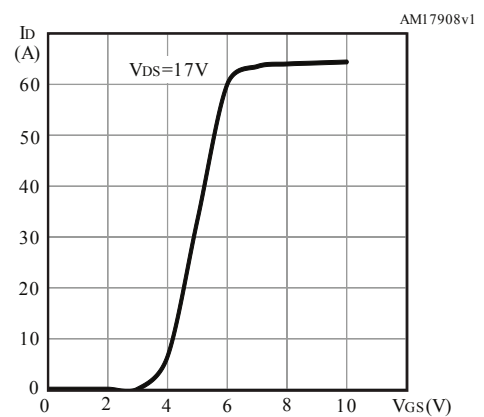
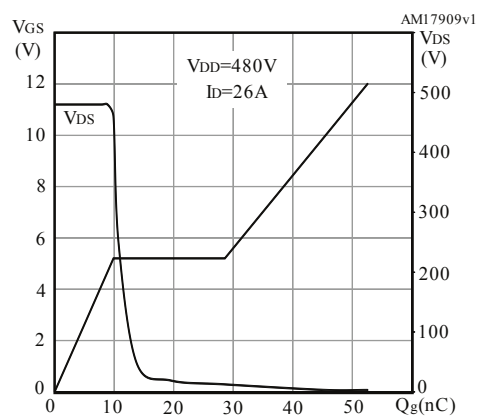
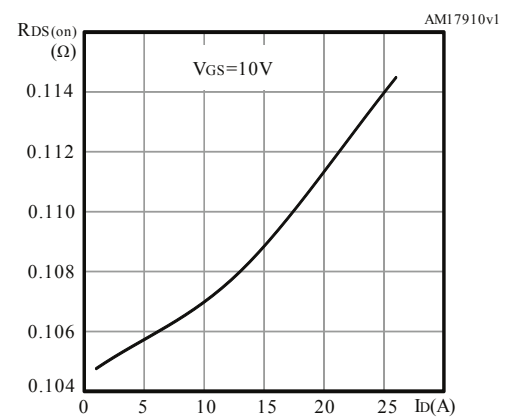
Figure 1. Safe operating area

Figure 2. Normalized thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


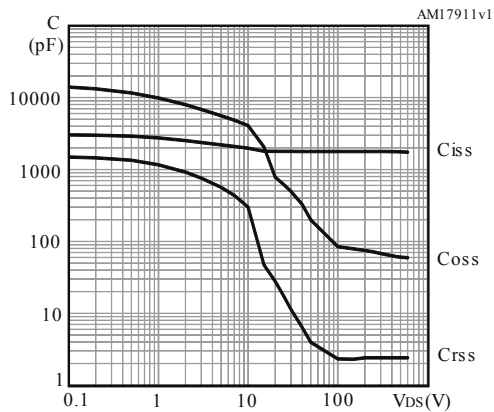
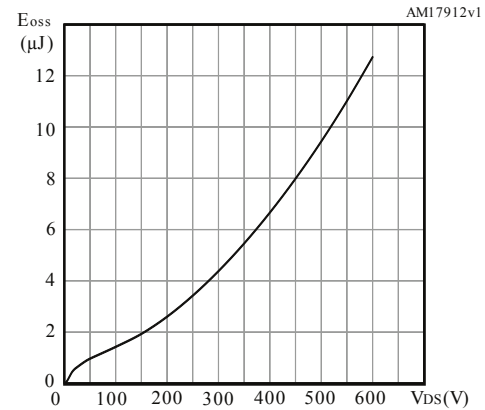
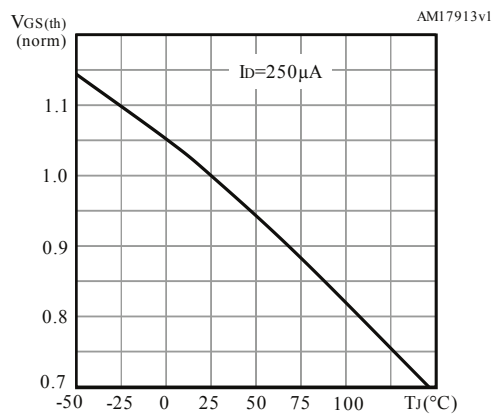
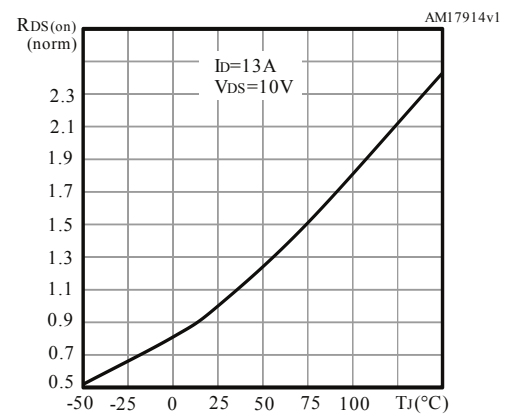
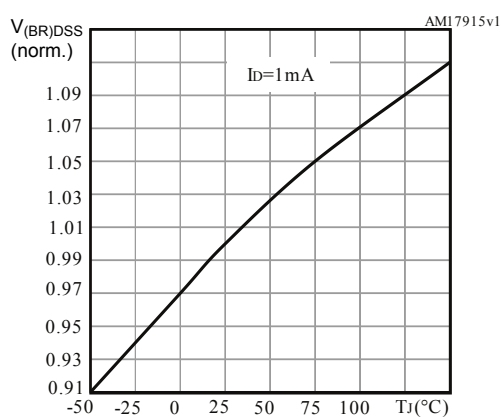
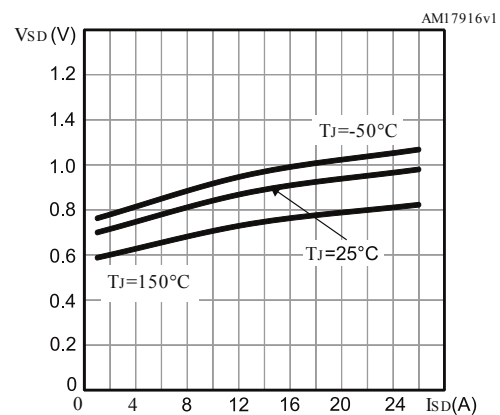
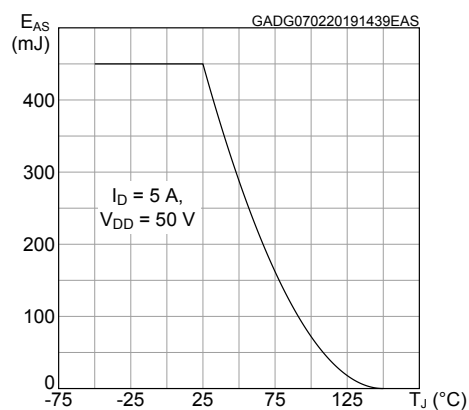
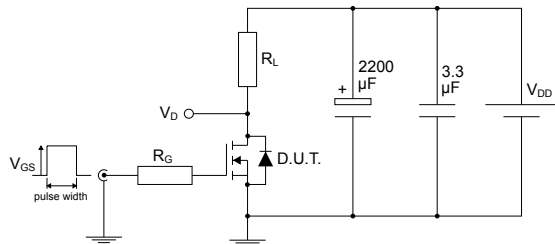
Figure 7. Capacitance variations

Figure 8. Output capacitance stored energy

Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Normalized V_{DS} vs temperature

Figure 12. Source-drain diode forward characteristics


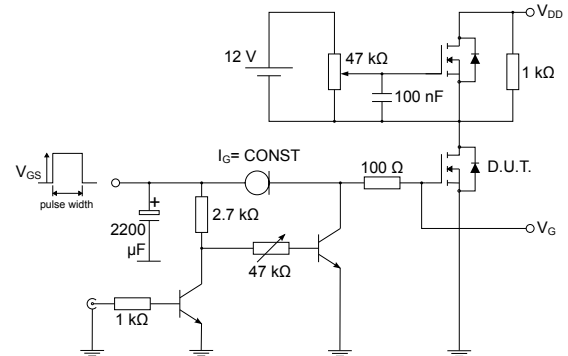
Figure 13. Maximum avalanche energy vs temperature



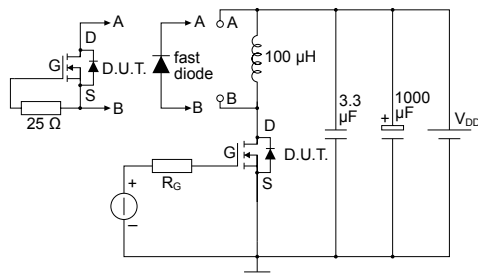
3 Test circuits

Figure 14. Test circuit for resistive load switching times


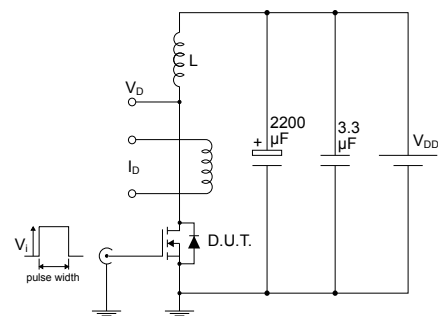
AM01468v1

Figure 15. Test circuit for gate charge behavior


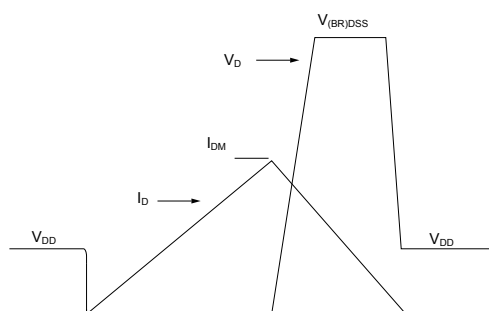
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times


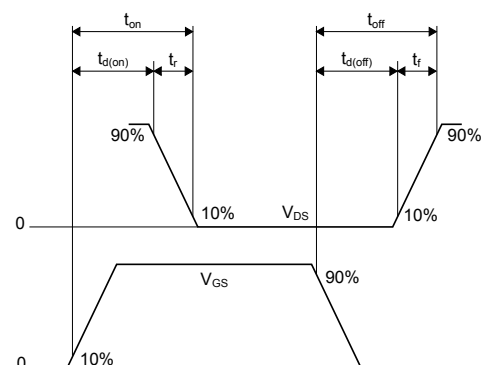
AM01470v1

Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


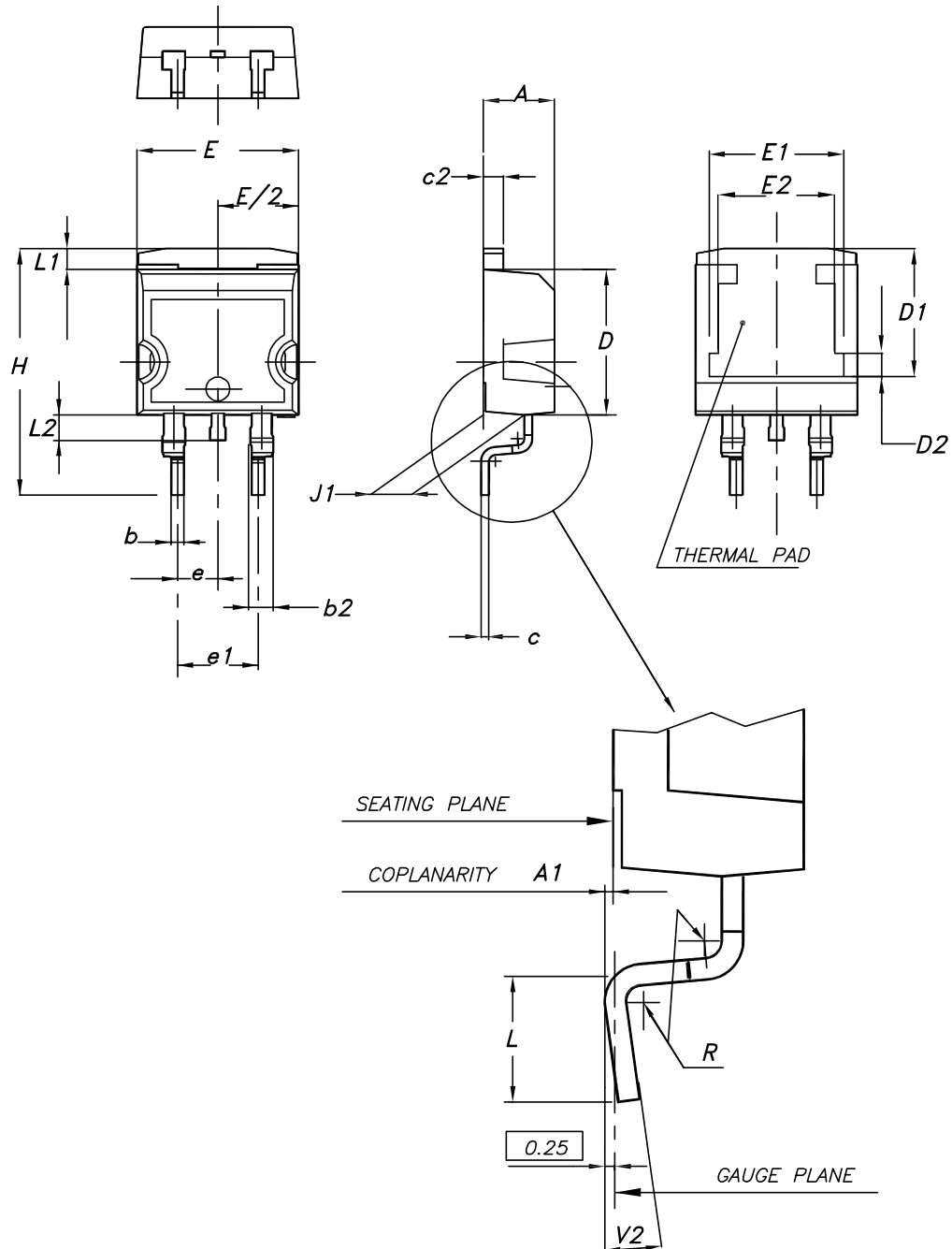
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 20. D²PAK (TO-263) type A package outline

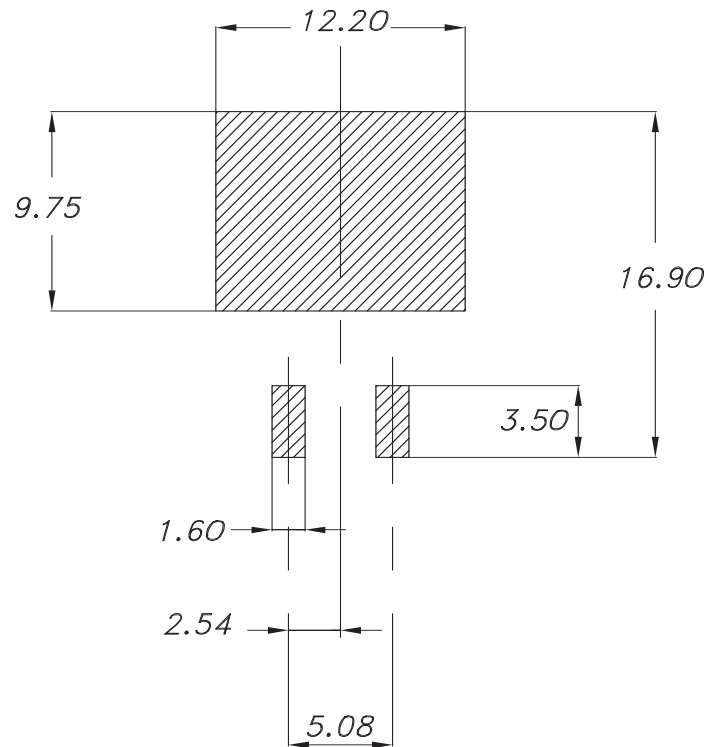


0079457_27

Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

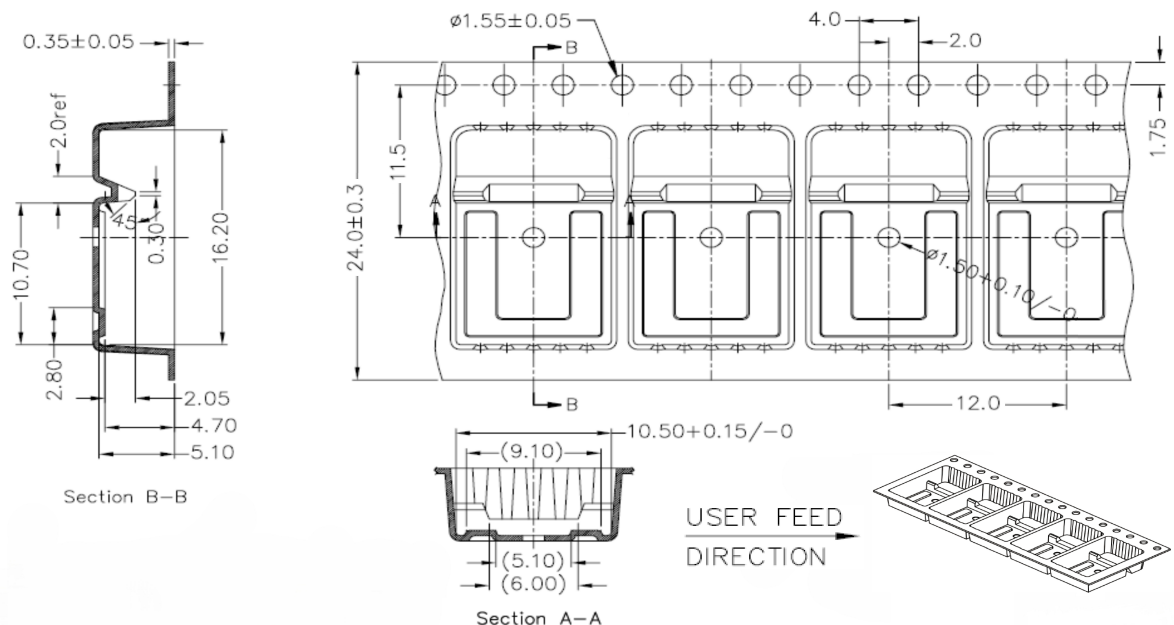
Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.2 D²PAK packing information

Figure 22. D²PAK tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 9. Document revision history

Date	Version	Changes
13-Sep-2013	1	First release.
19-Nov-2013	2	– Modified: $R_{DS(on)}$ and I_D values in cover page – Modified: values in <i>Table 4</i> – Modified: $R_{DS(on)}$ typical and maximum values in <i>Table 5</i>, the entire typical values in <i>Table 6</i>, <i>7</i> and <i>8</i> – Added: <i>Section 2.1: Electrical characteristics (curves)</i> – Minor text changes
18-Jun-2019	3	Removed maturity status indication from cover page. The document status is production data. Update <i>Table 3. Avalanche characteristics</i>. Added <i>Figure 13. Maximum avalanche energy vs temperature</i>. Minor text changes.
01-Aug-2025	4	Update Section 4: Package information. Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information.....	9
4.1	D ² PAK (TO-263) type A package information	9
4.2	D ² PAK packing information	11
	Revision history	12

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved