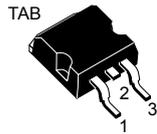
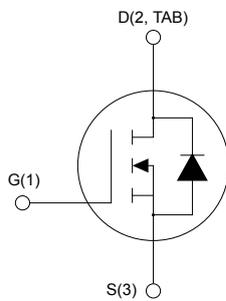


## N-channel 250 V, 15 mΩ typ., 56 A MDmesh M9 Power MOSFET in a D<sup>2</sup>PAK package


**D<sup>2</sup>PAK**


AM01475v1\_noZen



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB25N018M9	250 V	18 mΩ	56 A

- Very low FOM (R<sub>DS(on)</sub>·Q<sub>g</sub>)
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

### Application

- AC-DC converters
- DC-DC converters
- Microinverter

### Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low R<sub>DS(on)</sub> per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

#### Product status link

[STB25N018M9](#)

#### Product summary

<b>Order code</b>	STB25N018M9
<b>Marking</b>	25N018M9
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	56	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	54	
$I_{DM}^{(2)}$	Drain current (pulsed)	375	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	320	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	50	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	900	A/ $\mu\text{s}$
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	120	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

- Limited by package.
- Pulse width is limited by safe operating area.
- $I_{SD} \leq 28\text{ A}$ ,  $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 100\text{ V}$ .
- $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 100\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	0.39	$^\circ\text{C/W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C/W}$

- When mounted on a standard 1 inch<sup>2</sup> area of FR-4 PCB with 2-oz copper.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 100\text{ V}$ )	839	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On-/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	250			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 250\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 250\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			200	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 28\text{ A}$		15	18	m $\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 250\text{ kHz}$ , $V_{GS} = 0\text{ V}$	-	4600	-	pF
$C_{oss}$	Output capacitance		-	250	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }200\text{ V}$ , $V_{GS} = 0\text{ V}$	-	2130	-	pF
$R_g$	Intrinsic gate resistance	$f = 250\text{ kHz}$ , open drain	-	1	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 100\text{ V}$ , $I_D = 28\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	85	-	nC
$Q_{gs}$	Gate-source charge		-	23	-	nC
$Q_{gd}$	Gate-drain charge		-	32	-	nC

1.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to stated value.

**Table 6. Switching times**

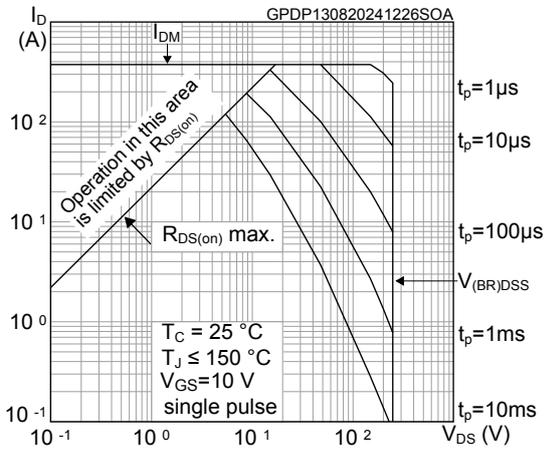
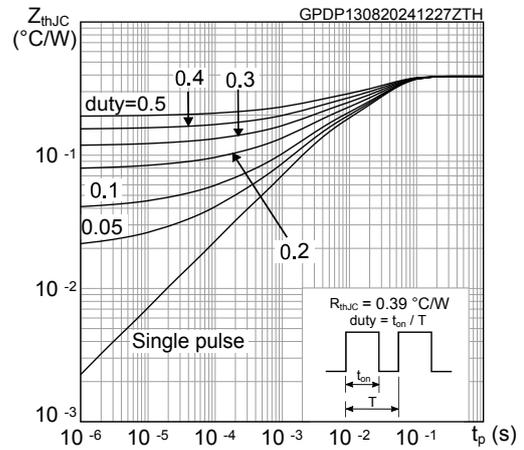
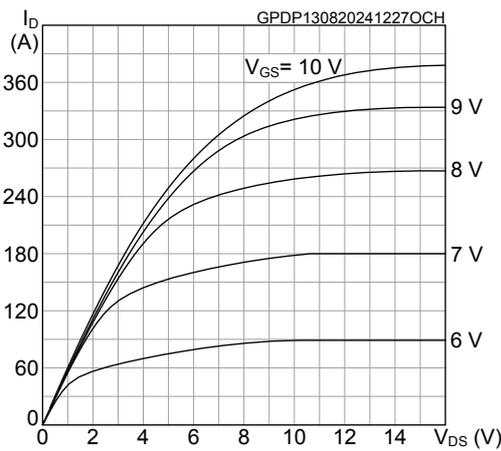
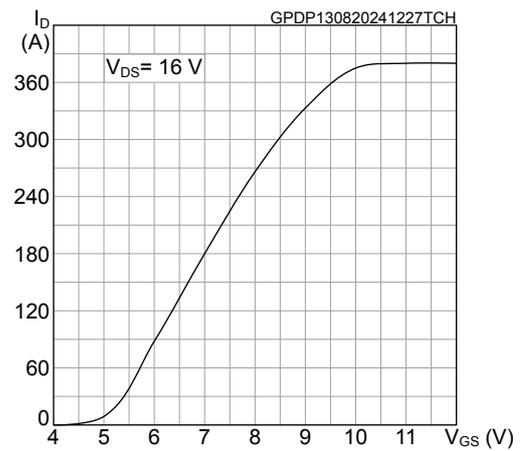
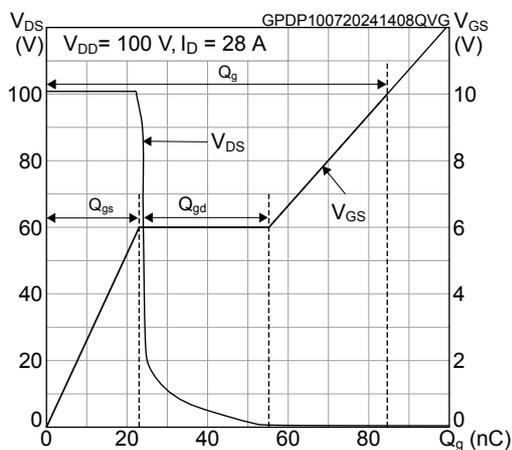
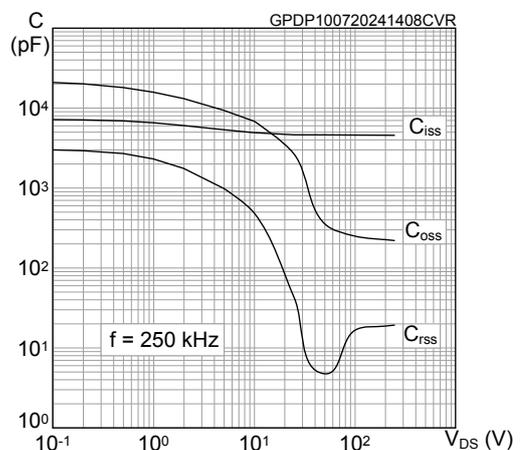
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 100\text{ V}$ , $I_D = 28\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	23	-	ns
$t_r$	Rise time		-	3.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	61	-	ns
$t_f$	Fall time		-	31	-	ns

**Table 7. Source-drain diode**

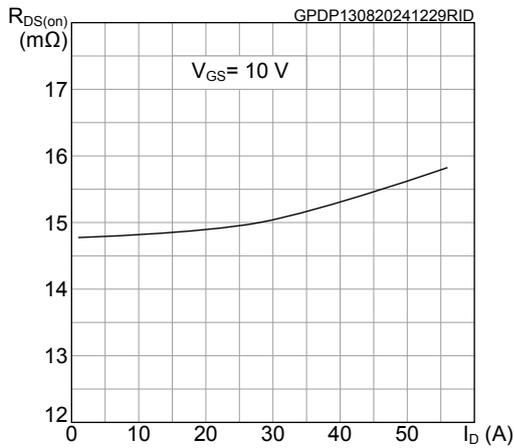
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		56	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		375	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 55 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 55 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	151		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$	-	0.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 55 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	213		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$	-	1.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	17.5		A

1. Limited by package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

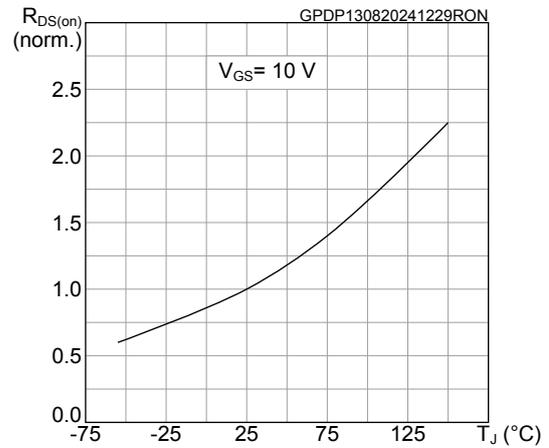
## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

**Figure 2. Maximum transient thermal impedance**

**Figure 3. Typical output characteristics**

**Figure 4. Typical transfer characteristics**

**Figure 5. Typical gate charge characteristics**

**Figure 6. Typical capacitance characteristics**


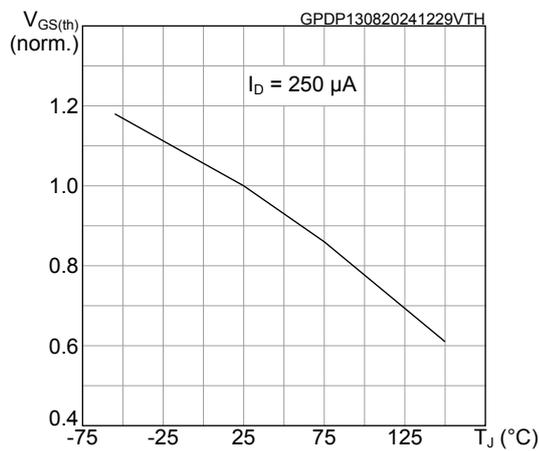
**Figure 7. Typical drain-source on-resistance**



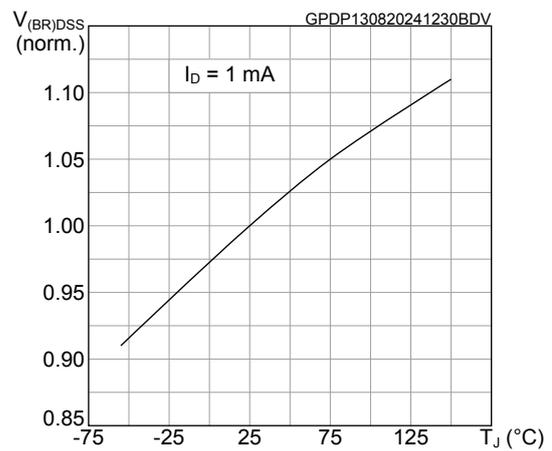
**Figure 8. Normalized on-resistance vs temperature**



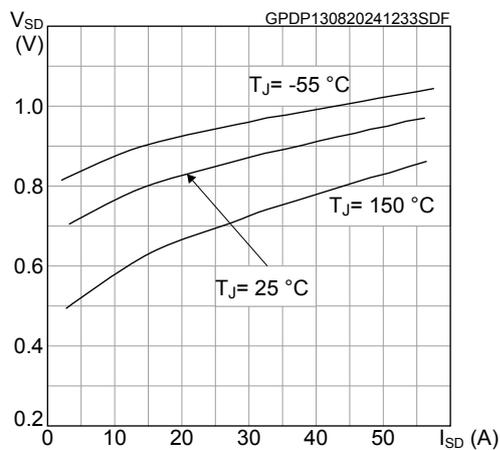
**Figure 9. Normalized gate threshold vs temperature**



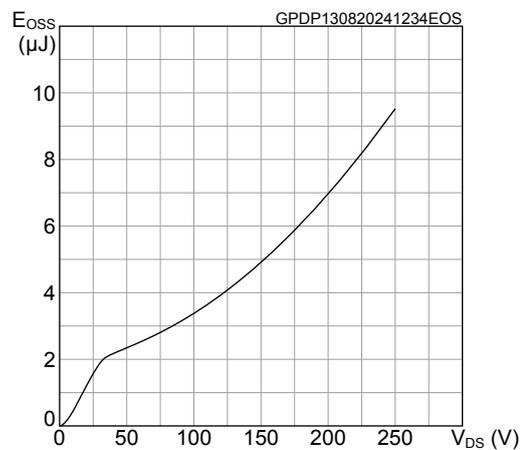
**Figure 10. Normalized breakdown voltage vs temperature**



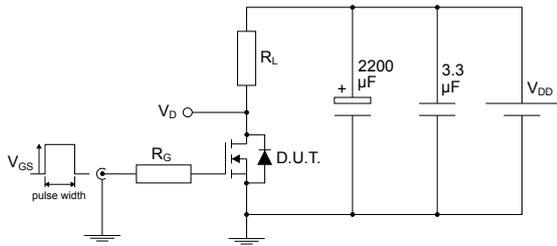
**Figure 11. Typical reverse diode forward characteristics**



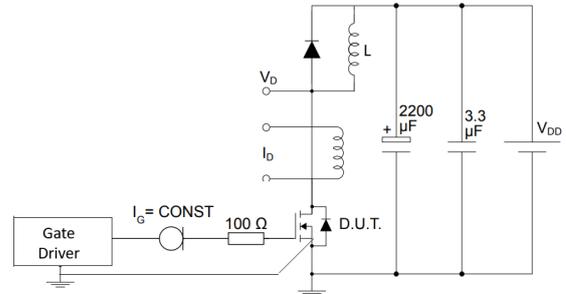
**Figure 12. Typical output capacitance stored energy**



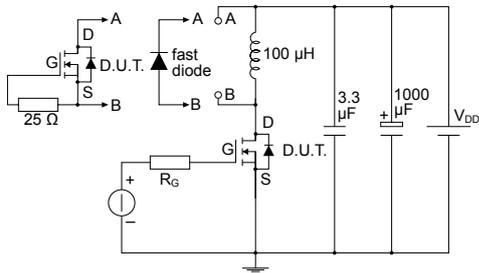
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


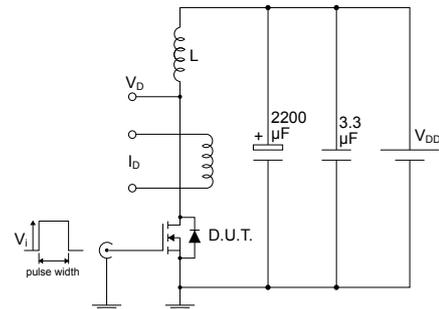
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**Figure 14. Test circuit for gate charge behavior**


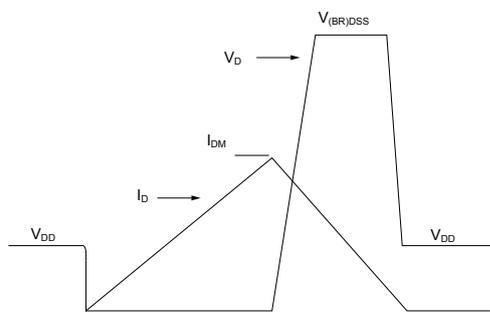
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


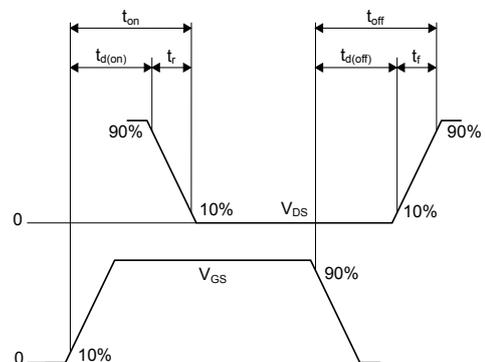
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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


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**Figure 18. Switching time waveform**


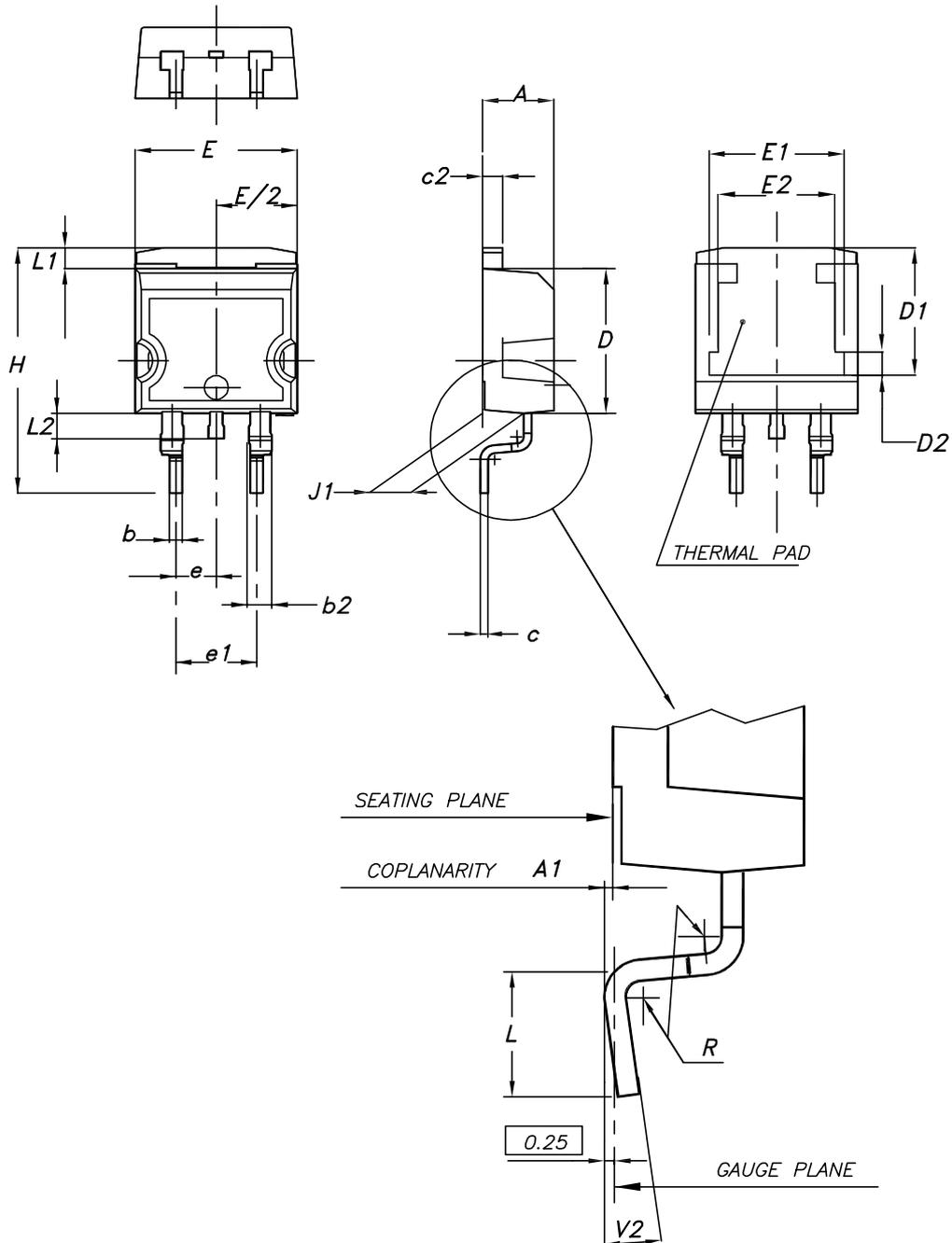
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## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A package information

Figure 19. D<sup>2</sup>PAK (TO-263) type A package outline

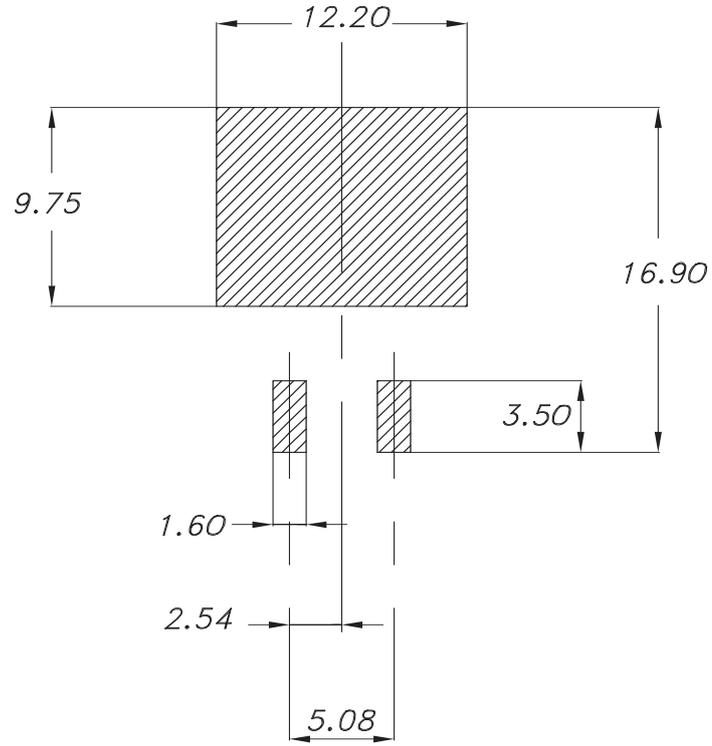


0079457\_27

**Table 8. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

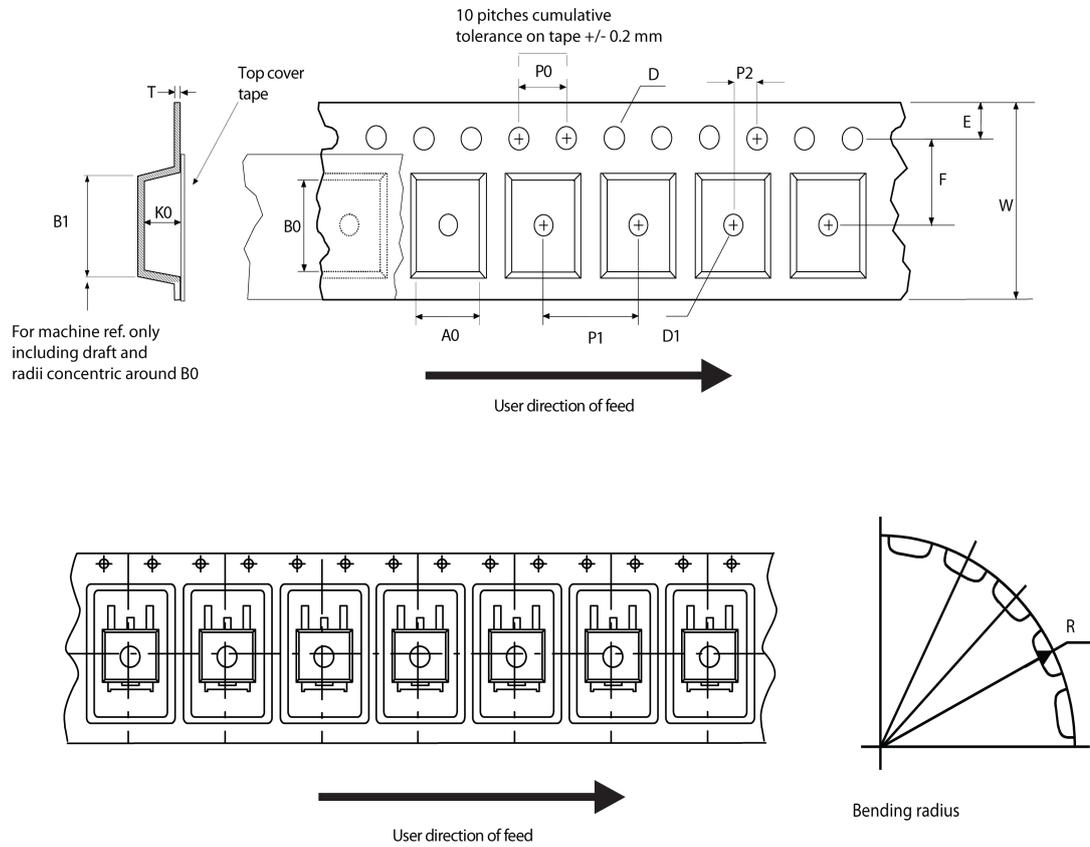
**Figure 20. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**



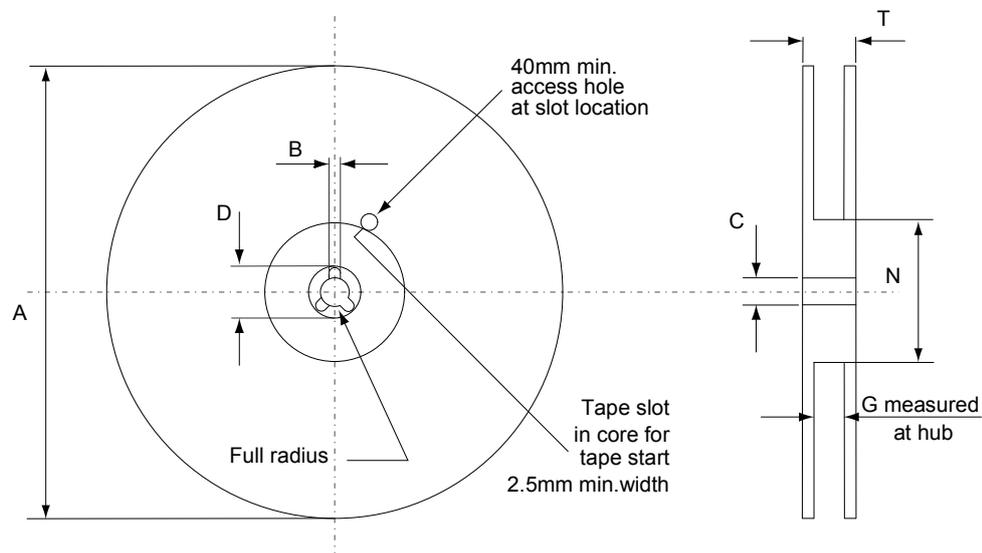
0079457\_Rev27\_footprint

## 4.2 D<sup>2</sup>PAK packing information

Figure 21. D<sup>2</sup>PAK tape outline



AM08852v1

**Figure 22. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 9. D<sup>2</sup>PAK tape and reel mechanical data**

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
21-Aug-2024	1	First release.
15-Jan-2025	2	Updated <a href="#">Features and Application</a> on cover page. Updated <a href="#">Table 5. Dynamic</a> . Updated <a href="#">Figure 5. Typical gate charge characteristics</a> and <a href="#">Figure 6. Typical capacitance characteristics</a> . Updated <a href="#">Section 3: Test circuits</a> .

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