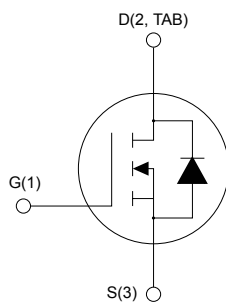
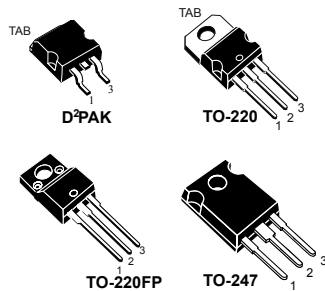




STB20NM60T4, STP20NM60 STP20NM60FP, STW20NM60

Datasheet

N-channel 600 V, 250 mΩ typ., 20 A MDmesh Power MOSFET in D²PAK, TO-220, TO-220FP and TO-247 packages



AM01475v1_noZen



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB20NM60T4	600 V	290 mΩ	20 A
STP20NM60			
STP20NM60FP			
STW20NM60			

- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance
- 100% avalanche tested

Applications

- Switching applications

Description

These N-channel Power MOSFETs are developed using STMicroelectronics' revolutionary MDmesh technology, which associates the multiple drain process with the company's PowerMESH horizontal layout. These devices offer extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, these Power MOSFETs boast an overall dynamic performance which is superior to similar products on the market.

Product status links

[STB20NM60T4](#)

[STP20NM60](#)

[STP20NM60FP](#)

[STW20NM60](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220 TO-247	TO-220FP	
V _{DS}	Drain-source voltage	600		V
V _{GS}	Gate-source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	20	20 ⁽¹⁾	A
	Drain current (continuous) at T _C = 100 °C	12.6	12.6 ⁽¹⁾	
I _{DM} ⁽²⁾	Drain current (pulsed)	80		A
P _{TOT}	Total power dissipation at T _C = 25 °C	192	45	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T _C = 25 °C)	-	2.5	kV
T _{stg}	Storage temperature range	-65 to 150		°C
T _J	Operation junction temperature range			°C

1. Limited by maximum junction temperature.
2. Pulse width is limited by safe operating area.
3. I_{SD} ≤ 20 A, di/dt ≤ 400 A/μs, V_{DD} ≤ V_{(BR)DSS}.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220 TO-247	TO-220FP	
R _{thJC}	Thermal resistance, junction-to-case	0.65	2.8	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	62.5		°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _J max.)	10	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AS} , V _{DD} = 50 V)	650	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	600	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	10	
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$	-	250	290	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 20\text{ A}$	-	11	-	S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1500	-	pF
C_{oss}	Output capacitance		-	350	-	pF
C_{rss}	Reverse transfer capacitance		-	35	-	pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	215	-	pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 15. Test circuit for gate charge behavior)	-	39	54 ⁽³⁾	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain charge		-	20	-	nC
R_g	Gate input resistance	$f = 1\text{ MHz}$ gate DC bias = 0 test signal level = 20 mV open drain	-	1.6	-	Ω

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

3. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	25	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	42	-	ns
t_f	Fall time		-	11	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$	-	390		ns
Q_{rr}	Reverse recovery charge		-	5		μC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	25		A
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	510		ns
Q_{rr}	Reverse recovery charge		-	6.5		μC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	26		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK, TO-220 and TO-247

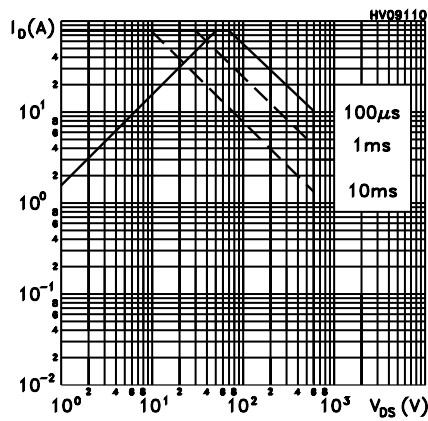


Figure 2. Thermal impedance for D²PAK, TO-220 and TO-247

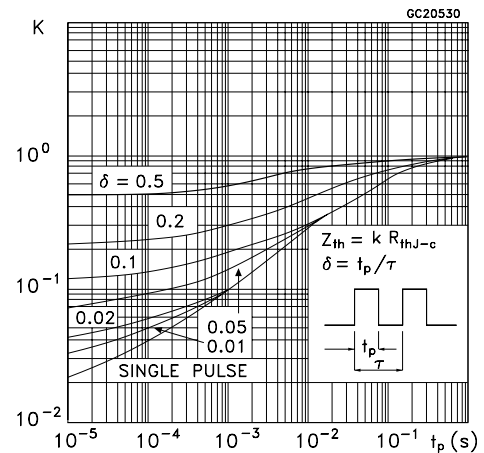


Figure 3. Safe operating area for TO-220FP

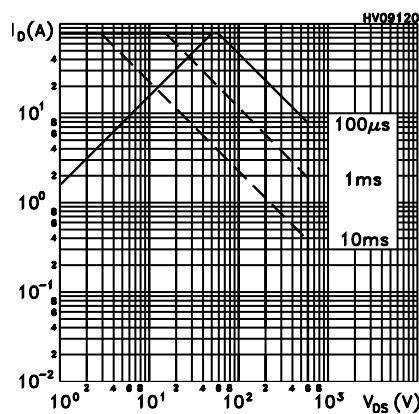


Figure 4. Thermal impedance for TO-220FP

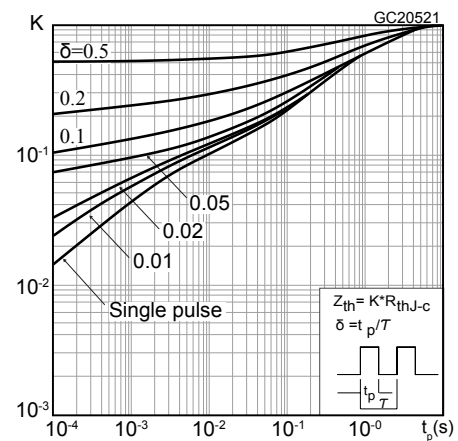


Figure 5. Output characteristics

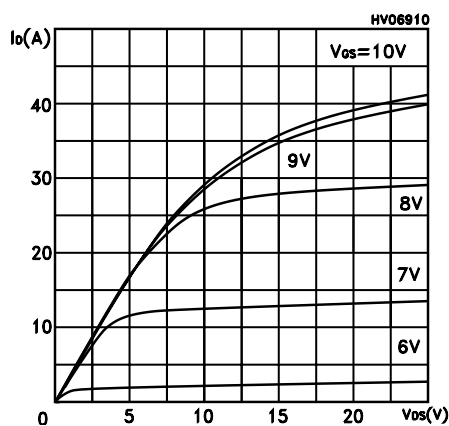


Figure 6. Transfer characteristics

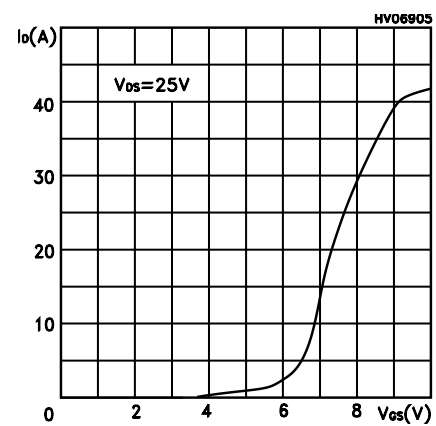


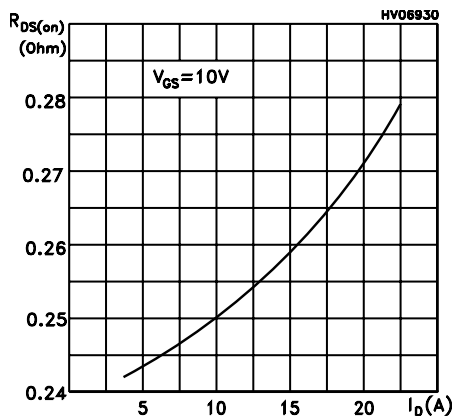
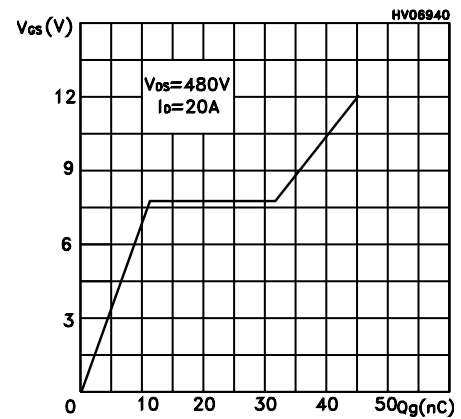
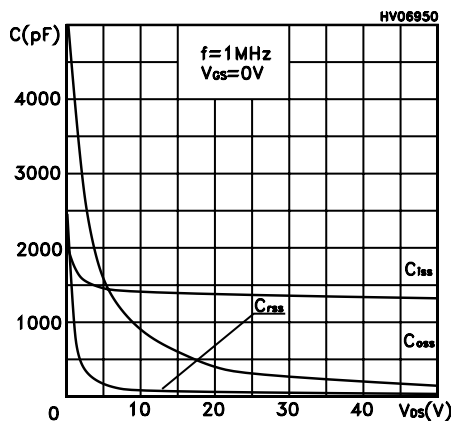
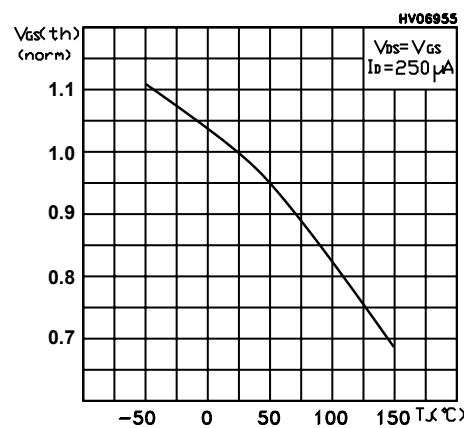
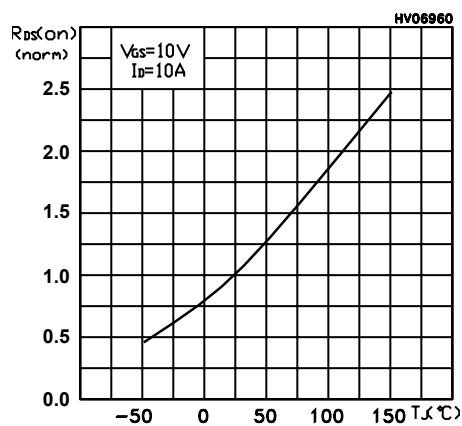
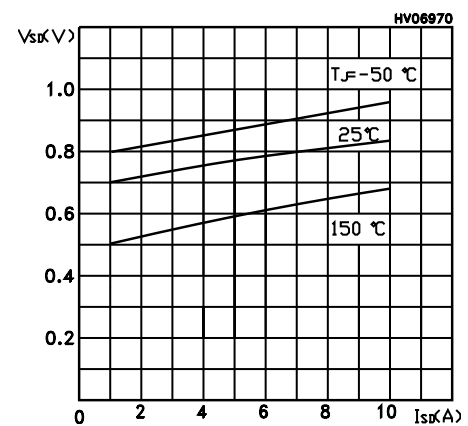
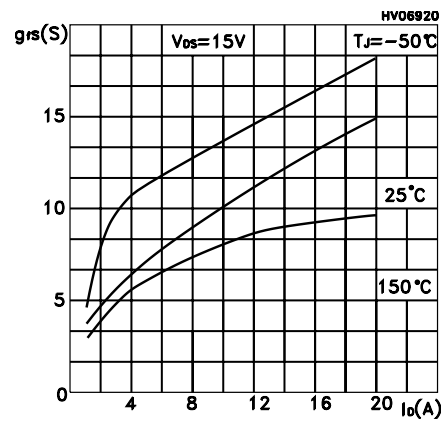
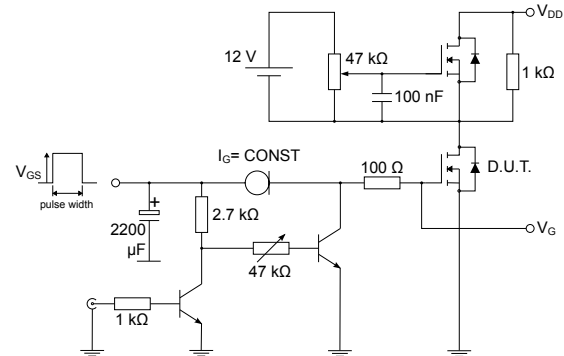
Figure 7. Static drain-source on-resistance

Figure 8. Gate charge vs gate-source voltage

Figure 9. Capacitance variations

Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature

Figure 12. Source-drain diode forward characteristics


Figure 13. Transconductance


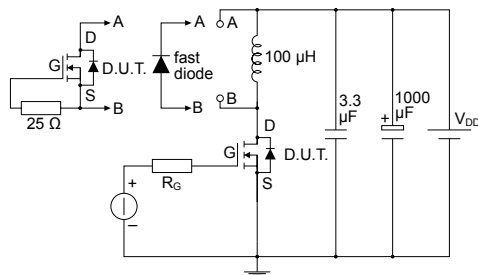
3 Test circuits

Figure 14. Test circuit for resistive load switching times


AM01468v1

Figure 15. Test circuit for gate charge behavior


AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times


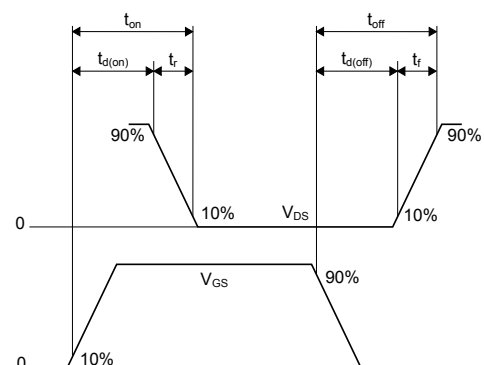
AM01470v1

Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


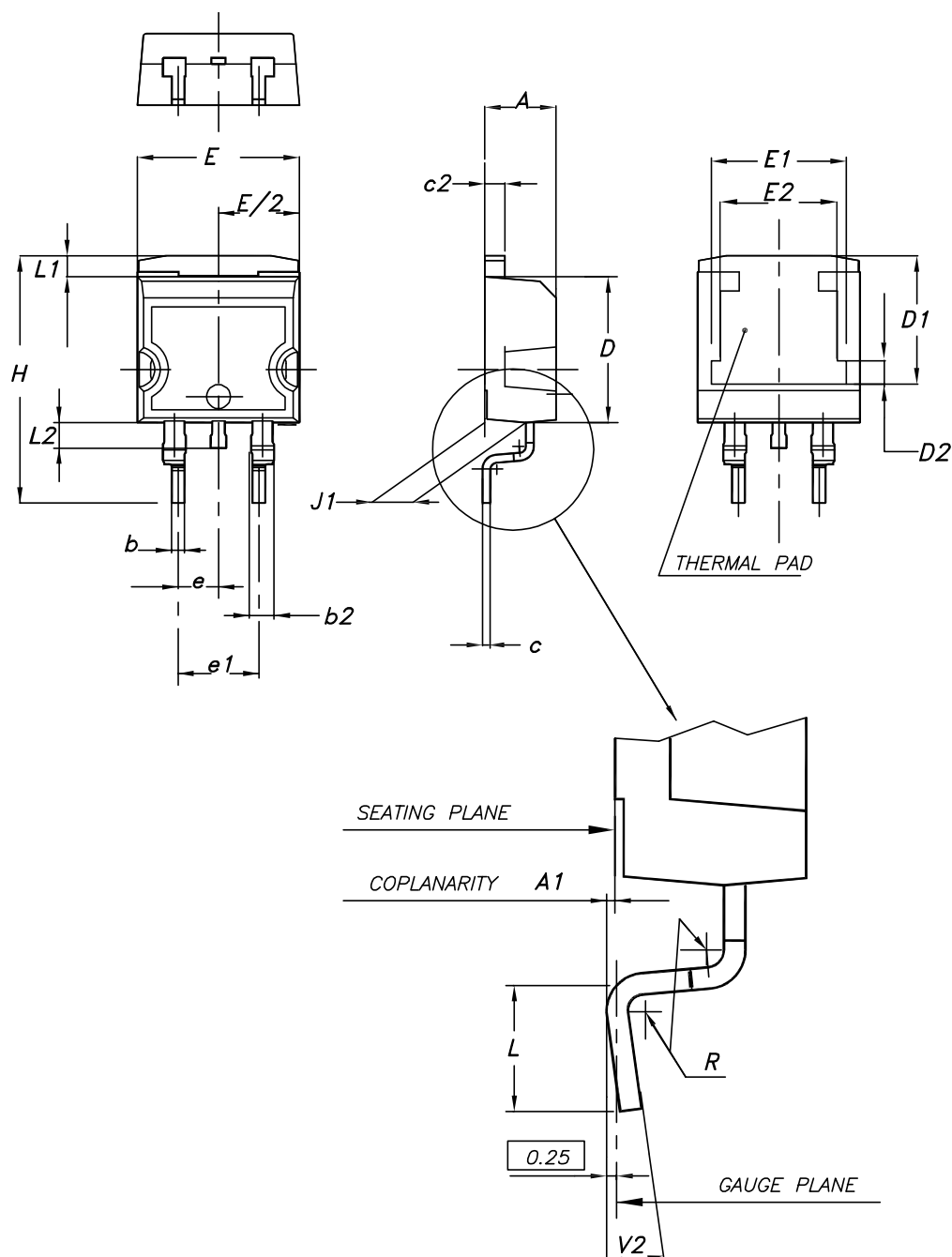
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

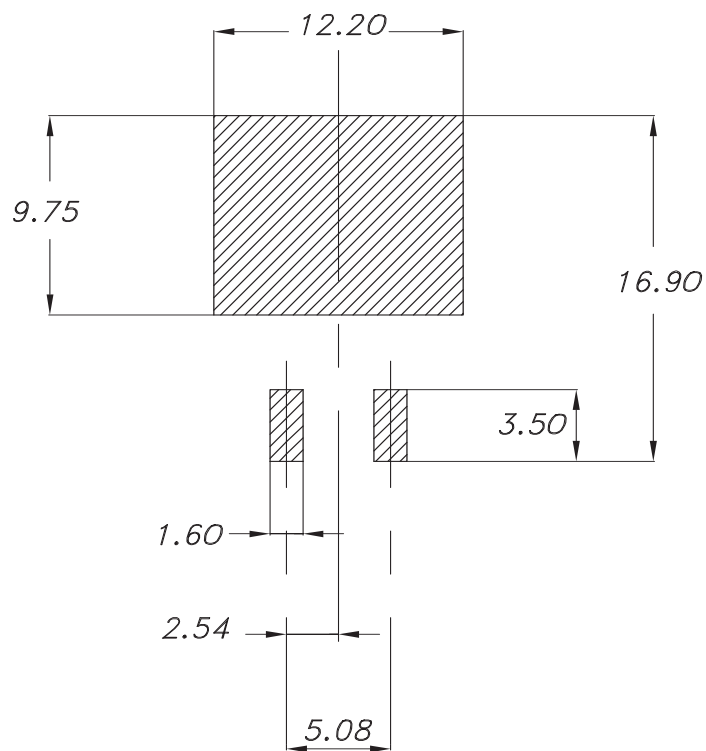
Figure 20. D²PAK (TO-263) type A package outline



0079457_27

Table 8. D²PAK (TO-263) type A package mechanical data

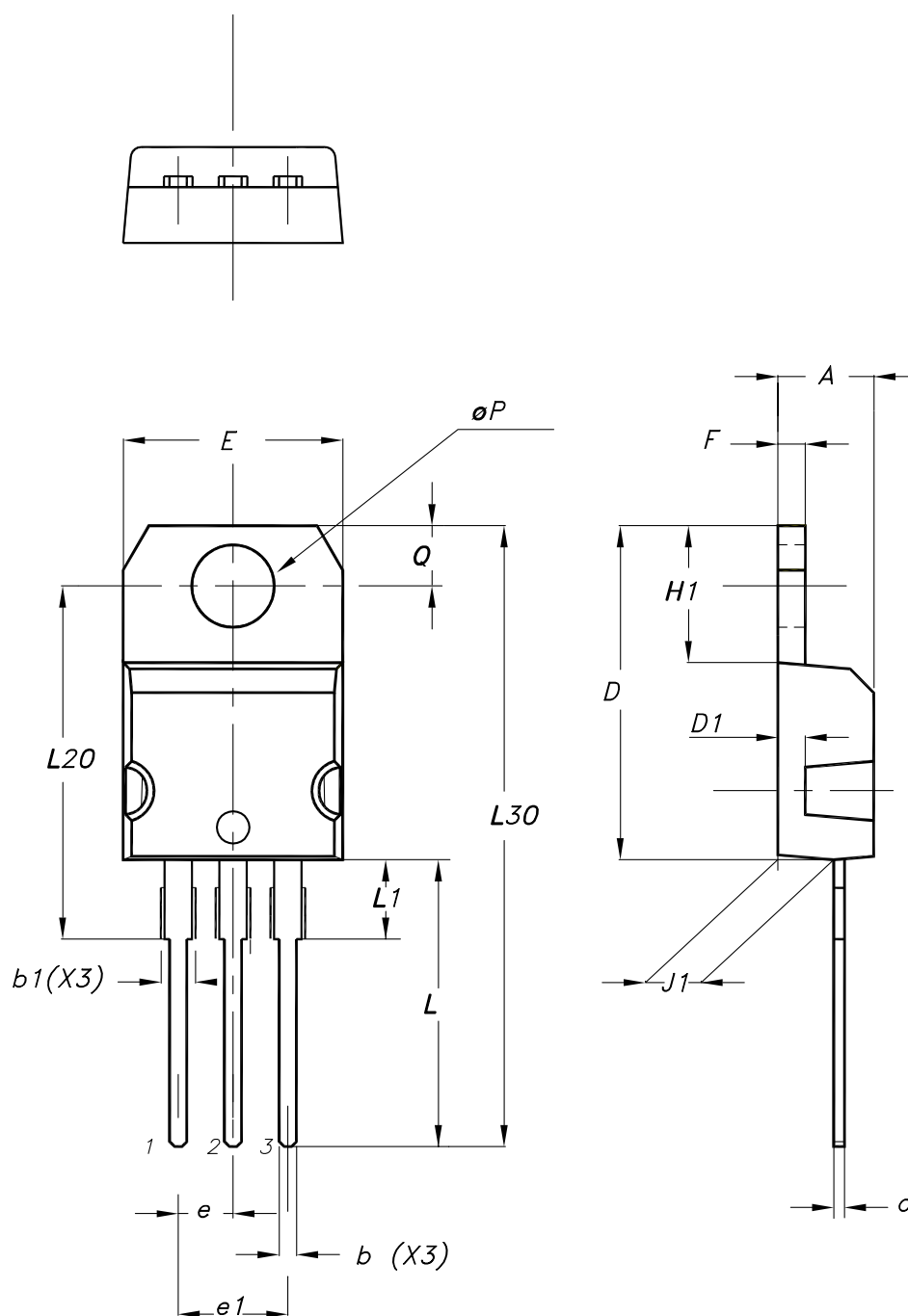
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)


0079457_Rev27_footprint

4.2 TO-220 type A package information

Figure 22. TO-220 type A package outline



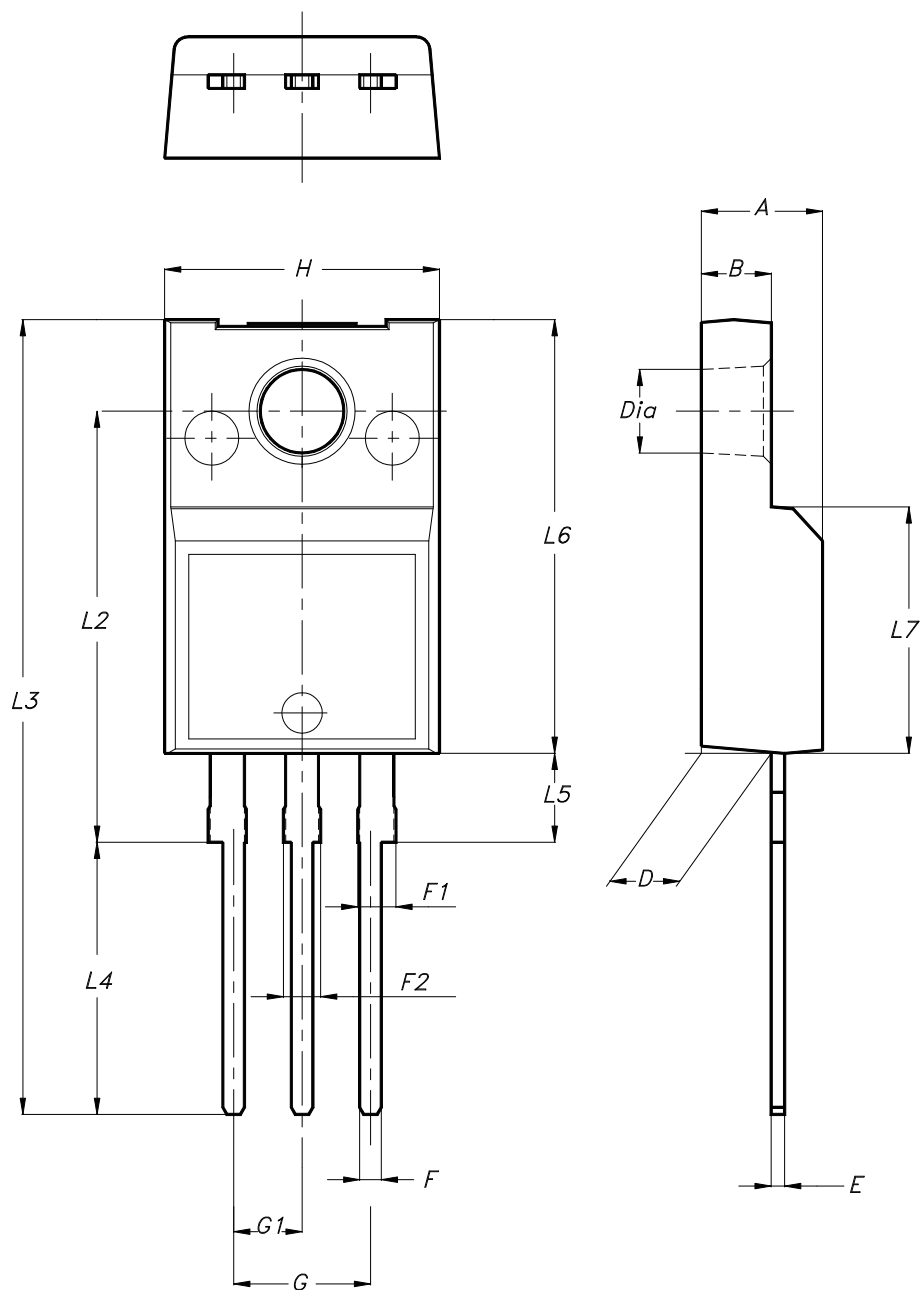
0015988_typeA_Rev_24

Table 9. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.3 TO-220FP type B package information

Figure 23. TO-220FP type B package outline



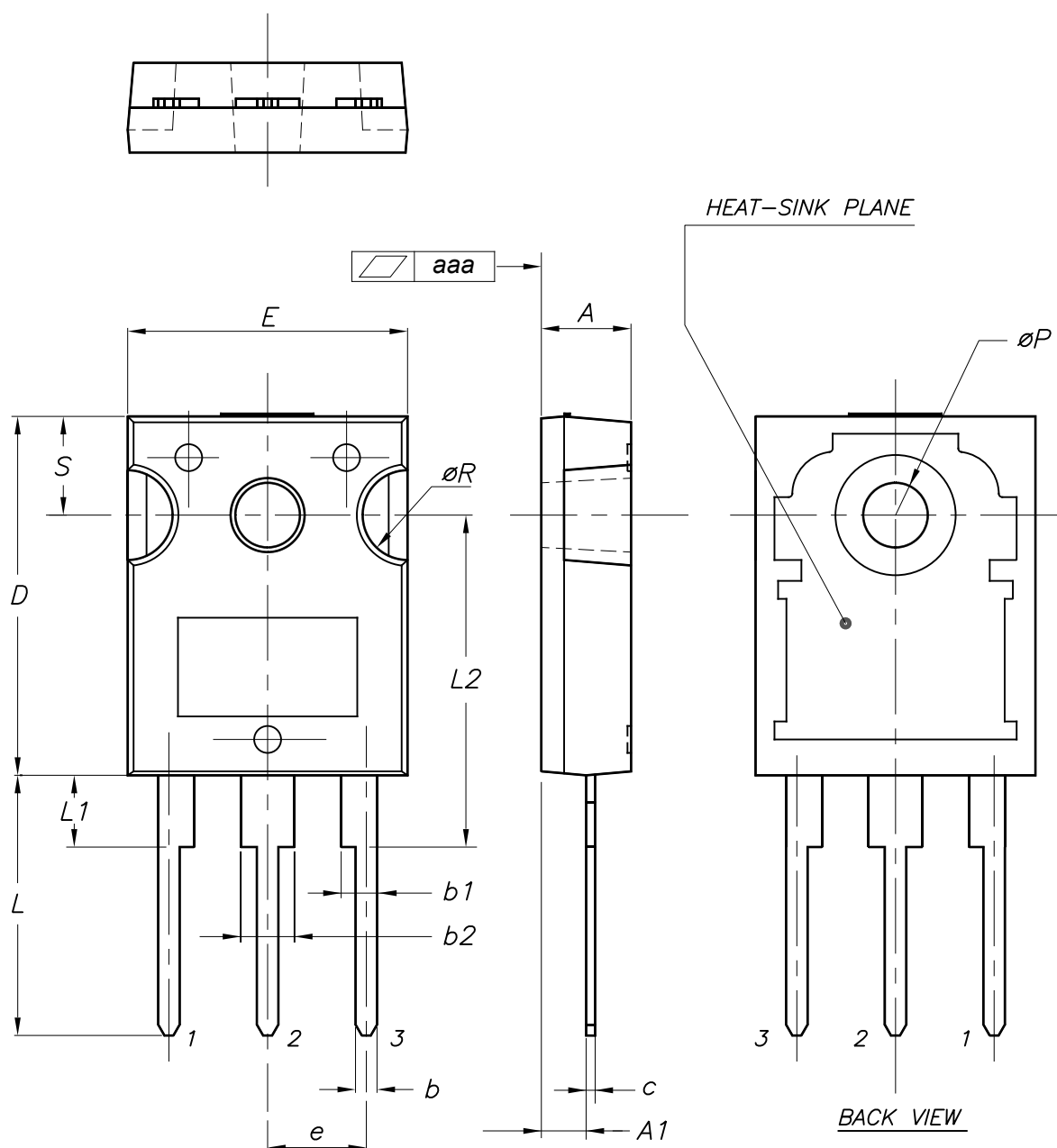
7012510_B_rev.14

Table 10. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.4 TO-247 package information

Figure 24. TO-247 package outline



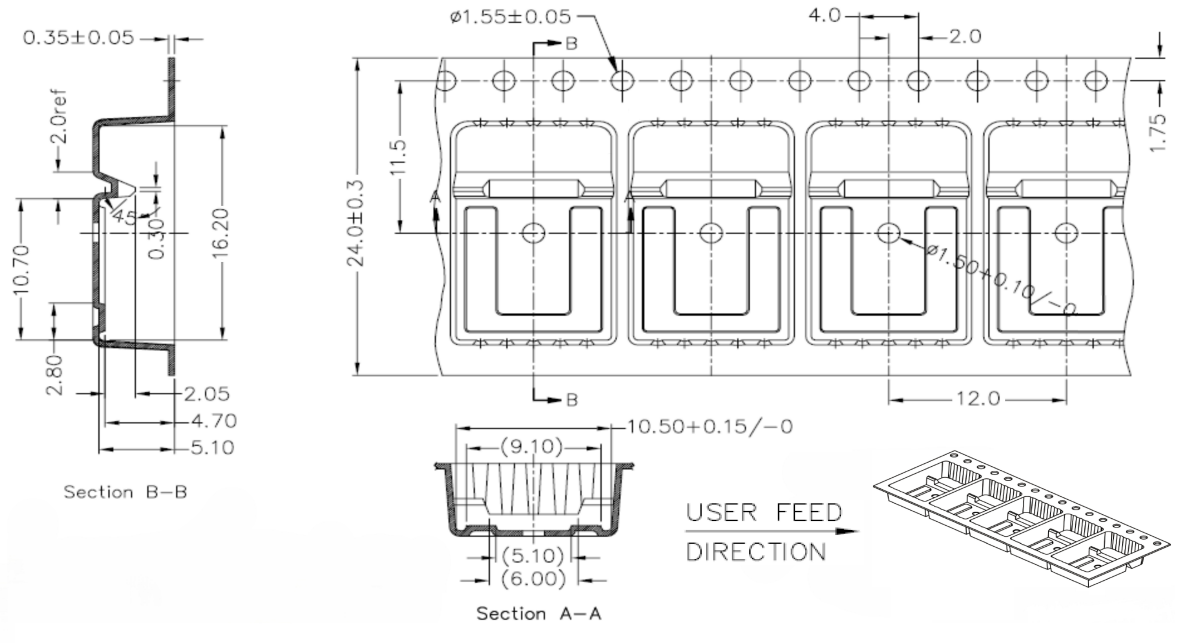
0075325_10

Table 11. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.5 D²PAK packing information

Figure 25. D²PAK tape drawing (dimensions are in mm)



DM01095771_2



5 Ordering information

Table 12. Order codes

Order codes	Marking	Package	Packing
STB20NM60T4	B20NM60	D ² PAK	Tape and reel
STP20NM60	P20NM60	TO-220	Tube
STP20NM60FP	P20NM60FP	TO-220FP	
STW20NM60	W20NM60	TO-247	



Revision history

Table 13. Document revision history

Date	Revision	Changes
17-Feb-2005	9	Insert the TO-247 package
25-Oct-2006	10	The document has been reformatted
18-Dec-2006	11	Text updates on <i>Table 5</i> .
27-Aug-2007	12	Updated <i>Figure 2</i> and <i>Figure 4</i> .
30-Jul-2025	13	Removed order code STB20NM60-1. Updated Section 4: Package information . Minor text changes.



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