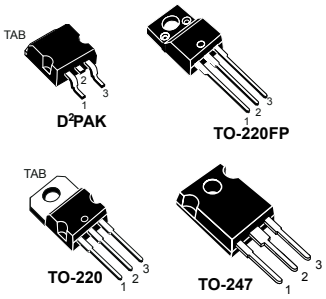
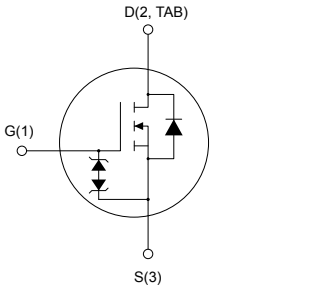
STB12NK80ZT4, STF12NK80Z
STP12NK80Z, STW12NK80Z

Datasheet

N-channel 800 V, 585 mΩ typ., 10.5 A SuperMESH Power MOSFETs in D²PAK, TO-220FP, TO-220 and TO-247 packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB12NK80ZT4	800 V	750 mΩ	10.5 A
STF12NK80Z			
STP12NK80Z			
STW12NK80Z			

- Extremely high dv/dt capability
- Improved ESD capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status links
STB12NK80ZT4
STF12NK80Z
STP12NK80Z
STW12NK80Z

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D^2PAK, TO-220, TO-247	TO-220FP	
V_{DS}	Drain-source voltage	800		V
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	10.5	10.5(1)	A
	Drain current (continuous) at T_C = 100 °C	6.6	6.6(1)	
I_{DM}(2)	Drain current (pulsed)	42	42(1)	A
P_{TOT}	Total power dissipation at T_C = 25 °C	190	40	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	4		kV
dv/dt(3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)		2.5	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Operating junction temperature range			

1. *Limited by maximum junction temperature.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 10.5 A, di/dt ≤ 200 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D^2PAK, TO-220	TO-247	TO-220FP	
R_{thJC}	Thermal resistance, junction-to-case	0.66		3.1	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	50	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	10.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	400	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3.00	3.75	4.50	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5.25 A		585	750	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2620	-	pF
C_{oss}	Output capacitance		-	250	-	pF
C_{rss}	Reverse transfer capacitance		-	53	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 640 V	-	100	-	pF
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 10.5 A, V_{GS} = 0 to 10 V (see Figure 18. Test circuit for gate charge behavior)	-	87	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	44	-	nC

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 5.25 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 17. Test circuit for resistive load switching times and Figure 22. Switching time waveform)	-	30	-	ns
t_r	Rise time		-	18	-	ns
$t_{d(off)}$	Turn-off delay time		-	70	-	ns
t_f	Fall time		-	20	-	ns
$t_{r(Voff)}$	Off voltage rise time	V_{DD} = 640 V, I_D= 10.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	16	-	ns
t_f	Fall time		-	15	-	ns
t_c	Cross-over time		-	28	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		42	A
V_{SD}(2)	Forward on voltage	I_{SD} = 10.5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 10.5 A, di/dt = 100 A/µs,	-	635		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	5.9		µC
I_{RRM}	Reverse recovery current	(see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	18.5		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK and TO-220

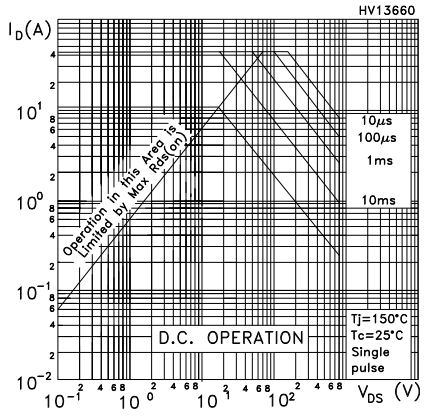


Figure 2. Normalized transient thermal impedance for D²PAK and TO-220

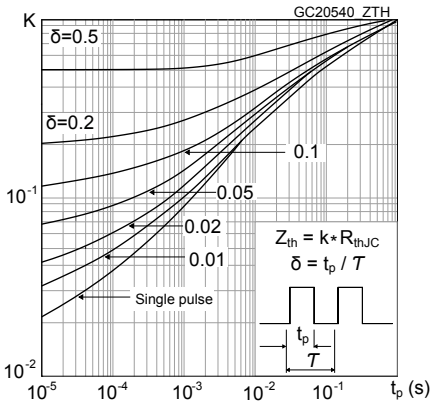


Figure 3. Safe operating area for TO-220FP

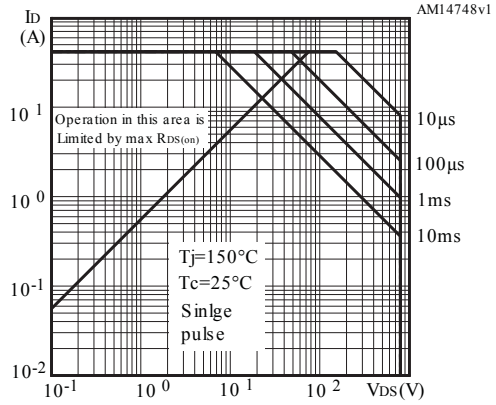


Figure 4. Normalized transient thermal impedance for TO-220FP

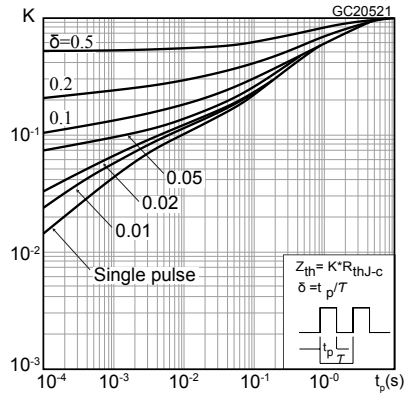


Figure 5. Safe operating area for TO-247

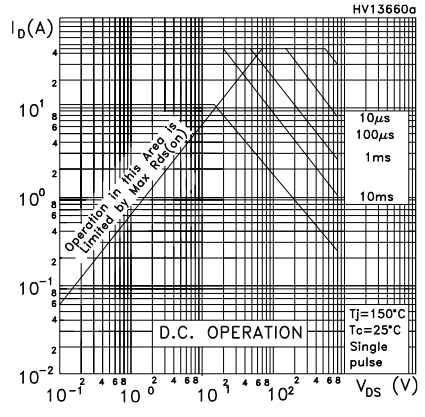


Figure 6. Normalized transient thermal impedance for TO-247

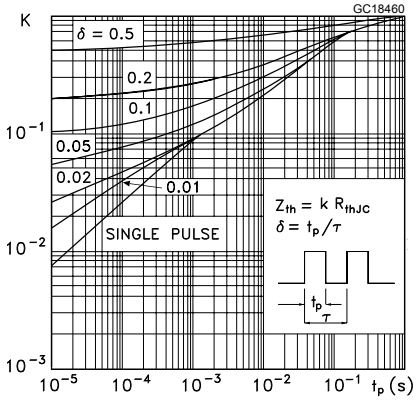


Figure 7. Typical output characteristics

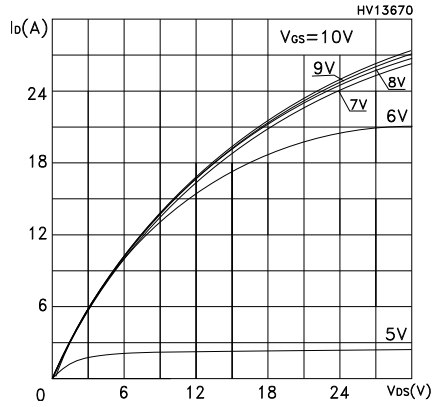


Figure 8. Typical transfer characteristics

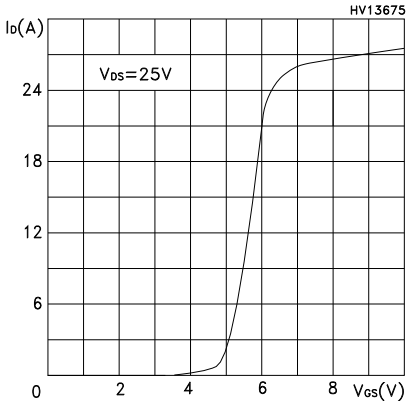


Figure 9. Typical drain-source on-resistance

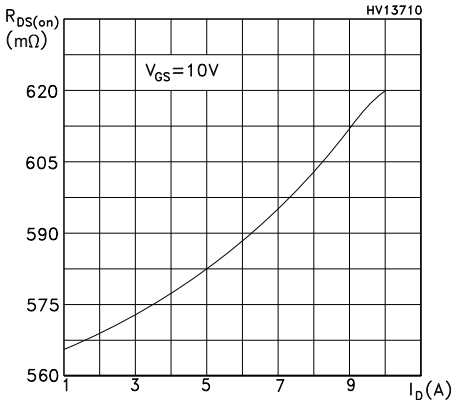


Figure 10. Typical gate charge characteristics

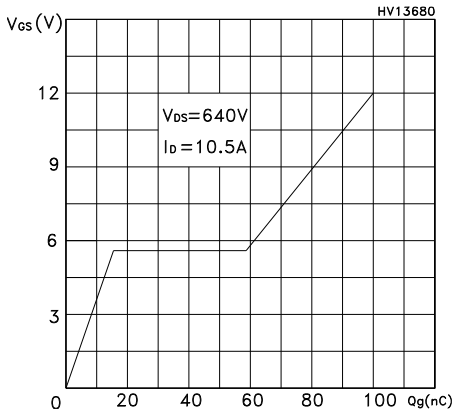


Figure 11. Typical capacitance characteristics

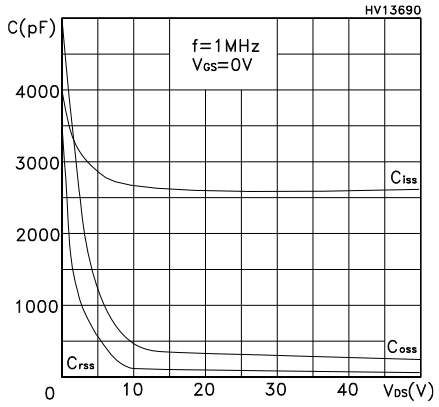


Figure 12. Normalized gate threshold vs temperature

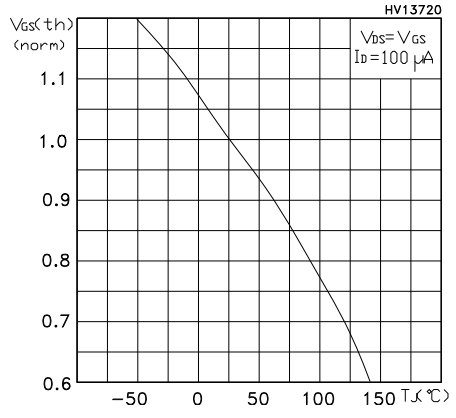


Figure 13. Normalized on-resistance vs temperature

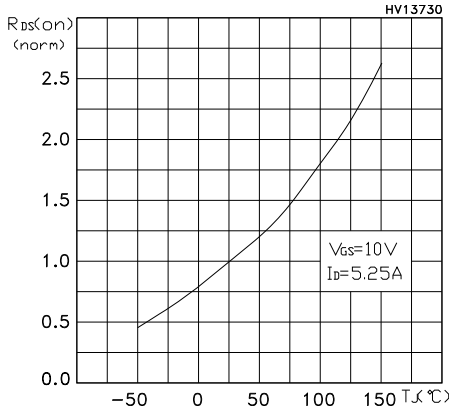


Figure 14. Typical reverse diode forward characteristics

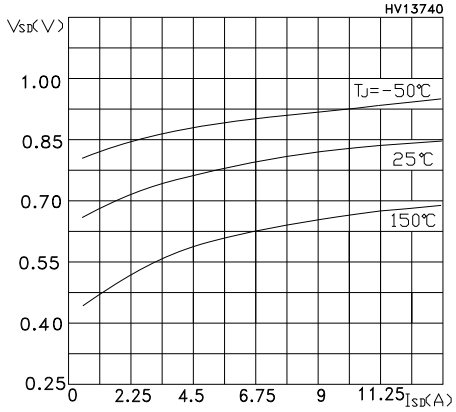


Figure 15. Maximum avalanche energy vs temperature

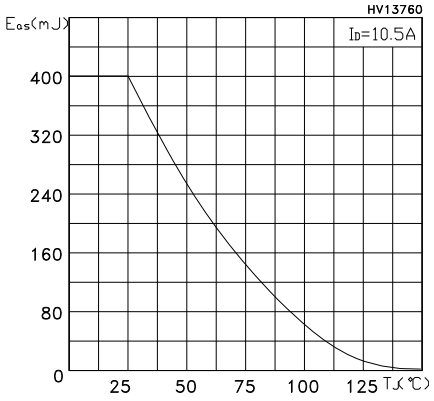
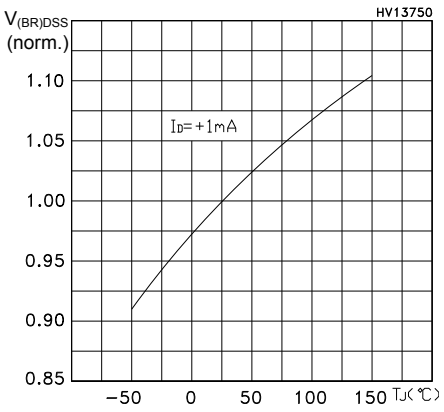


Figure 16. Normalized breakdown voltage vs temperature



3 Test circuits

Figure 17. Test circuit for resistive load switching times

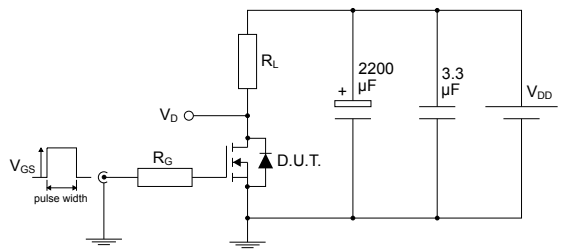


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Figure 18. Test circuit for gate charge behavior

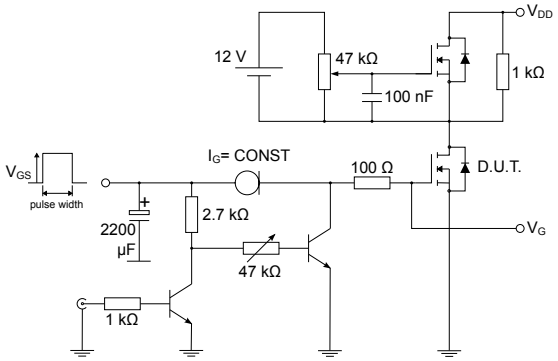

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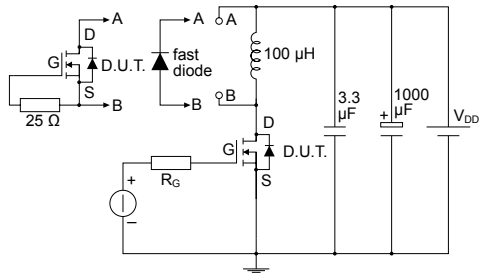
Figure 19. Test circuit for inductive load switching and diode recovery times



AM01470v1

Figure 20. Unclamped inductive load test circuit

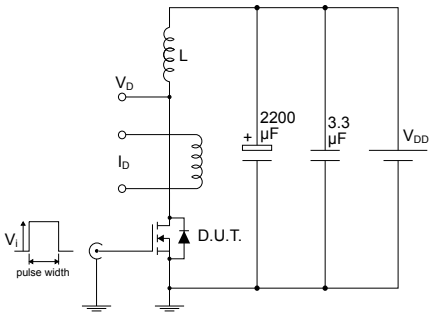


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Figure 21. Unclamped inductive waveform

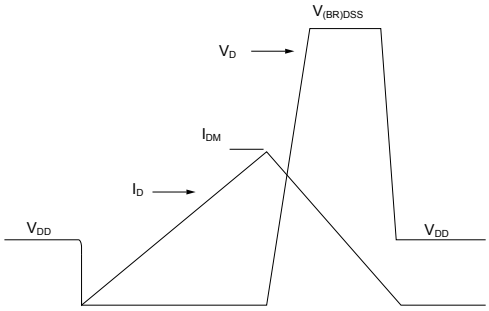

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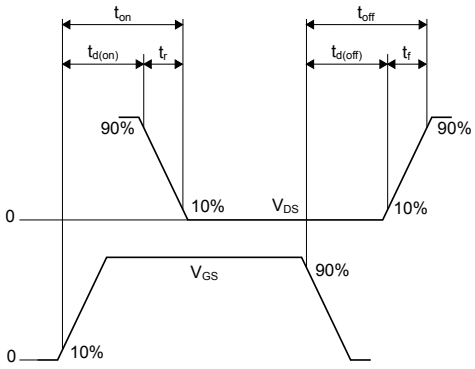
Figure 22. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 23. D²PAK (TO-263) type A2 package outline

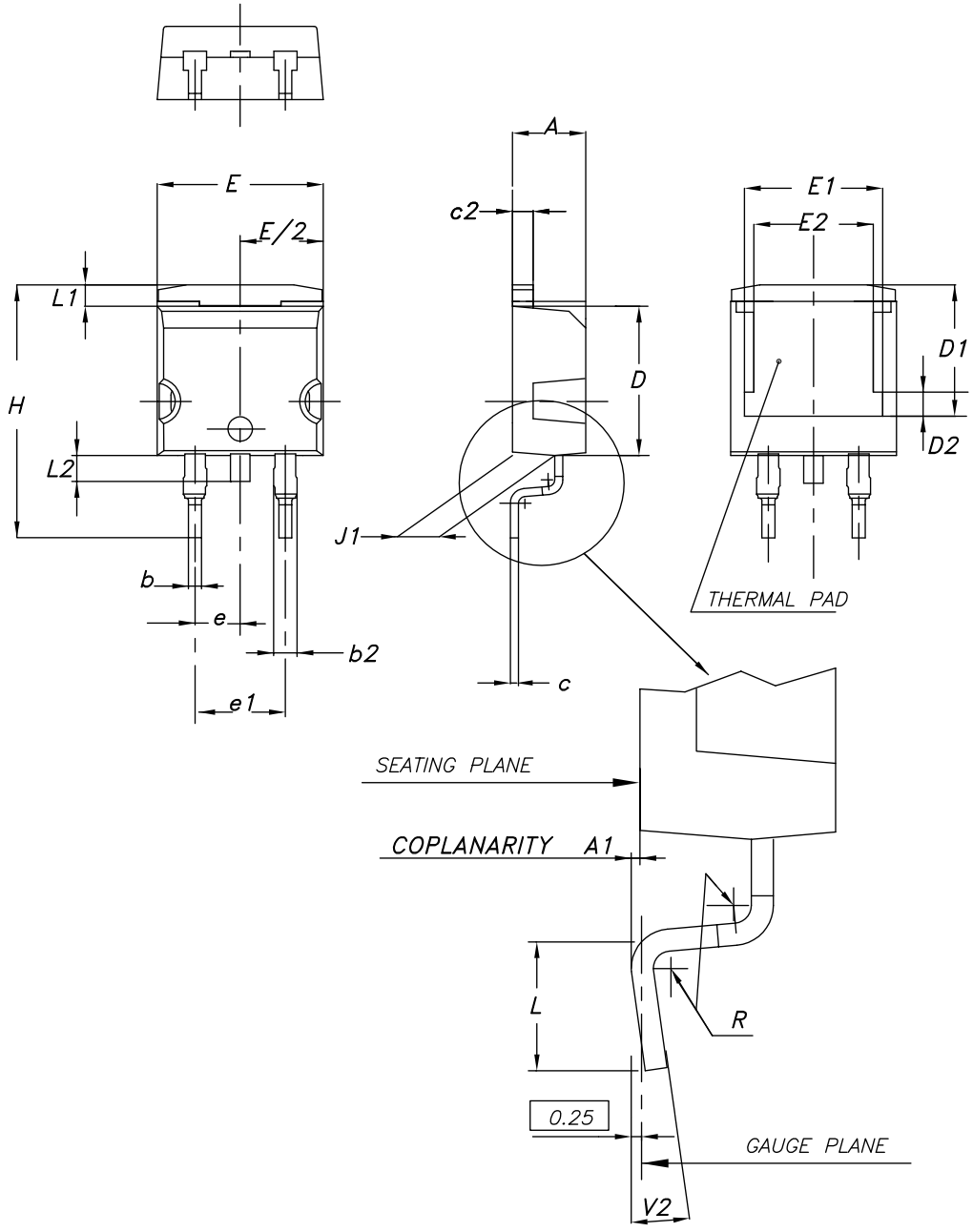

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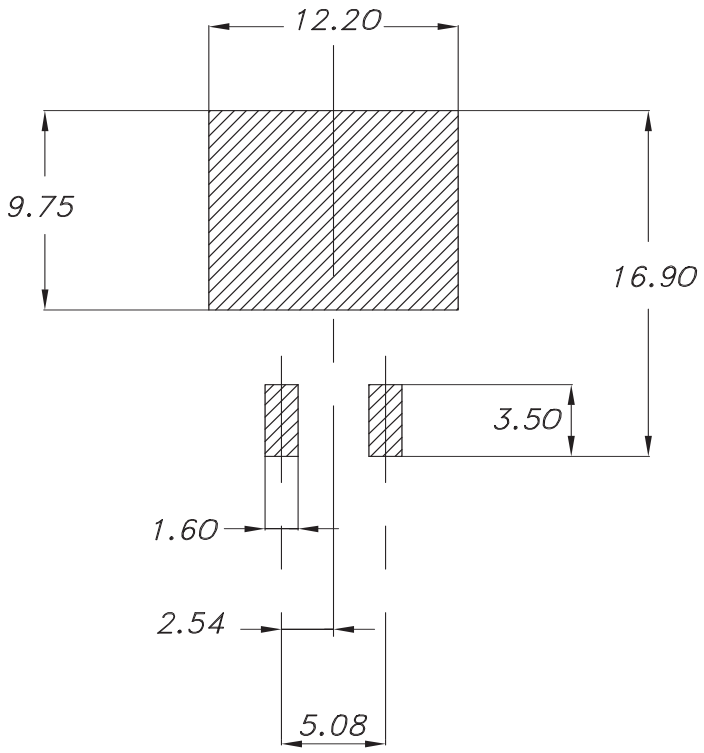
Table 8. **D²PAK (TO-263) type A2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 24. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220FP type B package information

Figure 25. **TO-220FP type B package outline**

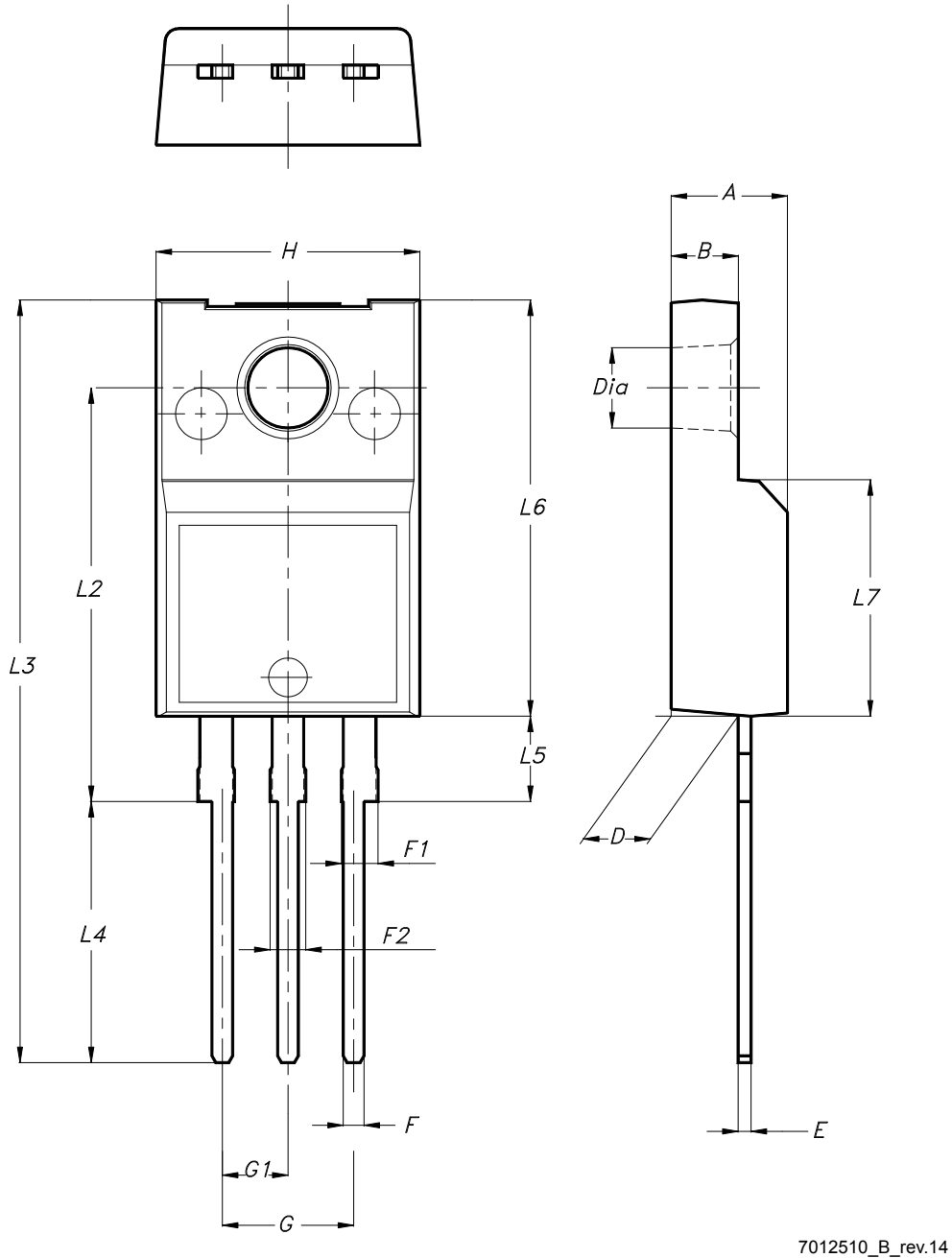


Table 9. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.3 TO-220 type A package information

Figure 26. **TO-220 type A package outline**

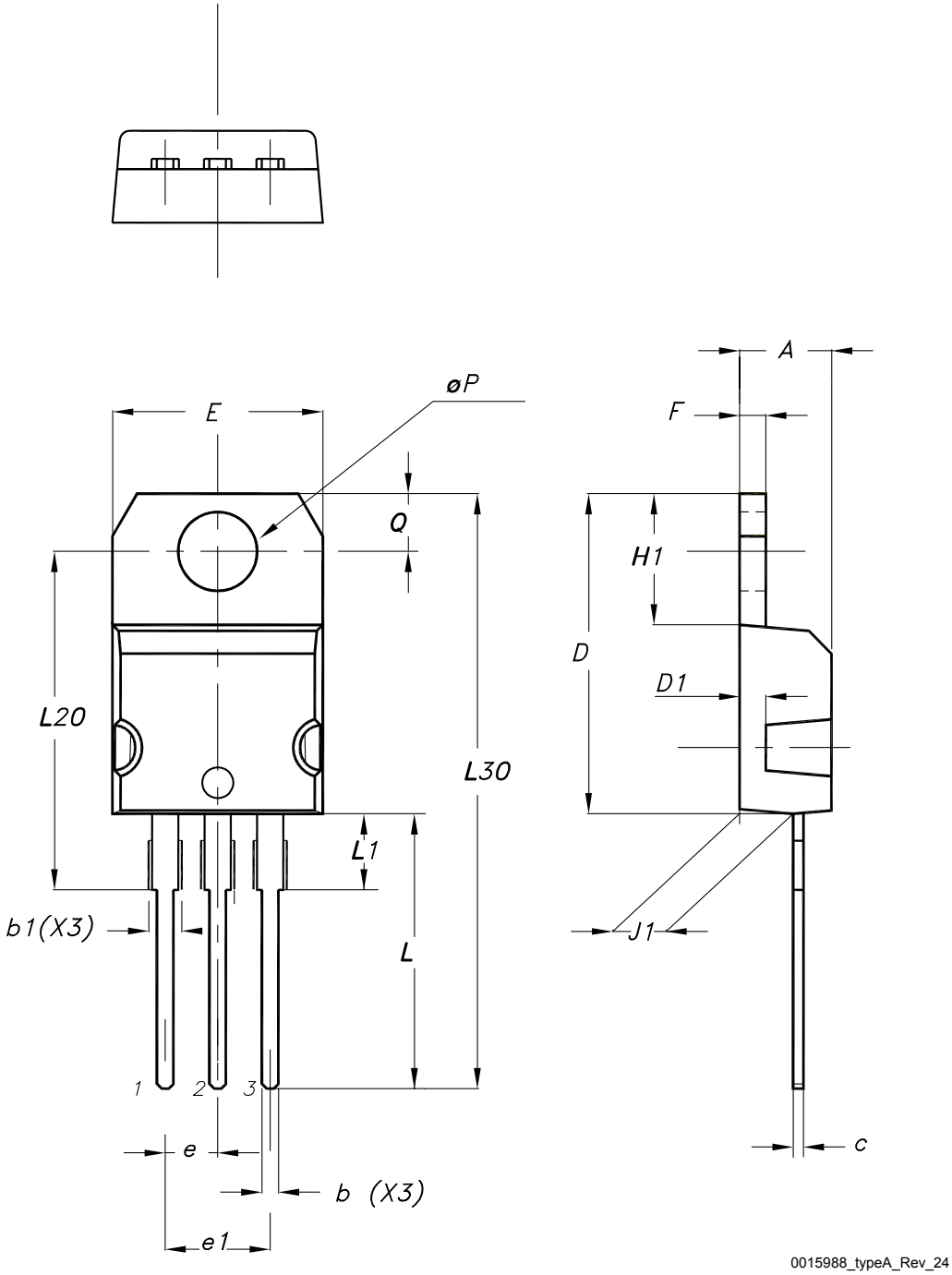
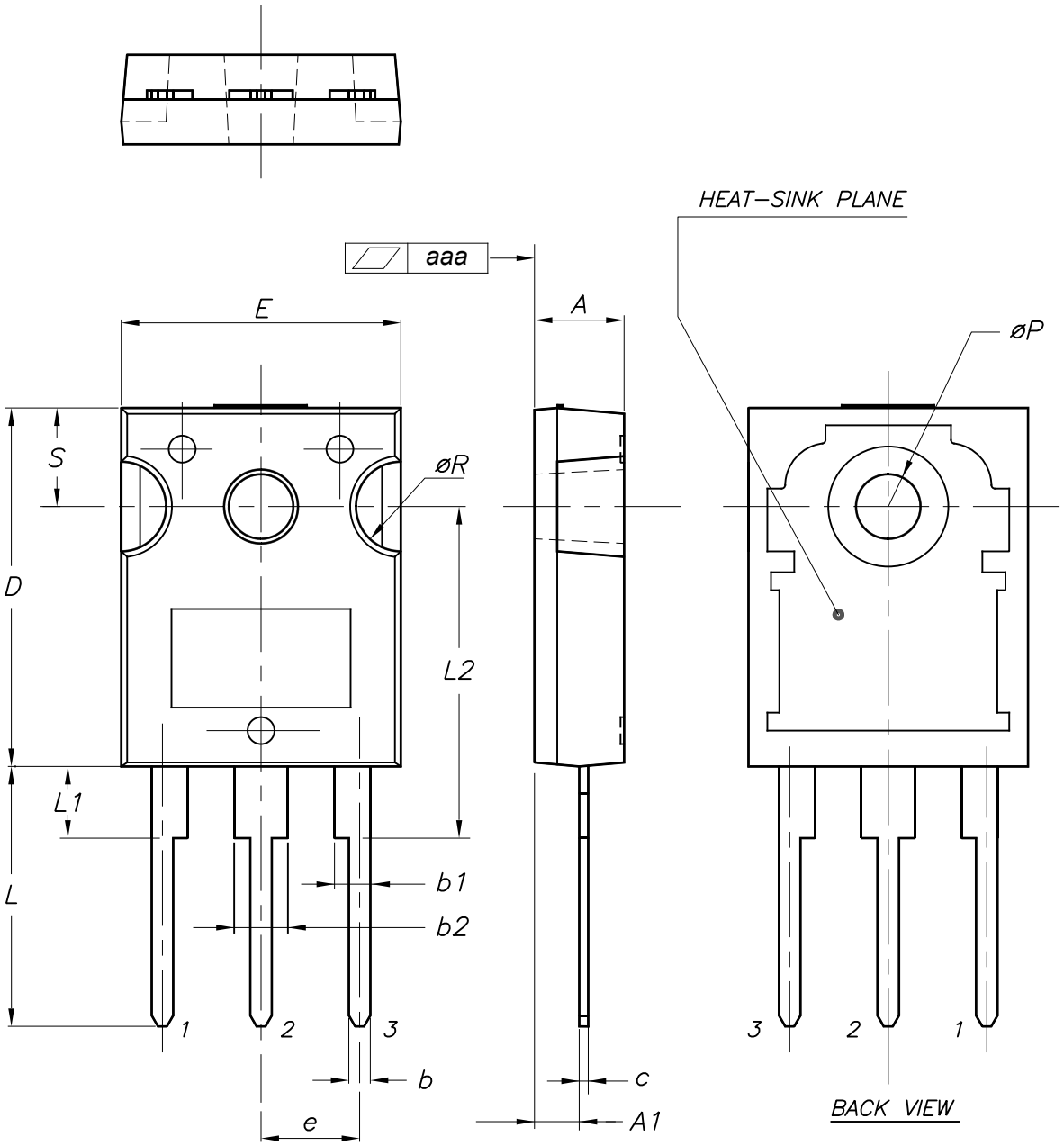


Table 10. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.4 TO-247 package information

Figure 27. **TO-247 package outline**



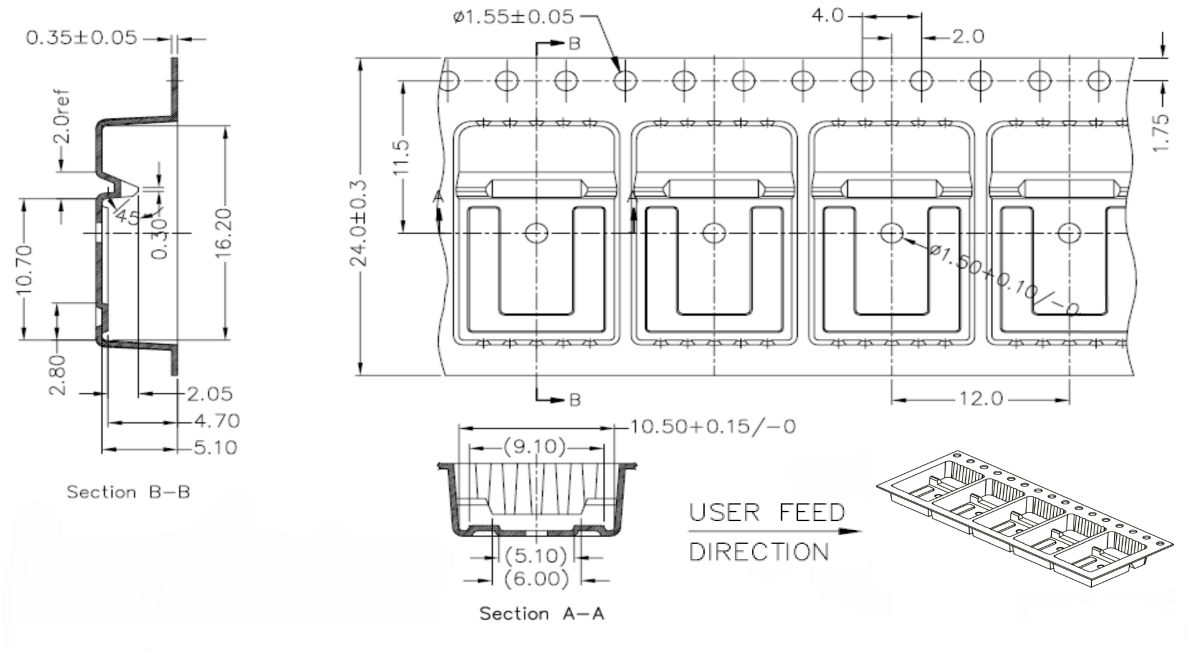
0075325_10

Table 11. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.5 D²PAK packing information

Figure 28. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

5 Ordering information

Table 12. **Order codes**

Order codes	Marking	Package	Packing
STB12NK80ZT4	B12NK80Z	D²PAK	Tape and reel
STF12NK80Z	F12NK80Z	TO-220FP	Tube
STP12NK80Z	P12NK80Z	TO-220	
STW12NK80Z	W12NK80Z	TO-247	

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
22-Jun-2004	2	Preliminary version.
28-Jan-2005	3	Complete version.
08-Sep-2005	4	*Figure 2* and *Figure 6* changed.
31-Jul-2006	5	The document has been reformatted.
27-Apr-2007	6	Modified $R_{DS(on)}$ value on *Table 5*.
28-Aug-2012	7	Inserted new device in TO-220FP. Updated *Table 1: Device summary*, *Table 2: Absolute maximum ratings* and *Table 3: Thermal data*. Updated *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data*. Minor text changes in the cover page.
28-Oct-2025	8	Updated Section 4: Package information. Minor text changes.

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