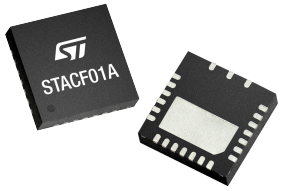
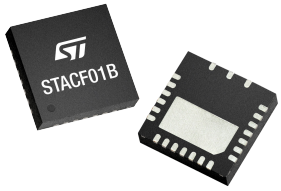
STACF01A, STACF01B

Datasheet

Active clamp flyback controller





Product status link
STACF01A
STACF01B

Product label
SUSTAINABLE TECHNOLOGY

Features

- Non-complementary control of active clamp flyback converter
- Multimode operation optimizes efficiency over a very wide load range
- Up to 500 kHz operating frequency with programmable deadtime
- Automatic reverse current control for ZVS of low-side switch
- ZCD circuit for demagnetization instant detection and OVP setting
- Embedded high-voltage startup and active x-cap discharge circuit
- Integrated buck-boost regulator for wide output voltage range
- Very low quiescent current enables ultra-low no-load input power
- Full set of protection features
- Interface with PFC controller
- Dual low-side driver and enable for easy pairing with MasterGaN family, other types of GaN power IC, or half-bridge driver IC

Applications

- High power density and USB PD chargers & adapters based on GaN HEMTS

Description

The STACF01A and STACF01B ICs drive and control active clamp flyback converters with non-complementary driving of the active clamp (high-side, HS) switch. It is specifically intended for high performance AC-DC adapters with GaN HEMTS rated up to 100 W and beyond, which are aimed at high efficiency as well as high power density.

The ICs seamlessly change operating mode with loading conditions to optimize efficiency under an extremely wide range of loads: variable frequency with frequency foldback at heavy-medium load, bottom-clamped, load-proportional frequency at light load, burst mode at very light, and no-load.

An automatic adjustment mechanism ensures that the reverse primary current needed to achieve ZVS is properly set for any input/output voltage combination.

This ICs can achieve output voltage regulation from the secondary side via an optocoupler-based feedback.

The ICs are provided with an embedded high-voltage startup circuit that also implements the line voltage monitoring system. The STACF01A also discharges the X capacitors when the converter gets disconnected from the AC power line. The STACF01B is intended for use with DC input, like SMPS with PFC in front or supplied by a DC bus.

The ICs incorporate two low-side low-power drivers intended to drive the inputs of an external high-voltage half-bridge driver ICs or an SiP such as one of the MasterGaN families.

It also provides an extensive set of protection features against primary and secondary side faults (two-level overcurrent, overpower, overload, short circuit, brownout, output overvoltage). A general protection input (active low latch type and active high autorestart) helps implement an external OTP, an external input OVP, or a general-purpose protection.

1 Block diagram

Figure 1. **Block diagram**

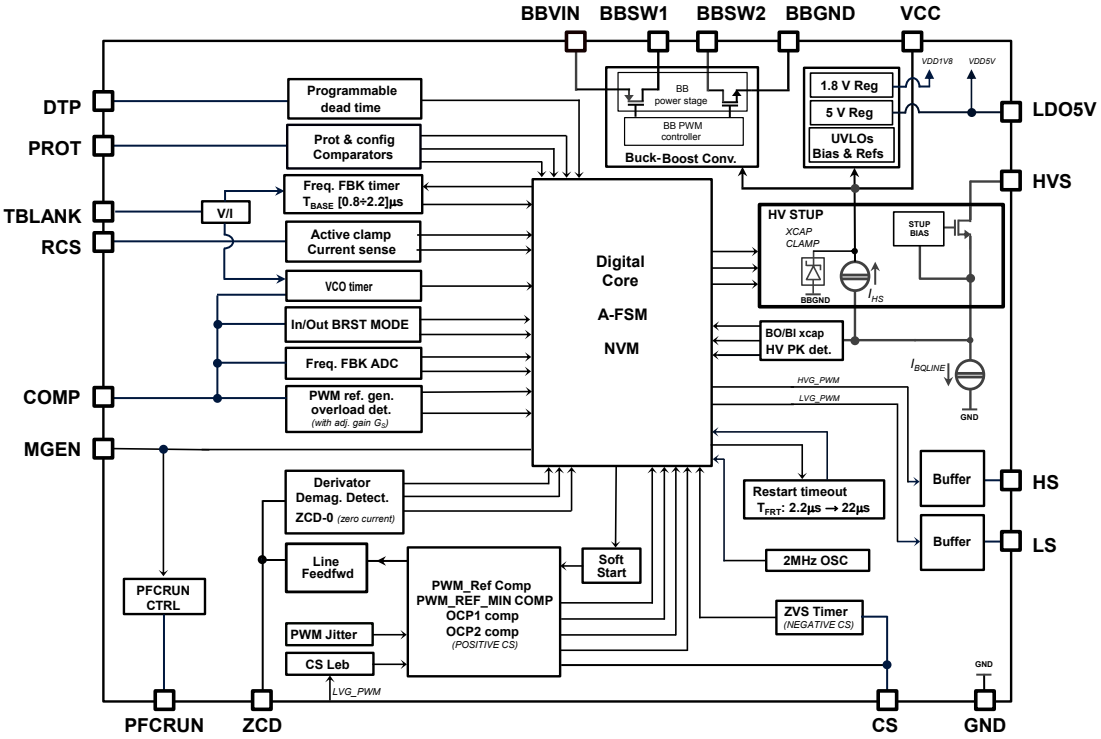


Table 1. **Device information**

Order code	X-cap discharge	Marking	Package	Packing
STACF01A	YES	STACF01A	QFN 5x5	Tray
STACF01ATR	YES	STACF01A	QFN 5x5	Tape and Reel
STACF01B	NO	STACF01B	QFN 5x5	Tray
STACF01BTR	NO	STACF01B	QFN 5x5	Tape and Reel

2 Max ratings, recommended conditions, ESD immunity levels, thermal data

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Min.	Max.	Unit
V_{HVS}	15	High-voltage startup voltage	-0.6 (1)	800	V
I_{HVS}	15	High-voltage startup source current		Self-limited	mA
I_{VCC}	9	VCC input current	0	25	mA
V_{VCC}	9	IC supply voltage (I_{VCC} < 25 mA)	-0.3	Self-limited	V
I_{LDO5V}	7	Regulator output source current	0	Self-limited	mA
V_{BBVIN}	6	Buck-boost input voltage	-0.3	30	V
V_{BBSW1}	5	Switching node voltage	-0.8	V_{BBVIN} + 0.3(2)	V
V_{BBSW2}	3	Switching node voltage	-0.3 (2)	V_{VCC} + 7	V
I_{ZCD}	22	Zero current detector sink/ source current	0	3	mA
V_{ZCD}	22	Zero current detector voltage ($\|I_{ZCD}\|$ < 3 mA)	Self-limited	Self-limited	V
V_{LS}	11	Low-side PWM drive voltage	-0.3	V_{LDO5V}	V
V_{HS}	12	High-side PWM drive voltage	-0.3	V_{LDO5V}	V
V_{RCS}	20	Reverse current sensing voltage	V_{LDO5V} –7.5	3	V
---	1, 18, 19, 21, 23	Analog inputs	-0.3	3.6	V
V_{PFCRUN}	2	Analog output voltage	-0.3	V_{VCC} + 0.3	V
V_{MGEN}	10	Analog output voltage	-0.3	V_{LDO5V} + 0.3	V
T_j	–-	Junction temperature operating range	-40	150	°C
T_{stg}	–-	Storage temperature	-55	150	°C

1. *This is a DC value. The application may experience a lower voltage for short pulses at system startup at mains zero-crossing. These undershoots must be limited to a few hundred ns.*
2. *These are DC values. Pulsed regime must be evaluated during buck-boost operation to analyze impact and set limits for overshoots of tenth of ns. All voltages are referred to GND = BBGND.*

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions. Exposure to any of the absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Min.	Max.	Unit
V_{HVS}	15	High-voltage startup voltage	-0.6	450	V
V_{BBVIN}	6	Buck-boost input voltage	0	27	V
I_{BB}	9	Total buck-boost output current (int. + ext.)	0	20	mA
V_{BBSW1}	5	Switching node voltage	-0.5	V_{BBVIN}	V
V_{BBSW2}	3	Switching node voltage	0	V_{VCC} + 0.5	V
I_{ZCD}	22	Zero current detector sink/ source current	0	2.5	mA
V_{ZCD}	22	Zero current detector voltage	-0.4	4.6	V
V_{RCS}	21	Reverse current sensing	V_{LDO5V} – 7	2.5	V
---	1, 18, 19, 21, 23	Analog inputs	0	3.3	V
V_{PFCRUN}	2	Analog output voltage	0	V_{VCC}	V
V_{MGEN}	10	Analog output voltage	0	V_{LDO5V}	V

Operating within the "recommended operating conditions", ensures performance and electrical parameter degradation remain within device specifications. Unless otherwise specified, these conditions are intended to be continuously applied.

Table 4. ESD immunity levels

Mode	Pin	Reference specification	Value	Unit
HBM	1 to 12, 19 to 24	According to JS001	± 2	kV
HBM	15	According to JS001	± 1	kV
CDM	All	According to JES002	± 500	V

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$\Theta_{th\ j\text{-}a}$	Thermal resistance, Junction-to-ambient (1)	45	°C/W
$\Psi_{th\ j\text{-}c}$	Thermal resistance, Junction-to-case	3	°C/W

1. *Obtained from simulations using JEDEC 1S1P (2 layers, 70 um Cu) FR4 PCB with thermal land and vias.*

3 Pin connections and functions

Figure 2. **Pin connection (top view)**

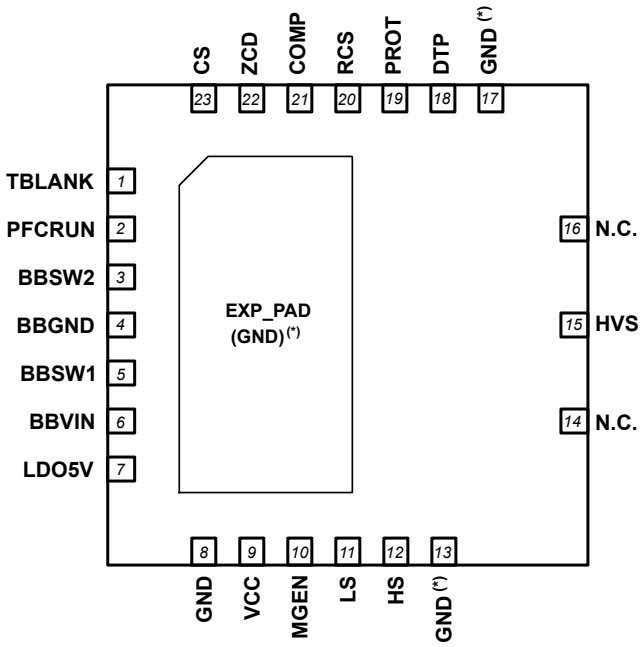


Table 6. **Pin functions**

No.	Name	Function
1	TBLANK	Frequency foldback programming input. Frequency foldback is achieved by inserting a blanking time after the turn-off of the LS drive. This blanking time increases as the load is reduced, assuming discrete values that are a multiple of a preset time interval. A resistor connected between this pin and GND sets the duration of this preset time interval in a range that goes from 0.8 to 2.2 µs with 0.2 µs steps.
2	PFCRUN	PFC stage control output. This pin is intended to enable/disable the PFC controller IC in systems comprising a PFC pre-regulator. The pin normally features a high impedance; an internal switch is closed, and the pin is pulled to ground, when the voltage at pin COMP is lower than a threshold (light load), whenever the IC is shut down by a protection function and during UVLO. If not used, the pin is left floating.
3	BBSW2	Drain connection of the low-side switch of the auxiliary buck-boost converter. The anode of the steering diode and one terminal of the buck-boost inductor are connected externally to this pin. A 30 V rated Schottky-type in SOD 123 package or similar is recommended as the steering diode. The buck-boost inductor (10 µH inductance is recommended) should have less than 1 W winding resistance to enable the converter to carry sufficient power when its input voltage is at the lowest end.
4	BBGND	Auxiliary buck-boost converter ground return. It internally connects the source of the low-side switch of the buck-boost and externally both the anode of the freewheeling diode and the (-) terminal of both the input bypass VBBIN capacitor and the output bypass VCC capacitor. A 30 V rated Schottky-type in SOD 123 package or similar is recommended as the freewheeling diode. This ground connection carries pulsed currents that should be kept separate from any bias current return. No bias component should be tied to the PCB track leading to this pin.
5	BBSW1	Source connection of the high-side switch of the auxiliary buck-boost converter. The cathode of the freewheeling diode and the other terminal of the buck-boost inductor are connected externally to this pin.

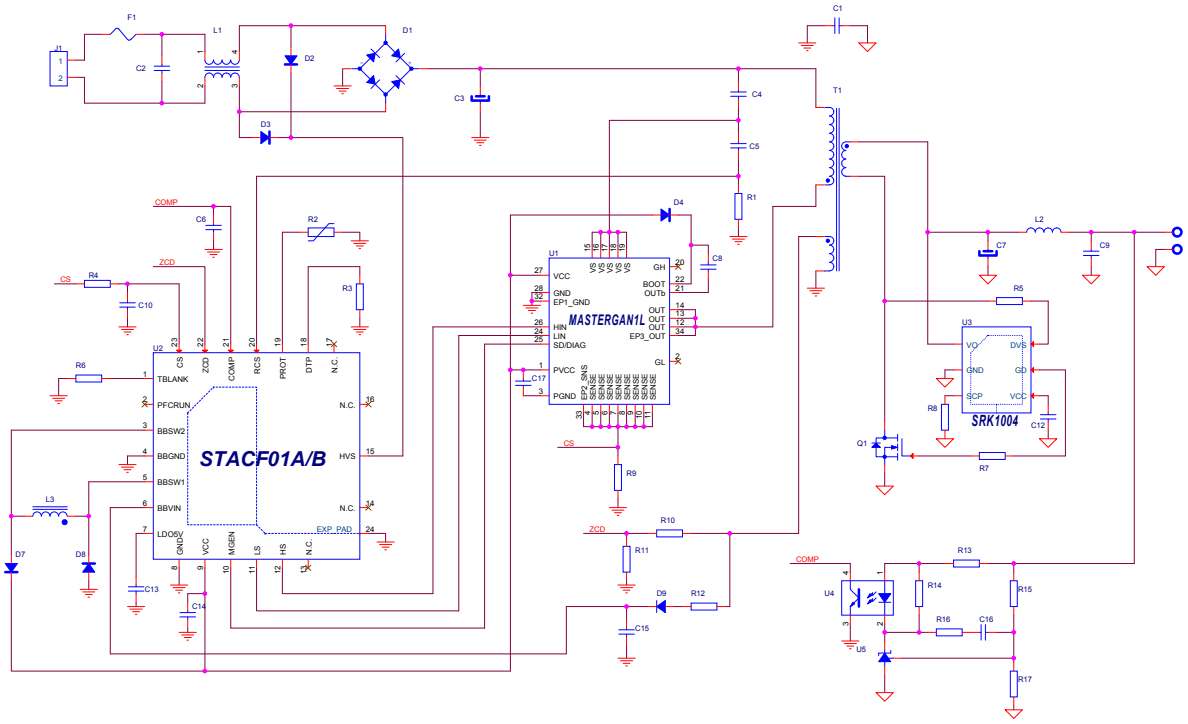
No.	Name	Function
6	BBVIN	Input pin of the auxiliary buck-boost converter. The pin internally connects the drain of the high-side switch and is externally connected to the DC voltage generated by the auxiliary winding of the flyback transformer through a diode and a reservoir capacitor. In addition to this capacitor (most likely an electrolytic one) that is located close to the diode and the winding, a few µF ceramic bypass capacitor to BBGND is connected as close as possible to the pins. This is needed to keep the pulsed currents provided by the auxiliary buck-boost converter confined within the switching loop of the converter itself. The voltage on the pin is internally monitored and if it is lower than a threshold, the buck-boost converter is disabled. Therefore, in applications where the buck-boost converter is unnecessary this pin can simply be tied to BBGND along with BBSW1 and BBSW2, and the auxiliary DC voltage brought directly to the VCC pin.
7	LDO5V	This pin is the output of the 5 V internal regulator that supplies the logic circuits of the IC. It requires a typical 47 nF ceramic bypass capacitor to the GND pin. The internal regulator can supply a limited external load current (not exceeding 1 mA).
8	GND	IC signal ground. Current return for the bias current of the IC. All the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
9	VCC	Supply voltage of the IC and output of the embedded auxiliary buck-boost converter. A capacitor to GND, whose value depends only on application requirements, serves as an energy buffer to sustain IC operation. A few µF ceramic bypass capacitor to BBGND, connected as close as possible to the pins, is needed to keep the pulsed currents provided by the auxiliary buck-boost converter confined within the switching loop of the converter itself. The cathode of the steering diode is connected to this pin too. An internal undervoltage lockout (UVLO) function enables the operation of the control circuit when the voltage on the pin reaches a certain threshold and inhibits the operation when it falls below a lower threshold.
10	MGEN	Enable/disable control output. This pin is intended to drive the enable/disable control input of an external high-voltage half-bridge driver IC or SiP such as the MASTERGAN®. While the STACF01A/B are switching, this pin provides a 5 V DC level, while providing a 0 V level whenever the IC is not switching (while in UVLO, after a fault or during the idle periods in burst mode operation). In this way, the quiescent consumption of the external driver or SiP can be reduced to help meet even the most severe light-load or no-load energy efficiency requirements. Note that the pin goes high about 500 us before the IC starts switching when exiting from UVLO, and about 16 us before restarting switching when exiting from a fault or while operating in burst mode.
11	LS	PWM output signal is used to control the gate of the low-side switch through an external half-bridge driver or SiP.
12	HS	PWM output signal is used to control the gate of the high-side switch through an external half-bridge driver or SiP.
13,17	GND	These pins are connected to the controller’s ground plane and substrate. Do not use as signal or power ground return. They can be connected to GND or left floating.
14, 16	N.C.	High-voltage spacers. These pins are not internally connected to isolate the high-voltage sections and ease compliance with safety regulations (creepage distance) on the PCB.

No.	Name	Function
15	HVS	High-voltage startup generator, AC voltage sensing input, X-cap discharger (STACF01A only). The pin, able to withstand 800 V, is to be connected to the AC side of the input bridge via a pair of diodes (1N400x type) to sense the AC input voltage. Their anodes are connected to the line and neutral conductors, while both cathodes are connected to the pin. It is recommended to connect the anodes just at the input of the rectifier bridge. If the voltage on the pin is higher than 15 V, an internal pull-up circuit charges the capacitor connected between the pin VCC and GND. Initially, the current is low for safety in case of a shorted VCC, and then it goes to the normal level as far as the VCC pin reaches the startup threshold. To reduce the hold-up requirement on the VCC cap, the generator is turned off at the end of the soft-start time. The generator is re-enabled when the voltage on the VCC pin falls below the UVLO threshold. In case the IC stops operating after a fault, the VCC cycles between the startup threshold and the UVLO threshold; the current is reduced to keep power dissipation low. The pin is also used to sense the AC voltage, which is used by the AC brownout functions. **STACF01A only:** An internal logic circuit detects that the unit has been disconnected from the power line and activates the high-voltage startup generator to discharge the X-capacitors of the EMI filter to a safe level. This allows the unit to meet safety regulations (such as IEC 62368-1) without using the traditional discharge resistor in parallel to the X-capacitors, thus saving the associated power losses and enabling ultra-low consumption in standby conditions.
18	DTP	Deadtime programming. A resistor connected between this pin and GND sets the deadtime from HS drive going low to LS drive going high. It also sets the deadtime from the LS drive going low to the first HS drive going high at half the value of the other transition.
19	PROT	General purpose external protection input. This pin is internally pulled up by a 50 µA current generator. For normal operation, the external circuit must keep the voltage on the pin between 1 and 3 V. When the voltage on this pin is forced below a set threshold (= 1 V), the controller is latched off. The unit needs to be disconnected from the power line to restart. An NTC thermistor can be connected between this pin to GND for overtemperature protection. When the voltage is allowed to reach a set threshold (= 3 V), the controller is stopped. It restarts immediately as the voltage falls below the threshold (minus hysteresis), going through a soft-start cycle. Typically, this function can be used to implement an input overvoltage protection. A small bypass capacitor to GND (≤ 330 pF) might be useful to get a clean bias voltage in noisy environments.
20	RCS	General purpose external protection input. This pin is internally pulled up by a 50 µA current generator. For normal operation, the external circuit must keep the voltage on the pin between 1 and 3 V. When the voltage on this pin is forced below a set threshold (= 1 V), the controller is latched off. The unit needs to be disconnected from the power line to restart. An NTC thermistor can be connected between this pin to GND for overtemperature protection. When the voltage is allowed to reach a set threshold (= 3 V), the controller is stopped. It restarts immediately as the voltage falls below the threshold (minus hysteresis), going through a soft-start cycle. Typically, this function can be used to implement an input overvoltage protection. A small bypass capacitor to GND (≤ 330 pF) might be useful to get a clean bias voltage in noisy environments.
21	COMP	Secondary side feedback input pin. It is used for output voltage regulation. This pin is connected to the transistor of the optocoupler; internally it is pulled up to a voltage reference. It is bypassed by a low value capacitor to GND. The error voltage at this node is also used internally for determining the various operating modes of the IC.

No.	Name	Function
22	ZCD	Multifunction pin. This pin senses a sample of signal derived from an auxiliary winding used for generating the IC bias power and to perform multiple functions. The positive signal in flyback mode is sampled and used for changing the PWM gain depending on the output voltage in variable output voltage applications (gain is higher at a high output voltage, lower at a low output voltage). This voltage information is used for overvoltage protection (OVP) too. This protection is an autorecovery type. The negative signal during the energizing period of the transformer is used to predict the input voltage for internal line feedforward. This signal is used to compensate both the propagation delay at turn-off and adjust the resulting cycle-by-cycle overcurrent setpoint. In both cases the objective is to minimize the dependence of the maximum deliverable power and of the light-load level for burst mode operation on the input voltage. The onset of the drain ringing after transformer demagnetization, which determines either the second turn-on of the high-side switch or the start of the blanking period before turning on the high-side switch (frequency foldback), is also detected through this pin. Another important functionality of the ZCD pin is to prevent CCM operation. Though DCM operation is inherent in case of normal operation, it might not be in case of operation under severe overload or short-circuit conditions.
23	CS	Current sense pin. The signal Vcs at this pin is compared with the scaled error signal for current mode control operation. An internal leading-edge blanking circuit helps achieve clean operation. A second comparator referred to a fixed level determines the maximum peak current in each switching cycle (overcurrent protection). At startup the overcurrent level reaches the final value starting from zero in 8 equal steps lasting 1 ms each (soft-start). A third comparator referred to a fixed level higher than that of the cycle-by-cycle overcurrent protection shuts down the IC in case of transformer saturation or secondary diode short-circuit. This protection is an autorestart type. A logic circuit improves sensitivity to temporary disturbances. The signal Vcs is also used by the self-adjustment mechanisms that determines the duration of the reverse current conduction (that is, the on-time of the high-side switch at the end of a switching cycle). During this period, the reverse current builds up in the primary winding by drawing energy from the clamp capacitor up to a level adequate to achieve ZVS for the low-side switch at its next turn-on. A resistance connected from this pin to the current sense resistor enables the user to tune the self-adjustment mechanism to achieve ZVS (or get close to it, if preferred) with just the right amount of reverse current. The duration of the on-time of the high-side switch just after the turn-off of the low-side one is set at 50% of the reverse current conduction interval at low line (67% at high line).
24	EXP_PAD (GND)	Exposed pad. Internally connected to the controller’s ground plane and substrate. It must be connected directly to ground and well soldered to an adequate PCB copper area to facilitate heat dissipation.

4 Typical application schematic

Figure 3. **Typical application schematic**



5 Electrical characteristics

T_j = -40 to +125 °C, V_{BBVIN} = 12 V, VCC regulated, C_{5V_LDO} = 47 nF, C_{HS} = C_{LS} = 20 pF, unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IC supply voltage (VCC)						
VCC	Operating range	After device turns on, V_{BBVIN} = gnd	5.25		6.64	V
VCC_{On}	Turn-on threshold	Voltage rising(1)	6	6.3	6.9	V
VCC_{Off}	Turn-off threshold	Voltage falling(1)	4.6	4.9	5.2	V
VCC_Z	Zener voltage	I_{VCC} = 20 mA	6.64	6.9	7.1	V
Supply current (VCC)						
I_{Q_UV}	Startup current	Before device turns on, VCC = VCC_{On} - 0.2 V		0.4		mA
I_{Q_BURST}	Quiescent current	Idle during burst mode, V_{COMP} = 1 V, T_j =25°C		0.85	1.3	mA
I_{Q_OP}	Operating current	Device on, switching		3.3	4.2	mA
I_{Q_FAULT}	Residual consumption	After protection tripping		0.8		mA
Auxiliary buck-boost converter (BBVIN, BBSW1, BBSW2, VCC)						
V_{BBVIN}	Operating range	After being enabling	2.4		27	V
V_{BBVIN_On}	Enable threshold	Voltage rising(1)	2.4	2.5	2.6	V
V_{BBVIN_Off}	Disable threshold	Voltage falling(1)	2.2	2.3	2.4	V
VCC_{reg}	Regulated output voltage	I_{VCC} = 10 mA, V_{BBVIN}≥ 2.5 V(1)	6.0	6.25	6.5	V
VCC_{res}	Restart threshold during burst mode operation	(1)	5.15	5.4	5.7	V
$R_{DS(on)-HS}$	Low-side switch on-resistance			2	3.5	Ω
$R_{DS(on)-LS}$	Low-side switch on-resistance			1.3	2.5	Ω
$I_{BBSW2pk}$	Peak current threshold		0.15	0.2	0.28	A
T_{OFF}	Switches off-time	V_{BBVIN} = 4 V		0.4		µs
		V_{BBVIN} = 20 V		1.5		
High-voltage startup current generator (HVS)						

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{HVS_BD}	Breakdown voltage	I_{HVS} < 100 µA	800			V
V_{HVS_start}	Start voltage (rising)	VCC can reach VCC_{On}	10		21	V
I_{HVS_CHARGE}	On-state VCC charge current	V_{HVS} > $V_{HVS\ start}$, VCC = 0.5 V @ T_j = 25 °C		0.75		mA
		V_{HVS} > $V_{HVS\ start}$, VCC = 2.8 V @ T_j = 25 °C		5.5		
I_{HVS_SINK}	Sink current (to GND)	VCC falling during brownout	250	360	470	µA
I_{HVS_OFF}	Off-state residual current	V_{HVS} = 400 V, T_j = 25 °C		16		µA
X-capacitor discharge function (HVS) - STACF01A only						
T_{DET}	Line disconnection detection timeout			64		ms
V_{HVSmin}	Residual voltage	After discharge is over			45	V
I_{HVS_DIS}	Discharge current	V_{HVS} > V_{HVSmin}	4			mA
LINE monitoring functions (HVS)						
V_{HVSpk_BO}	Brownout threshold	Voltage falling (peak) (2)	81	95	110	V
V_{HVSpk_BI}	Brown-in threshold	Voltage rising (peak)(2)	107	116	122	V
t_{DB}	Debounce time	Brown-in		40		ms
		Brown-in		1		
V_{HVSpk_HL}	High line detect threshold	Voltage rising (peak)(2)	218	234	248	V
V_{HVSpk_LL}	High line detect threshold	Voltage falling (peak)(2)	184	200	212	V
Deadtime programming (DTP)						
V_{DTP}	Voltage reference	R_{DTP} ≥ 10 kΩ(2)		0.6		V
T_D	Programming range	From LS ↓ to HS ↑ and from HS ↓ to LS ↑	50		350	ns
T_D	Programmed value from LS ↓ to HS ↑	R_{DTP} = 21 kW		105		ns
Current sense input (CS)						
I_{CS}	Bias current				1	µA
$t_{d(H-L)}$	Delay to output (from Vcs_{ref} hitting to LS ↓)	No load on LS, dV_{CS}/dt = 0.4 V/µs			80	ns
T_{LEB}	Leading edge blanking after LS turn-on	During soft-start & bursts	120	150	200	ns

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{LEB}	Leading edge blanking after LS turn-on	After soft-start end	40	50	75	ns
V_{CSx-0}	Cycle-by-cycle OCP level	V_{COMP} = V_{COMPhi}, I_{ZCD} = 0 (2)	0.71	0.75	0.79	V
V_{CSref_OL}	Overload threshold (voltage rising)	SampledV(ZCD)≥ V_{ZCD_HGs}(2)	0.76	0.8	0.84	V
		SampledV(ZCD)≤ V_{ZCD_LGs}(2)	0.475	0.5	0.525	
V_{CS_OCP2}	2nd OCP level	(2)	1.1	1.2	1.3	V
T_{Onmax}	Maximum on-time		6	8	10	µs
PWM control voltage (COMP)						
V_{COMPhi}	Upper saturation voltage	I_{COMP} = 0	2.98			V
V_{COMPlo}	Lower clamp level	I_{COMP} ≤-1 mA(2)		0.95	1	V
$I_{COMPmax}$	Maximum source current	V_{COMP} = V_{COMPlo}		300	410	µA
R_{COMP}	Dynamic resistance	V_{COMPlo} < V_{COMP} < $V_{COMPsat\_hi}$	11	14	17	kΩ
Gs	Gain (ΔVcs/ ΔV_{COMP})	Sampled V(ZCD) ≥ V_{ZCD_HGs}	0.377	0.386	0.4	V/V
		Sampled V(ZCD) ≤ V_{ZCD_LGs}	0.314	0.321	0.328	
V_{COMP_OFF}	Control voltage offset	(2)	0.18	0.2	0.225	V
Zero current detector (ZCD)						
V_{ZCDA}	ZCD arming voltage	Voltage rising(2)		75		mV
V_{ZCDT}	ZCD triggering voltage	Voltage falling(2)		50		mV
$(dV_{ZCD}/dt)_{min}$	Min. detectable slope	Voltage falling	0.055	0.1	0.165	V/µs
V_{ZCDLC}	Lower clamp voltage	I_{ZCD} = -100 µA to -2.5 mA	-0.4	-0.2	0	V
V_{ZCDUC}	Upper clamp voltage	I_{ZCD} = 10 µA to 2.5 mA	4.6			V
V_{ZCD_HGs}	High Gs setting threshold	Voltage rising(2)	1.64	1.7	1.77	V
V_{ZCD_LGs}	Low Gs setting threshold	Voltage falling(2)	1.59	1.65	1.71	V
I_{ZCDb}	Static input bias current	V_{ZCD} = 2.5 V			1.5	µA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{FRT}	Forced restart timeout	After soft-start end(3)	2	2.2	2.4	µs
		During soft-start(3)	17		26	
Reverse current self-adjustment (CS)						
Ics_{ZVS}	Adjustment current, active from HS ↓ to LS ↑	V_{HVSpk} = 120 V	25	30	40	µA
		V_{HVSpk} = 360 V	75	90	115	
Reverse current sensing (RCS)						
V_{RCSx}	Overcurrent threshold	(2)	-0.5	-0.46	-0.44	V
T_{RCS}	Propagation delay	From V_{RCSx} hitting to HS ↓		90	120	ns
Line feedforward function (ZCD)						
R_{FFe}	Feedforwardgain DV_{CSx} /I_{ZCD}	I_{ZCD} = -100 µA to -2.5 mA		240		mV/mA
Soft-start function						
T_{SS}	Soft-start time	(3)	5.5	8	11	ms
Tblank setting and frequency foldback function (TBLANK)						
T_{BASE_r}	Programmable range	Typical value	0.8		2.2	µs
T_{BASE}	Time base	R_{TBLANK} = 150 kΩ(3)	0.72	0.8	0.92	µs
		R_{TBLANK} = 71.5 kΩ(3)	1.44	1.6	1.76	
		R_{TBLANK} = 9.1 kΩ(3)	1.94	2.2	2.46	
T_{BLANK1}	1st blanking time	From instant of zero current detection	T_{BASE}			µs
T_{BLANK2}	2nd blanking time		2 T_{BASE}			
T_{BLANK3}	3rd blanking time		4 T_{BASE}			
T_{BLANK4}	4th blanking time		6 T_{BASE}			
T_{BLANK5}	5th blanking time		10 T_{BASE}			
V_{COMP_TB0-1}	No blanking → T_{BLANK1}	Voltage falling(2)		1.4		V
V_{COMP_TB1-2}	T_{BLANK1} → T_{BLANK2}	Voltage falling(2)		1.35		
V_{COMP_TB2-3}	T_{BLANK2}→ T_{BLANK3}	Voltage falling(2)		1.3		
V_{COMP_TB3-4}	T_{BLANK3}→ T_{BLANK4}	Voltage falling(2)		1.25		
V_{COMP_TB4-5}	T_{BLANK4}→ T_{BLANK5}	Voltage falling(2)		1.2		

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{COMP_TB5-4}	$T_{BLANK5}\rightarrow T_{BLANK4}$	Voltage rising(2)		1.7		V
V_{COMP_TB4-3}	$T_{BLANK4}\rightarrow T_{BLANK3}$	Voltage rising(2)		1.75		
V_{COMP_TB3-2}	$T_{BLANK3}\rightarrow T_{BLANK2}$	Voltage rising(2)		1.8		
V_{COMP_TB2-1}	$T_{BLANK2}\rightarrow T_{BLANK1}$	Voltage rising(2)		1.85		
V_{COMP_TB1-0}	$T_{BLANK1}\rightarrow$ No blanking	Voltage rising(2)		2.1		
Voltage-controlled oscillator						
F_{osc1}	Oscillation frequency	$V_{COMP} = V_{COMP\_TB4-5}$(3)		80 / T_{BASE} [us]		kHz
F_{osc2}	Oscillation frequency	$V_{COMP} = V_{COMP\_BM}$(3)	22.5	25	27.5	kHz
Burst mode function (COMP)						
V_{COMP_BM}	Onset threshold	Voltage falling(2)	0.95	1	1.05	V
V_{BM_Hys}	Hysteresis	Voltage rising		50		mV
V_{COMP_EBM}	Exit threshold	Voltage rising(2)	1.1	1.15	1.2	V
N_{CYmin}	Min. # cycles per burst			3		---
N_{CYmax}	Max. # cycles per burst			32		---
F_{sw_BM}	Switching frequency	Within a burst(3)		50		kHz
V_{CSref_BM}	Current sense reference during burst mode	Sampled $V(ZCD) \geq V_{ZCD\_HGs}$ $V_{COMP} < V_{COMP\_EBM}$	200	230	255	mV
		Sampled $V(ZCD) \leq V_{ZCD\_LGs}$ $V_{COMP} < V_{COMP\_EBM}$	125	155	190	
Overload/overcurrent protection timers						
T_{OVL}	Overload timeout	$V_{CSref} \geq V_{CSref\_OVL}$(3)	33	50	67	ms
$T_{RESTART}$	Restart delay after fault	(3)	0.8	1.2	1.6	s
OVP function (ZCD)						
V_{ZCD_OVP}	Voltage Reference for sampled V_{ZCD}	(2)	2.9	3	3.2	V
N_{OVP}	Consecutive cycles for OVP tripping			4		---
Linear regulator output (LDO5V)						
V_{LDO5V}	Regulator setpoint	I_{LDO5V} = 1 mA	4.8	5	5.2	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{LDO5V}	Max source current	Externally available	1			mA
C_{LDO5V}	Allowable cap range		10		100	nF
$UVLO_{LDO5V}$	Undervoltage threshold			3.75		V
PFC CONTROL FUNCTION (PFCRUN)						
I_{PFCRUN_high}	High level leakage current	V_{PFCRUN} = V_{VCC}			1	µA
V_{PFCRUN_low}	Low saturation level	I_{PFCRUN} = 1 mA			0.2	V
ENABLE/DISABLE output (MGEN)						
V_{MGEN_high}	Output high voltage	I_{MGEN} = -6 mA	4.5	4.9		V
V_{MGEN_low}	Output low voltage	I_{MGEN} = 6 mA			0.4	V
General purpose disable input (PROT)						
$V_{PROT\_TH\_L}$	Latch-off threshold	Voltage falling(2)	0.94	1	1.04	V
V_{PROT_Hys-l}	Hysteresis	Voltage rising		100		mV
V_{PROT_USV}	Upper saturation voltage	Pin open	3.8			V
I_{PROT}	Pull-up current	V_{PROT} = 1.1 V	-70	-50	-35	µA
$V_{PROT\_TH\_H}$	Autorestart halt threshold	Voltage rising(2)	2.88	3	3.3	V
V_{PROT_Hys-h}	Hysteresis	Voltage falling		100		mV
PWM outputs (LS & HS)						
V_{PWMH}	Output high voltage	I_{source} = -6 mA	4.5	4.9		V
V_{PWML}	Output low voltage	I_{sink} = 6 mA			0.4	V

1. *Parameters tracking each other.*
2. *Parameters tracking each other.*
3. *Parameters tracking each other.*

6 Application information

The STACF01A/B ICs are intended to drive and control active clamp flyback (ACF) converters with the non-complementary approach in high performance AC-DC adapters aimed at high efficiency and high power density.

The ICs achieve output voltage regulation using a control signal coming from the secondary side by means of an input pin intended to be driven by an optocoupler.

The device can work in different modes, depending on the converter's load conditions:

1. Variable frequency mode (VF mode) at heavy load
2. Frequency foldback mode (FFBK mode) at intermediate load
3. Voltage-controlled frequency mode (VCO mode) at light load
4. Burst mode (BM) at very light or no load.

Seamlessly changing from one mode to another as load conditions dynamically vary over time.

The objective of these multiple operating modes is to optimize converter efficiency over the widest load range. In an ACF converter this task is more challenging than in a conventional flyback converter. In fact, the energy necessary to achieve ZVS for the LS switch and controlled by the reverse current build-up process is essentially constant with the load. Then, although it involves a small portion of the processed power at nominal load, it may become a significant portion of it at light load, thus becoming a major source of the converters' efficiency drop.

Due to the nature of VF mode operation, when the converter is lightly loaded this effect is exacerbated by the switching frequency rising significantly. In addition, with a higher switching frequency switching losses increase correspondingly, and efficiency drops even more.

6.1 Theory of VF mode operation

As shown in the timing diagram of Figure 4, when the STACF01A/B ICs (and the ACF converter, consequently) works in this mode, each switching cycle includes three main distinct time intervals:

- Transformer magnetization. This time interval starts as the low-side (LS) switch is turned on and ends when the current in the transformer's primary winding reaches the level programmed by the control loop that regulates the output voltage. The LS switch is then turned off and its drain voltage goes up.

If the initial negative current (necessary condition to achieve zero-voltage switching, ZVS) is much smaller than the final peak current Ip_{pk}, the duration of this time interval can be expressed as:

$$T_{ON} \approx \frac{Lp}{Vin} Ip_{pk} \quad (1)$$

where *Lp* is the inductance of the primary winding and *Vin* the DC input voltage.

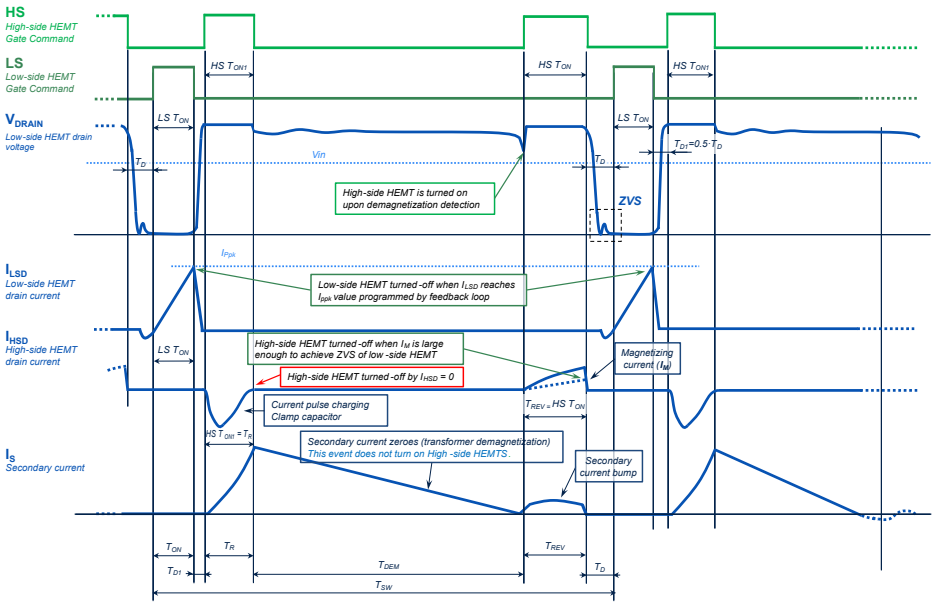
- Transformer demagnetization. After the LS switch turns off, in a first sub-interval the energy stored in the transformer's leakage inductance is transferred to the clamp capacitors in a resonant fashion. During this first sub-interval, whose duration is denoted with T_R, current starts to build up also on the secondary side and reaches a peak value as the primary current touches zero. During this time sub-interval, the high-side switch (HS) is turned on to let this current flow with a minimum source-drain voltage drop (when operated in the third quadrant, HEMT switches have a source-drain voltage drop of 3-4 V if the gate is not driven high).

Then, a second subsequent sub-interval starts where both primary switches are off and the secondary current linearly decays to zero while the energy stored in the clamp capacitor is retained. This time interval ends as the secondary current drops to zero, an event captured by the demagnetization detection circuit (ZCD).

Denoting with V_R the voltage reflected across the primary winding during this time interval, which equals the output voltage V_{out} times the primary-to-secondary turns ratio *n*, its overall duration is approximately:

$$T_{DEM} \approx \frac{Lp}{V_R} Ip_{pk} \quad (2)$$

Figure 4. ACF converter key waveforms (VF mode operation, steady-state full load conditions)



- Reverse current build-up. As the secondary current has zeroed, the high-side (HS) switch is turned on so that the energy of the leakage inductance stored in the clamp capacitor is put into play by driving the primary current in the reverse direction. The objective is to transfer enough energy to the transformer's primary magnetizing inductance to turn on the LS switch with ZVS. Note that, while energy is transferred to the magnetizing inductance, a significant amount of energy is transferred to the secondary winding too. In fact, due to the leakage energy charged during the previous time interval, the voltage across the clamp capacitor is larger than the reflected voltage V_R. As a result, as the HS switch is turned on, the secondary rectifier is forward-biased and current flows on the secondary side too. The duration T_{REV} of the reverse current build-up time interval is set by a timer controlled by an adaptive system that adjusts T_{REV} to achieve ZVS for the LS switch. At the end of this time, the HS switch is turned off and, after a short user-programmable time interval (deadtime, T_D), the LS switch is turned on, initiating a new switching cycle.

The total duration T_{sw} of the switching period is given by:

$$T_{sw} = T_{ON} + T_R + T_{DEM} + T_{REV} \approx Lp\left(\frac{1}{V_{in}} + \frac{1}{V_R}\right)Ip_{pk} + T_R + T_{REV} \quad (3)$$

Considering that, the ACF converter essentially being a DCM (Discontinuous Conduction Mode) flyback converter, switching frequency f_{sw} (= $1/T_{sw}$) and input power *Pin* are related by:

$$Pin = \frac{1}{2}LpIp_{pk}^2 f_{sw} \quad (4)$$

Combining this equation with Eq (3), after some algebra it is possible to find the following expression for the resulting switching frequency:

$$f_{sw} = 2\frac{f_B}{1 + 2(T_{REV} + T_R)f_B + \sqrt{1 + 4(T_{REV} + T_R)f_B}} \quad (5)$$

In this expression, f_B is the operating frequency the converter would work at, if operated exactly at the boundary between CCM (Continuous Conduction Mode) and DCM:

$$f_B = \frac{1}{2PinLp\left(\frac{1}{Vin} + \frac{1}{V_R}\right)^2} \quad (6)$$

It is apparent from this analysis that, when the ACF converter operates in VF mode, its switching frequency tends to increase as the load is reduced (both T_{ON} and T_{DEM} decrease, whereas T_{REV} does not change significantly).

Determining how the switching frequency changes with the input voltage V_{in} is less straightforward. Notice, however, that if we exclude T_{REV}, the timings of an ACF operated in VF mode are essentially those of a QR (quasi-resonant) flyback converter operated with valley switching. It is known that in this converter the switching frequency monotonically increases with the input voltage, though with a declining rate of rise. With a given load, the maximum switching frequency always occurs at the maximum input voltage.

In the ACF case, the presence of the term T_{REV}, which typically increases with V_{in} unlike the other terms, may slow down the rate of rise of the switching frequency further and even reverse the trend when T_{ON} and T_{DEM} are small. Especially in high-frequency designs and at light load, the maximum switching frequency is not reached at the maximum input voltage.

6.2 Theory of FFBK mode operation

As *Pin* decreases f_{sw} tends to increase and a mechanism of frequency foldback (FFBK) is introduced to prevent f_{sw} from reaching too high values and efficiency from quickly dropping at medium/light load.

In FFBK mode a fourth time interval (T_{WAIT}) is inserted between the transformer demagnetization interval T_{DEM} and the reverse current build-up interval T_{REV}: as the secondary current zeroes, the HS switch is not turned on immediately but after the time interval T_{WAIT} has elapsed. More specifically, a blanking time T_{BLANK} starts off as demagnetization ringing is detected and the turn-on of the HS switch is commanded on the first peak of the ringing after T_{BLANK} has elapsed (therefore, $T_{WAIT} \geq T_{BLANK}$). In this way, the turn-on losses of the HS switch are minimized. This operation is shown in the timing diagram of Figure 5.

T_{BLANK} is increased in discrete steps as the load is reduced (that is, as the control voltage V_{COMP} decreases), according to the diagram shown in Figure 6. In this way, the converter's switching frequency is forced to progressively lower values that depend more and more on the set T_{BLANK} rather than T_{ON}, T_{DEM}, and T_{REV}, as T_{BLANK} is increased.

The set of possible values of T_{BLANK} includes five elements, T_{BLANKx} (x = 1, …, 5), that are multiples of a time T_{BASE} that is user-programmable in a range going from 0.8 µs to 2.2 µs.

Figure 5. ACF converter key waveforms (FFBK mode, steady-state medium load conditions)

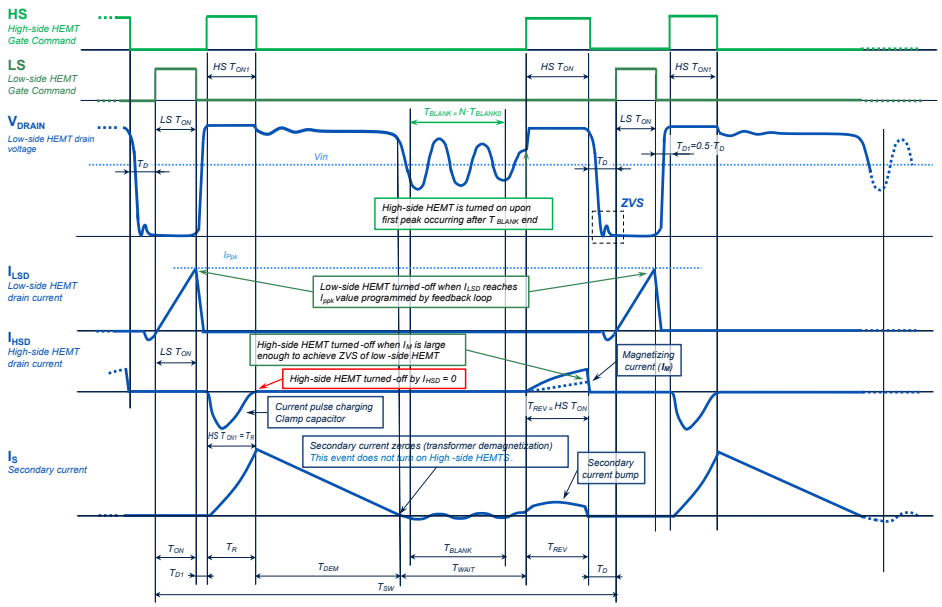
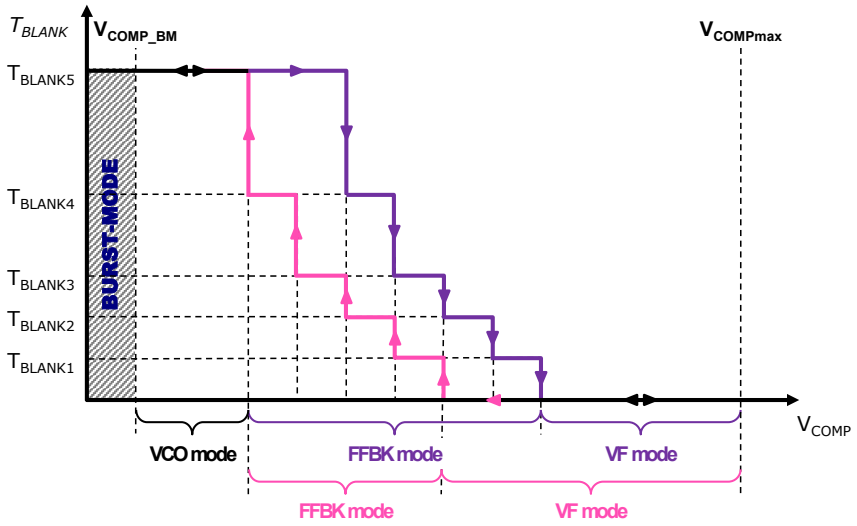


Figure 6. T_{BLANK} vs. V_{COMP} map



Compared to the traditional “valley skipping” technique, which consists in skipping one-by-one more cycles of the drain ringing as the load is reduced, the resulting frequency reduction is much larger. Especially in high frequency designs, where the drain ringing period is quite short, valley skipping results in a limited frequency reduction. With this technique, instead, the frequency reduction is substantial. In addition, it is worth noting that at the lower end of the FFBK region (that is, when T_{BLANK}=T_{BLANK5}) the switching frequency depends very little on the design of the converter.

An appropriate hysteresis in the comparators that set T_{BLANK} ensures that no “blanking jump” occurs. Once T_{BLANK} is set at T_{BLANKx} (x = 1, …, 5), it stays locked to that value unless the load changes significantly. Only in this case does it move to $T_{BLANKx-1}$ or $T_{BLANKx+1}$, depending on whether the load increases or decreases.

At light load, when the IC sets the longer blanking times, it is very likely that the damped oscillations of the drain ringing after T_{BLANK} has elapsed are so small that they cannot be detected by the ZCD circuit. In this case, to prevent the converter from getting stuck, T_{WAIT} is forced to an end by a timeout circuit that starts as T_{BLANK} has elapsed and forces the HS switch to turn on if the voltage on the ZCD pin is lower than the triggering threshold V_{ZCDT} and does not exceed the arming threshold V_{ZCDA} for more than T_{FRT} (about 2 µs). On the other hand, when the oscillations are so small that peaks cannot be detected anymore, turning on the HS switch in any instant does not make a difference in terms of turn-on losses. This situation is shown in Figure 7.

Whichever T_{BLANKx} it is, it is possible to state that $T_{BLANKx} \le T_{WAIT} \le T_{BLANKx} + T_{FRT}$.

6.3 Theory of VCO mode operation

Once the IC enters the T_{BLANK5} region, the minimum achievable switching frequency is relatively low: the switching period is largely dominated by T_{BLANK5}+ T_{FRT} (10·T_{BASE} + 2 µs); T_{ON}, T_{DEM}, and T_{REV} account for few additional µs. The FFBK mechanism does not provide any further frequency reduction and the resulting minimum frequency can still be a relatively high switching frequency to achieve good efficiency at very light load. To further decrease the switching frequency, the VCO mode operation is provided: with this mode, active in the T_{BLANK5} region only, the switching frequency is linearly reduced with the control voltage V_{COMP}:

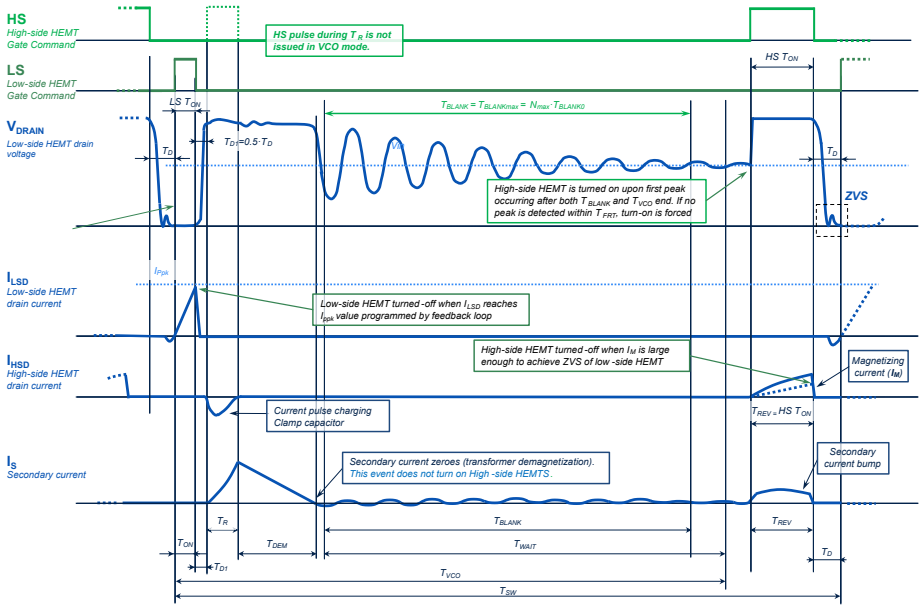
$$f_{sw} = 25 \cdot 10^3 + K_{sw}(T_{BASE})\,(V_{COMP} - V_{COMPBM}) \quad (7)$$

The VCO gain $K_{sw}(T_{BASE})$ is such that f_{sw} = 80·10^{-3}/T_{BASE} when V_{COMP} = $V_{COMP\_TB4\text{-}5}$, the threshold that marks the transition from the T_{BLANK4} region to the T_{BLANK5} region of FFBK mode. V_{COMPBM} is the lower end of the VCO mode region, where operation transitions to burst mode to handle very light or no-load conditions.

The VCO gain, $K_{SW}(T_{BASE})$, is inversely proportional to T_{BASE}. The expected f_{SW} transitions are shown in Figure 8 for two different T_{BASE} programmed values. It is important to note that, regardless of the $K_{SW}(T_{BASE})$ value, the switching frequency at the boundary between VCO and burst mode operating regions (that is, when V_{COMP} = V_{COMP_BM}) is constant and equal to 25 kHz.

To ensure a seamless transition between FFBK and VCO modes, the VCO oscillator provides a blanking time T_{VCO} that starts as the low-side switch is turned on.

Figure 7. ACF converter key waveforms (FFBK / VCO mode, steady-state light load conditions)



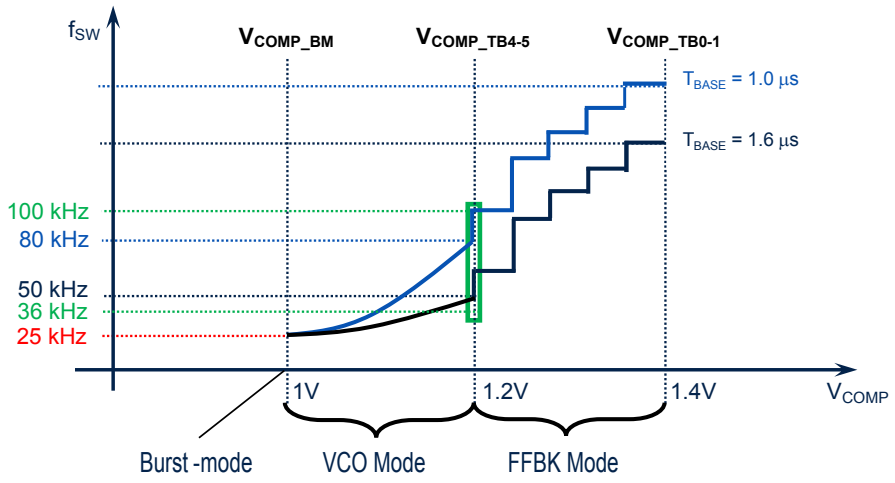
This blanking acts in logic AND with that of the FFBK mode, so that:

- If the drain ringing amplitude is such that it is still detectable by the ZCD circuit, the HS switch is turned on upon the first peak occurring after both T_{BLANK} and T_{VCO} have elapsed;
- If the drain ringing is no longer detectable by the ZCD circuit, since the T_{FRT} timeout circuit is enabled when both blanking times are over, the HS switch is turned on with a delay T_{FRT} after the longer time between T_{BLANK} and T_{VCO}.

When the converter operates in this mode the waveforms are essentially identical to those related to the operation in FFBK mode in the T_{BLANK4} or T_{BLANK5} regions and shown in Figure 7, just T_{WAIT} is longer.

Finally, note that in VCO mode the HS turn-on during the clamp capacitor recharge time T_R does not take place to reduce switching losses. The current for the clamp capacitor charge flows through the HEMT operating in the third quadrant.

Figure 8. **FFBK to VCO transition map for two different T_{BASE} values**



6.4 Theory of BM operation

When the load is extremely light or totally disconnected, the control voltage V_{COMP} eventually falls below V_{COMP_BM} (= 1 V), the lower end of the VCO mode operation. By construction of the VCO (see Eq. (7)), the switching frequency at this boundary condition is 25 kHz, then well above the audible range.

When this occurs, a HALT signal is sent to the state machine that supervises the operation of the IC to instruct the IC to stop upon the first turn-off of the LS switch occurring after receiving the HALT signal.

From this moment on, the converter operates intermittently with a series of a few switching cycles spaced out by long idle periods where both switches are in the OFF state. This is what is called burst mode (BM) operation. As a result, the average switching frequency, the average value of the reverse current and the associated losses are considerably cut down, thus facilitating the converter to comply with energy saving recommendations related to standby consumption.

In the idle state, the converter being stopped, no energy is delivered to the output, so the output voltage starts decaying. The feedback circuit reacts to this droop and, as a consequence, V_{COMP} increases and, as it exceeds V_{COMP_BM} by the comparator's hysteresis (50 mV), the IC restarts switching. If the load level has not changed, after a short while V_{COMP} falls again below V_{COMP_BM} in response to the energy burst and stops the IC again. Note that the state machine that supervises the operation of the IC envisages that each burst includes a minimum of three switching cycles.

As long as the converter works in burst mode, which is flagged by an internal signal (BM_ON) set high, three actions aimed at optimizing energy transfer are taken:

- The VCO is disabled, and the switching frequency is that corresponding to $V_{COMP} = V_{COMP\_TB4\text{-}5}$, that is: $f_{sw} \approx 80 \cdot 10^{-3} / T_{BASE}$.
- The reference V_{CSref} for the peak primary current is increased by 15% and is kept constant throughout the bursts.
- The HS switch is turned on in the second switching cycle in a burst and, in case of long bursts, after the following LS pulses: 9th, 16th, 24th, and 32nd. On the one hand, this substantially reduces the losses associated with the reverse current, as well as switching and driving losses of the HS switch; on the other hand, turning on the HS switch periodically helps prevent the clamp capacitor voltage from drifting high uncontrollably with no need of an external bleeder resistor.

The IC exits from burst mode, that is, the BM_ON flag is set low, when $V_{COMP} \geq V_{COMP\_EBM}$ or when there are more than 32 switching cycles in a single burst.

Burst mode operation is shown in the timing diagram of Figure 9.

Figure 9. ACF converter key waveforms (very light load, burst mode, view of a single burst)

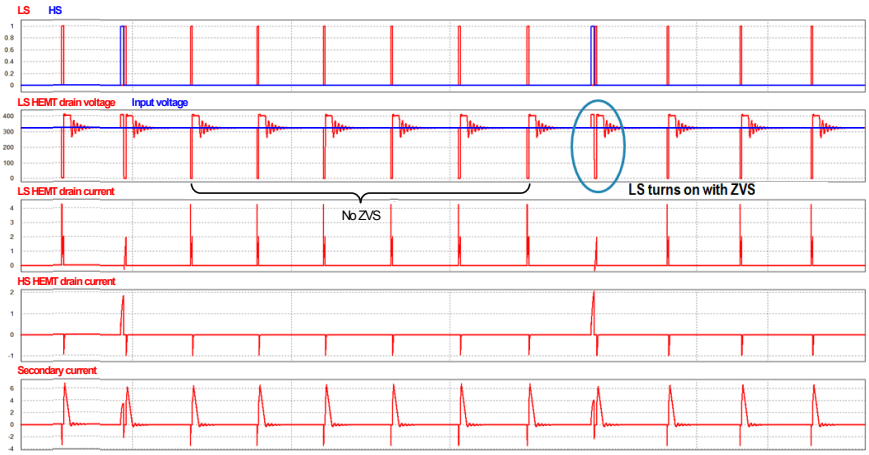
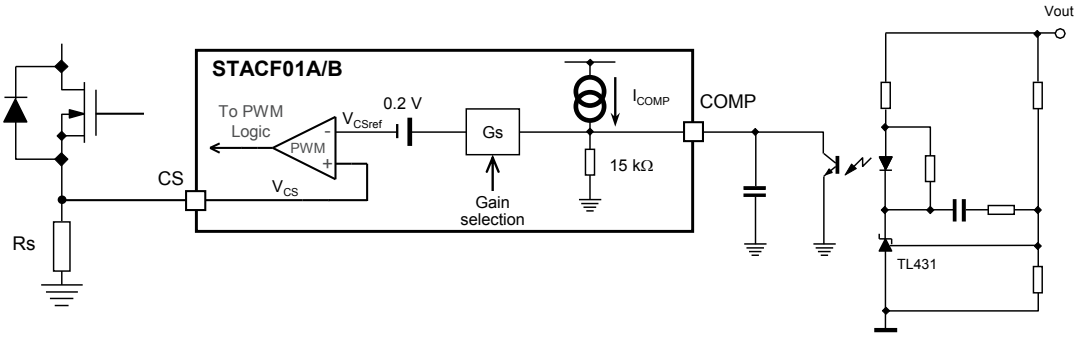


Figure 10. COMP pin internal schematic



6.5 PWM control block

The STACF01A/B ICs implements a peak current mode control scheme, where the voltage across a current sense resistor *Rs* is brought to a dedicated pin (CS) and compared to a programming signal V_{CSref} delivered by the PWM control block to determine the instant when the LS switch is to be turned off.

To prevent a premature termination of the conduction of the LS switch, the PWM system is equipped with a Leading-edge Blanking (LEB) function. Since the converter normally runs with ZVS under steady-state conditions, the LEB duration is normally set at 50 ns. However, during the startup phase ZVS is not ensured; also, during BM operation, in the cycles where the HS switch is not turned on, the converter does not run with ZVS. Therefore, the LEB duration is set at 150 ns during all the soft-start phase (see the "*Soft-start*" section) and during BM operation (specifically: as long as the BM_ON flag is set high, see the "*Theory of BM operation*" section).

With this configuration there is typically a TL431 on the secondary side and an optocoupler that transfers the output voltage information to the PWM control on the primary side, crossing the isolation barrier. The PWM control input (pin COMP) is driven by the phototransistor's collector (the emitter is connected to GND) to modulate the control voltage V_{COMP} and, consequently, the programming signal V_{CSref} of the peak primary current, as shown in Figure 7.

The reference V_{CSref} for the peak current programmed by the control voltage V_{COMP} is:

$$V_{CSref} = Gs\ V_{COMP} - V_{COMP\_OFF} = Gs\ V_{COMP} - 0.2 \quad (8)$$

The value of *Gs* depends on the converter's output voltage (detected through the sampling mechanism of the voltage on the ZCD pin, see the "*Demagnetization Detection and Reverse Current control*"section):

$$Gs = \begin{cases} 0.388 & \text{if ZCD sampled voltage} > 1.70\ \text{V} \\ 0.321 & \text{if ZCD sampled voltage} < 1.65\ \text{V} \end{cases} \quad (9)$$

The turn-off condition for the LS switch is therefore:

$$V_{CSref} = V_{CS} = RsIp_{pk} \quad (10)$$

And the link between the primary peak current Ip_{pk} and the control voltage V_{COMP} can be found by combining Eq. (8) and Eq. (10):

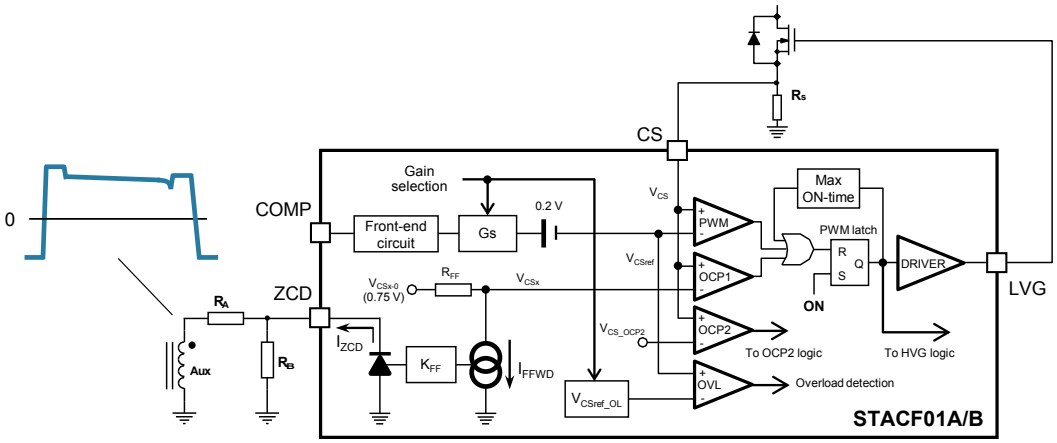
$$V_{COMP} = \frac{1}{Gs}\left(RsIp_{pk} + V_{COMP\_OFF}\right) \quad (11)$$

As shown in Figure 11, which illustrates a more detailed view of the “PWM logic” circuitry, a timeout circuit limits the maximum on-time of the LS switch: if the signal V_{CS} does not reach the programmed reference V_{CSref} within this timeout (T_{ONmax}), the LS switch is turned off.

6.6 Cycle-by-cycle current limitation and input feedforward (FFWD)

Figure 11 shows that the voltage across the current sensing resistor *Rs* and brought to the CS pin (V_{CS}) is compared not only to the reference V_{CSref} but also to a reference V_{CSx}. The outputs of the two comparators are OR-ed together before going to the reset input of the PWM latch, thus the lower level between V_{CSref} and V_{CSx} determines the turn-off of the LS switch. This sets an upper limit to the useful range of the V_{CSref} signal.

Figure 11. PWM control block, OCP and input voltage feedforward



The comparator referred to V_{CSx} performs the so-called “cycle-by-cycle current limitation”, which is basically an overcurrent protection (OCP) and determines the maximum power that the converter can deliver.

This power level is somehow under the control of the user by an appropriate selection of the sense resistor *Rs*: in general, if Ip_{pkmax} is the primary peak current associated to the maximum power level, the sense resistor is to be chosen so that:

$$V_{CSmax} = Rs\ Ip_{pkmax} \leq V_{CSx} \quad (12)$$

As a rule, condition Eq. (12) should be fulfilled considering the minimum value of V_{CSx}, to make sure that the required Ip_{pkmax} can be achieved even in the worst-case condition; the maximum value of V_{CSx} should be used as a reference for the minimum saturation current for the transformer:

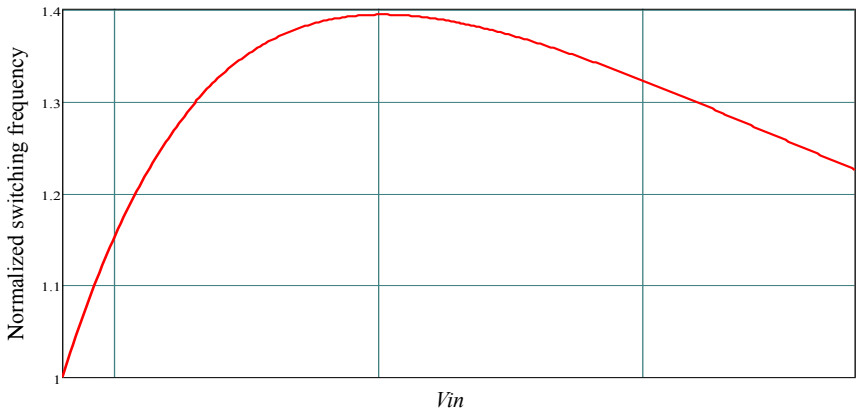
$$I_{SAT} \geq \frac{V_{CSxmax}}{Rs} \quad (13)$$

These general guidelines, Eq. (12), Eq. (13), for the selection of the sense resistor *Rs* needs to be better specified to formulate a true design rule. Normally, it is required that the maximum deliverable power changes little with the input voltage, which might be quite challenging in applications required to operate with a wide input AC voltage range (for example, from 90 to 264 Vac). Considering the ripple at twice the line voltage frequency that appears across the bulk capacitor after the bridge rectifier, it is possible to assume as a reference a DC input voltage (*Vin*) range spanning from 100 to 375 Vdc. The V_{CSx} level is an appropriate function of the input voltage (input voltage feedforward function).

$$V_{CSx} = f(V_{in}) \tag{14}$$

Doing otherwise, that is, having a fixed level V_{CSx} of the cycle-by-cycle current limitation, would translate into a maximum deliverable power that changes with *Vin* in a way that depends on some nonidealities of both the PWM block and the power circuit and, above all else, on the operating frequency vs. input voltage profile of the converter as expressed by Eq. (5) and Eq. (6) (an example is shown in Figure 12). The aim of the input voltage feedforward function is to minimize these changes.

Figure 12. Typical switching frequency vs. Vin profile in an ACF converter operated in VF mode



The purpose is served by subtracting a voltage V_{FFWD} proportional to *Vin* to a fixed level V_{CSx-0}, so that:

$$V_{CSx}(Vin) = V_{CSx-0} - V_{FFWD}(Vin) \tag{15}$$

In Figure 11 it is possible to see how this function is implemented.

The input voltage *Vin* is sensed through an auxiliary winding of the transformer (the same used in the self-supply circuit to power the IC while in operation): during the on-time of the LS switch the voltage across this winding is a negative voltage proportional to *Vin* via the turn ratio. With obvious symbolism:

$$V_{aux(ON)} = -\frac{N_{aux}}{N_p} Vin \tag{16}$$

A resistor divider brings this voltage to the ZCD pin, which contains an internal clamp circuit that clamps the voltage at approximately zero, thus the current sourced by the ZCD pin and flowing through the upper resistor R_A of the divider (that through R_B is negligible) is with very good approximation:

$$I_{ZCD(ON)} = \frac{N_{aux}}{N_p}\frac{Vin}{R_A} \tag{17}$$

This current is internally mirrored by a factor K_{FF} and the current $I_{FFWD} = K_{FF} I_{ZCD(ON)}$,flowing through the internal resistor R_{FF}, generates the desired offset V_{FFWD}:

$$V_{FFWD}(Vin) = R_{FF}K_{FF}I_{ZCD(ON)} = R_{FFe}I_{ZCD(ON)} = R_{FFe}\frac{N_{aux}}{N_p}\frac{Vin}{R_A} \tag{18}$$

In this relationship, N_{aux} and N_p are assumed to be known parameters; R_A is the tuning element that needs to be determined. Note that the feedforward gain R_{FFe} is dimensionally a resistance.

The maximum deliverable power Pin_{max} can be expressed with the following formula:

$$Pin_{\max} = \frac{1}{2}Lp\left(\frac{V_{CSx-0} - V_{FFWD}(Vin)}{Rs} + \frac{Vin}{Lp}T_{DEL}\right)^2 f_{sw}(Vin) \quad (19)$$

In this expression $f_{sw}(Vin)$ is given by Eq. (5) and Eq. (6) T_{DEL} is the cumulative result of some sequential delays:

1. Propagation delay of current sense path (PWM comparator + logic + driver) that causes the LS driving signal to start falling after some time from the voltage *Rs Ip* on the CS pin crossing the reference V_{CSref},
2. Fall time of gate drive voltage (time needed for gate voltage to reach turn-off plateau level),
3. Turn-off delay of the LS switch (time needed for its current to fall to zero).

During this time interval T_{DEL} the LS switch is still ON, and the input current keeps on ramping up, despite *Rs Ip* having already hit the internal level V_{CSref}.

When the cycle-by-cycle current limitation is tripped, T_{DEL} causes the peak current Ip_{pk} to be larger than the expected limit V_{CSx} / *Rs*. More specifically the extra current Δ*Ip* caused by T_{DEL} is:

$$\Delta Ip = \frac{Vin}{Lp}T_{DEL} \quad (20)$$

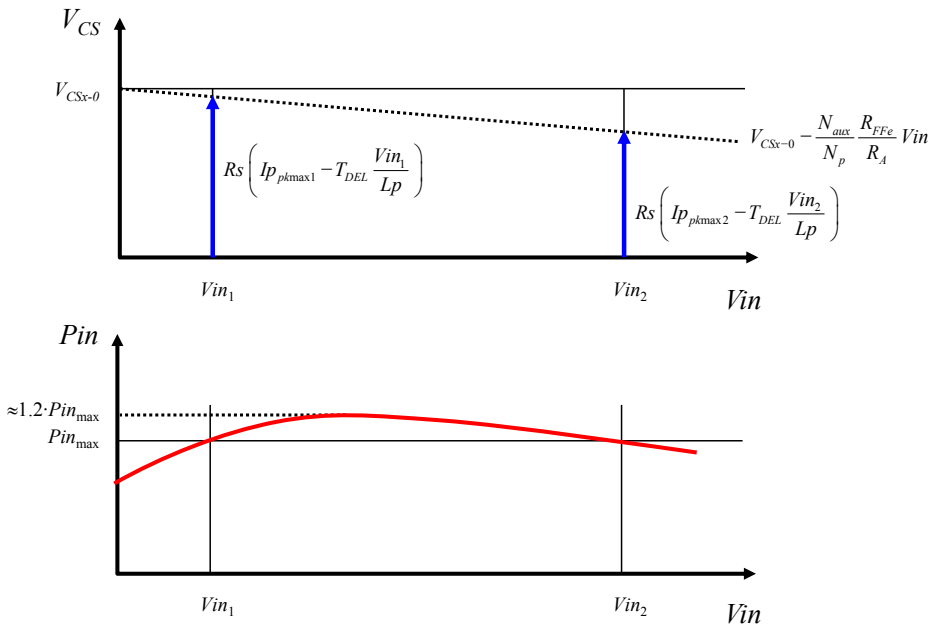
An analytic approach to finding the value of *Rs* that provides the required Pin_{max} as well as the optimum $V_{FFWD}(Vin)$ that minimizes the change in Pin_{max} over the input voltage range is too complex. However, it is possible to follow a semi-empirical approach, whose principle is illustrated schematically in the upper drawing of Figure 13.

This procedure results in determining *Rs* and R_A so that the converter delivers the same maximum power $Pout_{max}$ (equal to the nominal output power *Pout* plus some extra capability) at two input voltage values Vin_1, Vin_2 (not necessarily equal to the extremes of the range Vin_{min}, Vin_{max}), with $Vin_2 > Vin_1$.

Denoting with Ip_{pkmax1} and Ip_{pkmax2} the peak currents corresponding to $Pout_{max}$ at Vin_1 and Vin_2 respectively, this condition can be translated into the following system of two equations:

$$\begin{cases} V_{CSx-0} - \frac{R_{FFe}}{R_A}\frac{N_{aux}}{N_p}Vin_1 = Rs\left(Ip_{pk\max 1} - \frac{Vin_1}{Lp}T_{DEL}\right) \\ V_{CSx-0} - \frac{R_{FFe}}{R_A}\frac{N_{aux}}{N_p}Vin_2 = Rs\left(Ip_{pk\max 2} - \frac{Vin_2}{Lp}T_{DEL}\right) \end{cases} \quad (21)$$

Figure 13. Operating principle of suggested approach for determining *Rs* and R_A, and resulting Pin_{max} vs. *Vin* profile



Solving this system for *Rs* and R_A yields:

$$\begin{cases} Rs = \dfrac{Vin_2 - Vin_1}{Vin_2\ Ip_{pkmax1} - Vin_1\ Ip_{pkmax2}} V_{CSx-0} \\ R_A = \dfrac{R_{FFe}}{Rs}\dfrac{N_{aux}}{N_p}\dfrac{1}{\left(\frac{Ip_{pkmax1} - Ip_{pkmax2}}{Vin_2 - Vin_1} + \frac{T_{DEL}}{Lp}\right)} \end{cases} \quad (22)$$

To summarize, the following step-by-step semi-empirical procedure is suggested to find the sense resistor *Rs* and the optimum input voltage feedforward resistor R_A.

1. Characterize by experiments the typical total propagation delay T_{DEL}.
2. Use a sense resistor *Rs* lower than the expected value. A good starting point is:

$$Rs \leq \frac{V_{CSx-0}}{4Pout_{max}\left(\frac{1}{Vin_{min}} + \frac{1}{V_R}\right)} \quad (23)$$

This is intended to make sure that the measurements in the following steps are done with the output voltage still regulated. Check that the converter works in VF mode at both $Vin = Vin_1$ and $Vin = Vin_2$. If not, slightly increase *Rs* until V_{COMP} exceeds $V_{COMP\_TB1\text{-}0}$ at both input voltages. Also make sure that the negative signal on the RCS pin is lower than the overcurrent threshold V_{RCSx} (see the "*Reverse current sensing and limitation*" section).

1. Set $Vin = Vin_1$ and the load so that the converter outputs the required maximum deliverable power $Pout_{max}$; measure the primary peak current Ip_{pkmax1}.
2. Set $Vin = Vin_2$ and the load so that the converter outputs the required maximum deliverable power $Pout_{max}$; measure the primary peak current Ip_{pkmax2}.
3. Calculate the sense resistor *Rs* with the first of Eq. (22) and choose a commercial value (or a combination of them) as close as possible to the calculated value.
4. Calculate R_A with the second of Eq. (22) and choose a commercial value (or a combination of them) as close as possible to the calculated value.

5. Measure the maximum deliverable power $Pout_{max}$ (as the converter goes out of regulation) at different *Vin* values. $Pout_{max}$ still has a dependency on *Vin*, however in case of perfect compensation it is minimized as qualitatively shown in the lower drawing of Figure 13.
   A slightly different approach to the determination of *Rs* may be considered: instead of referring to the maximum deliverable power $Pout_{max}$, it is possible to refer to the nominal output power *Pout* (100% load) and make the measurements envisaged in steps 3 and 4 of the procedure with this load. Then, in Eq. (22) replace the specified V_{CSx-0} with a slightly lower fixed value to calculate *Rs*. For example, using 0.7 V as V_{CSx-0} gives about 15% margin for peak power.

6.7 Demagnetization detection

The demagnetization detection block has a key role in the control architecture of the STACF01A/B. Its simplified block diagram is shown in Figure 14.

The detection of the instant of demagnetization of the flyback transformer (that is, the instant when the secondary current zeroes) serves multiple purposes:

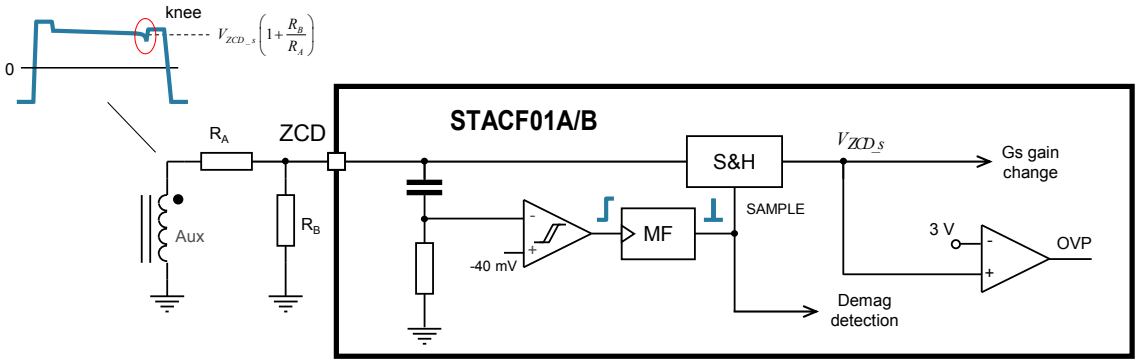
1. In VF mode, turns on the HS switch and starts the ZVS timer that controls the duration T_{REV} of the reverse current build-up time (that is, the duration of the conduction period of the HS switch), which the ability to achieve ZVS for the next turn-on of the LS switch depends on;
2. In FFBK and VCO modes, initiates the T_{WAIT} interval by starting the timer that generates T_{BLANK}; the turn-on of the HS switch and the start of the ZVS timer occur as described in the "*Theory of FFBK mode operation*" and "*Theory of VCO mode operation*" sections.
3. Samples and holds the voltage on the ZCD pin, V_{ZCD}, which in that instant is an accurate image of the converter's output voltage *Vout*. In turn, this voltage level, V_{ZCD_s}, serves a twofold purpose:
   a. Changes the gain of the PWM block as described by Eq. (9);
   b. Senses on OV condition (typically due to an open-loop condition) on the converter's output; refer to the "*Overvoltage protection (OVP)*" section.

The exact demagnetization instant is identified by detecting the knee in the V_{ZCD} voltage (see Figure 14). This is realized by an R-C differentiator that reacts to the negative edge in the V_{ZCD} waveform, which occurs upon transformer demagnetization, by releasing a pulse. This pulse triggers the events previously described at points 1, 2, and 3.

The differentiator is active in a time window that opens 500 ns after the time interval T_R needed to recharge the clamp capacitor is over (see Figure 4, Figure 5, and Figure 7; see also the "*Reverse current sensing*" section), to let the residual ringing fade away. The time window is normally closed as the knee is detected.

In the unlikely case of demagnetization occurring before the differentiator is active, so that the knee is missed, the first positive-going edge of the ringing in the V_{ZCD} voltage occurring while the differentiator is active causes the demagnetization pulse to be released, thus triggering the events at points 1, 2, 3.

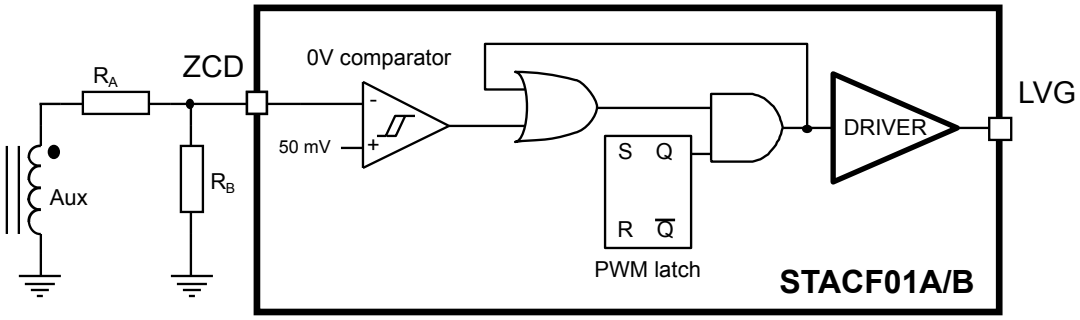
Figure 14. Simplified block diagram of demagnetization detection function



6.8 CCM prevention

As previously mentioned, the operation of an ACF converter controlled by the STACF01A/B are essentially DCM and this is a benign property because it is essential to achieve ZVS operation of the LS switch. In normal operation this is inherent in the control algorithm implemented in the IC (essentially, a new cycle can be initiated only after transformer demagnetization). The underlying assumption is that transformer demagnetization is detectable, which is true during normal operation but might not be during extreme overload conditions or short-circuit even in a correctly designed converter.

Figure 15. CCM prevention function: principle schematic



Under these conditions, the reflected voltage V_R (and, consequently, the voltage on the auxiliary winding) can be extremely low and the knee on the sensed voltage V_{ZCD} too small to be sensed. In this case, demagnetization cannot be detected and there is no assurance that DCM operation can be maintained. Rather, CCM operation is likely.

To prevent this condition, which might easily cause the converter to operate outside of its safe operating area, the ZCD pin is equipped with a “zero-volt comparator” that checks the consistency of the drain voltage with DCM operation. In fact, if operation is DCM, as the HS switch is turned off, the drain voltage collapses to zero (ZVS operation), whereas if current is still circulating on the secondary side (CCM operation) the drain voltage remains high. So does the voltage on the auxiliary winding, thus DCM operation can be ensured by initiating a new cycle only if the voltage on the ZCD pin is zero before turning on the LS switch. The principle circuit that implements this function is shown in Figure 15.

6.9 Clamp capacitor charge/discharge mechanism

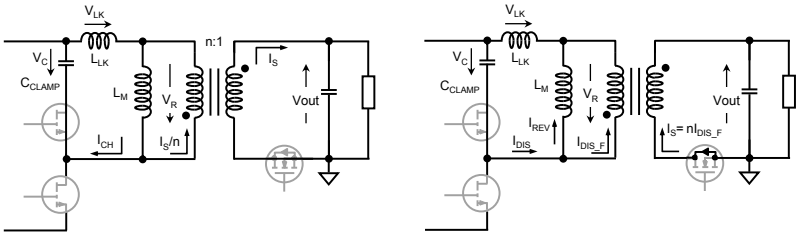
In an ACF converter the task of the clamp capacitor C_{CLAMP} is to temporarily store the energy in the leakage inductance of the transformer, which is not transferred to the secondary side by magnetic coupling, and then utilize part of it to turn on the LS switch with ZVS.

As mentioned in the “*Theory of VF mode operation*” section, the energy stored in the transformer’s leakage inductance is transferred to the clamp capacitor in a resonant fashion just after the LS switch is turned off. The resonant circuit active during this energy transfer phase is essentially composed of the transformer’s leakage inductance L_{LK} and the clamp capacitor C_{CLAMP}. In fact, as shown in the circuit of Figure 16 a), the primary current I_{CH} charges C_{CLAMP} through the high-side switch turned on to minimize the source-drain voltage drop but there is a constant voltage V_R across the magnetizing inductance L_M, thus this is not contributing to resonance.

Normally, C_{CLAMP} is selected in such a way that the duration T_R of this energy transfer phase, that is, the time needed for I_{CH} to decay from its peak value Ip_{pk} to zero, is much shorter than the ringing period of this resonant circuit, that is:

$$T_R \ll T_{ring} = 2\pi\sqrt{C_{CLAMP}\,L_{LK}} \quad (24)$$

Figure 16. Simplified circuit during clamp: a) charge phase; b) discharge phase



a) b)

It is therefore possible to assume that the voltage change DV_C across C_{CLAMP} is small compared to its average value V_C and that the current I_{CH} that charges C_{CLAMP} decays linearly. Assuming that the initial instant of the energy transfer is t = 0, it is possible to write:

$$I_{CH}(t) = Ip_{pk} - \frac{V_C - V_R}{L_{LK}}t \tag{25}$$

With these assumptions the time T_R can be estimated as:

$$T_R = Ip_{pk}\frac{L_{LK}}{V_C - V_R} \tag{26}$$

The total charge Q_{CH} transferred from L_{LK} to C_{CLAMP} is found by integrating Eq. (25) in the interval (0, T_R). The result is:

$$Q_{CH} = \frac{1}{2}\frac{L_{LK}\, Ip_{pk}^2}{V_C - V_R} \tag{27}$$

The voltage change DV_C across C_{CLAMP} is equal to Q_{CH}/C_{CLAMP} and it is possible to assume that the initial C_{CLAMP} voltage (@ t = 0) and the final C_{CLAMP} voltage (@ $t = T_R$) are respectively:

$$V_C(0) = V_C - \frac{1}{2}\frac{Q_{CH}}{C_{CLAMP}}; \quad V_C(T_R) = V_C + \frac{1}{2}\frac{Q_{CH}}{C_{CLAMP}} \tag{28}$$

As $I_{CH}(t)$ zeroes, the HS switch is turned off and the voltage across the primary winding goes from $V_C(T_R)$ to V_R, which is necessarily lower, thus reverse biasing the HS switch and stimulating the resonance between L_{LK} and C_{drain}, the total capacitance associated with the drain node of the LS switch. As a result, the end-of-charge of C_{CLAMP} is followed by a ringing whose initial amplitude equals the difference $V_C(T_R)$-V_R, which is relatively small.

The discharge phase of C_{CLAMP}, where the energy stored in it during the charge phase is released, is initiated by the turn-on of the HS switch that occurs when the secondary current has zeroed and drives the primary current in the reverse direction, as illustrated in the circuit of Figure 16 b) for a time T_{REV}.

As highlighted in the "*Theory of VF mode operation*" section, this energy is transferred both to the total primary inductance $Lp = L_M + L_{LK}$ and to the secondary winding too. In fact, due to the leakage energy charged during the previous time interval it is $V_C(T_R) > V_R$: thus, as the HS switch turns on the secondary rectifier is forward-biased and current flows again on the secondary side after it had gone to zero (the "secondary current bump" is shown in the waveforms of Figure 4, Figure 5, and Figure 7).

Energy is transferred from C_{CLAMP} to the secondary side through the resonance with L_{LK}, while L_M does not resonate. Still under the same assumptions, the discharge current of C_{CLAMP} is:

$$I_{DIS}(t) = \frac{V_C - V_R}{L_{LK}}t \tag{29}$$

and the current through the magnetizing inductance L_M is:

$$I_{REV}(t) = \frac{V_R}{L_M} t \tag{30}$$

Its peak value, which the ability of the LS switch to work with ZVS depends on, is:

$$I_{REV} = \frac{V_R}{L_M} T_{REV} \tag{31}$$

As previously said, during T_{REV} the transformer works in forward mode and a current equal to

$$I_S(t) = n\,[I_{DIS}(t) - I_{REV}(t)] \tag{32}$$

flows on the secondary side.

The charge Q_{DIS} lost by C_{CLAMP} is found by integrating Eq. (29) in the interval (0, T_{REV}):

$$Q_{DIS} = \frac{1}{2} \frac{V_C - V_R}{L_{LK}} T_{REV}^2 \tag{33}$$

In steady-state conditions the charge balance of C_{CLAMP} must be zero, that is $Q_{CH} = Q_{DIS}$. Equaling Eq. (27) to Eq. (33) and solving the resulting equation for V_C we find:

$$V_C = V_R + Ip_{pk} \frac{L_{LK}}{T_{REV}} \tag{34}$$

Its maximum value is reached when Ip_{pk} is at a maximum and T_{REV} is at a minimum. Both conditions occur at the minimum input voltage.

Note that if we substitute Eq. (34) in Eq. (26) we find that $T_R = T_{REV}$. In the end, the accuracy of this approximate result is quite good if condition Eq. (24) is fulfilled. This may be ensured by an appropriate selection of C_{CLAMP}. Experience shows that if C_{CLAMP} is selected so that:

$$T_{ring} = 2\pi \sqrt{C_{CLAMP}\, L_{LK}} \geq 4\, T_{REVmax} \tag{35}$$

Eq. (34) predicts the clamp voltage V_C with good accuracy under all operating conditions. Therefore, it is recommended that:

$$C_{CLAMP} \geq \frac{1}{L_{LK}} \frac{4}{\pi^2} T_{REVmax}^2 \tag{36}$$

In this equation T_{REVmax} is the maximum expected value of T_{REV} in the worst-case conditions: maximum input voltage and minimum output voltage, as clarified in the next section.

6.10 Reverse current control requirements and ZVS Timer

The general requirement for the LS switch to achieve ZVS at turn-on is that at the end of T_{REV} there must be sufficient energy stored in the transformer primary winding to completely discharge the total capacitance C_{drain} associated to its drain node. In other words, the current I_{REV} given by Eq. (31) must be greater than a minimum value.

As the HS switch is turned off, there is an initial short transient needed for the currents in the leakage inductance L_{LK} and the magnetizing inductance L_M to equalize. This is accomplished by a negative voltage across L_{LK} that causes an initial sudden drop of the drain voltage V_{drain}. Then the total transformer primary inductance, $L_P = L_{LK} + L_M$ starts resonating with C_{drain}, discharging it to zero if the following condition is satisfied:

$$\frac{1}{2} L_P\, I_{REV}^2 \geq \frac{1}{2} C_{drain}\, V_X^2 \tag{37}$$

where V_x is the drain voltage after the first discharge. $I_{REV}$is given by Eq. (31), so considering that $L_M \approx Lp$ the previous equation can be rewritten as follows:

$$\frac{1}{2} \frac{V_R^2}{L_P} T_{REV}^2 \geq \frac{1}{2} C_{drain}\, V_X^2. \tag{38}$$

Considering for simplicity $V_X \sim V_{in}$ and solving Eq. (38) for T_{REV}:

$$T_{REV} \sim \sqrt{C_{drain} L_P} \frac{V_{in}}{V_R}, \quad (39)$$

which shows the dependence of T_{REV} on the main circuit parameters.

The STACF01A/B control I_{REV} by controlling T_{REV}. To fulfill this task, the IC implements the ZVS Timer block that sets T_{REV} through a feedback mechanism that checks if there are the conditions for ZVS to occur, extends T_{REV} if not, or keeps it oscillating around the equilibrium value otherwise.

The user can fine-tune the reverse current I_{REV} using a resistor between the current sensing resistor Rs and the current sense pin CS. The fine-tuning is done empirically to find the resistor value that either provides full ZVS all over the input voltage range or the optimum efficiency under assigned conditions (maybe giving up ZVS in other conditions), or whatever criterion the user may have. Normally, a resistor in the few hundred ohms serves the purpose.

It is recommended that ZVS be achieved at high line because the shorter LEB might cause irregular behavior at intermediate and light load due to the PWM comparator triggered by the leading-edge spike.

6.11 Reverse current sensing and cycle-by-cycle limitation

Reverse current sensing cannot be used to control the reverse magnetizing current necessary to achieve ZVS because it is not possible to isolate it from the overall reverse current; regardless, it is useful to handle those conditions that may lead to an excessive reverse current Ip_{REV}:

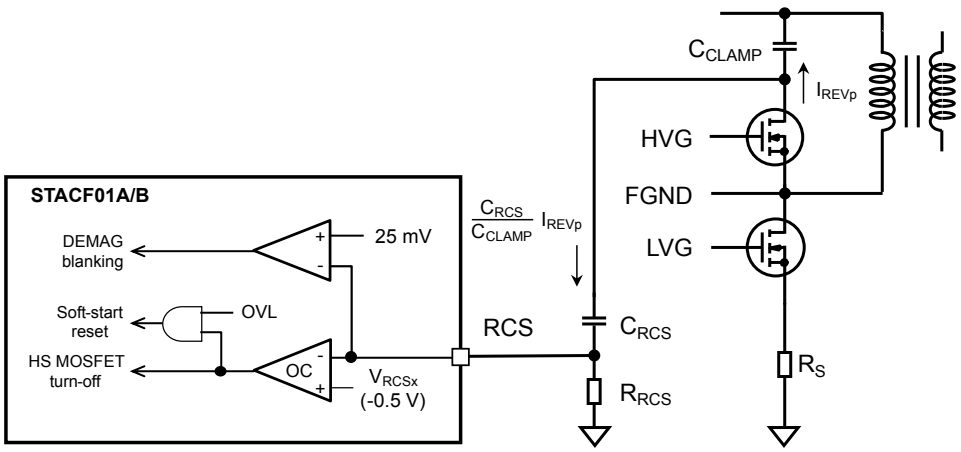
- Sudden output voltage drop due to a short-circuit.
- Switching restart after a negative output voltage transition in variable output voltage applications.

In both cases, the clamp capacitor C_{CLAMP}, charged at a voltage slightly higher than $V_R = (Np/Ns)\ Vout$, where $Vout$ is the output voltage before the perturbation or change occurs, after the perturbation or change now “sees” a much lower reflected voltage during the conduction of the HS switch. As a result, the forward current that flows on both the primary and the secondary side and, consequently, Ip_{REV}, may reach peak values that are much higher than those occurring during normal operation (see Figure 18). It is wise to limit them and the stress caused to the HS switch within acceptable limits.

The STACF01A/B implement reverse current sensing as shown in Figure 17. The capacitor C_{RCS} is essentially in parallel to the clamp capacitor C_{CLAMP}, so that they form a capacitive current divider. It is $C_{RCS} << C_{CLAMP}$, thus the voltage V_{RCS} developed across the sense resistor R_{RCS} is given by:

$$V_{RCS} = I_{REVp} R_{RCS} \frac{C_{RCS}}{C_{CLAMP}} \quad (40)$$

Figure 17. Reverse current sensing system



If V_{RCS} exceeds the (negative) reference V_{RCSx} the reverse overcurrent limitation is triggered. This causes the immediate turn-off of the HS switch, overriding the ZVS Timer and terminating T_{REV} beforehand. Simultaneously, the deadtime following the turn-off of the HS switch is changed from the programmed value (see the "*Deadtime programming*" section) to T_{BASE} (see the "*Theory of FFBK mode operation*" section) to let the forward component of the reverse current decay to zero. In fact, the interruption of a large forward current may severely stress the low-side switch at turn-on.

In addition, if the OVL flag is high, which happens if the programmed V_{CSref} is greater than V_{CSref_OL}, that is, in case of short-circuit, the soft-start is reset to reduce also the secondary current transferred from the primary side through the flyback mechanism. If the OVL flag is low, which happens when the reverse current limitation is triggered by the converter restarting switching after a downhill output voltage transition (during the idle time V_{COMP} was saturated low and then, V_{CSref} close to zero), the soft-start is not reset to let the control loop take over as soon as possible.

Normally, C_{RCS} is selected a hundred or more times smaller than C_{CLAMP} to minimize power losses on R_{RCS}. Once C_{RCS} is selected, R_{RCS} is such that the maximum voltage drop given by Eq. (40) is lower than V_{RCSx}, (typ. 20 to 30%). As a reference, the time constant $R_{RCS}C_{RCS}$ is typically in the 50-100 ns range.

Figure 18. High reverse current pulses upon short-circuit at full load with no limitation

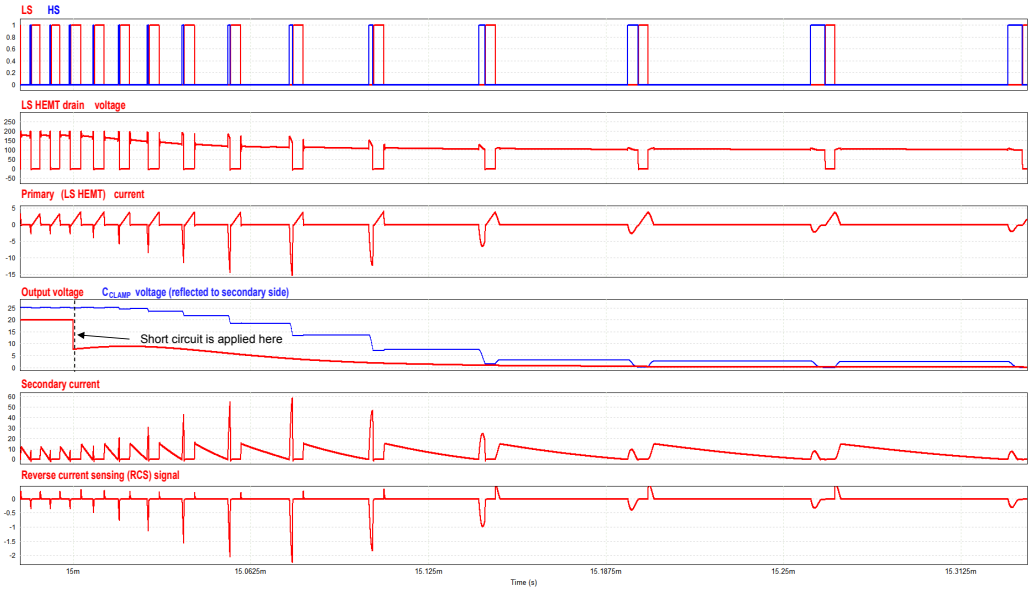
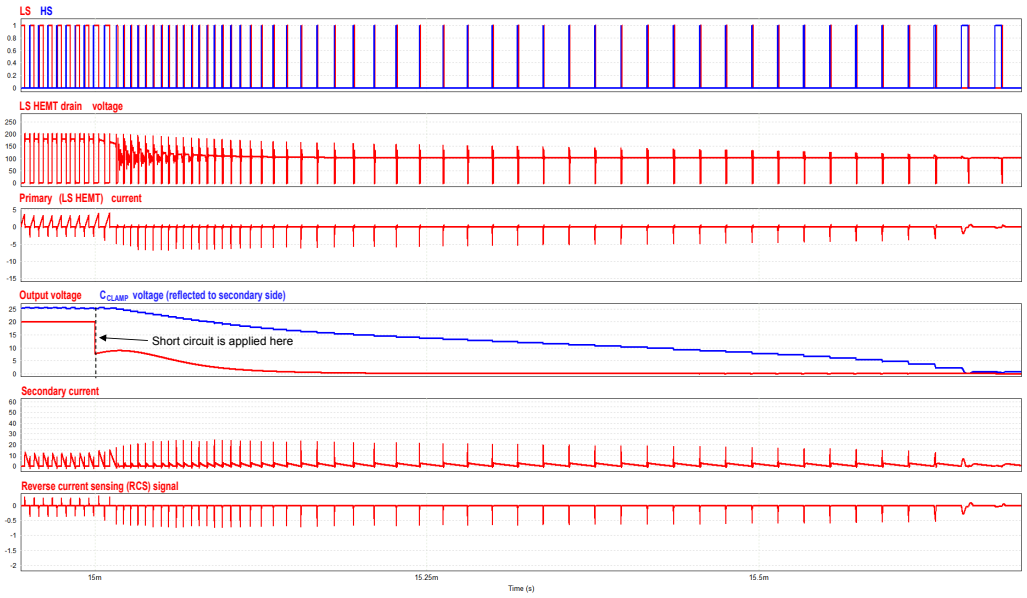


Figure 19. Reverse current pulses upon short-circuit at full load with reverse current limitation



Reverse current sensing is also useful to detect the end of the charging phase of C_{CLAMP}, occurring just after the LS switch is turned off, and determine the duration of the time interval T_R and the corresponding on-time of the HS switch shown in Figure 4, Figure 5, and Figure 7. A comparator referred to 25 mV detects that the V_{RCS} voltage has decayed to zero. This activates the differentiator for demagnetization detection after a delay of 500 ns to prevent the differentiator from being cheated by the ringing following the turn-off of the HS switch.

6.12 Deadtime programming

To achieve ZVS for the LS switch, adequate deadtime T_D needs to be ensured between the turn-off of the HS switch and the turn-on of the LS switch. If this deadtime is too short, then the drain node swing cannot be completed and there is a non-zero voltage at the instant of turn-on. Conversely, if T_D is too long, the (reverse) primary current may become positive again recharging C_{drain} and, again, there is a non-zero voltage at the instant of turn-on. Thus, in both cases ZVS is at least partially lost.

Theoretically, the optimum value of the deadtime is one-quarter of the resonant period formed by *Lp* and C_{drain}:

$$T_{D\_opt} = \frac{\pi}{2}\sqrt{Lp\ C_{drain}} \quad (41)$$

This equation is a simplification because of the nonlinear nature of the *Coss* of GaN HEMT switches, one contributor to C_{drain}; however, their nonlinearity is much less pronounced than, for example, in superjunction MOSFETs, so that Eq. (41) is a reasonable starting point. Note that, in this case, as to the various *Coss* definitions, their time-related equivalent value should be considered.

Also note that even if insufficient energy is stored in *Lp* at the end of the reverse current build-up time interval so that ZVS cannot be achieved, meeting the timing requirement Eq. (41) ensures that turn-on occurs with the minimum possible drain-to-source voltage, that is, with minimum additional losses and noise.

With the STACF01A/B, the deadtime T_D is programmed by the user with a resistor R_{DEAD_PROG} connected between the pin DTP and GND, according to the following formula:

$$T_D = 5\ R_{DTP} \quad (42)$$

where T_D is expressed in ns and R_{DTP} in kW.

Both the deadtimes following the high-side turn-off and the low-side turn-off are equal and set by the same program resistor with the programmed value given by Eq. (42).

6.13 Auxiliary regulator

The auxiliary regulator, shown in Figure 20, generates a regulated supply voltage for the IC, (VCC, 6.25 V typ.), starting from the voltage generated by the self-supply system via an auxiliary transformer winding.

This regulated voltage is intended for supplying also the external high-voltage half-bridge HEMT driver IC or SiP (for example, MasterGaN): the regulator guarantees at least 15 mA output current in the worst-case conditions as visible in the plot on the left-hand side of Figure 21.

In USB PD applications, the converter output voltage can be set from 5 V up to 20 V depending on the power contract negotiated with the load. The self-supply voltage bus generated by the auxiliary winding tracks the output voltage and has an even larger variation because of the transformer's parasitics. A buck-boost regulator, with its step up/down capability, can provide the required V_{CC} setpoint with an input voltage range V(BBVIN) from 2.4 V to 27 V in all these operating conditions.

Four pins of the IC, besides the VCC pin, are engaged for the connection of the external components: an inductor, two Schottky diodes, and the bypass capacitors for the input and output ports. As to the inductor, it is recommended to use a shielded-type 10 µH off-the-shelf part with a DC winding resistance not exceeding 1 Ω. The Schottky diodes should be 1 A / 30 V rated parts. The bypass capacitors should be low-ESR ceramic type with few µF capacitance.

Note that two separate capacitors are recommended for the input of the regulator. The first one, placed close to the auxiliary winding and its rectification diode to minimize the switching loop area, serves the purpose of energy storing, so it can be a ceramic or electrolytic type of some ten µF. The second one, the bypass capacitor for high frequency decoupling, should be connected as close as possible to the BBVIN and BBGND pins for the same reason.

The output bypass capacitor should be connected as close as possible to the VCC and BBGND pins too. If the VCC bus voltage is used to power the half-bridge HEMT driver or SiP, the supply voltage is bypassed by a local high frequency decoupling capacitor as close to the supply and ground pins of the companion IC as possible.

Specifically, the auxiliary regulator utilizes a non-inverting buck-boost converter, where the two active switches, integrated in the STACF01A/B, are driven on and off simultaneously. The converter works with a fixed peak current and a fixed off-time of the two switches.

When the switches are on, the inductor gets charged and its current ramps up linearly with a slope proportional to the input voltage. As the peak current reaches an internally set value (0.2 A typ.), the two switches are turned off and the inductor demagnetizes via the two diodes. After the preset off-time has elapsed the switches are turned on again to start another switching cycle. Working with a fixed off-time instead of a fixed frequency ensures unconditional stability of the peak current control loop.

To limit the switching frequency at a high input voltage, which would cause unacceptable switching losses, the off-time is modulated with the input voltage V(BBVIN). With the suggested inductance value, the expected switching frequency of the converter is shown in the plot on the right-hand side of Figure 21.

The output voltage is regulated in a hysteretic manner: when the output voltage exceeds the regulation setpoint, the converter is stopped and restarts switching when the output voltage falls about 30 mV below the setpoint. In this way, no frequency compensation is required for the voltage loop stability.

Figure 20. Auxiliary buck-boost regulator

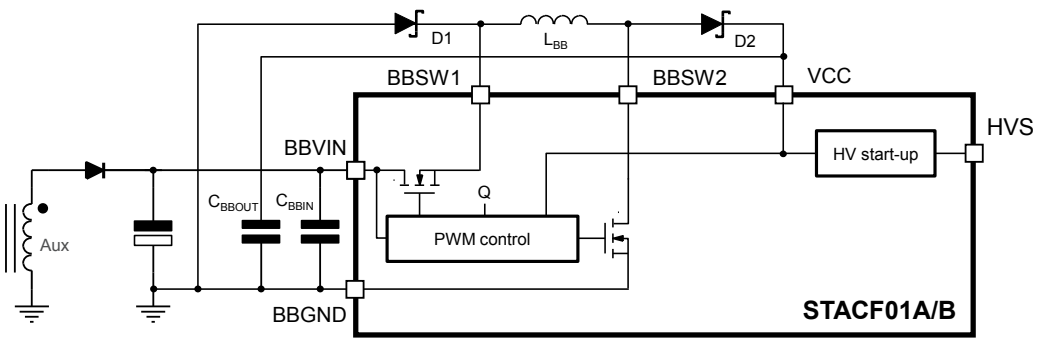
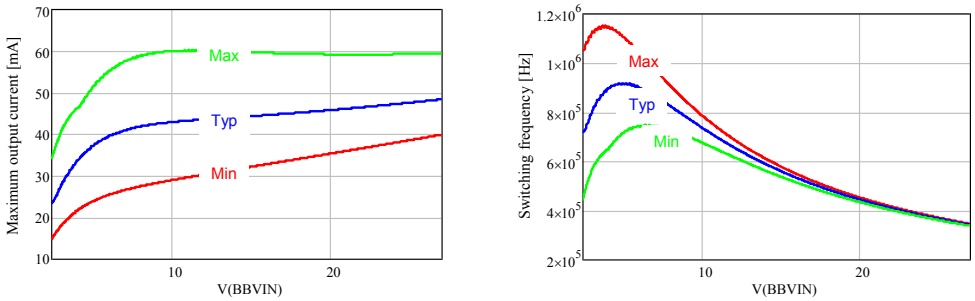


Figure 21. Auxiliary buck-boost regulator: current capability (left) and switching frequency (right)



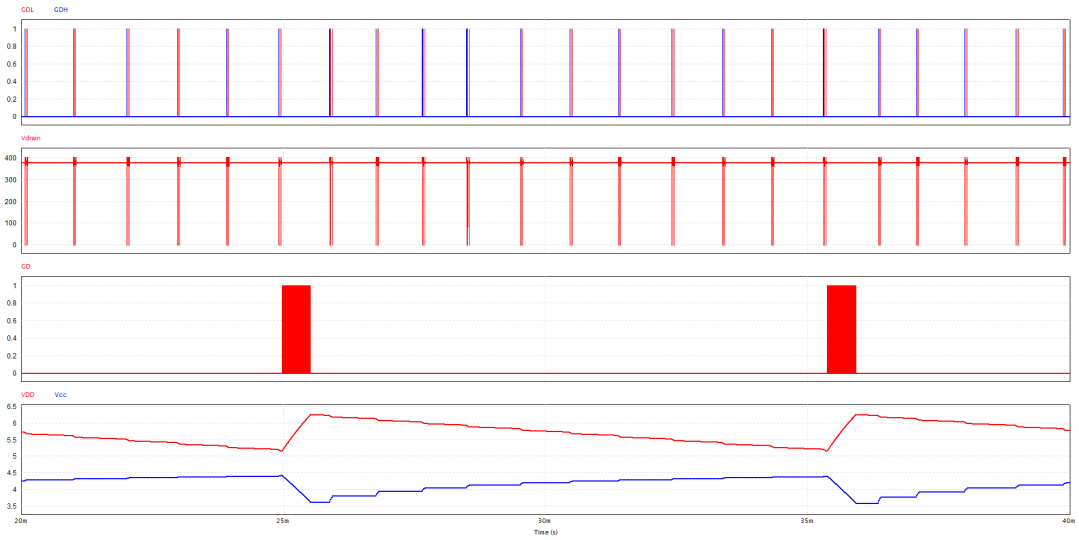
When the STACF01A/B work in burst mode, (the BM_ON flag is high, see the "*Theory of burst mode operation*" section), the buck-boost regulator works intermittently to increase system efficiency, making the VCC voltage oscillate between the regulation setpoint (= 6.25 V) and the restart threshold V_{CCres} (= 5.4 V typ.).

In order for the buck-boost to operate its input voltage, V(BBVIN) must be larger than its disable threshold V_{BBVIN_Off} (= 2.3 V typ.). Only at startup, to make it start, V(BBVIN) must be larger than the enable threshold V_{BBVIN_On} (= 2.5 V typ.). Normally, V(BBVIN) can get close to these levels only during burst mode at the maximum line voltage and minimum output voltage, as shown in the timing diagram of Figure 22.

Should V(BBVIN) fall below V_{BBVIN_Off} during burst mode so that VCC cannot be sustained above V_{CCres} by the disabled buck-boost regulator, then the high-voltage startup generator kicks in, taking the VCC voltage up to the regulation setpoint. In this way, the converter keeps on running, and the output voltage regulation is maintained, only the input consumption is larger.

It is important that the switching activity of the auxiliary regulator does not disturb the operation of the ACF converter. More specifically, it must not interfere with the turn-off of the low-side switch. An anti-interference circuit prevents the switches of the auxiliary regulators to be turned on or off when this is too close to the turn-off of the low-side switch. The intervention of the anti-interference circuit can be seen as a shorter on-time or a delayed turn-on of the switches.

Figure 22. Auxiliary buck-boost operation during burst mode of main converter



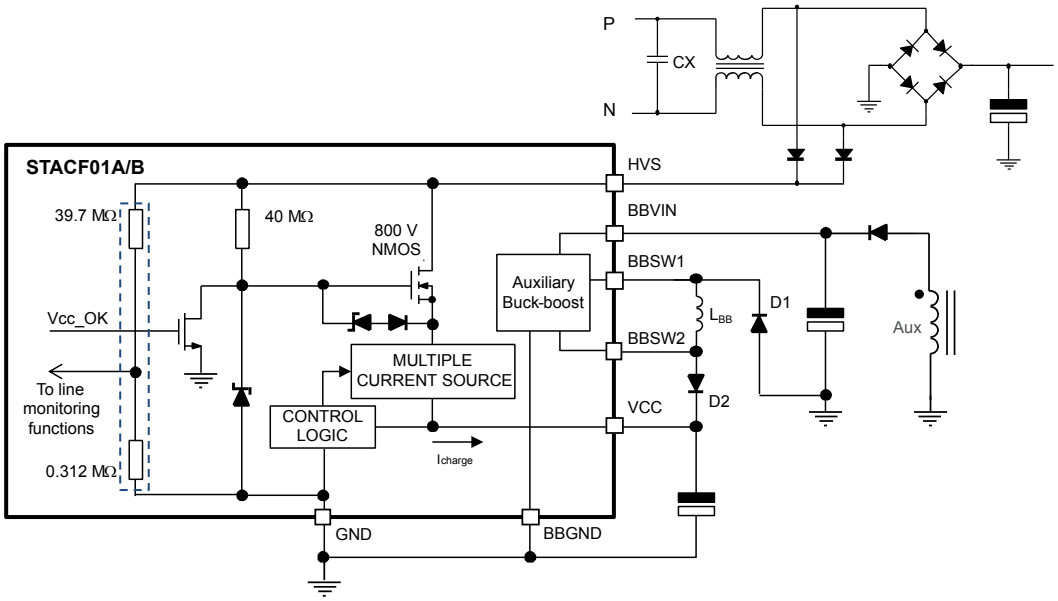
6.14 High-voltage startup generator and LINE voltage monitoring functions

During normal operation the IC is powered through its supply pin (VCC) by the auxiliary converter that, in turn, steps up or down a voltage rail generated by the self-supply system (typically, an auxiliary winding of the transformer, a steering diode, and a buffer capacitor). This means that this voltage is not available if the IC is not operating. On the other hand, the undervoltage lockout (UVLO) function enables the IC to operate only if the supply voltage is high enough to guarantee its proper operation.

An additional supply circuit is therefore needed, which brings this voltage in the operating region to initiate IC operation and wake up the converter as this is connected to the input source. Additionally, since this startup circuit is to be connected to the high-voltage input rail, the only available source of energy when the converter is not yet operating, it is required to disconnect itself from the input rail once the self-supply system is able to power the IC and it is no longer needed: in fact, drawing DC power directly from the high-voltage rail is extremely inefficient and would make the standby power targets impossible to meet.

This is the purpose of the high-voltage startup generator. Figure 23 shows a high-level internal schematic of the high-voltage block that implements this function and its connection to the power stage.

Figure 23. High-voltage startup generator and LINE voltage monitor: internal schematic



The major building block is a high-voltage N-channel enhancement MOSFET able to withstand 800 V, whose gate is biased by a 40 MΩ resistor. The gate is also connected to the drain of a small-signal MOSFET, whose purpose is to completely shut down the startup generator by cutting off the high-voltage MOSFET when the logic signal V_{CC_OK} (provided by the state machine that supervises the operation of the chip) is asserted high. The current I_{charge} sourced to the buffer capacitor connected to the VCC pin is controlled by a multiple current generator with different capabilities depending on the voltage VCC itself and on whether the IC is undergoing a cold start or is restarting after a protection has been triggered.

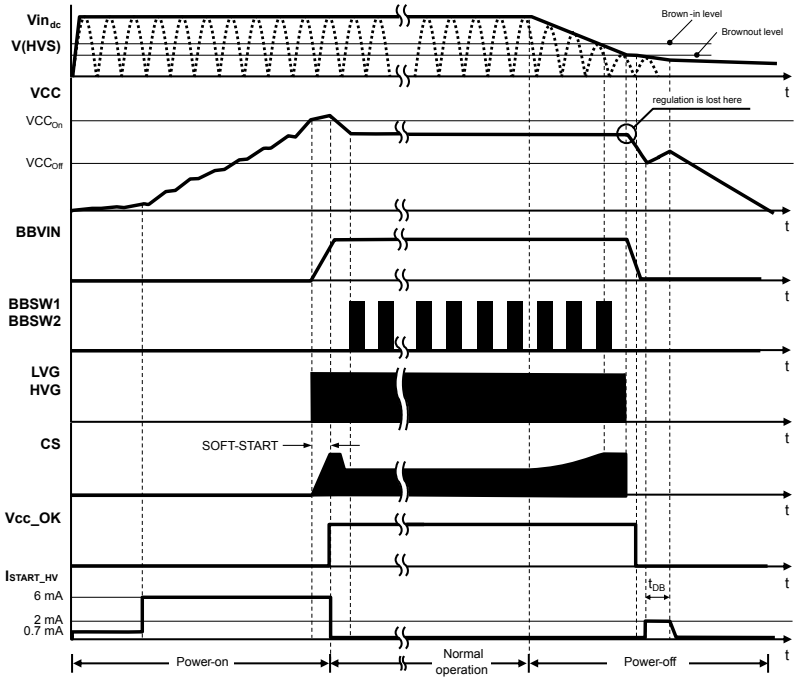
With reference to the timing diagram of Figure 24, which refers to a cold start, when power is first applied to the converter the voltage on the bulk capacitor (*Vin*) builds up and, at about 18 V, the startup generator is sufficiently biased to start sourcing current. This current, drawn from the AC line via the HVS pin and diminished by the device's own consumption, is output from the VCC pin and charges the buffer capacitor connected from the VCC pin to ground, making its voltage rise. At this point, the startup process undergoes different phases:

- As long as the voltage on the VCC buffer capacitor is lower than a threshold (located at around 2 V), the source current (output from the VCC pin) has a lower value (0.75 mA typ.) to prevent the IC from overheating in case the VCC pin is shorted to ground by mistake;
- As the voltage on the VCC buffer capacitor exceeds that threshold, the source current has a large value (5.5 mA typ.) to quickly charge the VCC buffer capacitor up to the startup threshold VCC_{On}. During this phase the IC consumes very little current (essentially, only the circuits associated with the UVLO function are active), hence it is nearly all the current provided by the startup generator that is sourced from the VCC pin and charges the VCC buffer capacitor;

- As the voltage on the VCC buffer capacitor exceeds the startup threshold VCC_{On}, the IC exits from the UVLO state, performs its internal initialization procedures, and checks fault flags for fault conditions that occurred before the last IC turn-off; at this point, the decision is made on whether the IC is to start normally or some fault handling procedure is to be carried out.

During this phase, the quiescent current of the IC becomes far larger than in the previous phase. The startup generator is kept active to contribute to powering the IC, so that not all the burden is on the VCC buffer capacitor. Rather, in most cases the VCC voltage keeps on rising at a lower rate.

Figure 24. Timing diagram: normal power-up and power-down sequences



- If everything is good, PWM operation is enabled: the gate driver outputs start being driven and the chip enters the “soft-start” phase (see the relevant section); the BBVIN voltage starts rising and exceeds the minimum operating level of the auxiliary buck-boost regulator. If not, the IC enters a fault state (see Section 6.13: Auxiliary regulator and Section 6.18: Protections).
- At the end of the soft-start phase, the startup generator is shut down by the V_{CC_OK} signal asserted high. At the same time, the auxiliary buck-boost is enabled but does not start switching because the VCC voltage is greater than the regulation setpoint.

The residual current consumption of the HVS pin is the one on the 40 MΩ bias resistor plus that of the 40 MΩ resistor divider that senses the voltage on the HVS pin to perform the line monitoring functions (< 3 mW total at 230 Vac).

Now that the startup generator is off, the VCC voltage droops because the IC is powered only by the energy in the VCC buffer capacitor. This droop lasts until the VCC voltage reaches the regulation setpoint of the auxiliary buck-boost regulator. At this point, the auxiliary regulator starts switching and steadily powers the IC. Eventually, the converter reaches its steady-state operation.

At converter power-down different scenarios may be observed, depending on the converter design and on its operating conditions (input voltage and output load) at that moment. Figure 24 shows a typical situation that is described here.

The system loses regulation as soon as the input voltage is so low that the cycle-by-cycle peak current limitation is tripped. BBVIN then drops too, following somehow the output voltage drop. As the input voltage falls below the brownout threshold (see the relevant section) the IC stops switching, and the auxiliary regulator stops too. VCC falls below the UVLO turn-off threshold and the V_{CC_OK} signal is de-asserted. The startup generator could now restart.

However, the input voltage is so low that the generator is not properly biased and cannot source current. In this way, converter restart attempts are not possible, and the output voltage decays to zero with no bounce. Anyway, as long as the input voltage is lower than the brown-in threshold (see relevant section), even if the startup generator brings VCC over the startup threshold there is no switching and then, no bounce of the output voltage.

More details on the HV startup generator's behavior after a fault can be found in the "*Protections*" section.

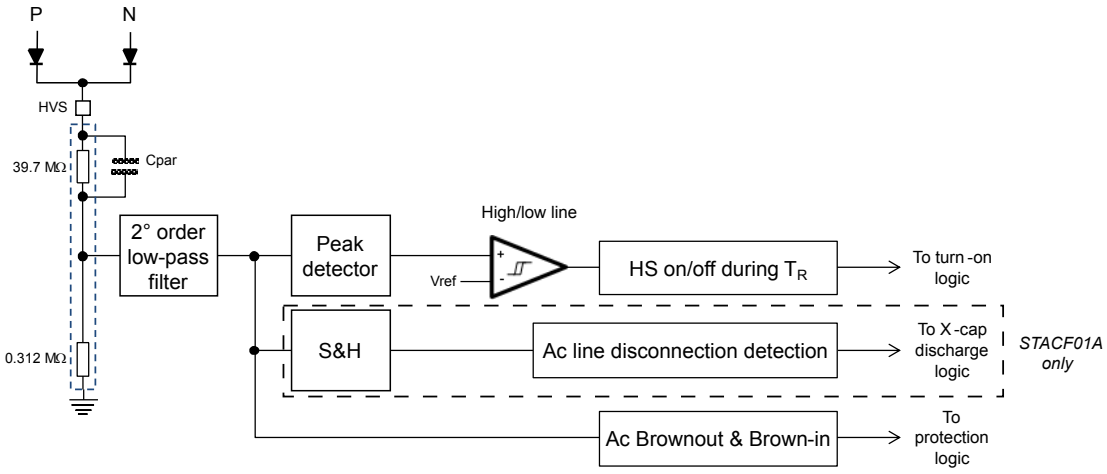
The resistor divider in the boxed area in Figure 23 and redrawn in Figure 25 is the input voltage sensor used by the input voltage monitoring functions of the IC. The divider ratio is $K_p = 7.8 \cdot 10^{-3}$.

The sensed voltage is conditioned by a 2nd order low-pass filter before being fed into the line monitoring functions. One pole compensates for the capacitive parasitic effects associated with the structure that realizes the upper resistor and lumped into a parallel capacitor (Cpar). Essentially, this pole cancels out the zero introduced by this parasitic capacitor. The second pole attenuates any high-frequency noise that may be superimposed on the low-frequency line voltage (for example, the noise generated by the switching activity of the converter itself) and alter the sensing.

The line monitoring functions serve three purposes:

- AC brownout protection and brown-in (see the relevant description in the "*Protections*" section)
- AC mains disconnection detection (see the "*X-cap discharge function*" section), for the STACF01A only
- ON/OFF logic of the high-side switch during the T_R time interval (first turn-on of the high-side switch during off-time of low-side switch). This is enabled only at high line.

Figure 25. LINE voltage monitoring functions



6.15 LDO5V regulator and PWM outputs

A dedicated LDO (low-dropout) regulator provides a 5 V supply voltage for the logic circuits of the IC and for the PWM outputs LS, HS. The output of the regulator is externally available on pin LDO5V. For regulator stability and energy buffering, a typical 47 nF ceramic bypass capacitor is to be connected from the LDO5V pin and the GND pin. The LDO regulator can supply a 1 mA current to power some external circuitry.

The LS and HS PWM outputs are to be connected to the inputs of a high-voltage half-bridge driver that drives the discrete GaN HEMTs used as low-side switch and high-side switch respectively, or an SiP device that embeds both the high-voltage half-bridge driver and the totem pole of GaN HEMTs.

Figure 26. **Connection between STACF01A/B and a MasterGaN SiP**

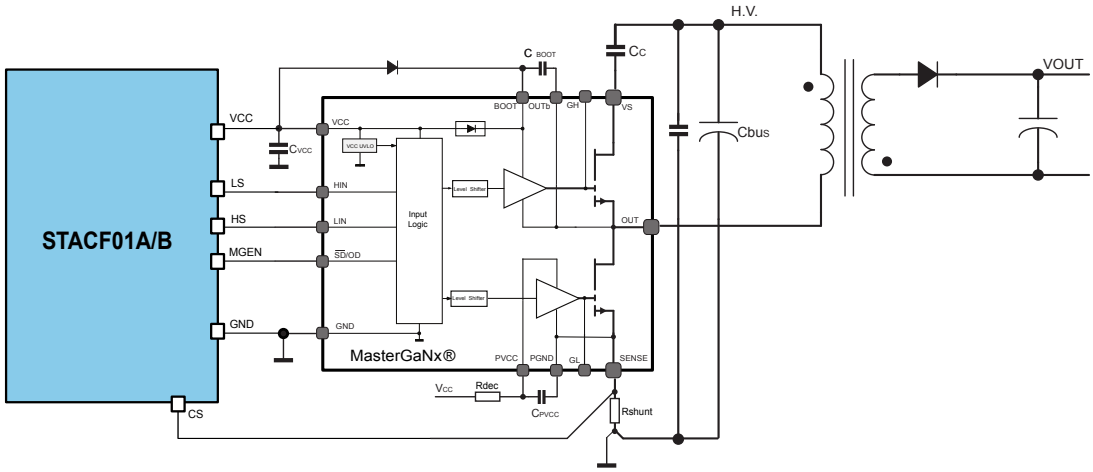


Figure 26 shows a typical connection between the STACF01A/B and a MasterGaN SiP (not to be intended as a suggested application schematic).

6.16 Soft-start

During the converter startup phase, the soft-start function progressively increases the cycle-by-cycle current limitation setpoint in 8 steps, each one having 1 ms duration, up to the final value $V_{CSx\text{-}0}$ (= 0.75 V). This helps reduce the stress on all power components and provides a smooth rise of the output voltage. No external programming component is required.

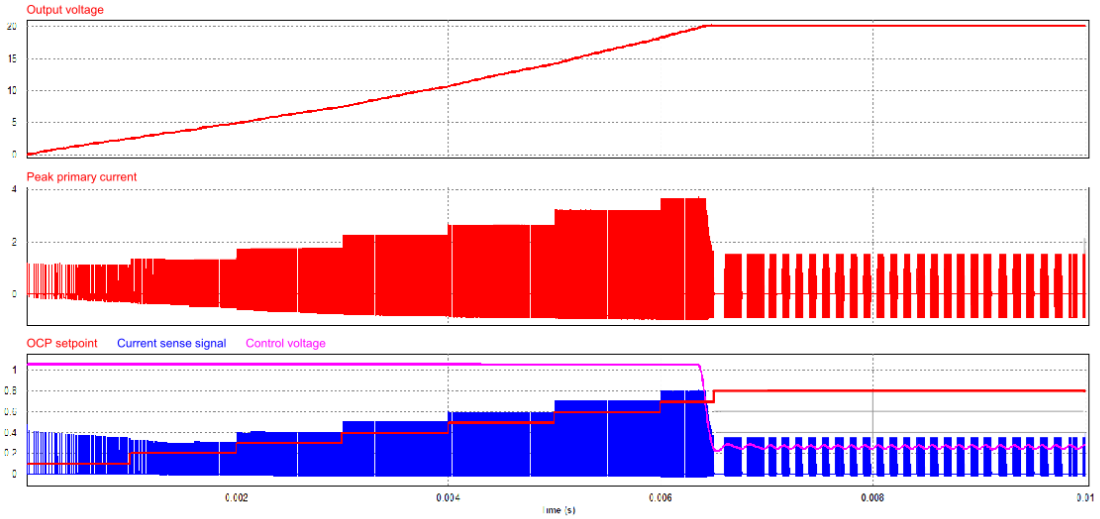
This function is active at every attempt of converter startup or restart after a fault.

At the end of the 8th step an internal logic flag (SSE, soft-start end) is asserted high to inform the state machine that supervises the operation of the IC that the startup phase of the converter is completed and that the following actions are to be taken:

- The LEB on the current sense is reduced from 150 ns to 50 ns;
- The overload protection function (OLP, see the relevant section) is enabled;
- The timer T_{FRT}, set at 20 µs during the soft-start phase to reduce the risk of CCM operation when the signal on the ZCD pin is low, is set at 2 µs;
- Burst mode operation with high-side switch turned on every eight cycles (that is, BM_ON flag may be set high).

If the COMP voltage enters the frequency foldback region before the 8th step of soft-start is completed (like the case shown in Figure 27), the counter is forced to end-of-count and the SSE flag is asserted high.

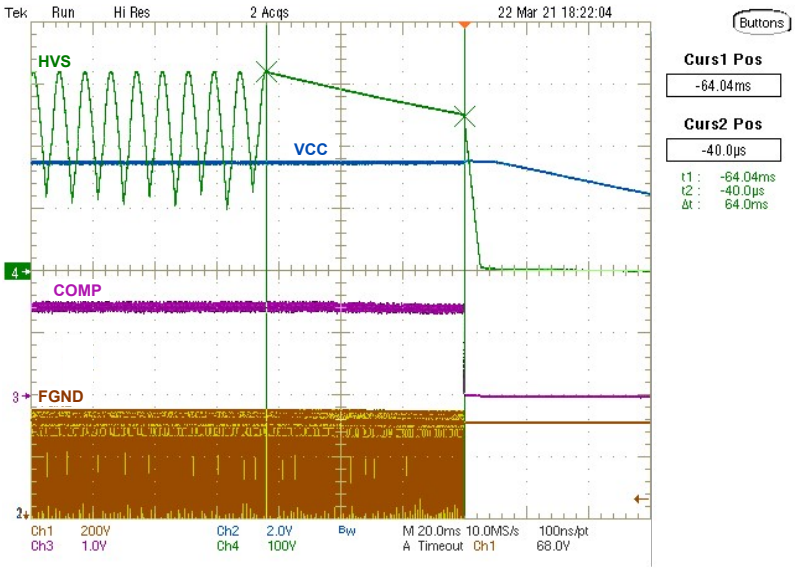
Figure 27. **Simulated startup at light load of an STACF01A/B based converter showing soft-start**



6.17 X-cap discharge function (STACF01A only)

The compliance of consumer equipment powered from the AC line with safety regulations such as IEC 61010-1, IEC 62368-1 and others, requires that the EMI filter capacitors connected between the phase and neutral wires (the so-called X-caps) must be discharged at a safe level when the converter's plug is disconnected from the socket if they are larger than 100 nF. The objective is to avoid any risk of electrical shock due to the energy stored in the X-caps in case the user touches the pins of the plug.

Figure 28. **X-cap discharge operation**



Typically, this function is performed with a resistor in parallel to the X-caps but this method cannot be applied in case the converter is required to consume very-low power during light or no-load conditions: the power losses associated with the discharge resistor could be too high and prevent reaching the target.

To overcome this issue, the STACF01A/B use the HV startup circuit to perform the X-cap discharge function, allowing the removal of the traditional X-cap discharge resistor without any specific external component.

The STACF01A/B detect the AC mains plug disconnection by sensing the voltage on the HVS pin and using a proprietary algorithm. After a typical detection time of 64 ms from mains disconnection, the HV startup cell is turned on: a discharge current (4 mA minimum) is drawn from the HVS pin ensuring the X-cap discharge until the voltage on the HVS pin falls below a SELV (safety extra low voltage) level, well within the maximum discharging time envisaged by the regulations, as shown in Figure 28. The worst-case discharge time needed to reach the final value (45 V max.) is:

$$T_{DIS} \approx 78 + 82.5 Cx_{Tot} \quad (43)$$

where Cx_{Tot}, the total X capacitance on the AC side of the input bridge, is expressed in µF and T_{DIS} in ms.

The current from the HVS pin flows to ground through an internal structure that prevents the voltage on the VCC pin from dropping below the UVLO threshold, so that the IC is correctly supplied until the end of the discharge.

The STACF01B does not have the X-cap discharge function because it is considered for ACF stages with a DC input voltage (like an ACF stage with a PFC in front or supplied by a DC bus, for example, emergency lighting applications). In this case the DC voltage would be interpreted as a mains disconnection, the HVS current generator would be turned on and, since the input voltage would not be discharged, the IC is overheated and damaged.

6.18 Protections

The IC is equipped with a full set of protection features that aim to protect the load and the converter itself against a number of possible failures that may occur on both the primary and the secondary side.

Faults are classified as follows:

- Latched: unrecoverable faults that hang the converter until manual intervention from the user (power recycling: the unit is to be disconnected from the input source and then reconnected after a while to attempt a restart)
- Autorecovery: faults that cause the converter to temporarily stop and try to restart after a timeout has elapsed. This operation continues until the fault is removed
- Direct: faults that are detected immediately on their first occurrence
- Filtered: faults requiring occurance a number of times before triggering a fault condition.

Once one of the protection features is triggered, the control is passed to the fault management state machine (FMSM) that handles the fault according to the specific handling rules set for each of them.

More specifically, any fault detected by the analog circuitry is processed by the FMSM as soon as the first deadtime is encountered: the control loop execution is stopped, switching is inhibited, and the IC is put in a low consumption mode. Being the converter is stopped too, no energy comes from the self-supply circuit and the IC supply voltage (VCC) decays slowly.

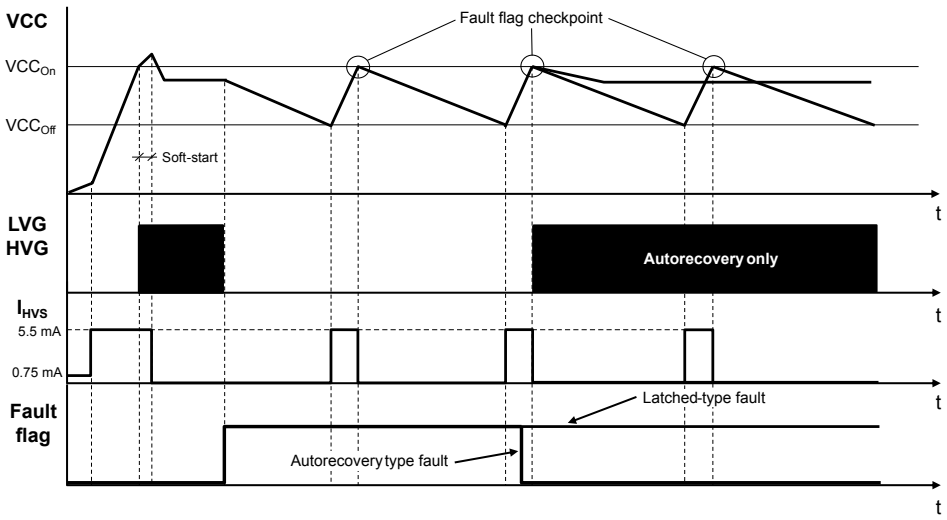
To ensure that the internal logic is always properly supplied, so that the appropriate fault handling procedure can be executed, the FMSM keeps VCC oscillating between the thresholds VCC_{On} and VCC_{off} by means of the HV startup generator, which is periodically active. This is illustrated in the timing diagram of Figure 29.

Whenever VCC exceeds the VCC_{On} threshold, the FMSM checks if a fault flag is active, then:

- If a fault flag of a latched protection is active, the IC remains inoperative with low consumption. The VCC voltage keeps on oscillating and there is no way to exit from this operation other than by removing the supply voltage of the converter. This removal must be long enough to let the voltage on the HVS pin go below the brownout threshold (see the “*AC brownout*” section), which clears the fault flag
- If a fault flag of an autorecovery protection is active, then the IC checks for the restart conditions. If these are fulfilled, then the IC is turned on and the normal operating sequence at startup takes place (see the “*High-voltage startup generator and Line voltage monitoring functions*” section). If not, the IC remains inoperative with low consumption until the next VCC cycle
- If no fault flag is active, the IC is turned on and the normal operating sequence at startup takes place (see the “*High-voltage startup generator and Line voltage monitoring functions*” section).

Fault events are managed based on a FIFO approach: the first active fault is the first being serviced. If the fault is recovered and there is no other pending fault, then the IC resumes the normal operation.

Figure 29. **Timing diagram: HV startup and VCC behavior after a fault (timings are not to scale)**



6.18.1 Overvoltage protection (OVP)

The OVP function monitors the voltage V_{ZCD_s} sampled on the ZCD pin at the demagnetization instant, which is an accurate image of the output voltage of the converter. Figure 30 shows the internal block diagram and the timing diagrams in Figure 31 illustrate the operation.

If this voltage exceeds an internal reference V_{REF_OVP} (= 3 V), a comparator is triggered, and a potential overvoltage condition is assumed. In fact, to reduce sensitivity to noise and distinguish a real failure from a disturbance (for example, induced during ESD tests), the OVP comparator must be triggered for four consecutive switching cycles in order for the protection to be tripped (filtered protection). A 2-bit counter, which is reset every time the OVP comparator is not triggered in a switching cycle, serves this purpose.

Note that V_{ZCD_s} is the output of the sample-and-hold block S/H, which has its own internal time constants, thus under dynamic conditions V_{ZCD_s} may take more than one switching cycle to align to the instantaneous value of V_{ZCD} at the demagnetization instant. Then, there are situations where it is possible to observe more than 4 cycles with V_{ZCD}>3 V before tripping the protection.

Such an overvoltage is assumed to be caused by a hardware failure in the feedback loop (for example, the optocoupler breaks down), thus it is considered unrecoverable and is a latched type (see the previous section for the description of how this is handled).

Figure 30. **OVP function: internal principle schematic**

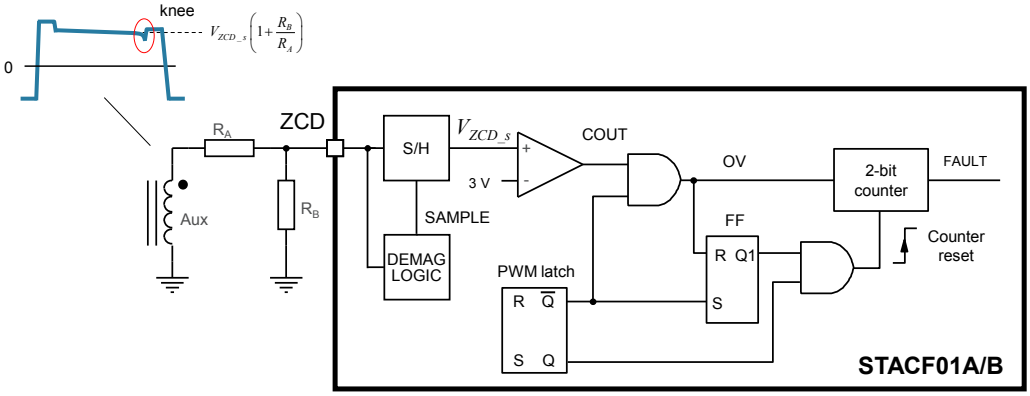
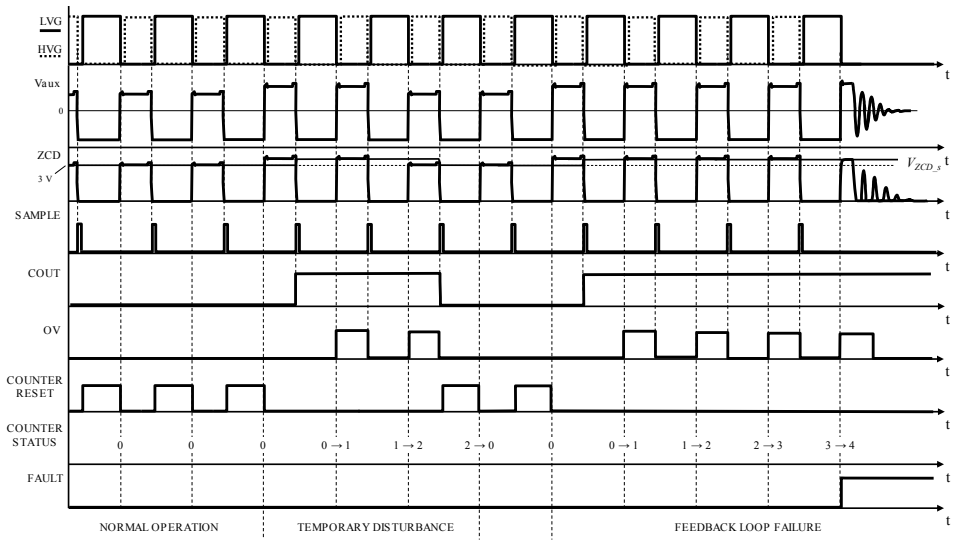


Figure 31. **OVP function: timing diagram**



The OVP detection level $Vout_{OVP}$ can be defined according to the formula:

$$R_B = \frac{V_{REF\_OVP}}{\frac{N_{aux}}{N_{sec}} Vout_{OVP} - V_{REF\_OVP}} R_A \quad (44)$$

where N_{sec} and N_{aux} are the secondary and auxiliary turns number, respectively. The R_A value is defined as described in the "*Input voltage feedforward*" section.

6.18.2 Overload protection (OLP)

OLP aims to protect the converter in case of overload or short-circuit by forcing the converter to work intermittently with a small duty cycle as long as the anomalous loading conditions lasts, so that it works safely with extremely low-power throughput and limited stress of power components.

An overload condition is detected when the signal V_{CSref} that programs the peak primary current exceeds the threshold V_{CSref_OL}, which occurs whenever the control voltage V_{COMP} is saturated high. In general, this condition reveals an open-loop condition for the feedback system and a loss of output voltage regulation.

This condition normally occurs at startup (therefore OLP is inhibited during the soft-start phase) but may also be caused by either a control loop failure or an overload or a short-circuit at the output. A control loop failure results in an output overvoltage that is handled by the OVP function (see the relevant section). Therefore, the condition $V_{CSref} > V_{CSref\_OL}$ is used only as an overload/short-circuit detector.

The handling rule of OLP considers that in many applications there are peak loading conditions that might bring the converter out of regulation for a short time. In any case, it is normally required that the converter have some ride-through capability and does not interrupt its operation immediately if out of regulation.

When the $V_{CSref} > V_{CSref\_OL}$ condition is detected, a timer with 50 ms timeout consisting of an up-down counter is started up and keeps on counting up as long as this condition lasts. Two possible scenarios, shown in the timing diagram of Figure 32, are to be considered:

- The $V_{CSref} > V_{CSref\_OL}$ condition is continuously maintained until the OLP timer reaches the 50 ms timeout.

The FMSM stops the converter, resets the 50 ms timer, and starts up another timer with a 1.2 s timeout. This timeout must be elapsed before clearing the fault flag; thus the converter is enabled to restart at the first VCC > VCC_{On} occurrence after the 1.2 s timeout has elapsed.

In this way, the FMSM ensures that under continuous overload or short-circuit conditions the converter runs with a duty cycle lower than 5%. The average output current and power throughput is then attenuated more than 20 times compared to the levels that would occur in case of continuous operation.

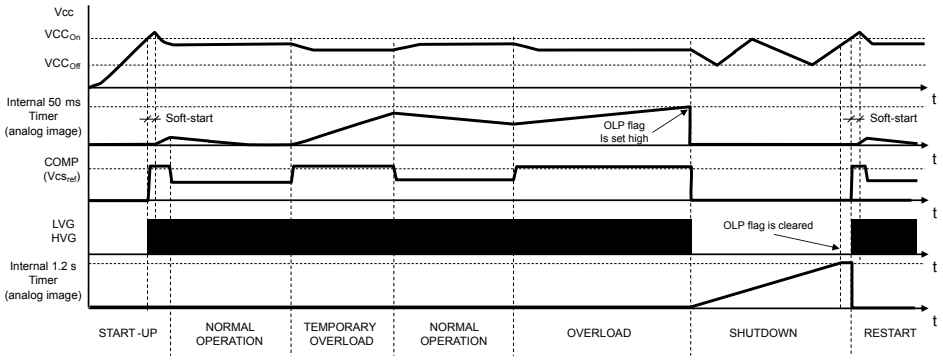
- The $V_{CSref} > V_{CSref\_OL}$ condition disappears before the OLP timer reaches the 50 ms timeout.

As this happens, the counter starts counting down at a speed four times slower until it reaches zero or it is $V_{CSref} > V_{CSref\_OL}$ again. In the first case, the counter stops and stays at zero, in the second case, it starts counting up again. In this way, if another overload occurs before the timer reaches zero, the actual timeout is now shorter than 50 ms; the closer to the previous one, the shorter the current timeout.

Also, in case the IC enters UVLO (VCC < VCC_{Off}) before the 50 ms timeout has elapsed, the counter is frozen, so that if the overload is still there the timer starts counting from the value it had when it was interrupted.

These features are essential to prevent that recurrent overloads may bring to a paradoxical situation where the converter runs overloaded most of the time with no OLP intervention.

Figure 32. OLP function: timing diagram showing typical behavior under overload/short-circuit



6.18.3 2nd level overcurrent protection (OCP2)

As shown in Figure 11, a dedicated comparator senses and compares the voltage on the current sense pin to a 1.2 V reference, which is well above the cycle-by-cycle current limitation threshold V_{CSx-0} (= 0.75 V). Its output provides a signal to the “OCP2 logic” block.

Normally, even with a dead short at the output of the converter the peak current does not rise to the point that the current sense signal touches this second reference.

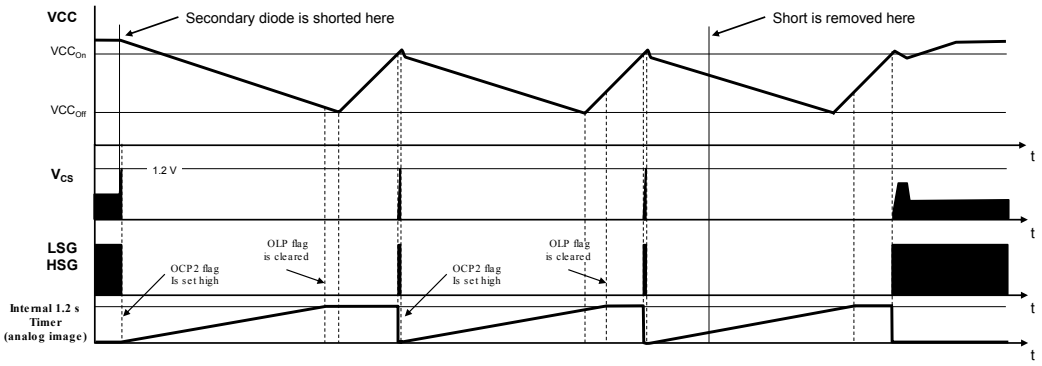
However, under some hardware failures such as a short-circuit of the secondary rectifier or a shorted secondary winding, or in case of a hard-saturated transformer, the primary inductance essentially disappears. As a result, during the on-time of the LS switch the primary current ramps up with a slope determined by the leakage inductance of the transformer, typically 20 to 100 times larger.

With so high a slope, during the total propagation delay of current sense T_{DEL} (see the “*Cycle-by-cycle current limitation and input voltage feedforward*” section) the primary current builds up well over V_{CSx-0}.

Additionally, with a hard-saturated transformer or a hardware failure such as those previously mentioned, demagnetization might not be properly sensed, and a new switching cycle might be initiated before the transformer is demagnetized. This would cause an uncontrolled primary current build-up until something breaks down (most likely, the LS switch brought to work in its linear region, then with an extremely high power dissipation).

For these reasons, running into this condition must be prevented and, when this 2nd level overcurrent threshold is hit, the converter needs to be stopped. This function is embedded in the STACF01A/B and its operation is shown in the timing diagram of Figure 33.

Figure 33. **OCP2 function: timing diagram showing typical behavior**



To distinguish a real failure from a disturbance (for example, induced during ESD tests), the first time the OCP2 comparator is tripped the protection circuit enters a “warning state”. If in the next switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic is reset; if in the next cycle the comparator is tripped again, a real malfunction is assumed and the IC enters the relevant fault handling procedure. This is the purpose of the “OCP2 logic” block.

The handling rule of OCP2 is the same as that of OLP, with the 50 ms latency replaced by the two-switching-cycle latency. Therefore, as the OCP2 comparator is triggered in two consecutive switching cycles, the FMSM stops the converter and resets the protection logic; the 1.2 s timer is started up and the converter allowed to restart at the first VCC > VCC_{On} occurrence after the 1.2 s timeout has elapsed.

6.18.4 AC brownout protection

Brownout is essentially a long-term undervoltage of the power line, that is, a condition where the line voltage is lower than the minimum specified by the utility, or required for normal operation, for minutes or even hours. They may be harmful if not properly handled. The reason is that converters need to draw more current to compensate for the lower supply voltage condition, which may be very stressful for the primary power section and cause it to overheat.

It is therefore recommended to shut down the converter during brownouts and enable it to restart once the line voltage comes back to normal (autorestart protection).

In the STACF01A/B, the information on the input voltage to the converter is available via the line monitoring system (see the relevant section), and the relevant signal is processed as shown in Figure 34.

The DC level provided by the line monitoring system is compared to two reference voltages, V_{TH1} and V_{TH2} (> V_{TH1}). V_{TH1} corresponds to a DC voltage on the HVS pin equal to 95 V, V_{TH2} to 116 V. In terms of AC peak voltage, these values correspond to 67 and 82 Vrms respectively. These are the brownout and the brown-in level respectively.

The brownout detection logic is equipped with a debounce time (40 ms) long enough to let the converter ride through missing cycles (filtered protection); the brown-in condition is recognized if it persists for more than 1 ms.

The resulting behavior, shown in the timing diagrams of Figure 35, can be described as follows:

- As the IC turns on (VCC > VCC_{On}) for the first time after the AC line is applied, no fault flag is active and the IC checks whether the voltage on the HVS pin swings over the brown-in threshold (116 V):
  - If so, switching is enabled immediately, and the converter starts up;
  - If not, the AC_FAULT flag is asserted high and the FMSM forces the IC into protection mode, waiting for the restart conditions to be fulfilled. Note that the decision is immediate.

Figure 34. **AC brownout protection function: block diagram**

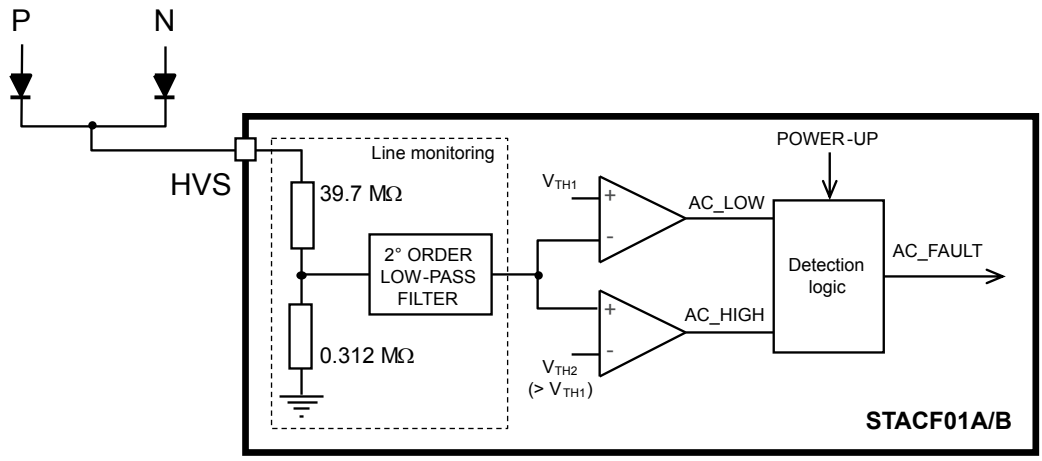
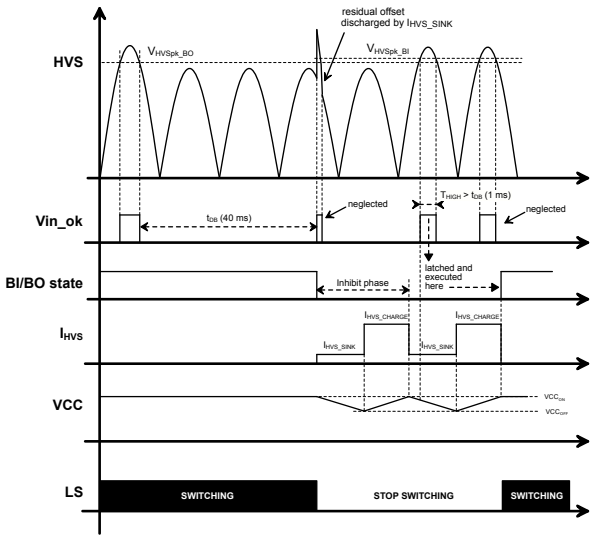


Figure 35. **AC brownout protection function: timing diagram showing typical operation**



- If the converter is running and the voltage on the HVS pin does not exceed the brownout threshold (95 V) for more than 40 ms, the AC_FAULT flag is asserted high and the FMSM forces the IC into protection (brownout) mode, waiting for the restart conditions to be fulfilled. As the converter stops and VCC starts bouncing between VCC_{On} and VCC_{RES}, brown-in detection is inhibited until VCC hits VCC_{On} for the first time. In this way any voltage spike generated by the EMI filter as the converter stops is blanked out.

- When the converter is in brownout mode, after VCC hits VCC_{On} for the first time, brown-in starts being monitored. Monitoring occurs only while VCC is discharging and during this phase the HV startup generator sinks a small current from pin HVS to ground that keeps the voltage on the pin always linked to the actual input voltage. If, while VCC is discharging the voltage on the HVS pin swings over the brown-in threshold (116 V) for more than 1 ms, the AC_FAULT flag is cleared. At the next VCC > VCC_{On} occurrence the converter restarts switching.

Whenever the brownout protection is triggered, fault flags of latched protections are cleared. This may allow a quicker restart of the converter as it is disconnected from the input source.

6.18.5 General purpose protection input

The STACF01A/B is provided with a general purpose protection input, PROT pin, that can be used for latch mode and autorestart mode protections.

- *Latched protection*
  The PROT pin is connected to the input of two internal comparators. If the voltage on the pin falls below a preset threshold $V_{PROT\_TH\_L}$ (= 1 V), a fault flag is set high. As with all other faults, after being synchronized to the FMSM, it causes the device to stop operating upon the first deadtime in the switching cycle occurring after synchronization. Then the IC is latched off, goes into low consumption mode, and VCC goes on bouncing between VCC_{On} and VCC_{Off}. The converter must be disconnected from the power line and then reconnected to restart.
- *Autorestart protection*
  The second comparator connected to the PROT pin has a threshold set at $V_{PROT\_TH\_H}$ (= 3 V). If the voltage on the pin goes above such threshold, a fault flag is set high and the IC stops switching immediately, not waiting for synchronization to the FMSM. Simultaneously, the restart threshold VCC_{RES} of the HV startup circuit is changed from VCC_{Off} to two times VCC_{Off} so that VCC goes on bouncing between levels that make sure the IC cannot enter UVLO and is ready to restart.
  The IC stays in this condition as long as the PROT voltage is higher than $V_{PROT\_TH\_H}$ minus 100 mV hysteresis; when the voltage falls below this value the fault flag is cleared and the IC restarts switching immediately.

An internal 50 µA source current is provided by the pin, therefore, to keep the IC running, the external resistance connected between PROT and GND must be in the range 20 ÷ 60 kΩ.

The pin can be used, for example, to realize an input overvoltage protection, an OTP protection or a remote ON/OFF control.

A small capacitor (max. standard value 330 pF) from the pin to ground, placed as close to the IC as possible to reduce switching noise pick-up, may help obtain clean operation.

Figure 36. Latched OTP protection using the PROT pin: principle schematic

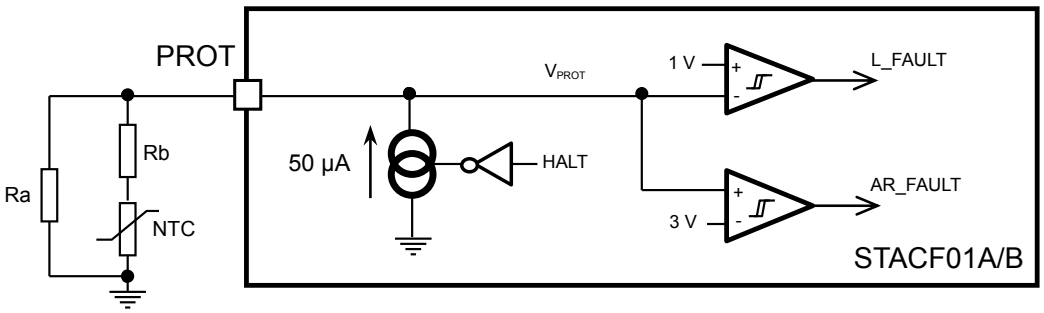


Figure 37. **Autorestart input OVP protection using the PROT pin: principle schematic**

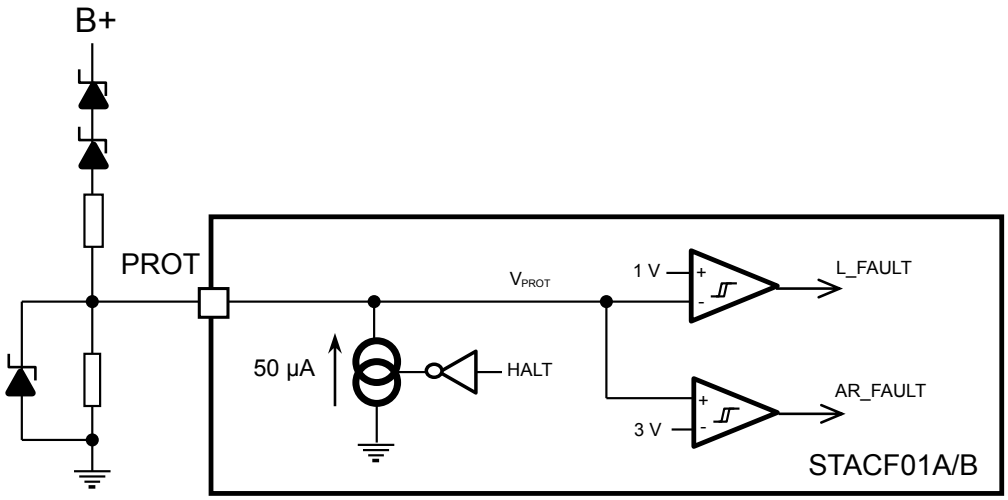
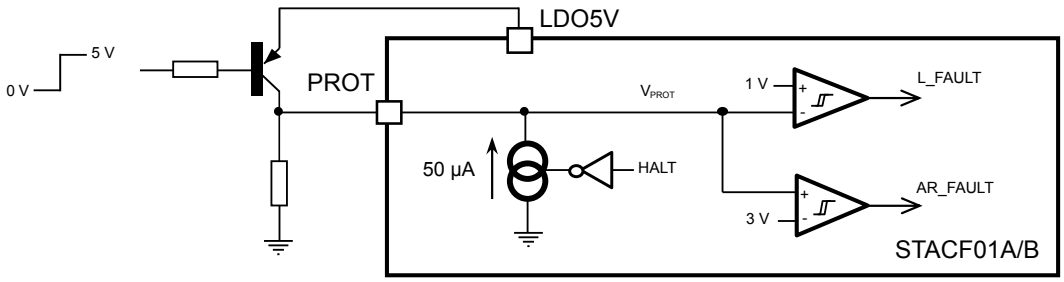


Figure 38. **Remote ON/OFF function using the PROT pin: principle schematic**



6.18.6 Summary of protection functions

To help the user familiarize with the protection functions of the device, Table 8 summarizes all of them with their respective activation and deactivation mechanisms.

This table can be useful not only for a correct use of the IC but also for diagnostic purposes: especially at the prototyping/debugging stage; it is quite common to bump into unwanted activation of some protection function, and the table can be used as a quick troubleshooting guide.

Table 8. **Faults/protections summary table**

Description	Detection	System behavior	Restart condition
VCC undervoltage	$VCC \le VCC_{Off}$	IC stopped HV STARTUP enabled	$VCC \ge VCC_{On}$
BBVIN undervoltage	$BBVIN \le V_{BBVIN\_Off}$	Buck-boost stopped HV STARTUP recycles VCC between VCC_{Off} and VCC_{On}	$BBVIN > V_{BBVIN\_On}$
AC line brownout	$V_{HVS} < V_{HVSpk\_BO}$ for 40 ms	IC stopped HV STARTUP recycles VCC between VCC_{Off} and VCC_{On} All previous faults are reset	$V_{HVS} \ge V_{HVSpk\_BI}$ for 1 ms & $VCC \ge VCC_{On}$

Description	Detection	System behavior	Restart condition
External shutdown (latch mode)	$V_{PROT} < V_{PROT\_TH\_L}$	IC latched off HV STARTUP recycles VCC between VCC_{Off} and VCC_{On}	$V_{HVS} < V_{HVSpk\_BO}$ for 40 ms, then: $V_{HVS} \geq V_{HVSpk\_BI}$ for 1 ms & $VCC \geq VCC_{On}$ & $V_{PROT} \geq (V_{PROT\_TH\_L} + V_{PROT\_Hys-l})$
External shutdown (autorestart mode)	$V_{PROT} > V_{PROT\_TH\_H}$	IC stopped HV STARTUP recycles VCC between VCC_{RES} and VCC_{On}	$V_{PROT} < (V_{PROT\_TH\_H} - V_{PROT\_Hys-h})$
OVP	$V_{ZCD\_s} > V_{ZCD\_OVP}$ for 4 consecutive switching cycles	IC latched off HV STARTUP recycles VCC between VCC_{Off} and VCC_{On}	$V_{HVS} < V_{HVSpk\_BO}$ for 40 ms, then: $V_{HVS} \geq V_{HVSpk\_BI}$ for 1 ms & $VCC \geq VCC_{On}$
Cycle-by-cycle OCP level	$V_{CS} > V_{CSx}$	LS switch on-time terminated earlier than PWM control would. 50 ms OLP timeout counter counts up if soft-start is over	Normal restart in next switching cycle
OLP	$V_{CSref} > V_{CSref\_OL}$ for 50 ms Soft-start is over	HV STARTUP recycles VCC between VCC_{Off} and VCC_{On} The system waits 1.2 s and then restarts	Internal timer = 1.2 s & $VCC \geq VCC_{On}$
2nd level OCP	$V_{CS} > V_{CS\_OCP2}$ for 2 consecutive switching cycles	HV STARTUP recycles VCC between VCC_{Off} and VCC_{On} The system waits 1.2 s and then restarts	Internal timer = 1.2 s & $VCC \geq VCC_{On}$
CCM operation	$V_{ZCD} \geq V_{ZCDT}$ when LS switch is to be turned on	Turn-on of the LS switch is delayed as long as the detection condition is maintained	Normal restart of the next switching cycle occurs as $V_{ZCD} < V_{ZCDT}$
Short-circuit	$\lvert V_{RCS} \rvert > \lvert V_{RCSx} \rvert$ & $V_{CSref} > V_{CSref\_OL}$	HS switch on-time terminated earlier than ZVS Timer would. Soft start is reset.	Normal restart in the next switching cycle after a longer deadtime (= T_{BASE})
Cycle-by-cycle reverse current limitation (for example, output voltage transition)	$\lvert V_{RCS} \rvert > \lvert V_{RCSx} \rvert$	HS switch on-time terminated earlier than ZVS Timer would.	Normal restart in the next switching cycle after a longer deadtime (= T_{BASE})

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 QFN 5x5 package mechanical data

Figure 39. QFN5x-23L mechanical data

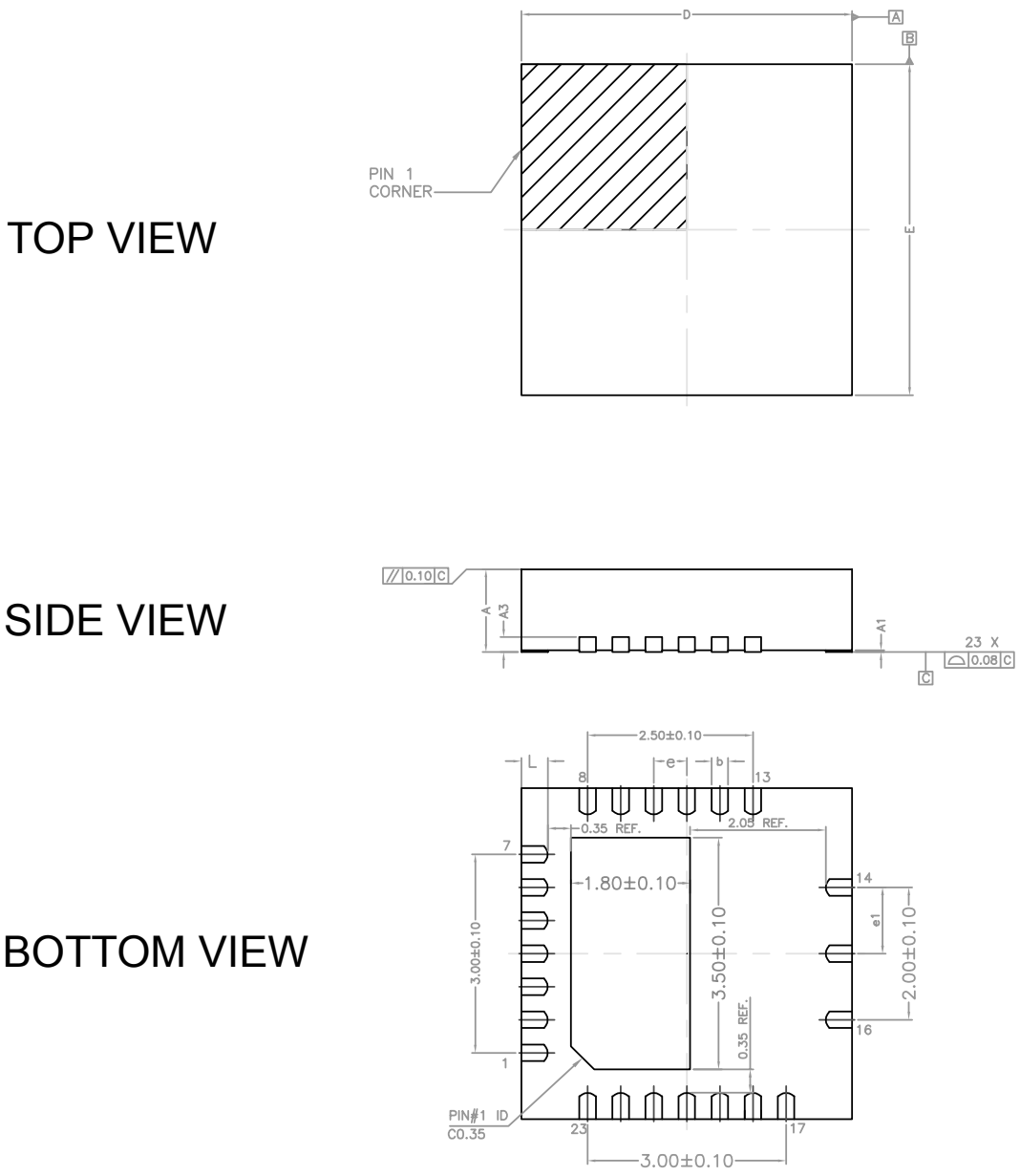
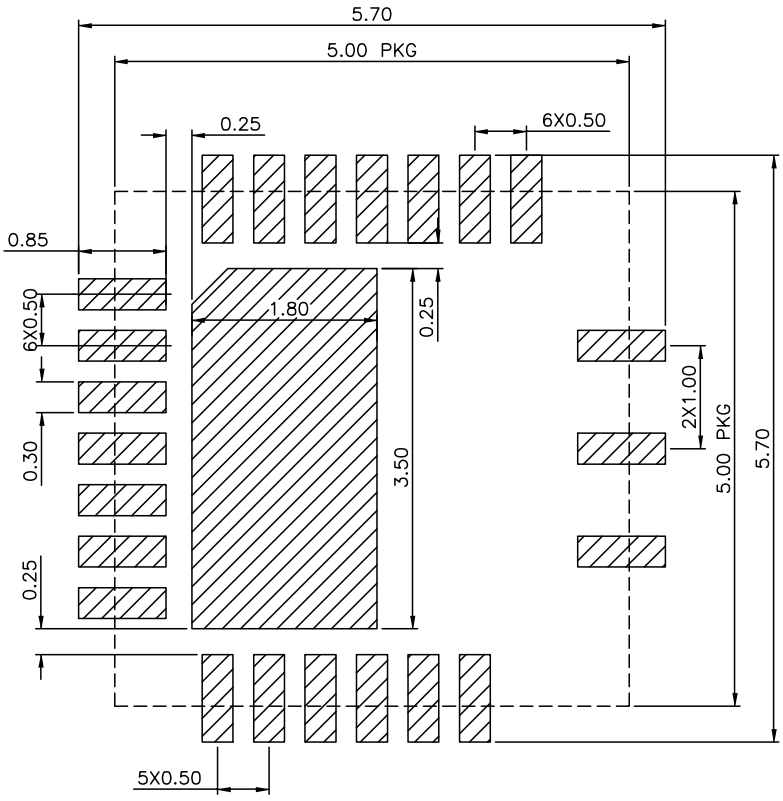


Table 9. Package dimensions

Drawing (mm)				
Ref.	Min.	Typ.	Max.	Notes
A	1.127	1.177	1.227	
A1	0.00	-	0.05	
A3		0.15 Ref		
b	0.20	0.25	0.30	
D	4.90	5.00	5.10	
D1	SEE EXPOSED PAD VARIATION			
E	4.90	5.00	5.10	
E1	SEE EXPOSED PAD VARIATION			
e	0.50 BSC			
e1	1.00 BSC			
L	0.30	0.40	0.50	

Figure 40. Suggested footprint



8 Ordering information

Table 10. **Ordering codes**

Order code	Marking	Package	Packing
STACF01A	STACF01A	QFN 5x5	Tray
STACF01ATR	STACF01A	QFN 5x5	Tape and Reel
STACF01B	STACF01B	QFN 5x5	Tray
STACF01BTR	STACF01B	QFN 5x5	Tape and Reel

Revision history

Table 11. **Document revision history**

Date	Version	Changes
05-Dec-2024	1	Initial release.
13-Mar-2025	2	Modified following parameters limits in Table 7: I_{Q_BURST}, I_{Q_OP}, $I_{COMPmax}$, V_{ZCD_HGs}, T_{FRT}, V_{CSref_BM}, I_{PROT}

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