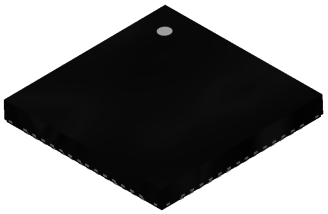
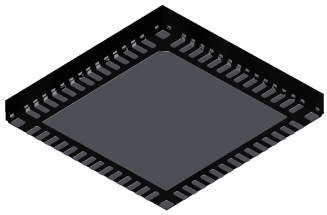
STA8600

Datasheet

TeseoVI single-die quad-band GNSS receiver





VFQFPN56 (7 × 7 × 0.9 mm)
with wettable flanks

Product status link
STA8600

Product summary		
Order code	**Packing**	**Secure**
STA8600	Tray	No
STA8600E		No
STA8600P		No
STA8600TR	Tape and reel	No
STA8600ETR		No
STA8600PTR		No

Features

Highlights

- Arm® Cortex®-M7
- Embedded RAM/NVM/cache
- Dedicated ADC for antenna sensing
- *ESD*: 2 kV (*HBM*) and 500 V (*CDM*)
- Temperature range: -40°C to +105°C

GNSS features

- STMicroelectronics' sixth generation positioning receiver with six constellations: *GPS*, *Galileo*, *GLONASS*, *BeiDou*, *QZSS*, *NAVIC* (former *IRNSS*)
- Standard *PVT* positioning supporting up to quad-band (dual-band on STA8600E) for submeter accuracy applications
- Precise *PVT* positioning supporting up to quad-band for centimeter-level accuracy applications (STA8600P only)
- TESEO-DRAW (dead reckoning automotive way) support
- Measurement engine with up to quad-band (dual-band on STA8600E) to support precise positioning algorithms
- Code phase, carrier phase, doppler frequency measurement
- Support any *SBAS* systems
- Independent *GPS*/*QZSS* L5, *Galileo* E5a/b, *BeiDou* B2a acquisition & tracking
- 192 (96 data & 96 pilot) signal tracking channels
- Signal integrity (antijamming/antispoofing)

Communication interfaces

- Two *UART* ports for host communication supporting hardware flow control
- One synchronous serial port (*SSP*) for host communication
- One I²C port for sensor interfacing
- One *SPIQ* port for sensor interfacing
- Two *PPS* configurable I/Os

Core peripherals

- Embedded *DMA*
- 32 kHz oscillator real-time clock
- Watchdog timer
- One extended function timer

Power management unit

- Separate power supply domains:
  - Backup domain: 1.71 V to 3.63 V
  - Switchable domain: 1.71 V to 3.63 V
  - Optional external core supply voltage: 0.9 V to 1.0 V
- On-chip *LDO*s with high-voltage/low-voltage monitors

1 Introduction

1.1 Description

The STA8600 is a quad-band multiconstellation positioning receiver IC. It requires minimal external components since it embeds enough *MIPS*/memory resources for supporting up to quad-band (dual-band on STA8600E) algorithms on chip (with submeter accuracy). It supports dead reckoning automotive way (TESEO-DRAW) and dead reckoning unplugged mode (Teseo-DRUM) to ensure high-accuracy positioning in harsh environments such as tunnels, garages, and deep urban areas.

The STA8600 provides measurement data with up to quad-band (dual-band on STA8600E). Combined with the *PPP*/*RTK* algorithm, the device provides high positioning accuracy. It shows great flexibility due to the capability to handle all software configurations with a unique binary firmware component.

The STA8600P supports a *RTK* embedded precise positioning algorithm enabling centimeter-level accuracy application without the need for an external host. It is suitable for drones, robotic lawn mowers and agriculture.

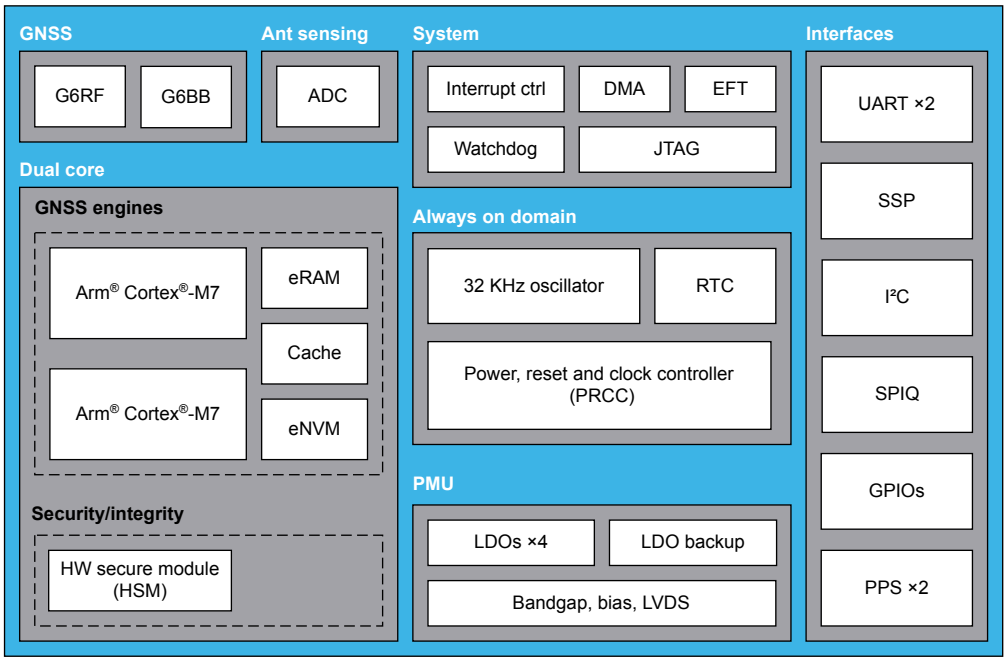
The STA8600 supports a highly evolved antijamming and antispoofing mechanism to mitigate attacks thanks to independent L5 acquisition and tracking, and to the *Galileo OSNMA* capability. The innovative RF architecture and *GNSS* baseband make it ready to support new emerging low Earth orbit (*LEO*) constellations.

The device is delivered in a QFN package.

2 Pin description

2.1 Block diagram

Figure 1. **Block diagram**



2.2 Pinout

Figure 2. **Pinout**

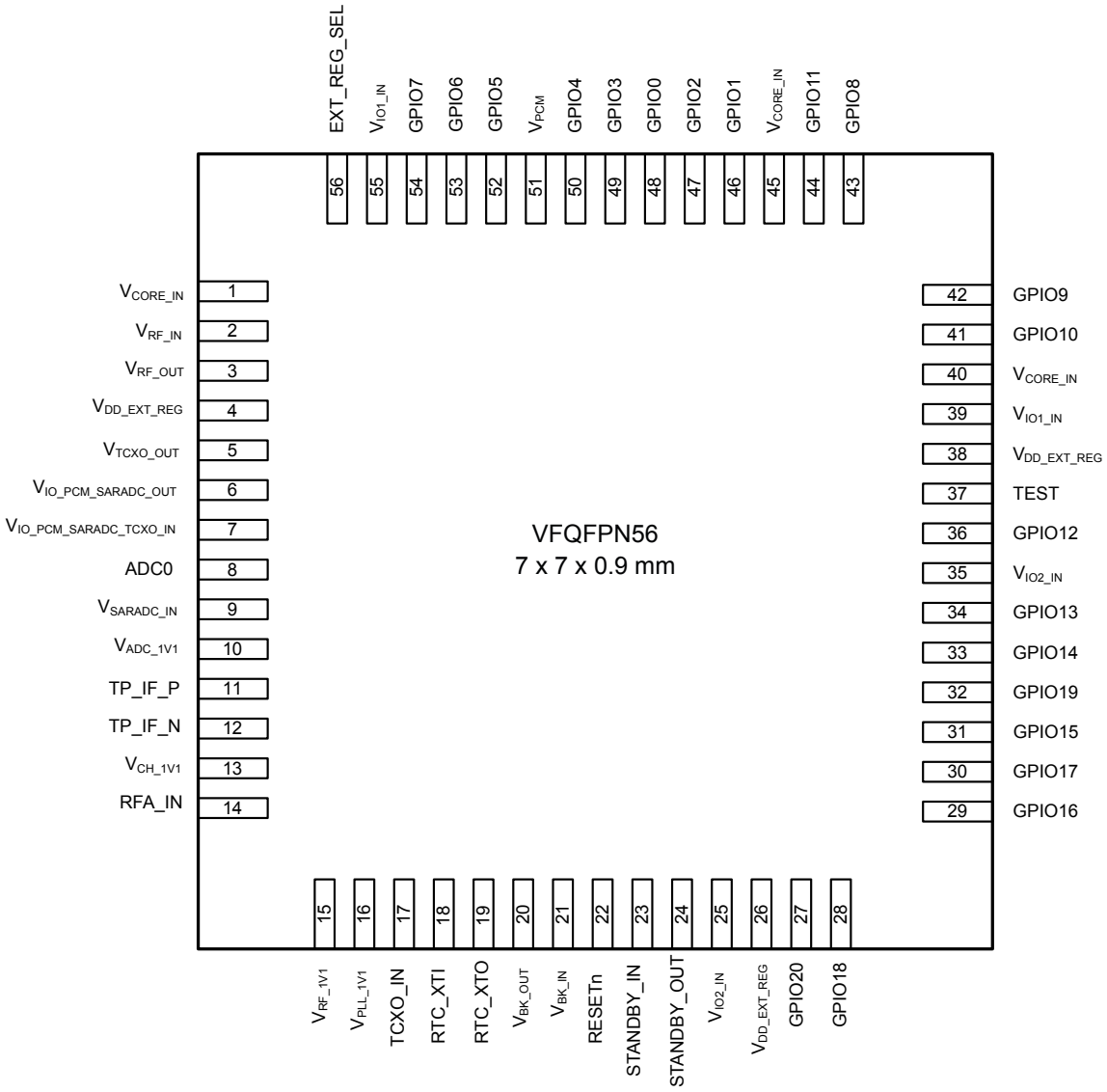


Table 1. **Power supply pins**

Symbol	Voltage domain	I/O	Description	Pin
V_{RF_IN}[(1)]	—	PWR	LDO RF power input	2
V_{RF_OUT}	RF domain	PWR	LDO RF power output	3
V_{ADC_1V1}	RF domain	PWR	RF ADC power	10
V_{RF_1V1}	RF domain	PWR	RF chain power	15
V_{PLL_1V1}	RF domain	PWR	RF PLL power	16
V_{CH_1V1}	RF domain	PWR	RF channel power	13
V_{BK_IN}	—	PWR	LDO backup power input	21
V_{BK_OUT}	Backup domain	PWR	LDO backup power output	20

Symbol	Voltage domain	I/O	Description	Pin
V_{CORE_IN}	—	PWR	LDO core power input	1, 40, 45
$V_{DD\_EXT\_REG}$	Core domain	PWR	LDO core power output/external power to core	4, 26, 38
V_{IO2_IN}	Ring2	PWR	IO Ring2 power supply	25, 35
V_{IO1_IN}	Ring1	PWR	IO Ring1 power supply	39, 55
V_{PCM}	PCM_SARADC domain	PWR	NVM power supply	51
$V_{IO\_PCM\_SARADC\_TCXO\_IN}$	—	PWR	Power input to LDO 3.3 V to 1.8 V	7
$V_{IO\_PCM\_SARADC\_OUT}$	PCM_SARADC domain	PWR	3.3 V to 1.8 V LDO output	6
V_{TCXO_OUT}	TCXO domain	PWR	Low noise 3.3 V to 1.8 V LDO output	5
V_{SARADC_IN}	PCM_SARADC domain	PWR	Power supply of SARADC	9
GND	GND	GND	Ground	Ground pad(2)

1. *Special care must be taken for V_{RF_IN} supply noise filtering. When possible, supplying it through a switching regulator must be avoided.*
2. *In addition to the exposed ground pad, four extra GND leads are positioned at the corners on the bottom side of the IC. See VFQFPN56 package information for additional information.*

Table 2. Main function pins

Symbol	Voltage domain	I/O	Description	Pin	Reset state
EXT_REG_SEL	VCORE_IN	I	LDO core disable. If latched high,at V_{CORE_IN} power-up, the LDO CORE is off. The core is supplied by an external power source.	56	NA
TEST	—	I	TEST - In mission/application mode, this pin must be connected to GND.	37	Hi-Z/PD
RTC_XTI	Backup domain	I	If 32 kHz oscillator is enabled, then this pin is the input of the 32 kHz oscillator amplifier circuit. Else, it is the CMOS input as per electrical characteristic table. Both cases, it is the reference for real time clock counter circuitry.	18	NA
RTC_XTO	Backup domain	O	Output of the oscillator amplifier circuit.	19	NA
RESETn	Backup domain	I	Reset input with Schmitt-Trigger characteristics and noise.	22	Hi-Z/PD
STANDBY_IN	Backup domain	I	Used to enter or exit standby mode, depending on configuration set by registers.	23	Hi-Z
STANDBY_OUT	Backup domain	O	Reflects internal mode of always on domain logic, depending on configuration by registers.	24	Hi-Z

Table 3. RF front-end pins

Symbol	Voltage domain	I/O	Description	Pin
TP_IF_P	RF domain	O	Only for test purposes	11
TP_IF_N	RF domain	O	Only for test purposes	12
RFA_IN	RF domain	I	RFA input	14
TCXO_IN	RF domain	I	TCXO input	17

Table 4. SARADC inputs

Symbol	Voltage domain	I/O	Description	Pin
ADC0	PCM_SARADC domain	I	SARADC input 0	8

Table 5. **Communication interface pins**

Symbol	Voltage domain	I/O	AF	Function	Description	Pin	Reset
GPIO0	Ring1	I	Default	JTAG-TRSTn/GPIO0[1]	—	48	PU
		I	ALT A	UART2_RX	UART2		—
		O	ALT B	PPS0_OUT	PPS		—
		O	ALT C	SSP0_TXD	SSP0		—
GPIO1	Ring1	I	Default	JTAG-TCK/GPIO1[1]	—	46	PD
		O	ALT A	EFT_OCMPB	EFT		—
		O	ALT B	PPS1_OUT	PPS		—
		O	ALT C	PP_CLK	PP		—
GPIO2	Ring1	I	Default	JTAG-TMS/GPIO2[1]	—	47	PU
		I	ALT A	EFT_ICAPB	EFT		—
		I	ALT C	BLANK_INT	—		—
GPIO3	Ring1	I	Default	JTAG-TDI/GPIO3[1]	—	49	PU
		I	ALT A	EFT_CLK	EFT		—
		I	ALT B	PPS1_IN	PPS		—
		I/O	ALT C	SSP0_CLK	SSP0		—
GPIO4	Ring1	O	Default	JTAG-TDO/GPIO4	—	50	—
		O	ALT A	UART2_TX	UART2		—
		I/O	ALT C	SSP0_FRM	SSP0		—
GPIO5	Ring1	I	Default	GPIO5	—	52	PD
		I	ALT A	SPIQ_IN	SPIQ		—
		O	ALT B	EFT_OCMPA	EFT		—
		I	ALT C	Ext_Q_mag1	External RF		—
GPIO6	Ring1	I	Default	GPIO6	—	53	PD
		O	ALT A	SPIQ_OUT	SPIQ		—
		I/O	ALT B	I2C_SDA	I2C		—
		I	ALT C	Ext_I_mag1	External RF		—
GPIO7	Ring1	I	Default	GPIO7	—	54	PD
		I/O	ALT A	SPIQ_CLK	SPIQ		—
		I/O	ALT B	I2C_CLK	I2C		—
		I	ALT C	Ext_Q_sign1	External RF		—
GPIO8	Ring1	I	Default	GPIO8	—	43	PD
		I/O	ALT A	SPIQ_CS	SPIQ		—
		I	ALTB	EFT_ICAPA	EFT		—
		I	ALT C	Ext_I_sign1	External RF		—
GPIO9	Ring1	I	Default	GPIO9	—	42	PD
		I	ALT A	UART0_RX	UART0		—
		I	ALT B	SSP1_RXD	SSP1		—
		—	ALT C	—	—		—
GPIO10	Ring1	I	Default	GPIO10	—	41	PD
		O	ALT A	UART0_TX	UART0		—

Symbol	Voltage domain	I/O	AF	Function	Description	Pin	Reset
GPIO10	Ring1	O	ALT B	SSP1_TXD	SSP1	41	—
GPIO11	Ring1	I	Default	GPIO11	—	44	PD
		I	ALT A	UART0_CTS	UART0		—
		I/O	ALT B	SSP1_FRM	SSP1		—
		I/O	ALT C	I2C_SDA	I2C		—
GPIO12	Ring1	I	Default	GPIO12	—	36	PD
		O	ALT A	UART0_RTS	—		—
		I/O	ALT B	SSP1_CLK	SSP1		—
		I/O	ALT C	I2C_CLK	I2C		—
GPIO13	Ring2	I	Default	GPIO13	—	34	PD
		O	ALT A	UART1_TX	UART1		—
		O	ALT B	PP_CLK	PP		—
		I	ALT C	EFT_ICAPA	EFT		—
GPIO14	Ring2	I	Default	GPIO14	—	33	PD
		I	ALT A	UART1_RX	UART1		—
		I	ALT B	PPS0_IN	PPS0		—
		O	ALT C	EFT_OCMPA	EFT		—
GPIO15	Ring2	I	Default	GPIO15	—	31	PD
		I	ALT A	UART1_CTS	UART1		—
		—	ALT B	—	—		—
		I/O	ALT C	I2C_CLK	I2C		—
GPIO16	Ring2	I	Default	GPIO16	—	29	PD
		O	ALT A	UART1_RTS	UART1		—
		I	ALT B	—	—		—
		I/O	ALT C	I2C_SDA	I2C		—
GPIO17	Ring2	I	Default	GPIO17	—	30	PD
		I	ALT A	PPS1_IN	PPS1		—
		—	ALT B	—	—		—
		I	ALT C	SSP0_RXD	SSP0		—
GPIO18	Ring2	I	Default	GPIO18	—	28	PD
		I/O	ALT A	I2C_CLK	I2C		—
		—	ALT B	—	—		—
		I/O	ALT C	SSP1_CLK	SSP1		—
GPIO19	Ring2	I	Default	GPIO19	—	32	PD
		I/O	ALT A	I2C_SDA	I2C		—
		—	ALT B	—	—		—
		I/O	ALT C	SSP1_FRM	SSP1		—
GPIO20	Ring2	I	Default	GPIO20	—	27	PD
		I	ALT A	PPS0_IN	PPS		—
		I	ALT B	—	—		—
		I	ALT C	EFT_CLK	—		—

1. *JTAG pins may be configured as GPIOs in a dedicated alternate function mode as: TRSTn=GPIO0, TCK=GPIO1, TMS=GPIO2, TDI=GPIO3, TDO=GPIO4*

3 General description

3.1 Multi-constellation and multi-band

The STA8600 supports the following constellations:

- GPS (L1 C/A, L2C, and L5)
- GLONASS (L1OF, L2OF)
- BeiDou (B1C, B1I, B2A, B2B, B3i)
- GALILEO (E1, E5a, E5b, E6)
- QZSS (L1 C/A, L1 C/b, L2C, L5)
- NAVIC - former IRNSS (L5)

The STA8600 can also provide carrier phase raw measurements.

The STA8600 supports different GNSS use cases. Some examples are listed in the table below. The desired use case can be selected through a proper firmware configuration.

Table 6. GNSS use-cases

Constellation	GPS/QZSS				GLONASS		BeiDou					Galileo				IRNSS	SBAS
Frequency	L1 C/A	L1C	L2C	L5	L1OF	L2OF	B1I	B1C	B2I, B2B	B2A	B3I	E1	E5b	E5A	E6	L5	Regional
Case 1: single band (narrow)	X	—	—	—	X	—	X	—	—	—	—	X	—	—	—	—	X
Case 2: single band (wide)	—	—	—	X	—	—	—	—	—	X	—	—	—	X	—	X	X
Case 3: dual band (narrow)	X	X	X	—	X	X	X	X	X	—	—	X	—	X	—	—	X
Case 4: dual band (wide)	X	X	—	X	—	—	X	X	—	X	—	X	—	X	—	X	X
Case 5: triple band	X	—	X	X	X	X	X	—	X	X	—	X	X	X	—	—	X
Case 6: quad band	X	—	X	X	X	X	X	—	X	X	X	X	X	X	X	—	X

3.2 RF front end (G6RF)

The integrated RF front end can support different bands (L1, L2, L5, and E6) thanks to a programmable and flexible RF-IF chain driven by a fractional PLL.The RF_IF chain is followed by a wide band ADC able to convert the IF signals to digital stream for base-band digital processor (G6BB).

The TCXO working frequency is 26 MHz.

3.3 Multi-band multi-constellation base band (G6BB) processor

The G6BB proprietary IP is the STMicroelectronics latest generation high-sensitivity baseband processor fully compliant with all different constellations and bands: GPS, Galileo, GLONASS, BeiDou, NAVIC (former IRNSS) and QZSS systems.

3.4 MCU subsystem

The microcontroller unit is based upon dual Cortex®-M7 cores. It masters the system resources (memories, registers, and external memory controllers) through the AXI, AHB and APB interconnections present in the SoC.

3.4.1 Caches

The size of the instruction and data cache used for Arm® subsystem in STA8600 is 16 KB for instruction cache and 16KB for data cache.

3.4.2 Tightly coupled memory (TCM)

Arm® Cortex®-M7 has a TCM control unit (TCU) with ITCM and DTCM interfaces with error detection logic.

An AHBS interface is connected to the AMBA infrastructure to allow the DMA to access the TCM memories.

3.4.3 Nested vector interrupt controller (NVIC)

This nested vectored interrupt controller (NVIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. Arm® Cortex®-M7 has an NVIC module for handling the interrupts. The NVIC supports up to 16 levels of priority, which may be changed dynamically. The software controls each request line to generate software interrupts.

3.4.4 AXI bus

The AXI bus matrix handles major high bandwidth transactions for the STA8600. It connects the SRAM, NVM, external memory controllers and digital interfaces supporting different protocols. The Arm® core acts as a manager on this bus: it has the highest priority.

3.4.5 Nonvolatile memory

NVM is based on the phase-change memory (PCM) technology, which allows the MCU to access with read/write operations at bit level. PCM does not need sector erase procedures before writing. The size is 2 MB, which is divided into two separate arrays of 1 MB each. Some space may be locked for write protection. NVM has redundancy files and dedicated logic for data error detection and correction at any read operation. A test is performed each time the device is powered up to check the NVM health state.

3.5 APB peripherals

A dedicated AHB-to-APB architecture has been implemented to connect all the STA8600 peripherals to the AHB bus.

3.6 eSRAM

Two blocks of eSRAM are available on top of the TCM RAM.

The eSRAM is directly connected to the MCU through the AXI bus. It is used for data and instruction.

3.7 SSP

The STA8600 supports two synchronous serial ports (SSPs). The SSP is a controller or target interface that enables synchronous serial communication with target or controller peripherals compliant with one of the following:

- Serial peripheral interface bus (SPI)
- Synchronous serial protocol bus standards
- Microwire interface bus standards
- Unidirectional interface

3.8 Queued serial peripheral interface (SPIQ)

The SPIQ module provides means for communication between the STA8600 and an external peripheral device using a synchronous serial interface. It provides multiple transfer group support for handling SPI sequences. A transfer group is a logical entity which uses DMA channels to establish a fully automated bidirectional memory transfer of SPI sequences and data.

3.9 I²C high-speed interface

The I²C high-speed module can work in controller and target modes. It supports the following baud rates: 100/400/1000/3400 kbit/s.

3.10 UART

The two UARTx (supporting HW flow control) perform serial-to-parallel conversion on data asynchronously received from a peripheral device on the UARTx_RX pin, and parallel-to-serial conversion on data written by the CPU for transmission on the UARTx_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data bytes for transmission, and 64 data bytes with 4-bit status (break, frame, parity, and overrun) for receive. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to sixteen words per transfer.

3.11 Watchdog timer (WDT)

Watchdog timer (WDT) provides a way of recovering from software crashes.

The watchdog monitors the interrupt and asserts a hardware reset signal if the interrupt remains unserviced for the entire programmed period. The WDT counts down at a fixed frequency of 32.768 kHz.

3.12 GPIO

The GPIO block provides programmable inputs or outputs. Each input or output is controlled in two modes:

- Software mode through an APB bus interface
- Alternate function mode, where GPIO becomes a peripheral input or output line

Any GPIO input may be independently enabled or disabled (masked) for interrupt generation. For each GPIO, the edge (rising, falling, both) that triggers an interrupt can be selected.

All GPIOs are fail-safe to avoid leakage consumption in any condition even when the ring-domain is off and the external line is logic level high.

3.13 Multi timer unit (MTU)

The two MTUs consist of eight timers each.

3.14 Real time clock (RTC)

It belongs to the always-on power domain dedicated logic (backup system) with 32 bytes of SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high-resolution clock which is used for GPS. It keeps the time when the system is inactive and is used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

3.15 Hardware security module (HSM)

The embedded HSM concept is based on a strict and clean boundary definition between the HSM domain and the rest of chip. To prevent any unauthorized access to secure resources, either secrets or functionally related to secret information, the proposed architecture does not allow the main Cortex®-M7 core to access the HSM internals directly. All exchanges are controlled by a dedicated software API, which is implemented on top of the mailbox hardware IP.

The HSM subsystem has an internal bus matrix architecture to interact between the different modules present inside the security subsystem.

The HSM architecture is essentially composed of:

- A secure core, dedicated to implementing a strict set of commands that may be activated from the host processor by means of a well-defined interprocessor communication mechanism. The HSM core acts as a transmitter on this HSM bus matrix.
- A mailbox IP allowing commands and data to be exchanged with the host processor in a controlled way.
- A field programmable OTP for storing the secret keys, as well as handling the product life cycle.
- A programmable hardware crypto accelerator, called C3, able to perform memory-to-memory transfers, along with cryptography operations which support SHA, SHA3, AES with ECB, CBC, CTR, CCM, CMAC, GCM, GMAC modes, and PKA.

Only the HSM can access security-sensitive hardware resources from the outside.

3.16 Direct memory access (DMA)

The DMAC is an advanced microcontroller bus architecture (AMBA®) compliant system-on-chip (SoC) peripheral. The DMAC connects to the advanced high-performance bus (AHB).

3.17 Successive approximation register analog to digital converter (SARADC)

The SARADC is a one-input channel 10-bit SARADC with capacitive DAC. Its implementation intrinsically guarantees very low sensitivity to internal component mismatch.

3.18 Temperature sensor (VTsense)

The thermal sensor provides the digital measurement of the junction temperature. The temperature measurement range is −40 to 125 °C. It uses integrated bandgap reference and 8-bit ADC.

Table 7. Temperature sensor

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Tsens	CC	C	Sensitivity	—	—	—	1	°C
Tacc(1)	CC	P	Accuracy	Calibration performed at 110 °C	±3(2)	—	±10	°C

1. *Best accuracy is at calibrated temperature.*
2. *Limited by manufacturing calibration environment.*

3.19 Reset

After a reset, the Cortex®-M7 is woken up by the boot code.

The PRCC module is used to sequence through all the steps needed to properly reset the device and prepare it to fetch the first instruction of the user application code.

The STA8600 has the following reset options:

1. Pad reset: SoC has an active low chip reset (RESETn) pad. Low (zero) status on this pad keeps the device under reset.
2. Power on reset: The power on reset circuitry is embedded in the main voltage regulator built on HV supply (V_{CORE_IN}) of regulator. It ensures all logics on this supply are under reset state until V_{CORE_IN} (or $V_{DD\_EXT\_REG}$) minimum voltage is reached.
3. Hardware resets: The internal voltage regulator embeds multiple low voltage detectors (LVD) and high voltage detectors (HVD) which are used in the reset sequence.
4. Soft reset: Different peripherals present on STA8600 reset independently through registers present inside PRCC module.

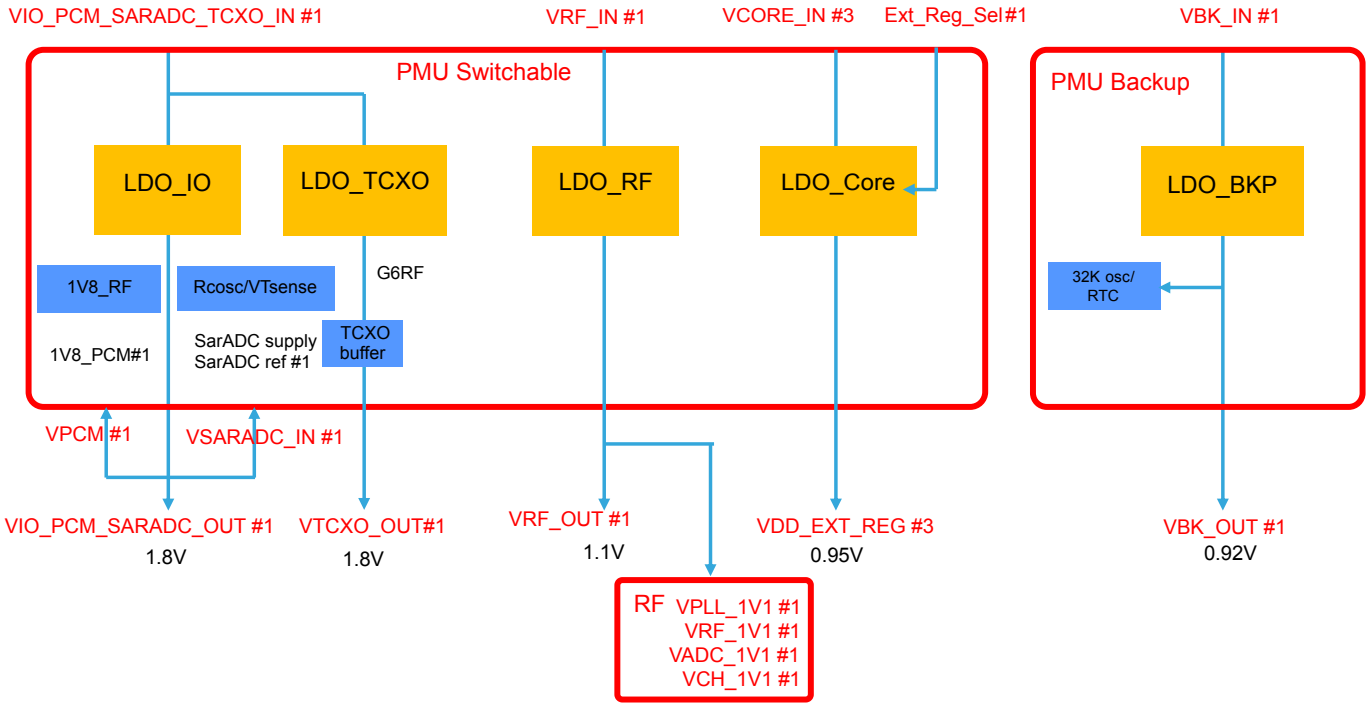
3.20 Power management unit (PMU)

STA8600 embeds five voltage regulators (LDO):

Table 8. LDO on-chip regulators

LDO	Supplied modules	Input voltage	Typical output voltage at 25°C
LDO_Core	Core (switchable domain logic)	V_{CORE_IN} = 1.71 – 3.63 V	0.95 V
LDO_IO	NVM, VTsense, SARADC, RF 1.8 V voltage reference	$V_{IO\_PCM\_SARADC\_TCXO\_IN}$ = 3.0 – 3.63 V	$V_{IO\_PCM\_SARADC\_OUT}$ = 1.8 V
LDO_TCXO	External TCXO	$V_{IO\_PCM\_SARADC\_TCXO\_IN}$ = 3.0 – 3.63 V	V_{TCXO_OUT} = 1.8 V
LDO_BKP	Always on logic domain	V_{BK_IN} = 1.71 – 3.63 V	0.92 V
LDO_RF	RF	V_{RF_IN} = 1.71 – 3.63 V	1.1 V

Figure 3. **LDO on-chip regulators dependencies**



Internal 1.8 V LDOs (LDO_IO and LDO_TCXO) can be switched off if an 1.8 V source is available from the external. In this case, the external 1.8 V source must be directly connected to the 1.8 V LDO outputs and to their inputs as well.

3.20.1 Power regions

STA8600 has two major power regions. The modules present inside each power region are listed below:

1. Always on backup region: 0.92 V (backup domain)
   a. prcc_backup
   b. RTC
   c. Backup RAM 32 bytes
2. Switchable region:
   a. Arm® core and other digital IPs: 0.95 V (core domain)
   b. RF: 1.1 V (RF domain)
   c. NVM/PCM: 1.8 V (PCM_SARADC domain)
   d. I/O ring1: 1.8 V or 3.3 V
   e. I/O ring2: 1.8 V or 3.3 V
   f. SARADC: 1.8 V (PCM_SARADC domain)

If the core power region is supplied by an external voltage regulator directly at pin $V_{DD\_EXT\_REG}$, the integrated LDO CORE must be switched off by forcing EXT_REG_SEL to V_{CORE_IN} at power up.

4 Electrical specifications

4.1 Introduction

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (controller characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (system requirement) is included in the “Symbol” column.

The electrical parameters shown in this document are classified by various methods. To give the customer a better understanding, the classifications listed in the table below are used and the parameters are tagged accordingly in the tables where appropriate.

Table 9. Parameter classifications

Classification tag	Tag description
P	Those parameters are tested in production on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

4.2 Absolute maximum ratings

Table 10. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{RF_IN}	SR	D	Supply voltages	—	-0.3	—	3.9	V
V_{CORE_IN}	SR	D	Supply voltages	—	-0.3	—	3.9	V
V_{BK_IN}	SR	D	Supply voltages	—	-0.3	—	3.9	V
V_{IO1_IN}	SR	D	Supply voltages	—	-0.3	—	3.9	V
V_{IO2_IN}	SR	D	Supply voltages	—	-0.3	—	3.9	V
$V_{IO\_SARADC\_PCM\_TCXO\_IN}$	SR	D	RF power supply	—	-0.3	—	3.9	V
V_{ADC_1V1}	SR	D	RF power supply	—	-0.3	—	1.15	V
V_{CH_1V1}	SR	D	RF power supply	—	-0.3	—	1.15	V
V_{RF_1V1}	SR	D	RF power supply	—	-0.3	—	1.15	V
V_{PLL_1V1}	SR	D	RF power supply	—	-0.3	—	1.15	V
TCXO_IN	SR	D	TCXO input	—	-0.3	—	1.15	V
RFA_IN	SR	D	RF input	—	—	—	8	dBm
V_{PCM}	SR	D	NVM power supply	—	-0.3	—	1.98	V
V_{SARADC_IN}	SR	D	SARADC supply voltage	—	-0.3	—	1.98	V
$V_{DD\_EXT\_REG}$ (1)	SR	D	Supply voltages	—	-0.3	—	1.15	V
T_S (2)	SR	D	Storage temperature	—	-55	—	150	°C
ESDHBM	SR	T	Electro static discharge — Human body model	—	—	—	±2	kV
ESDCDM	SR	T	Electro static discharge — Charge device model	—	—	—	±500	V
LU	SR	T	Latch up	—	-100	—	+100	mA

1. *EXT_REG_SEL = V_{CORE_IN}.*
2. *Normative reference JESD22A.*

4.3 Electrical characteristics

Table 11. Operating junction temperature range

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
T_J	SR	P	Junction temperature	—	-40	27	125	°C

Table 12. Backup PMU — Functional specifications

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
LDO_BK								
V_{BK_IN}	SR	P	Input voltage	External capacitance 1 µF.	1.71	3.3	3.63	V
V_{BK_OUT}	SR	P	Output voltage	Generated by dedicated on-chip LDO. No external supply allowed (backup domain).	0.84	0.92	0.95	V

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
$I_{BK\_OUT\_LOAD}$	SR	P	Load current at normal mode	—	—	—	2	mA
C_{BK_OUT}	SR	D	External capacitance	—	0.5	1	1.2	µF
$C_{BK\_OUT\_EMC}$	SR	D	EMC external capacitance	Ceramic capacitor ESR 5 - 100 mΩ	50	100	135	nF
$T_{BK\_OUT\_STARTUP}$	SR	D	Start-up time	—	—	—	1	ms
$V_{BK\_IN\_SLEW}$	SR	D	Slew rate	A 10 Ω serial resistance is recommended on V_{BK_IN} line	0.04	—	40	ms

Table 13. Main PMU — Functional specifications

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
LDO_CORE								
V_{CORE_IN}	SR	D	Input voltage	External capacitance = 4.7 µF, if internal core LDO is used	1.71	3.3	3.63	V
V_{CORE_OUT}	SR	D	Output voltage available at balls ($V_{DD\_EXT\_REG}$)	EXT_REG_SEL = GND ($V_{DD\_EXT\_REG}$)	0.90	0.95	1.0	V
I_{VCORE_OUT}	SR	P	Load current	—	—	—	450	mA
V_{CORE_OUT}	SR	D	External capacitance	EXT_REG_SEL = GND ($V_{DD\_EXT\_REG}$)	2.35	4.7	6.35	µF
$C_{LDO\_CORE\_EMC}$	SR	D	External EMC capacitance	Ceramic/on each pin	50	100	135	nF
$T_{LDO\_CORE\_START}$	SR	D	Start-up time	—	—	—	300	µs
LDO IO/PCM/SARADC/TCXO (3.3 V to 1.8 V internal LDO)								
$V_{IO\_PCM\_SARADC\_TCXO\_IN}$	SR	P	Input voltage	External capacitance 2.2 µF	3	3.3	3.63	V
$V_{IO\_PCM\_SARADC\_OUT}$	SR	P	Output voltage	PCM_SARADC domain	1.7	1.80	1.83	V
I_{LDO_IO}	SR	P	Load current	—	—	—	150	mA
C_{LDO_IO}	SR	D	External capacitance	—	1.1	2.2	3	µF
$T_{LDO\_IO\_START}$	SR	D	Start-up time	—	—	—	100	µs
LDO TCXO								
V_{TCXO_OUT}	SR	P	Output voltage	TCXO domain	1.7	1.8	1.83	V
I_{LDO_TCXO}	SR	P	Load current	—	—	—	5	mA
C_{LDO_TCXO}	SR	D	External capacitance	—	0.5	1	1.35	µF
LDO_TCXO_ESR	SR	D	ESR	—	5	—	100	mΩ
$T_{LDO\_TCXO\_START}$	SR	D	Start-up time	Assuming V_{core_out} and V_{bk_out} are already present	—	—	100	µs
LDO_RF								
V_{RF_IN}	SR	P	Input voltage	—	1.71	3.3	3.63	V
V_{RF_OUT}	SR	P	Output voltage	RF domain	1.03	1.1	1.12	V
C_{LDO_RF}	SR	D	External capacitance	—	1.1	2.2	3.00	µF
$C_{LDO\_RF\_EMC}$	SR	D	External EMC capacitance(1)	—	50	100	135	nF
I_{LDO_RF}	SR	P	Load current	—	—	—	70	mA
$T_{LDO\_RF\_START}$	SR	D	Start-up time	—	—	—	300	µs

1. *On RF supply input pins.*

Table 14. External core power supply

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
$V_{DD\_EXT\_REG}$	SR	P	External core power supply	EXT_SEL_REG = V_{CORE_IN}	0.90	0.95	1.0	V

Table 15. I/O Ring1/2 power supply

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
V_{18_IO}	SR	D	I/O Ring1/2 power supply input voltage - VIO1_IN/VIO2_IN input range	1.8 V interface	1.62	1.8	1.98	V
V_{33_IO}	SR	D	I/O Ring1/2 power supply input voltage - VIO1_IN/VIO2_IN input range	3.3 V interface	3	3.3	3.63	V

Table 16. Current consumption

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ(1)	Max(2)	
I_{CC_BK}	SR	T	Current consumption at V_{BK_IN} in functional mode	V_{BK_IN} = 3.3 V	—	0.2	2	mA
$I_{CC\_BK\_HW\_STANDBY}$	SR	T	Current consumption at V_{BK_IN} in HW standby mode	V_{BK_IN} = 3.3 V STANDBY_IN = LOW	—	20(3)	—	µA
$I_{CC\_VRF\_IN}$	SR	T	Current consumption at V_{RF_IN}	Quad-band scenario V_{RF_IN} = 3.3 V	—	55	75	mA
				Dual-band scenario V_{RF_IN} = 3.3 V	—	42	62	
$I_{CC\_CORE\_105}$	SR	T	Current consumption at $V_{DD\_EXT\_REG}$ with ST quad-band reference application FW in acquisition mode	V_{CORE_IN} = 3.3 V EXT_REG_SEL = V_{CORE_IN} $V_{DD\_EXT\_REG}$ = 1 V (the maximum value is specified at 105°C ambient, Tj = 125°C)	—	185	300	mA
$I_{CC\_CORE\_85}$	SR	T		V_{CORE_IN} = 3.3 V EXT_REG_SEL = V_{CORE_IN} $V_{DD\_EXT\_REG}$ = 1 V (the maximum value is specified at 85°C ambient)	—	—	270	mA

1. *Typical values are measured in application conditions at an ambient temperature of 25°C under standard process and voltage conditions.*
2. *Maximum values are measured in application conditions at an ambient temperature of 105°C under worst-case process and voltage conditions, unless otherwise specified.*
3. *The internal pull-up resistor is disabled (otherwise, the typical value is 70 µA).*

Table 17. RF Electrical characteristics

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
RFA – mixer – IF filter – VGA								
Gp_{RFA}	SR	P	RFA voltage gain	RFA 00 (max)	19	20	—	dB
	SR	P		RFA 11 (min)	—	2	3	dB

Symbol	C		Parameter	Condition	Value			Unit
					Min	Typ	Max	
GC	SR	P	Conversion gain (from RFA in to ADC input)	VGA & RFA at max gain	—	80	90	dB
	SR	P		VGA & RFA at min gain	20	40	—	
Δ_{VGA}	SR	P	VGA dynamic range	—	45	50	—	dB
P_{1DB}	SR	P	RF-IF-VGA input compression point	In band RFA max VGA max	-95	-90	—	dBm
	SR	P		In band RFA max VGA min	-60	-50	—	
ImgRej	SR	P	Image rejection	all channels	15	25	—	dB
NF_{RF-IF}	SR	P	RF-IF-VGA noise figure	VGA at min & RFA at max gain in L1-L2-L5 band	—	5	11	dB
Fractional synthesizer – VCO								
TCXO_IN	SR	T	TCXO frequency	—	—	26	—	MHz
TCXO_IN_lev	SR	D	TCXO_IN pin input level	peak to peak voltage	0.8	—	1.1	V

Table 18. Electrical characteristics of digital input and output buffers

Symbol		C		Parameter	Condition	Value			Unit
						Min	Typ	Max	
Input and output buffers									
V_{IH_1V8}	SR	P		CMOS input high level	—	0.65 × V_{18_IO}	—	0.3 + V_{18_IO}	V
V_{IL_1V8}	SR	P		CMOS input low level	—	- 0.3	—	0.35 × V_{18_IO}	V
V_{IH_3V3}	SR	P		CMOS input high level	—	2.0	—	0.3 + V_{33_IO}	V
V_{IL_3V3}	SR	P		CMOS input low level	—	- 0.3	—	0.8	V
V_{HYST}	SR	P		Input hysteresis	—	150	—	—	mV
RPU/RPD	SR	P		Pull-up/down	—	—	50	—	kΩ
C_{IN}	SR	D		CMOS input capacitance	—	—	—	3	pF
V_{OH}	SR	P		CMOS output high level (where V_{IO} can be 1.8 V or 3.3 V)	At max I_{OH}	V_{IO} - 0.4	—	—	V
V_{OL}	SR	P		CMOS output low level (valid for both 1.8 and 3.3 V IO)	At max I_{OL}	—	—	0.4	V
I_{OL}/I_{OH} IO ring1 and ring2	SR	P		Driving current to sustain V_{OL}/V_{OH} (LOWEMI disabled)	V_{OL}/V_{OH}	0	—	4	mA
I_{OL}/I_{OH} IO ring1 and ring2	SR	P		Driving current to sustain V_{OL}/V_{OH} (LOWEMI enabled)	V_{OL}/V_{OH}	0	—	2	mA
I_{OL}/I_{OH} IO ring0 (STANDBY_OUT)	SR	P		Driving current to sustain V_{OL}/V_{OH} at STANDBY_OUT	V_{OL}/V_{OH}	0	—	2	mA
t_{RISE}	SR	T		CMOS output rise time with C_L = 15 pF, from 10 to 90 %; 3.3 V	2 mA max current drive	—	3	—	ns
	SR	T			4 mA max current drive	—	2	—	

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
t_{FALL}	SR	T	CMOS output fall time with C_L = 15 pF, from 10 to 90 %; 3.3 V	2 mA max current drive	—	3	—	ns
	SR	T		4 mA max current drive	—	2	—	

4.4 RTC 32.768 kHz oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF (using crystal with recommended characteristics as per Table 19. Crystal recommended specifications) as shown in the Figure 4. 32.768 kHz crystal connection.

The recommended oscillator specifications are shown in the table below:

Table 19. Crystal recommended specifications

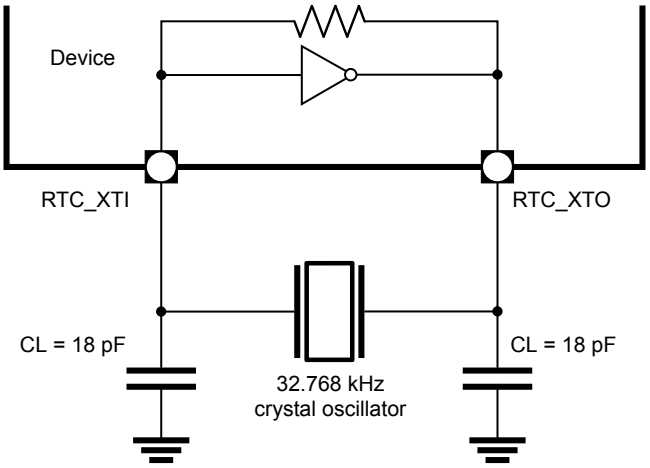
Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
F_{SXTAL}	SR	D	Crystal frequency	—	—	32.768	—	kHz
LM_{SXTAL}	SR	D	Motion inductance	—	3.5	5	6.5	H
CM_{SXTAL}	SR	D	Motional capacitance	—	4.0	5.0	6.0	fF
CO_{SXTAL}	SR	D	Shunt capacitance	—	1.0	1.3	1.6	pF
ESR	SR	D	Resonance resistance	—	—	—	120	kΩ
C_L	SR	D	External load capacitance	—	—	18 ±2 %	—	pF

The oscillator amplifier specifications are shown in the following table:

Table 20. Oscillator amplifier specifications

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
t_S	SR	D	Startup time	—	—	0.4	1.0	s
DL	SR	D	Drive level	—	—	—	< 0.1	µW
RLC	SR	D	Required load capacitance	—	—	12.5	—	pF
GO	SR	D	Startup conductance	—	22.5	33.6	60	µA/V

Figure 4. **32.768 kHz crystal connection**



4.5 Power up timing sequence

Figure 5. **Power up timing diagram**

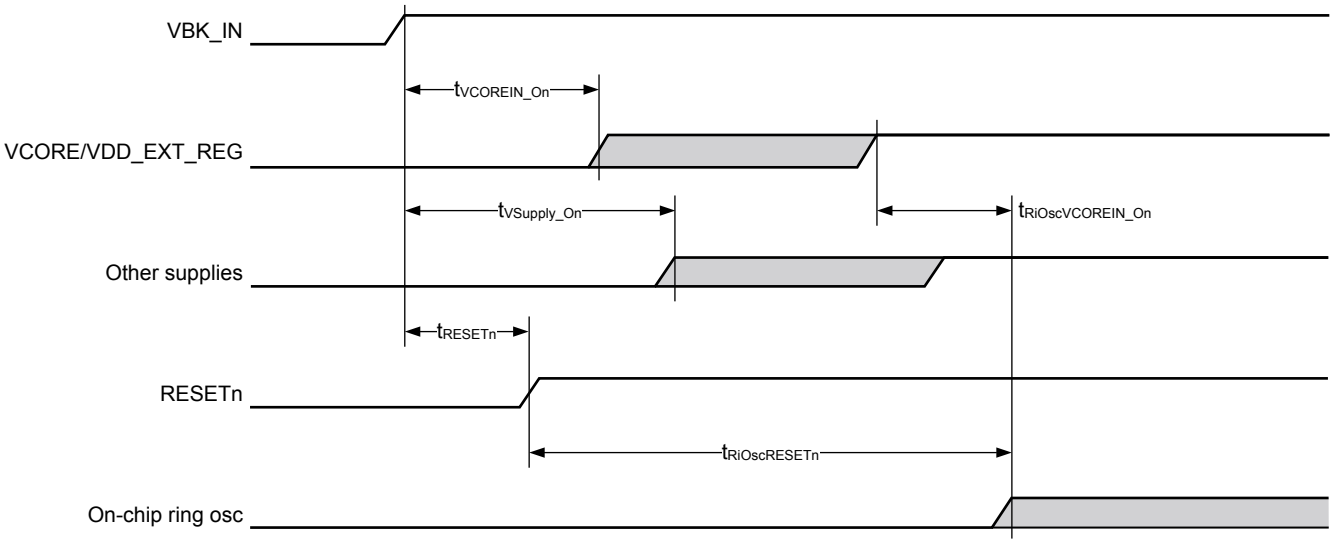


Table 21. **Power up timing data**

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
$t_{VCORE\_IN\_On}$	SR	T	Simultaneous power on of V_{BK_IN} and V_{CORE_IN}/$V_{DD\_EXT\_REG}$	V_{BK_IN} > 1.71 V	0	—	—	ms
$t_{VSupply\_On}$	SR	T	Simultaneous power on of V_{BK_IN} and other supplies are allowed	V_{BK_IN} > 1.71 V	0	—	—	ms
t_{RESETn}	SR	D	—	V_{BK_IN} > 1.71 V	4	—	—	ms
$t_{RiOscRESETn}$	SR	D	—	V_{CORE_IN} > 1.71 V or $V_{DD\_EXT\_REG}$ > 0.90 V	0.5	—	—	ms
$t_{RiOscVCOREIN\_On}$	SR	D	—	RESETn = high	0.5	—	—	ms

4.6 Nonvolatile memory

The following tables show the wait state configuration.

Table 22. Wait state configuration for core

RWSC[1]	C	Core frequency (MHz)
4	P	314
3	T	261
2	T	196 157
1	T	130

1. *There must be no access to an NVM module when the RWSC configuration is being updated.*

Table 23. NVM memory write specifications

Symbol	Characteristics[1]	Value								Unit
		Typ[2]	C	Initial max			Typical end of life[6]	Lifetime max[3]	C	
				25 °C[4]	All temperatures[5]	C		< 250 kwrite cycles		
t_{qwprog}	Quad word (128 bits) write time	90	C	144	225	C	99	168	C	µs
t_{pprog}	Page (256 bits) write time	134	C	220	375	C	147	267	C	µs
t_{qpprog}	Quad page (1024 bits) program time	450	C	878	1500	P	500	1000	C	µs
$t_{16kprogram}$	16 KB block write time	45	C	59	105	P	—	—	C	ms
$t_{32kprogram}$	32 KB block write time	90	C	117	210	P	—	—	C	ms
$t_{64kprogram}$	64 KB block write time	180	C	234	425	P	—	—	C	ms
$t_{128kprogram}$	128 KB block write time	360	C	468	850	P	—	—	C	ms

1. *Actual hardware writing times. This does not include software overhead.*
2. *Typical write times assume nominal supply values and operation at 25 °C.*
3. *Maximum lifetime write times apply across the voltages and temperatures, and occur after the specified number of write cycles. These maximum values are characterized but not tested or specified.*
4. *Initial factory condition: < 100 write cycles, –40 °C < T_J < 125 °C junction temperature, and nominal (±5%) supply voltages. These values are verified at production testing.*
5. *Initial maximum "All temperatures" write times provide guidance for timeout limits used in the factory, and apply to less than or equal to 100 write cycles, –40 °C < T_J < 125 °C junction temperature, and nominal (±5%) supply voltages. These values are verified at production testing.*
6. *Typical end-of-life write times represent the median performance and assume nominal supply values. Typical end-of-life write values can be used for throughput calculations. These values are characteristic, but not tested.*

All the NVM operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low-frequency system clock is used.

Note: There is no corruption of data when a reset or power-down is triggered while a programming operation is ongoing.

Table 24. NVM life specification

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
N_{DERK}	KB data memory endurance	250	C	—	—	Kwrite

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
t_{DR1K}	Minimum data retention blocks with 0 - 1 500 write cycles	20	C	—	—	Years
t_{DR10K}	Minimum data retention blocks with 1 501 - 1 000 write cycles	15	C	—	—	Years
t_{DR100K}	Minimum data retention blocks with 1 001 - 100 000 write cycles	10	C	—	—	Years
t_{DR250K}	Minimum data retention blocks with 100 001 - 250 000 write cycles	5	C	—	—	Years

1. *Write operations supported across specified temperature ranges. NVM life specification data are valid only if the NVM is written after the soldering process. A reflow process after NVM writing can cause NVM data corruption.*

4.7 Digital interface AC timing characteristics (specified by design)

Figure 6. Clock block diagram

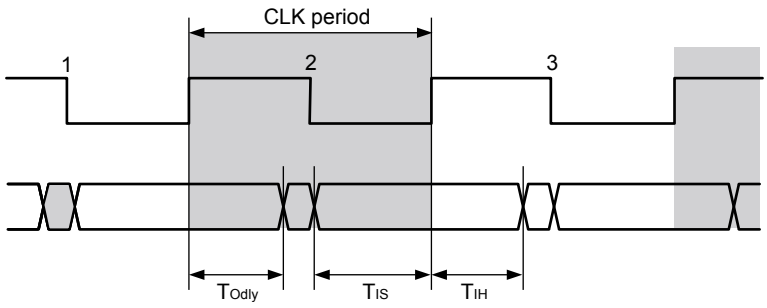


Table 25. Clock data

Symbol	Comment
CLK period	Clock time period
t_{Odly}	Output data delay from rising clock edge, unless differently specified
t_{IS}	Input data setup time to rising clock edge, unless differently specified
t_{IH}	Input data hold time from rising clock edge, unless differently specified

4.7.1 SPIQ

Table 26. SPIQ (controller mode)

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
CLK frequency	SR	T	Clock	C_{load} = 25 pF	—	—	19.625	MHz
CLK period	SR	T			50.95	—	—	ns
CLK duty cycle	SR	D			40	—	60	%
t_{IS}	SR	D	Input	—	10	—	—	ns
t_{IH}	SR	D		—	2	—	—	ns
t_{Odly}	SR	D	Output	C_{load} = 25 pF	2	—	10	ns

Table 27. **SPIQ (target mode)**

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
CLK frequency	SR	T	Clock	C_{load} = 25 pF	—	—	8	MHz
CLK period	SR	T			125	—	—	ns
CLK duty cycle	SR	D			40	—	60	%
t_{IS}	SR	D	Input	—	10	—	—	ns
t_{IH}	SR	D		—	2	—	—	ns
t_{Odly}	SR	D	Output	C_{load} = 25 pF	2	—	10	ns

4.7.2 SSP

Table 28. **SSP (controller mode)**

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
CLK frequency	SR	T	Clock	C_{load} = 25 pF	—	—	19.625	MHz
CLK period	SR	T			50.95	—	—	ns
CLK duty cycle	SR	D			40	—	60	%
t_{IS}	SR	D	Input	—	18	—	—	ns
t_{IH}	SR	D		—	2	—	—	ns
t_{Odly}	SR	D	Output	C_{load} = 25 pF	2	—	10	ns

Table 29. **SSP (target mode)**

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
CLK frequency	SR	T	Clock	C_{load} = 25 pF	—	—	8	MHz
CLK period	SR	T			125	—	—	ns
CLK duty cycle	SR	D			40	—	60	%
t_{IS}	SR	D	Input	—	10	—	—	ns
t_{IH}	SR	D		—	4	—	—	ns
t_{Odly}	SR	D	Output	C_{load} = 25 pF	0	—	14.5	ns

4.7.3 I2C

Table 30. **I2C**

Symbol		C	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
SCL CLK frequency f_{SCL}	SR	T	0	100	0	400	0	1000	kHz
Hold time (repeated) START condition $t_{HD,STA}$	SR	D	4.0	—	0.6	—	0.26	—	µs
LOW period of the SCL clock t_{LOW}	SR	D	4.7	—	1.3	—	0.5	—	µs
HIGH period of the SCL clock t_{HIGH}	SR	D	4.0	—	0.6	—	0.26	—	µs

Symbol		C	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
Setup time for a repeated START condition $t_{SU,STA}$	SR	D	4.7	—	0.6	—	0.26	—	µs
Data hold time for I2C bus devices $t_{HD,DAT}$	SR	D	0	3.45	0	0.9	0	0.45	µs
Data setup time $t_{SU,DAT}$	SR	D	250	—	100	—	50	—	ns
Rise time of both SDA and SCL signals t_R	SR	D	—	1000	—	300	—	120	ns
Fall time of both SDA and SCL signals t_F	SR	D	—	300	—	300	—	120	ns
Setup time for stop conditions $t_{SU,STO}$	SR	D	4.0	—	0.6	—	0.26	—	µs
Bus free time between STOP and START condition t_{BUF}	SR	D	4.7	—	1.3	—	0.5	—	µs
Capacitive load for each bus line C_b	SR	D	—	400	—	400	—	550	pF

4.7.4 UART

Table 31. **UART**

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
Baud rate	SR	T	—	—	—	—	3	Mbaud

5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 VFQFPN56 package information

Figure 7. VFQFPN56 package outline

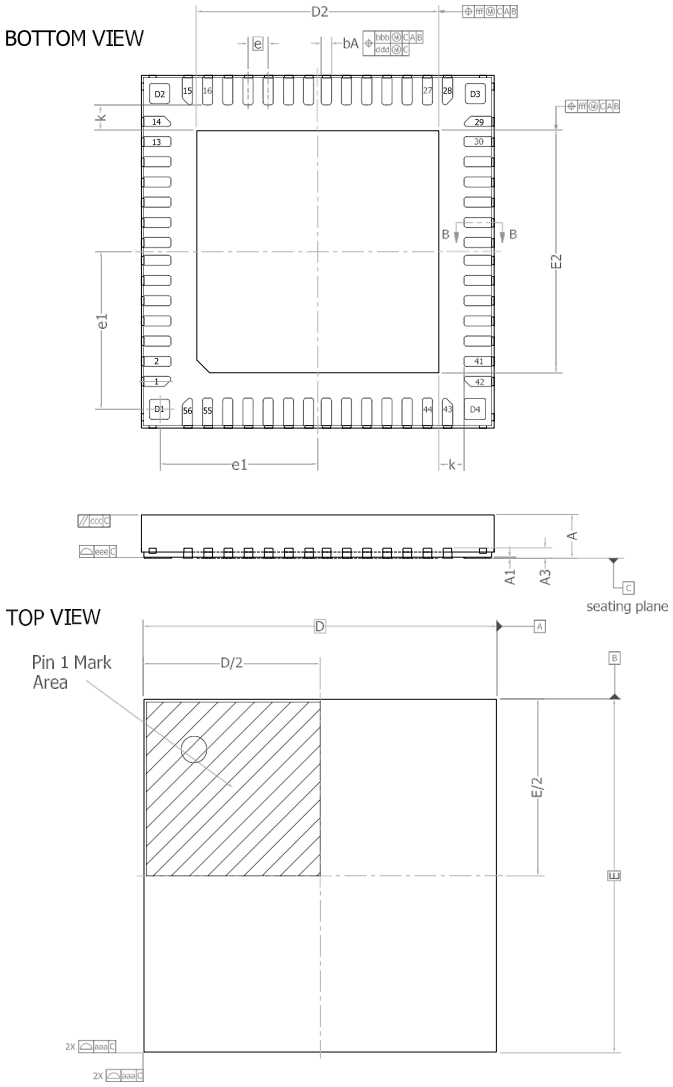


Figure 8. **VFQFPN56 package outline additional information**

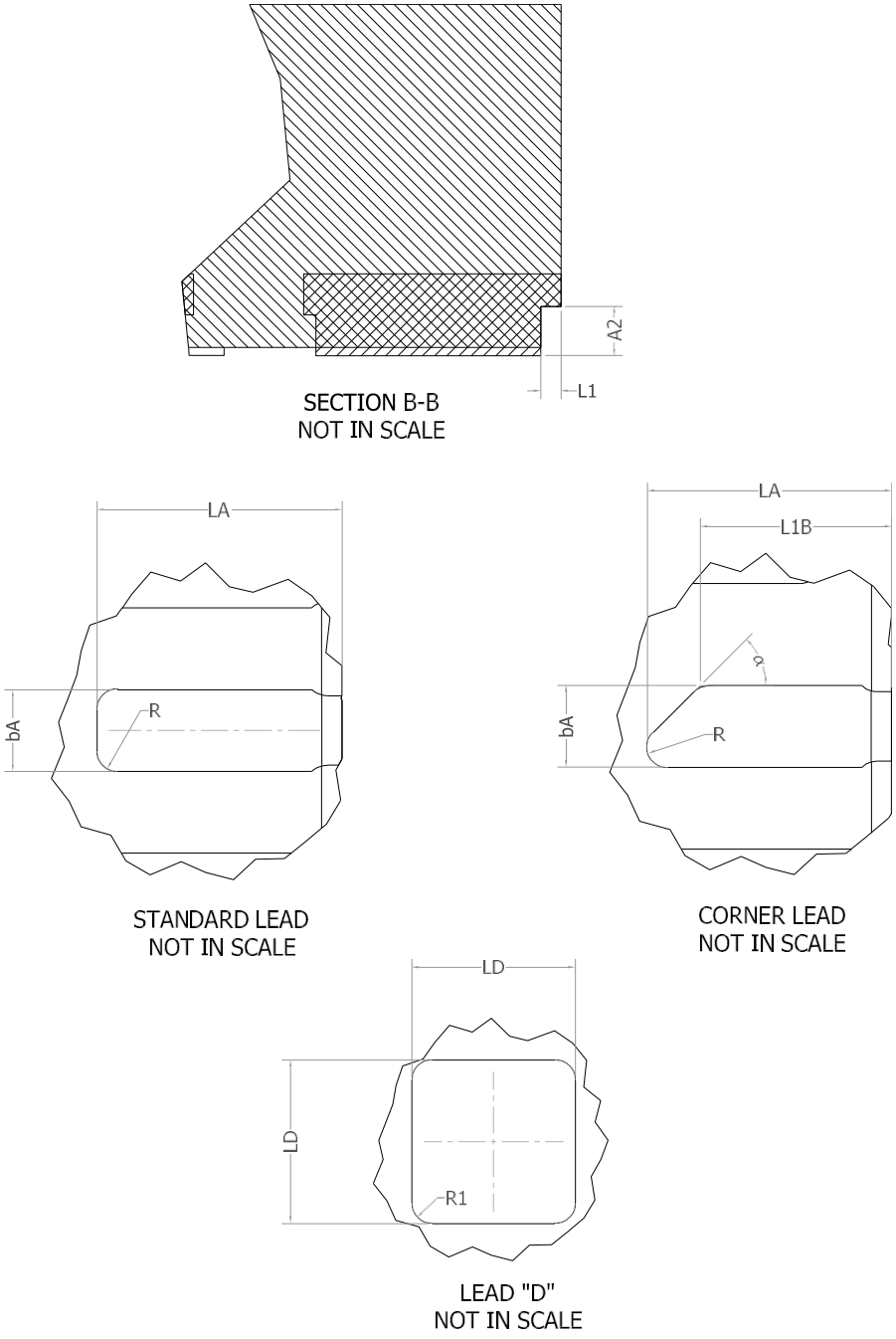


Table 32. **VFQFPN56 package mechanical data**

Symbol	Min	Typ	Max	Note
Common dimensions				
A	0.80	0.90	1.00	—
A1	0	—	0.05	—
A2	0.1	—	—	—
A3		0.20 REF		—
D		7.00 BSC		4
D2	5.15	5.20	5.25	8
E		7.00 BSC		4
E2	5.15	5.20	5.25	8
e		0.40 BSC		—
e1		3.125 REF		—
k	0.20	—	—	—
L1		0.05 REF		12
LA	0.50	0.55	0.60	13
bA	0.17	0.20	0.23	13
L1B	0.42	0.47	0.52	13
LD	0.35	0.40	0.45	—
α		45° REF		—
N		56+4		6
R		0.1 REF		—
R1		0.075 REF		—
Tolerance of form and position				
aaa		0.10		1, 2, 14
bbb		0.07		
ccc		0.10		
ddd		0.05		
eee		0.08		
fff		0.10		

Note:

1. *Dimensioning and tolerancing schemes are conform to ASME Y14.5M-1994.*
2. *All dimensions are in millimeters.*
3. *Terminal A1 identifier and terminal numbering convention must conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator can be a molded or metalized feature. The optional indicator on bottom surface can be a molded, marked or metallized feature.*
4. *Outlines with "D" and "E" that increment less than 0.5 mm must be registered as "stand alone" outlines. These outlines must use as many of the algorithms and dimensions states in the design standard as possible to ensure predictability in manufacturing.*
5. *The inner edge of corner terminals can be chamfered or rounded to achieve the minimum gap "k". This feature must not affect the terminal width "b", which is measured L/2 from the edge of the package body.*
6. *"N" is the maximum number of terminal positions for the specified body size. Depopulation is allowed, but only under the following conditions:*
   - *Depopulation scheme must be consistent in each quadrant of the package.*
   - *Non-symmetric variations must be broken out as separate mechanical outline variations, including depopulation graphics.*
7. *A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).*
8. *Dimension D2 and E2 refer to the exposed pad. PAD optional dimensions are 4.65 mm by 4.65 mm.*
9. *The extra corner leads, identified as D1, D2, D3, and D4 in Figure 7. VFQFPN56 package outline, are internally connected to the IC ground exposed pad.*
10. *The IC ground exposed pad must be connected to the PCB ground.*
11. *The Dx corner leads can be connected to the PCB ground or left floating. If left floating, care must be taken to prevent short-circuits with traces or through running beneath the leads.*
12. *Critical dimension: L1.*
13. *Dimensions "b" and "L" are measured at terminal plating surface.*
14. *For Symbols, recommended values and tolerances, refer to the table below (according to package or JEDEC specification if registered).*

Table 33. Tolerance of form and position definitions

Symbol	Definition
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.
bbb	The tolerance that controls the position of the entire terminal pattern with respect to Datum's A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to Datum's A and B.
ccc	The tolerance located in parallel to the seating plane in which the top surface of the package must be located.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e". This tolerance is normally compounded with the tolerance zone defined by bbb.
eee	The unilateral tolerance located above the seating plane where the bottom surface of all terminals must be located. This tolerance is commonly known as the "coplanarity" of the package terminals.
fff	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone is the datum defined by the centerlines of the package body.

5.2 Package thermal characteristics

This section describes the thermal characteristics of the device.

5.2.1 VFQFPN56 thermal characteristics

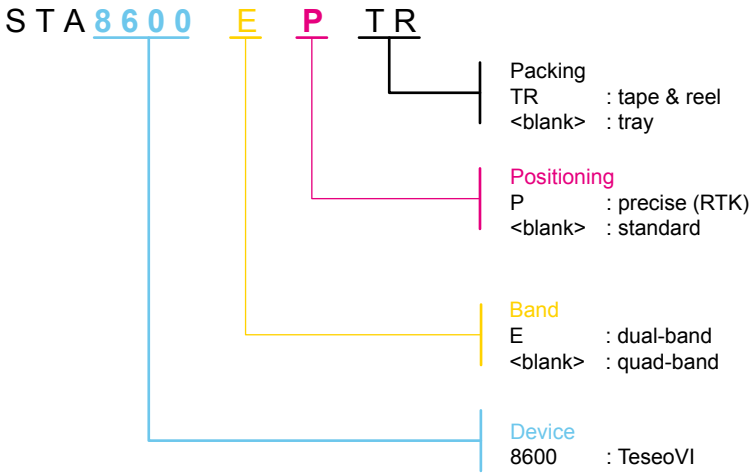
Table 34. VFQFPN56 thermal characteristics

Symbol	Parameter	Value	Unit
T_{AMB}	Ambient operating temperature	-40 to 105	°C
Θ_{JA} (1)	Thermal resistance junction-ambient	24	°C/W
Ψ_{JC} (2)	Thermal characterization parameter junction-case top	0.2	°C/W

1. *Multilayer 2s2p as per JEDEC JESD51-2*
2. *JESD51-8*

6 Ordering information

Figure 9. Ordering information scheme



Not all combinations are allowed. For a complete list of supported order codes, refer to Product summary.

7 Soldering profile

Reflow soldering profile according to IPC/JEDEC J-STD-020.

Revision history

Table 35. **Document revision history**

Date	Version	Changes
31-Jul-2026	1	Initial release.

Contents

Glossary

ADC Analog-to-digital converter

BeiDou Chinese navigation satellite-based radio navigation system

CBC Cipher block chaining

CDM Charged device model

DMA Direct memory access

DRAW Dead reckoning automotive way

DRUM Dead reckoning unplugged mode

ESD Electrostatic discharge

Galileo EU´s global navigation satellite system

GLONASS Russian satellite navigation system. Acronym for GLObalnaya NAvigatsionnaya Sputnikovaya Sistema (Russian). The role of the GLONASS satellite navigation system is similar to the GPS of the United States, the Galileo satellite positioning system of Europe, and the BeiDou satellite navigation system of China.

GNSS Global navigation satellite system

GPIO General-purpose input/output

GPS Global positioning system

HBM Human body model

HSM Hardware security module

I^2C Inter-integrated circuit

IRNSS Indian regional navigation satellite system, with the operational name of Navigation with Indian constellation (NAVIC).

ISO International organization for standardization

JTAG Joint test action group

LDO Low-dropout regulator

LEO Low earth orbit

LVDS Low-voltage differential signaling

MIPS Million instructions per second

NAVIC Navigation with Indian constellation. The Indian regional navigation satellite system (IRNSS) is an autonomous regional satellite navigation system that provides accurate real-time positioning and timing services.

NVM Nonvolatile memory - a memory that retains its contents even when powered down, such as flash memory, PCM, OTP memory, or EEPROM

OSNMA Open service navigation message authentication

PCB Printed-circuit board

PPP Precise point positioning

PPS Pulse per second

PVT Position-velocity-time

QFN Quad-flat no-leads

QZSS Quasi-zenith satellite system.

A Japanese satellite positioning system composed mainly of satellites in quasi-zenith orbits (QZO), but also of satellites in geostationary orbits (GEO).

RAM Random access memory

RTK Real-time kinematic

SBAS Satellite-based augmentation system. It provides services for improving the accuracy, integrity, and availability of basic GNSS signals.

SPI Serial peripheral interface

SPIQ Queued serial peripheral interface

SSP Synchronous serial port

ST STMicroelectronics

UART Universal asynchronous receiver/transmitter