STA8100GA

Datasheet

Teseo V family automotive multiband multiconstellation GNSS precise engine receiver

LFBGA81 8 × 8 × 1.7 mm, 0.8 mm ball pitch

Product status link
STA8100GA

Product summary		
Order code	**Packing**	**Description**
STA8100GA	Tray	GNSS only
STA8100GAD		GNSS + TESEO-DRAW/ DRUM
STA8100GATR	Tape and reel	GNSS only
STA8100GADTR		GNSS + TESEO-DRAW/ DRUM

Features

- AEC-Q100 qualified
- TESEO-DRAW (dead reckoning automotive way) is supported on STA8100GAD only
- Code phase, carrier phase, and doppler frequency measurement
- Antenna sensing
- Notch filter for antijamming
- ESD: 2 kV (HBM) and 500 V (CDM)
- Automotive grade: 105 °C
- 81-ball, 8 × 8 × 1.7 mm, 0.8 mm pitch, LFBGA package

Core

- Arm® Cortex®-M7 core:
  - Maximum clock frequency 314 MHz
  - 16 KB instruction cache and 16 KB data cache
  - 64 KB instruction TCM and 384 KB data TCM core clock speed
  - Nested vector interrupt controller
  - JTAG debugging capability
  - 256 Kbyte system RAM

Memory interfaces

- SFC (octal/quad serial flash memory controller, SDR)
- SD multimedia card

GNSS features

- STMicroelectronics's 5th generation positioning receiver with 80 tracking channels and 4 fast acquisition channels compatible with 6 constellations: GPS, Galileo, GLONASS, BeiDou, QZSS, and NAVIC (former IRNSS)
- Dual band L1 and L5 single chip solution
- Triple band capability with external RF STA5635A
- L-band raw correction data reception
- SBAS systems: WAAS, EGNOS, MSAS, GAGAN, and BeiDou

Communication interfaces

- PPS output
- 3 × UART
- Synchronous serial port (SPI supported)
- I²C
- 2 × multimode serial interfaces
- 2 × CAN controllers
- USB 2.0 full speed (12 Mbit/s) with integrated physical layer transceiver

Core peripherals

- 32-channel DMA
- 32 kHz oscillator real-time clock
- 2 × multitimer units
- Watchdog timer
- 1 × extended function timers

Power management unit

- Separate power-supply domains and on-chip LDO and high-voltage/low-voltage monitors:
  - Backup voltage domain: 1.62 V to 3.6 V with LDO for the always-on core supply and high-voltage/low-voltage detectors, and a dedicated IO-ring0
  - Main voltage domain:
    1.62 V to 3.6 V with LDO for the switchable logic domain and high-voltage/low-voltage detectors for operation at 85 °C maximum ambient temperature
    1.2 V ± 5% external voltage supply for operation at 105 °C maximum ambient temperature
  - Separate RF domain with dedicated LDO
  - IO-ring1 1.8 or 3.3 V capable, with a dedicated 1.8 V LDO
  - IO-ring2 3.3 V ±10 % capable
  - Fail-safe GPIOs available

Description

The STA8100GA is part of the TeseoV family. The STA8100GA is a multiband multiconstellation positioning receiver IC able to manage all the GNSS constellations such as GPS, Galileo, Glonass, BeiDou, NAVIC (former IRNSS), and QZSS in the L1, L2, L5, and E6 frequency bands. The STA8100GA supports L2 and E6 baseband signal processing. The RF reception of the L2 and E6 signals requires an external front-end IC (STA5635A). The STA8100GAD comes with STMicroelectronics's dead reckoning firmware called TESEO-DRAW.

1 Introduction

1.1 Document overview

The STA8100GA device can receive GPS, Galileo, and Beidou on the L1 and L5 bands simultaneously without the need for an external RF front-end.

A dedicated interface allows the reception of GNSS data from the STA5635A external RF front-end to manage the other GNSS bands (L2, L5, and E6) simultaneously with the L1 band signals. This interface also allows a triple frequency mode: L1/L2/L5 or L1/L5/E6. The STA8100GA device can also be used to receive the correction service data from the L-band satellites.

The device provides the precise raw measurements of all the visible GNSS satellites on the serial interface to allow the host to run the precise position algorithm. The STA8100GA also provides an autonomous precision positioning calculation to the main host using all the satellite constellations.

The STA8100GA device is compliant with the ST automotive-grade qualification, which, in addition to the AEC-Q100 requirements, includes a set of production flow methodologies that target zero defect per million. It fulfills the high-quality and service-level requirements of the automotive market. It is the ideal solution for in-dash navigation, smart antenna, car to car, V2X, OEM telematics, marine, drone, lawnmower, and many other applications that require precise position calculation.

The STA8100GA embeds separated LDOs to supply the analog parts, the digital core, and the IO-ring of the device facilitating requirements for the external power supply.

The chip is manufactured in CMOS technology and housed in an 81-ball LFBGA package with 8 × 8 × 1.7 mm body size and 0.8 mm ball pitch.

Note: For information on the STA8100GA core, refer to the Arm® Cortex®-M7 technical reference manual, available from the www.arm.com website.

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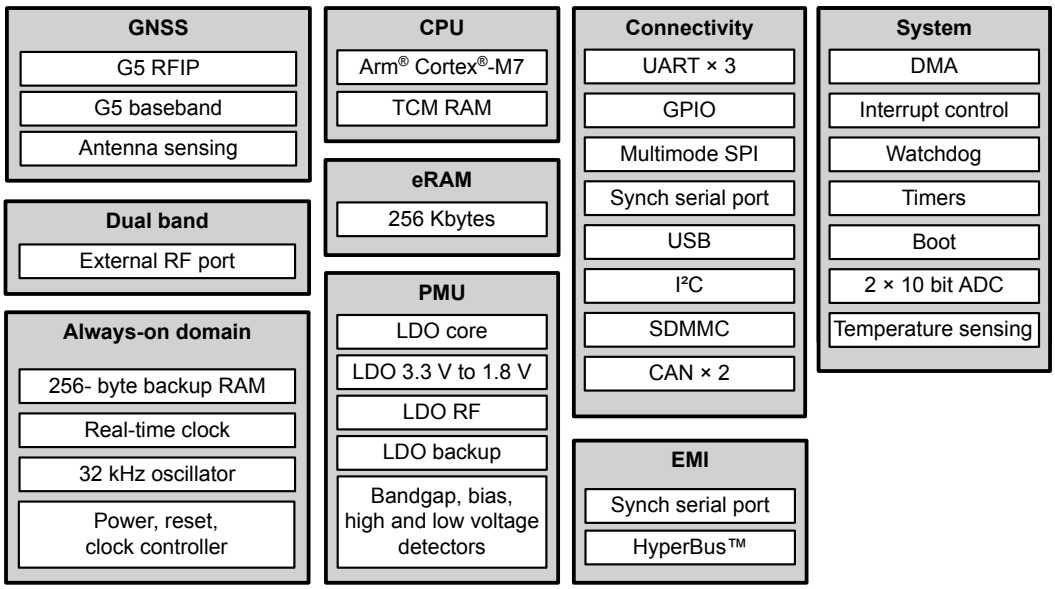
1.2 Block diagram

Figure 1. Block diagram



2 Pin description

2.1 Ball list

Figure 2. **STA8100GA ballout**

	1	2	3	4	5	6	7	8	9
A	GND	SFC_CSN	VIO1_EXT	QMAG1	QSIG2	GPIO6	GPIO5	EXT_REG_SEL	GND
B	SFC_CLK	GPIO27	SFC_SIO2	IMAG1	IMAG2	VDD_EXT_REG	VDD_EXT_REG	VDD_EXT_REG	UART2_RX
C	VIO1_EXT	GPIO28	SFC_SIO3	SFC_SIO1	QMAG2	ISIG1	TEST	UART2_TX	GND_PMU
D	RTC_XTI	GPIO29	GPIO26	SFC_SIO0	ISIG2	QSIG1	VCORE_IN	VIO2_IN	STANDBY_OUT
E	RTC_XTO	RESETn	WAKEUP	GND_BKP_PMU	GND	GND	JTAG-TMS	JTAG-TDI	JTAG-TDO
F	TCXO_IN	VBK_OUT	VBK_IN	STANDBY_IN	GND	GND	V2V5_OUT	JTAG-TRSTn	JTAG-TCK
G	VCC_PLL	GND_RF	GND_RF	GND_RF	GND_RF	VDD_EXT_REG	MSP1_Dout	GPIO67	GND_TSENS
H	LNA_IN	GND_RF	GND_RF	ANTSens1/AIN0	ANTSens2/AIN1	VIO2_IN	VIO2_IN	PPS_OUT	MSP1_CS
J	VCC_LNA	NA_OUT	RFA_IN	VRF_OUT	VRF_IN	UART1_TX	UART1_RX	MSP1_clk_out	MSP1_Din

Note: Most balls have alternate functions, which are selectable through the relevant registers.

Table 1. **Power-supply pins**

Symbol	I/O voltage(1)	I/O	Description	Ball
V_{RF_IN}	1.62 V to 3.6 V	PWR	LDO RF power input - IO-ring RF	J5
V_{RF_OUT}	1.15 V	PWR	LDO RF power output	J4
V_{CC_LNA}	1.2 V	PWR	LNA power input	J1
V_{CC_PLL}	1.2 V	PWR	RF VCC power input	G1
V_{BK_IN}(2)	1.62 V to 3.6 V	PWR	LDO backup power input - IO-ring0	F3
V_{BK_OUT}	1.2 V	PWR	LDO backup power output	F2
V_{CORE_IN}	1.62 V to 3.6 V	PWR	LDO core power input	D7
$V_{DD\_EXT\_REG}$	1.2 V	PWR	LDO core power output	B6, B7, B8, G6
V_{IO2_IN}	3 V to 3.6 V	PWR	IO-ring2 power input	D8, H6, H7
V_{IO1_EXT}	1.72 V or 3.6 V	PWR	IO-ring1 power input or 1.8 V IO-ring1 LDO output	A3, C1
V_{2V5_OUT}	2.5 V	PWR	LDO core 2.5 V output	F7
GND_PMU	GND	GND	Main voltage regulator ground	C9
GND_BKP_PMU	GND	GND	Backup voltage regulator ground	E4
GND_TSENS	GND	GND	Temperature sense block ground	G9
GND_RF	GND	GND	RF ground	G2, G3, G4, G5, H2, H3
GND	GND	GND	Ground	A1, A9, E5, E6, F5, F6

1. *Refer to Section 4: Electrical specifications.*
2. *Backup power must be applied at the same time as or before V_{CORE_IN}, not after.*

Table 2. Main function pins

Symbol	I/O voltage(1)	I/O	Description	Ball	Reset state
EXT_REG_SEL	V_{CORE_IN}	I	LDO core disable. When a high level is applied to that pin, the LDO core is off and an external power source must supply it.	A8	NA
TEST	IO-ring2	I	TEST- JTAG enable. In mission/application mode, this pin must be connected to GND.	C7	Hi-Z/PD
RTC_XTI	V_{BK_IN}/IO-ring0	I	It is the reference for the circuitry of the real-time clock counter. If the 32 kHz oscillator is enabled, it is the input of the 32 kHz oscillator amplifier circuit; else it is a CMOS input as specified in Table 18. Electrical characteristics of digital input and output buffers.	D1	NA
RTC_XTO	V_{BK_IN}/IO-ring0	O	Output of the oscillator amplifier circuit.	E1	NA
RESETn	V_{BK_IN}/IO-ring0	I	Reset input with Schmitt-trigger characteristics and noise.	E2	Hi-Z/PD
WAKEUP	V_{BK_IN}/IO-ring0	I	Wake-up from standby mode. When a high level is applied to that pin, the device wakes up and exits standby mode. It has higher priority compared to the STANDBY_IN pin.	E3	Hi-Z
STANDBY_IN(2)	V_{BK_IN}/IO-ring0	I	When a low level is applied to that pin, the chip is forced to standby mode.	F4	Hi-Z
STANDBY_OUT	V_{BK_IN}	O	Standby mode monitor. A low level applied to that pin indicates that the device is in standby mode.	D9	Hi-Z

1. *In standby mode, if VIO1 and VIO2 are powered, the GPIOs have no driving capabilities and no PD/PU is active.*
2. *If V_{CORE_IN} is removed before STANDBY_IN has switched from high to low, STANDBY_OUT remains high level, even if the device enters standby mode.*

Table 3. RF front-end pins

Symbol	I/O voltage	I/O	Description	Ball
ANTSens2/ AIN1	IO-ring RF	I	Antenna sensing–TPIF_P	H5
ANTSens1/ AIN0	IO-ring RF	I	Antenna sensing–TPIF_N	H4
LNA_IN	LNA V_{CC}	I	LNA input	H1
LNA_OUT	LNA V_{CC}	O	LNA output	J2
RFA_IN	V_{RF_OUT}	I	RFA input	J3
TCXO_IN	PLL V_{CC}	I	TCXO input	F1

Table 4. Memory interface (power fail-safe I/Os)

Symbol	I/O voltage	I/O	Description	Ball	Reset state
SFC_CLK	IO-ring1	O	Serial flash controller clock	B1	Hi-Z/PD
SFC_CSN	IO-ring1	O	Serial flash controller chip select	A2	Hi-Z/PD
SFC_SIO0	IO-ring1	I/O	Serial flash controller data I/O 0	D4	Hi-Z/PD
SFC_SIO1	IO-ring1	I/O	Serial flash controller data I/O 1	C4	Hi-Z/PD
SFC_SIO2	IO-ring1	I/O	Serial flash controller data I/O 2	B3	Hi-Z/PD
SFC_SIO3	IO-ring1	I/O	Serial flash controller data I/O 3	C3	Hi-Z/PD

Table 5. External RF interface (power fail safe I/Os)

Symbol	I/O voltage(1)	I/O	Description	Ball
ISIG1	IO-ring1 (FS)	I	Ex RF interface I-Sign1	C6
IMAG1	IO-ring1 (FS)	I	Ex RF interface I-Mag1	B4
QSIG1	IO-ring1 (FS)	I	Ex RF interface Q-Sign1	D6
QMAG1	IO-ring1 (FS)	I	Ex RF interface Q-Mag1	A4
ISIG2	IO-ring1 (FS)	I	Ex RF interface I-Sign2	D5
IMAG2	IO-ring1 (FS)	I	Ex RF interface I-Mag2	B5
QSIG2	IO-ring1 (FS)	I	Ex RF interface Q-Sign2	A5
QMAG2	IO-ring1 (FS)	I	Ex RF interface Q-Mag2	C5

1. *FS: fail-safe I/O.*

Table 6. Communication interface pins

Symbol	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO6	IO-ring2 (FS)	I/O	Default	GPIO6	—	A6	PD
		I	ALT A	CAN0_RX	CAN receiver		—
		I	ALT B	—	—		—
		I/O	ALT C	I2C_SDA	I²C data		—
GPIO5	IO-ring2 (FS)	I/O	Default	GPIO5	—	A7	PD
		O	ALT A	CAN0_TX	CAN transmitter		—
		I	ALT B	SFC_DQS	Serial flash controller DQS		—
		I/O	ALT C	I2C_CLK	I²C clock		—
PPS_OUT	IO-ring2 (FS)	I/O	Default	GPIO32	—	H8	PD
		I	ALT A	—	—		—
		O	ALT B	UART0_TX	UART0 transmitter		—
		O	ALT C	PPS_OUT	—		—
MSP1_clk_out	IO-ring1 (FS)	I/O	Default	GPIO91	—	J8	PD
		I/O	ALT A	MSP1_clk	MSP1 clock		—
		I/O	ALT B	SSPCLK	SSP clock		—
		O	ALT C	CLKOUT	Clock output		—
MSP1_CS	IO-ring1 (FS)	I/O	Default	GPIO90	—	H9	PD
		I/O	ALT A	MSP1_CS	MSP1 chip select		—
		I/O	ALT B	SSPFRM	SSP chip select		—
		I	ALT C	UART2_RX	UART2 receiver		—
MSP1_Din	IO-ring1 (FS)	I/O	Default	GPIO94	—	J9	PD
		I	ALT A	MSP1_Din	MSP1 data input		—
		I	ALT B	SSPRXD	SSP data receive		—
		O	ALT C	—	—		—
MSP1_Dout	IO-ring1 (FS)	I/O	Default	GPIO95	—	G7	PD
		O	ALT A	MSP1_Dout	MSP1 data output		—
		O	ALT B	SSPTXD	SSP data transmit		—
		O	ALT C	UART2 TX	UART2 transmitter		—

Symbol	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
JTAG-TRSTn(2)	IO-ring2 (FS)	I/O	Default	JTAG-TRSTn	JTAG reset	F8	PD
		O	ALT A	PPS_OUT	—		—
		I	ALT B	—	—		—
		I	ALT C	Timer_OCMPA	Timer A input		—
JTAG-TCK(2)	IO-ring2 (FS)	I/O	Default	JTAG-TCK	JTAG clock	F9	PD
		I/O	ALT A	SSPCLK	SSP clock		—
		I/O	ALT B	MSP0_clk	MSP0 clock		—
		I	ALT C	Timer_ICAPA1	Timer A input		—
JTAG-TMS(2)	IO-ring2 (FS)	I/O	Default	JTAG-TMS	JTAG TMS	E7	PU
		I/O	ALT A	SSPFRM	SSP chip select		—
		I	ALT B	MSP0_Din	MSP0 data input		—
		O	ALT C	UART0_RTS	UART0 RTS		—
JTAG-TDI(2)	IO-ring2 (FS)	I/O	Default	JTAG-TDI	JTAG data input	E8	PU
		I	ALT A	SSPRXD	SSP data receive		—
		O	ALT B	MSP0_Dout	MSP0 data output		—
		O	ALT C	UART0_CTS	UART0 CLR		—
JTAG-TDO(2)	IO-ring2 (FS)	I/O	Default	JTAG-TDO	JTAG data output	E9	PD
		O	ALT A	SSPTXD	SSP data transmit		—
		I/O	ALT B	MSP0_CS	MSP0 chip select		—
		I	ALT C	PPS_IN	PPS input		—
UART1_RX	IO-ring2	I/O	Default	USB_DM	USB minus	J7	PD
		I	ALT A	UART1_RX	UART1 receiver		—
		I/O	ALT B	I2C_SDA	I²C data		—
		I	ALT C	CAN1_RX	CAN1 receiver		—
UART1_TX	IO-ring2	I/O	Default	USB_DP	USB positive	J6	PD
		O	ALT A	UART1_TX	UART1 transmitter		—
		I/O	ALT B	I2C_CLK	I²C clock		—
		O	ALT C	CAN1_TX	CAN1 transmitter		—
UART2_RX	IO-ring2 (FS)	I/O	Default	GPIO89	—	B9	PD
		I	ALT A	UART2_RX	UART2 receiver		—
		I/O	ALT B	—	—		—
		O	ALT C	—	—		—
UART2_TX	IO-ring2 (FS)	I/O	Default	GPIO88	—	C8	PD
		O	ALT A	UART2_TX	UART2 transmitter		—
		I/O	ALT B	—	—		—
		O	ALT C	—	—		—
GPIO67	IO-ring2	I/O	Default	GPIO67	—	G8	PD
		O	ALT A	—	—		—
		I/O	ALT B	UART0_RX	—		—
		I	ALT C	PPS_IN	—		—
GPIO26	IO-ring1 (FS)	I/O	Default	GPIO26	—	D3	PD

Symbol	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO26	IO-ring1 (FS)	I/O	ALT A	SFC_SIO4	—	D3	—
		O	ALT B	—	—		—
		I/O	ALT C	—	—		—
GPIO27	IO-ring1 (FS)	I/O	Default	GPIO27	—	B2	PD
		I/O	ALT A	SFC_SIO5	—		—
		I	ALT B	—	—		—
		I/O	ALT C	—	—		—
GPIO28	IO-ring1 (FS)	I/O	Default	GPIO28	—	C2	PD
		I/O	ALT A	SFC_SIO6	—		—
		O	ALT B	—	—		—
		I/O	ALT C	—	—		—
GPIO29	IO-ring1 (FS)	I/O	Default	GPIO29	—	D2	PD
		I/O	ALT A	SFC_SIO7	—		—
		O	ALT B	—	—		—
		I/O	ALT C	—	—		—

1. *FS: fail-safe I/O.*
2. *The JTAG pins can be configured as GPIOs in a dedicated alternate function mode such as: TRSTn = GPIO0, TCK = GPIO1, TMS = GPIO2, TDI = GPIO3, and TDO = GPIO4.*

3 General description

3.1 Multiconstellation and multiband

The STA8100GA supports the following GNSS constellations and bands. (Some scenario combinations require the use of the external front-end, STA5635A).

- GPS (L1 C/A, L2C, and L5)
- GLONASS (L1OF, L2OF)
- BeiDou (B1C, B1I, B2a, B2I)
- Galileo (E1, E5a, E5b, E6)
- QZSS (L1 C/A, L2C, L5)
- NAVIC–former IRNSS (L5)

The STA8100GA also provides raw carrier phase measurements.

In standalone operation mode, the STA8100GA supports the simultaneous usage of all constellations in parallel on the L1 band: GPS, GLONASS, Galileo, BeiDou, and QZSS in addition to SBAS. Combined with the external STA5635A radio-frequency front-end, the STA8100GA also supports all the other bands. The table below lists the main GNSS scenarios–or use cases– that the STA8100GA supports, either in standalone mode or combined with the STA5635A. Each of these scenarios requires a dedicated configuration.

Table 7. GNSS user cases

I = Internal STA8100GA RF block.
E = External STA5635A RF receiver.

Constellation	GPS/QZSS			GLONASS		BeiDou			Galileo				NAVIC	SBAS
Frequency	L1C/A	L2C	L5	L1OF	L2OF	B1I	B2I	B2A	E1	E5b	E5A	E6	L5	L1C/A
Case 0	I	E	—	I	E	I	—	—	I	—	—	—	—	I
Case 1	I	E	—	I	—	I	E	—	I	—	—	—	—	I
Case 2	I	E	—	I	—	I	—	—	I	E	—	—	—	I
Case 3	I	—	E	I	—	I	—	E	I	—	—	—	—	I
Case 4	I	—	E	I	—	I	—	—	I	—	E	—	—	I
Case 5	I	—	E	I	—	I	—	—	I	—	—	—	E	I
Case 6	I	—	I	—	—	—	—	—	I	—	I	E	—	I
Case 7	I	—	I	—	—	I	—	I	I	—	—	—	I	I
Case 8	I	—	I	—	—	I	—	—	I	—	I	—	—	I
Case 9	I	E	I	—	—	I	E	I	—	—	—	—	—	I
Case 10	I	E	I	—	—	—	—	—	I	E	I	—	—	I

Note: Up to 80 satellites can be tracked simultaneously.

3.2 L-band raw correction data reception

The STA8100GA allows the reception of wide-area correction services from L-band satellites. Each correction service provider covers a specific area of the world with a different transmission frequency and service ID. The internal RF block of the STA8100GA can be tuned to receive L-band channels. A 10-bit ADC converts I and Q analog data. A digital downconversion (DDC) and decimation chain shifts the selected L-band channel to zero intermediate frequency (IF) and provides the requested sampling rate. The L-band data can then be processed using the proper software development kit (SDK) software interface.

3.3 RF front end (G5RF)

The integrated RF front end can support different bands (L1 and L5) thanks to a programmable and flexible RF-IF chain driven by a fractional PLL.

The RF-IF chain is followed by a 3-bit ADC that can convert the IF signal to sign (SIGN) and magnitude (MAG1, MAG0) bits. The MAG bit is integrated internally to control the variable-gain amplifiers.

The embedded fractional PLL allows a wide range of reference clocks to be supported (typical value of 26 MHz).

3.4 Multiband multiconstellation baseband (G5BB) processor

The STA8100GA integrates a G5BB-proprietary IP, which is STMicroelectronics's latest generation of high-sensitivity baseband processor fully compliant with all different constellations and bands: GPS, Galileo, GLONASS, BeiDou, NAVIC (former IRNSS), and QZSS systems.

3.5 MCU subsystem

The Cortex®-M7 core controls the system resources (memories, registers, and external memory controllers) through the AXI, AHB, and APB interconnections present in the SoC.

3.5.1 Caches

The size of the instruction and data cache used for the Arm® subsystem in the STA8100GA is 16 Kbytes each.

3.5.2 Tightly coupled memory (TCM)

The Arm® Cortex®-M7 core has a TCM control unit (TCU) with TCM interfaces and an AHB subordinate (AHBS) interface for system access to the TCMs. These TCMs are integrated outside the Arm® subsystem. The STA8100GA has a 64 Kbyte instruction TCM and 384 Kbytes of data TCM.

In the data TCM, 160 KB are dedicated to the Arm® core usage. The Arm® subsystem and the G5BB module share the remaining 224-KB data TCM.

The Arm® subsystem provides access to the TCMs through an AHB subordinate interface. This AHBS interface is connected to the AMBA® infrastructure so that the DMA present on the bus can access the TCMs.

3.5.3 Nested vector interrupt controller (NVIC)

This nested vector interrupt controller (NVIC) allows the interrupt handler of the operating system to execute interrupt service routines quickly in response to peripheral interrupts. It provides a software interface to the interrupt system. The Arm® Cortex®-M7 core has an NVIC module for handling the interrupts. The NVIC supports 128 interrupts with 16 levels of priority, which can be changed dynamically. The software controls each request line to generate software interrupts.

3.5.4 AXI bus

The AXI bus matrix handles major high-bandwidth transactions for the STA8100GA. It connects the SRAM, boot ROM, and external memory controllers, which provide access to the external flash memory. The Arm® core acts as the manager with the highest priority on this bus.

3.6 APB peripherals

3.6.1 APB bridge 0 peripherals

The AHB-to-APB bridge 0 sits on the AHB bus matrix 0 as a subordinate and is used to connect peripherals. The AHB managers connected to the AHB bus matrix 0 access the APB 0 peripherals.

The peripherals connected to APB 0 are the ones on the always-on domain: power, reset, and clock controller (PRCC) always ON and RTC.

3.6.2 APB bridge 1 peripherals

The AHB-to-APB bridge 1 sits on the AHB bus matrix 0 as a subordinate and is used to connect peripherals. The AHB managers connected to the AHB bus matrix 0 access the APB 1 peripherals.

The peripherals connected to APB 1 are UART1, EFT0, EFT1, GPIO ports 0 & 1, MTU0, OTP, SSP, the thermal sensor, and the watchdog timer.

3.6.3 APB bridge 2 peripherals

The AHB-to-APB bridge 2 sits on the AHB bus matrix 0 as a subordinate and is used to connect peripherals. The AHB managers connected to the AHB bus matrix 0 access the APB 2 peripherals.

The peripherals connected to APB 2 are: UART2, MSP1, GPIO port 2, and MTU1.

3.6.4 AHB subordinate devices

Some AHB subordinate devices are connected to AHB bus matrix 0.

3.7 eSRAM

256 KB of embedded RAM are available on top of the TCM RAM.

The eSRAM is directly connected to the MCU through the AXI bus. It is used for data and instruction.

3.8 Serial flash memory controller (SFC)

The serial flash memory controller supports single, quad, and octal memories. It is used for execution in place (XIP) thanks to direct memory mapping.

3.9 SSP

The STA8100GA has one synchronous serial port (SSP). The SSP is a controller or target interface that enables synchronous serial communication with target or controller peripherals having one of the following:

- A serial peripheral interface bus
- A synchronous serial protocol bus
- A MICROWIRE interface bus
- A unidirectional interface

In both the controller and target configurations, the SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location deep receive FIFO
- Programmable data frame size from 4 to 32 bits
- Programmable clock bit rate and prescaler
- Programmable clock phase and polarity in SPI mode
- Support for direct memory access (DMA)

3.10 I²C high-speed controller

One I²C high-speed controller interface is capable of controller/target modes in a multicontroller environment. It is DMA-capable and supports multiple baud rates: 100/400/1000/3400 kbits/s.

3.11 UART

The UART performs the following operations:

- Serial-to-parallel conversion on the data asynchronously received from a peripheral device on the UARTx_RX pin
- Parallel-to-serial conversion on the data written by the CPU for transmission on the UARTx_TX pin

The transmit and receive paths are buffered with internal FIFO memories that allow up to 64 data bytes for transmission, and 64 data bytes with 4-bit status (break, frame, parity, and overrun) for reception. The system processor or DMA can burst-load or empty the FIFOs, from 1 to 16 words per transfer.

3.12 Watchdog timer (WDT)

The watchdog timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (Irq_wdt) depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserved for the entire programmed period. The WDT counts down at a fixed frequency of 32.768 kHz.

The watchdog timer peripheral is used as a free-running timer or as a watchdog to resolve processor malfunctions due to hardware or software failures.

Feature set overview:

- 16-bit down counter
- 8-bit clock prescaler
- Safe reload sequence
- Free-running timer mode
- End-of-counting interrupt generation

3.13 GPIO

There are 34 GPIOs in this device.

The GPIO block provides programmable inputs or outputs. Each input or output is controlled in two modes:

- Software mode through an APB bus interface
- Alternate function mode, where the GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. For each GPIO, the user can select the edge (rising, falling, or both) that triggers an interrupt.

All GPIOs are fail-safe to avoid leakage consumption in any condition even when the ring is off and the external line is logic level high.

3.14 Multitimer unit (MTU)

The MTU consists of eight timers. Each timer is clocked by either of:

- The TCXO frequency (TCKO_IN) divided by 8 (refer to Table 17. RF electrical characteristics for the value of TCKO_IN.)
- The REFCLK (32.768 kHz) frequency

3.14.1 MTU feature overview

- The multitimer unit provides access to four interrupts that generate programmable, 32-bit, free-running, decrementing counters (FRCs). These counters allow up to four counts in parallel.
- The FRCs have their own clock input. This allows the counters to run from a much slower clock than the system clock.
- In each FRC, the 32-bit counter is split up into two 16-bit counters.

3.15 RTC

This is an always-on power domain dedicated to the RTC logic (backup system). It has a 256-byte SRAM and a dedicated voltage regulator to supply it.

The RTC provides a high-resolution clock that is used for GPS. It keeps the time when the system is inactive and is used to wake up the system when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal oscillator, and a secure time update.

RTC features:

- A 47-bit counter clocked by the 32.768 kHz clock:
  - 32 bits are for the integer part (seconds) and 15 bits are for the fractional part.
  - The integer part and the fractional part are readable independently.
  - The counter, once enabled, can be stopped.
- An integer part load register (32-bit)
- A fractional part load register (15-bit)
- A load bit that transfers the content of the entire load register (integer + fractional part) to the 47-bit counter Once the MCU has set this bit, the hardware clears it to signal to the MCU that the RTC has been updated.

3.16 MSP

The STA8100GA has one multimode serial port (MSP).

The multimode serial port is a synchronous transmitter serial interface.

It provides:

- Data elements of 8, 10, 12, 14, 16, 20, 24, and 32 bits, sent LSB or MSB first
- A programmable frequency shift clock for data transfer
- A direct interface to SPI-compliant devices
- Transmit first-in, first-out memory buffers (FIFOs), which are 32 bits wide and eight locations deep

3.17 Direct memory access (DMA)

The DMA controller (DMAC) is an advanced microcontroller bus architecture (AMBA®)-compliant system-on-chip (SoC) peripheral. The DMAC is an AMBA® AHB module; it connects to the advanced high-performance bus (AHB).

Module key features:

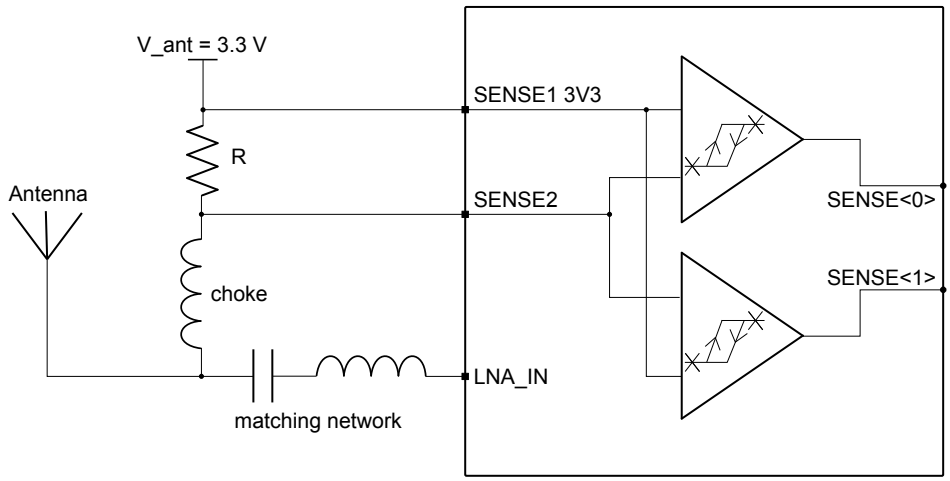
- Eight DMA channels. Each channel supports unidirectional transfer.
- The DMAC provides 32 peripheral DMA request lines.
- Single DMA and burst DMA request signals
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers
- Scatter or gather DMA support using linked lists
- Hardware DMA channel priority. DMA channel 0 has the highest priority and channel 31 has the lowest priority.
- If requests from two channels become active at the same time, the channel with the highest priority is served first.
- AHB subordinate DMA programming interface to the DMA control registers
- Two AHB bus managers for transferring data
- Programmable DMA burst size
- Working on the AHB clock

3.18 Antenna sensing

The following figure shows an example of an antenna sensing circuit working with a 3.3 V antenna. The input voltage range must be between V_{RF_IN} and GND.

Note: A dedicated application note exists on the STA8100GA antenna management features and options. ST can provide it upon request.

Figure 3. Antenna sensing configuration



The STA8100GA uses two comparators with hysteresis for antenna sensing. If a voltage of 3.3 V supplies the antenna, the antenna sensing block must be connected as illustrated in the above figure.

Antenna monitoring can also be implemented using the ADC embedded in the STA8100GA. (Ask ST for the dedicated application note for further details.)

3.19 Temperature sensor

A thermal sensor provides digital measurements of the junction temperature. The temperature measurement range is −40 °C to 125 °C. It uses an integrated bandgap reference and 8-bit ADC.

The temperature sensor block includes two programmable threshold registers. After enabling the temperature sensor and programming the threshold registers, the recorded temperature is compared with the threshold value. If the temperature is higher than the upper threshold register or lower than the lower threshold register, the temperature sensor block generates an interrupt.

Table 8. Temperature sensor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tsens	Sensitivity	—	—	—	1	°C
Tacc(1)	Accuracy	Calibration performed at 125 °C	±3(2)	—	±10	°C

1. *Best accuracy is obtained at the calibrated temperature.*
2. *Limited by the manufacturing calibration environment.*

3.20 Serial boot pins

The ROM code initiates the boot process and selects one of the boot options listed in the table below based on the value stored in the PRCC register. The status of the UART2-TX pin (ball C8), which is latched after the release of the internal reset, determines the boot value stored in the PRCC register.

Table 9. Boot peripheral selection

Pin	ROM action
UART2-TX = 0	Boot from flash memory - SFC controller
UART2-TX = 1	Boot from peripheral - UART

3.21 Reset

After a reset, the ROM code wakes up the Cortex®-M7 core.

The PRCC module executes all the steps needed to reset the device properly and prepare it to fetch the first instruction of the user application code.

The STA8100GA supports the following reset options:

- Pad reset: the SoC has an active-low chip reset (RESET) pad. A low (zero) level applied to this pad keeps the device in the reset state.
- Power-on reset: the power-on reset circuitry is embedded in the main voltage regulator built on the high-voltage (HV) supply (V_{CORE_IN}) of the regulator. It ensures that all voltage monitors are in the reset state until the V_{CORE_IN} (or $V_{DD\_EXT\_REG}$) minimum voltage is reached.
- Hardware resets: the internal voltage regulator embeds multiple low-voltage detectors (LVDs) and high-voltage detectors (HVDs), which are used in the reset sequence.
- Soft reset: different peripherals present on the STA8100GA reset independently through the registers present inside the PRCC module.

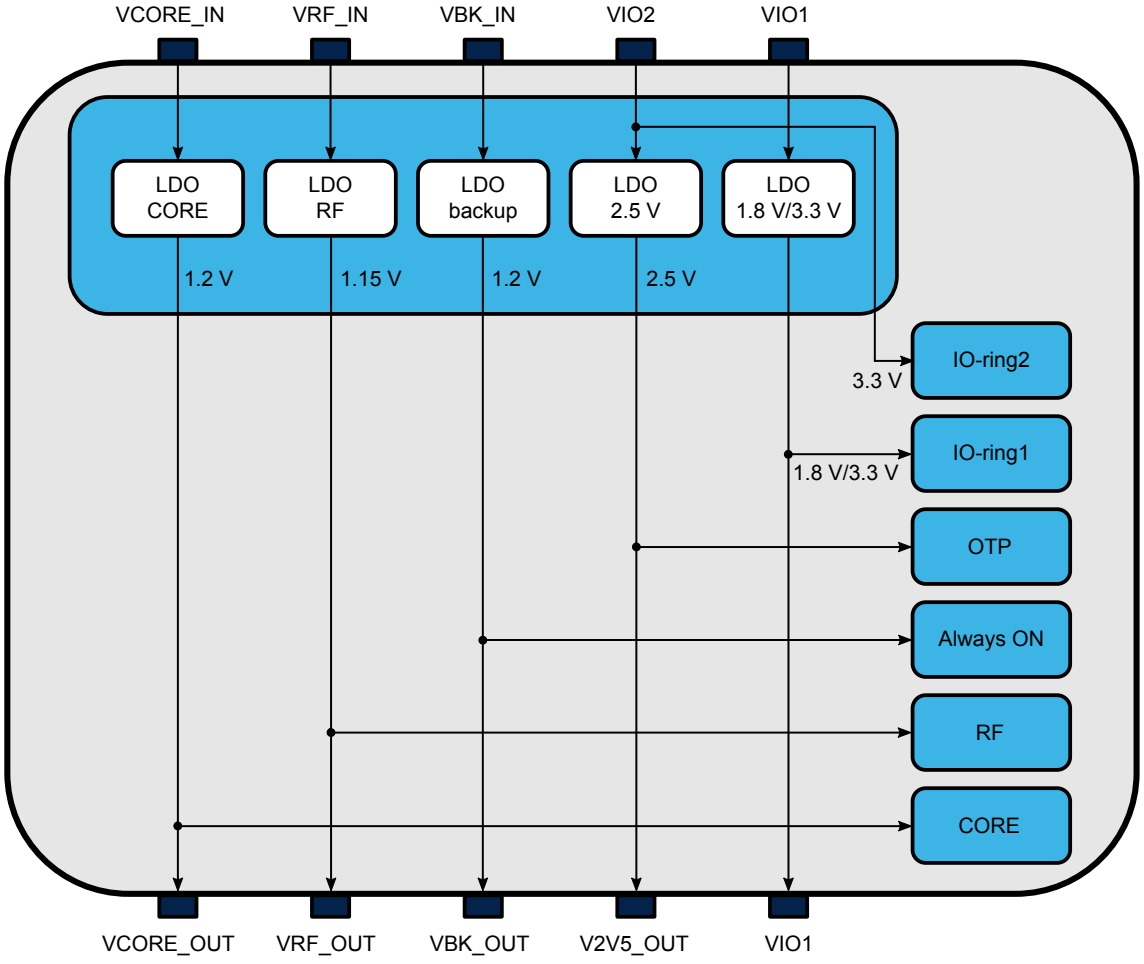
3.22 Power management unit (PMU)

The STA8100GA embeds five voltage regulators (LDOs).

Table 10. On-chip LDO regulators

LDO	Supply regions	Input voltage	Typical output voltage at 25 °C
Core LDO	Core	V_{CORE_IN} = 1.62 V to 3.6 V	1.2 V
LDO2v5	Temperature sensor	V_{IO_IN} = 3.3 V	2.5 V
I/O LDO	IO-ring 1	V_{IO_IN} = 3.3 V	1.8 V
Backup LDO	Always on	V_{BK_IN} = 1.62 V to 3.6 V	1.2 V
RF LDO	RF	V_{RF_IN} = 1.62 V to 3.6 V	1.15 V

Figure 4. On-chip LDO regulator dependencies



3.22.1 Power regions

The STA8100GA has six major power regions. The modules present inside each power region are listed below.

- Always-on backup region: 1.2 V
  - prcc_backup
  - RTC
  - Backup RAM: 256 bytes

- Switchable region: 1.2 V
  - Arm® core
  - Other digital IPs
- RF: 1.15 V
- OTP: 2.5 V
- IO-ring1: 1.8 V or 3.3 V
- IO-ring2: 3.3 V

IO-ring1 is set to 1.8 V when the internal I/O LDO supplies it. If a 3.3 V supply is applied to VIO1_EXT, IO-ring1 is set to 3.3 V (bypassing the internal I/O LDO).

An external voltage regulator supplies the switchable power region directly at pin VDD_EXT_REG. The integrated LDO CORE has to be switched off by forcing EXT_REG_SEL to high voltage.

The usage of the external regulator to supply the switchable power region is mandatory in applications that require sustaining 105 °C.

3.23 CAN interface

The CAN subsystem comprises two fully independent CAN FD® controllers: CAN0 and CAN1. Both controllers conform with the CAN protocol version 2.0 part A and B, and ISO 11898-1: 2015. The maximum data bit rate supported is 1 Mbit/s.

3.24 Full-speed USB 2.0

It supports 12 Mbit/s (full-speed) and 1.5 Mbit/s (low-speed) serial data transmission according to the USB 2.0 OTG controller specification.

4 Electrical specifications

4.1 Absolute maximum ratings

The table below describes the maximum ratings for the device. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

Table 11. Absolute maximum ratings

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{RF_IN}	Supply voltage	—	-0.3	—	3.9	V
V_{CORE_IN}	Supply voltage	—	-0.3	—	3.9	V
V_{BK_IN}	Supply voltage	—	-0.3	—	3.9	V
V_{IO_IN}	Supply voltage	—	-0.3	—	3.9	V
$V_{DD\_EXT\_REG}$(1)	Supply voltage	—	-0.3	—	1.4	V
T_J	Junction operating temperature	—	-40	—	125	°C
T_S	Storage temperature	—	-55	—	150	°C
ESDHBM	Electrostatic discharge–Human body model	—	—	—	±2	kV
ESDCDM(2)	Electrostatic discharge–Charge device model	—	—	—	±500	V
LU	Latch up	—	-100	—	+100	mA

1. *EXT_REG_SEL = high.*
2. *RFA_IN ESDCDM Max is ±50 V. LNA_IN ESDCDM max is ±250 V.*

4.2 Electrical characteristics

Table 12. Operating junction temperature range

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
T_J	Junction temperature	—	-40	27	125	°C

Table 13. $V_{DD\_EXT\_REG}$ — External core power supply

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$V_{DD\_EXT\_REG}$	External core power supply	EXT_SEL_REG = High	1.14	—	1.32	V

Table 14. Backup PMU–functional specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
LDO_BK						
V_{BK_IN}	Input voltage	—	1.62	3.3	3.6	V
V_{BK_OUT}	Output voltage	—	1.10	1.2	1.26	V
$I_{BK\_OUT\_LOAD}$	Load current in normal mode	—	—	—	2	mA

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{BK\_OUT\_LDO}$	LDO power consumption in normal mode(1)	—	—	—	20	µA
$I_{BK\_OUT\_PD\_LDO}$	LDO power-down consumption (1)	—	—	—	1	µA
C_{BK_OUT}	External capacitance(1)	—	0.5	1	1.2	µF
$V_{BK\_OUT\_LREG}$	Line regulation	—	—	—	10	mV
$V_{BK\_OUT\_LOAD\_REG}$	Load regulation	V_{BK_OUT} = 1.2 V at I_{OUT} = 0 mA V_{BK_OUT} = 1.1 V at I_{OUT} = 2 mA	—	—	100	mV
$T_{BK\_OUT\_STARTUP}$	Startup time(1)	—	—	—	600	µs
$V_{BK\_IN\_SLEW}$	Slew rate	(2)	0.04	—	40(1)	ms

1. *Specified by design.*
2. *If V_{BK_IN} = 3.3 V, add a 100 Ω series resistor and a 1 µF capacitor between GND and the V_{BK_IN} pin.*

Table 15. Main PMU–Functional specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
LDO_CORE						
V_{CORE_IN}	Input voltage	—	1.62	3.3	3.6	V
V_{CORE_OUT}	Output voltage available at balls $V_{DD\_EXT\_REG}$	EXT_REG_SEL = low ($V_{DD\_EXT\_REG}$)	1.14	1.2	1.30	V
I_{VCORE_OUT}	Load current	—	—	—	450	mA
I_{LDO_CORE}	LDO power consumption(1)	—	—	—	200	µA
$I_{LDO\_CORE\_OFF}$	LDO power down consumption(1)	—	—	—	4	µA
C_{CORE_OUT}	External capacitance(1)	EXT_REG_SEL= low ($V_{DD\_EXT\_REG}$)	2.35	4.7	6.35	µF
$V_{LDO\_CORE\_LINE}$	Line regulation	—	—	—	10	mV
$V_{LDO\_CORE\_LOAD\_REG}$	Load regulation	—	—	—	70	mV
$V_{LDO\_CORE\_SLEW}$	Load current transient(1)	—	—	—	150/100	mA/ns
$T_{LDO\_CORE\_START}$	Startup time(1)	—	—	15	—	µs
LDO I/O						
V_{IO2_IN}	Input voltage	—	3	3.3	3.6	V
V_{IO1_EXT}	Output voltage	With the internal 1.8 V IO-ring1 LDO used (no external voltage applied to V_{IO1_EXT}).	1.72	1.80	1.90	V
I_{LDO_IO}	Load current	—	—	—	90	mA
$I_{LDO\_IO\_CORE}$	LDO power consumption	—	—	—	200	µA
$I_{LDO\_IO\_CORE\_OFF}$	LDO power-down consumption	—	—	—	4	µA
C_{LDO_IO}	External capacitance (1)	—	1.1	2.2	3	µF
$V_{LDO\_IO\_LINE}$	Line regulation	—	—	—	10	mV
$V_{LDO\_IO\_LOAD\_REG}$	Load regulation	—	—	—	100	mV
$V_{LDO\_IO\_SLEW}$	Load current transient(1)	—	—	—	90/100	mA/ns
$T_{LDO\_IO\_START}$	Startup time(1)	—	—	25	—	µs

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
LDO_RF						
V_{RF_IN}	Input voltage	—	1.62	3.3	3.6	V
V_{RF_OUT}	Output voltage	—	1.05	1.15	1.25	V
	Load current	—	—	27	—	mA

1. *Specified by design.*

Table 16. Current consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{BK_Normal}	Current consumption at V_{BK_IN} in normal mode	V_{BK_IN} = 3.3 V T_j = 125 °C	—	—	1	mA
$I_{BK\_Standby}$	Current consumption at V_{BK_IN} standby mode	V_{BK_IN} = 3.3 V T_{AMB} = −40 °C	—	—	45	µA
$I_{CORE\_Functional\_85}$	Current consumption at V_{CORE_IN} with the ST reference application design running	V_{CORE_IN} = 3.3 V EXT_REG_SEL = Low Max. ambient temperature = 85 °C	—	—	300(1)	mA
$I_{CORE\_Functional\_105}$	Current consumption at $V_{DD\_EXT\_REG}$ with the ST reference application design running	V_{CORE_IN} = 3.3 V EXT_REG_SEL = High $V_{DD\_EXT\_REG}$ = 1.25 V Max. ambient temperature = 105 °C	—	—	400	mA
I_{CC_VRFIN}	Current consumption at V_{RF_IN}	V_{RF_IN} = 3.3 V All RF block ON, with V_{CC_LNA} and V_{CC_PLL} connected to V_{BK_OUT} on PCB T_{AMB} = 25 °C	—	28	—	mA
$I_{CC\_VRFIN\_off}$	Current consumption at V_{RF_IN} with G5RF in standby (off)	V_{RF_IN} = 3.3 V All RF block OFF, with V_{CC_LNA} and V_{CC_PLL} connected to V_{BK_OUT} on PCB. T_{AMB} = 25 °C	—	150	—	µA

1. *The maximum current at V_{CORE} is limited by the maximum junction temperature at 125 °C and Θ_{JA} = 33 °C/W (which depends on the printed circuit board of the application).*

Table 17. RF electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
LNA						
Gp	Power gain	L1 band	—	15	—	dB
		L5 band	—	15	—	
NF	Noise figure(1)	L1 band	—	2.5	—	dB
		L5 band	—	2.5	—	
LNA P_{1dB}	Input compression point	—	—	-16	—	dBm

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
RFA – MIXER – IF FILTER – VGA						
Gp_{RFA}	RFA voltage gain	Maximum gain	—	15	—	dB
		Minimum gain	—	5	—	dB
GC	Conversion gain (from RFA into ADC input)	VGA and RFA at maximum gain	—	90	—	dB
		VGA and RFA at minimum gain	—	40	—	
Δ_{VGA}	VGA dynamic range	—	—	50	—	dB
P_{1dB}	RF-IF-VGA input compression Point	In band RFA max VGA max	—	-100	—	dBm
		In band RFA max VGA min	—	-50	—	
NF_{RF-IF}	RF-IF-VGA noise figure(1)	VGA and RFA at maximum gain in the L1-L5-L bands	—	5	—	dB
BW	-1 dB high-frequency corner IF filter	—	—	13	—	MHz
ATT	Aliasing frequency rejection	F = 51 MHz (corner #1)	20	—	—	dB
Fractional synthesizer – VCO						
TCXO_IN	TCXO frequency	—	—	26	—	MHz
R_{DIV}	Reference divider range	—	1	—	63	—
N_{DIV}	Loop divider range	—	56	—	2047	—
Frac	PLL fractionality	—	—	18	—	bit
F_{LO}	LO operating frequency	—	2300	—	3300	MHz

1. *Specified by design.*

Table 18. Electrical characteristics of digital input and output buffers

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Input and output buffers						
V_{IH_1V8}	CMOS input high level	—	0.65 × V_{18_IO}	—	0.3 + V_{18_IO}	V
V_{IL_1V8}	CMOS input low level	—	- 0.3	—	0.35 × V_{18_IO}	V
V_{IH_3V3}	CMOS input high level	—	2.0	—	0.3 + V_{33_IO}	V
V_{IL_3V3}	CMOS input low level	—	- 0.3	—	0.8	V
C_{IN}	CMOS input capacitance	—		—	3	pF
V_{OH}	CMOS output high level	At max I_{OH}	V_{IO} - 0.4	—	—	V
V_{OL}	CMOS output low level	At max I_{OL}	—	—	0.4	V
I_{OL}/I_{OH} IO-ring1 and PPS_OUT	Driving current to sustain V_{OL}/V_{OH}	V_{OL}/V_{OH}	0	—	4	mA
I_{OL}/I_{OH} IO-ring2 except PPS_OUT	Driving current to sustain V_{OL}/V_{OH}	V_{OL}/V_{OH}	0	—	2	mA
t_{RISE}(1)	CMOS output rise time with C_L = 15 pF, from 10 to 90%; 3.3 V	2 mA max current drive	—	3	—	ns
		4 mA max current drive	—	2	—	
t_{FALL}(1)	CMOS output fall time with C_L = 15 pF, from 90 to 10%; 3.3 V	2 mA max current drive	—	3	—	ns
		4 mA max current drive	—	2	—	

1. *Specified by design.*

4.3 RTC 32.768 kHz oscillator specifications

The 32.768 kHz RTC oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF (using a crystal oscillator with recommended characteristics as per Table 19 below) as shown in Figure 5. 32.768 kHz crystal oscillator connection.

The 32.768 kHz RTC oscillator is disabled by default and must be enabled by setting bit 28-OSCI_EN of PRCC_BACKUP_REG0 to have 32.768 kHz oscillations when an XTAL pi-network is connected to the RTC_XTI/ RTC_XTO pins.

The table below gives the recommended oscillator specifications.

Table 19. Recommended crystal oscillator specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{SXTAL}	Crystal oscillator frequency	—	—	32.768	—	kHz
LM_{SXTAL}	Motion inductance(1)	—	3500	5	6500	H
CM_{SXTAL}	Motional capacitance(1)	—	4.0	5.0	6.0	fF
CO_{SXTAL}	Shunt capacitance(1)	—	1.0	1.3	1.6	pF
ESR	Resonance resistance(1)	—	—	—	80	kΩ
C_L	External load capacitance(1)	—	—	18 ±2%	—	pF

1. *Specified by design.*

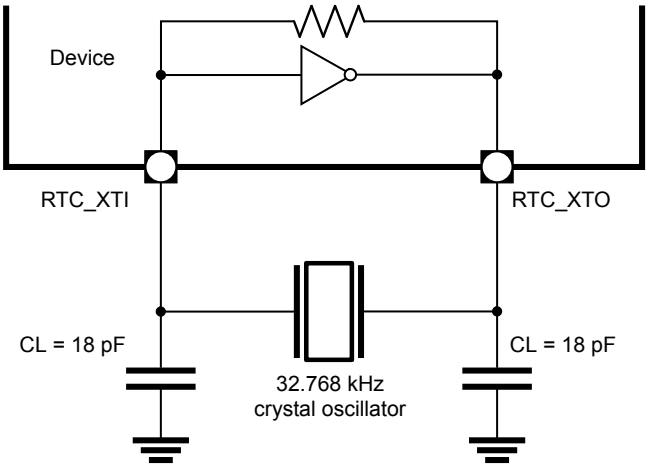
The following table provides the oscillator amplifier specifications.

Table 20. Oscillator amplifier specifications

Specified by design.

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_S	Startup time	—	—	0.3	0.6	s
DL	Drive level	—	—	—	< 0.1	µW
RLC	Required load capacitance	—	—	12.5	—	pF
GO	Startup conductance	—	22.5	33.6	60	µA/V

Figure 5. **32.768 kHz crystal oscillator connection**



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit 28-OSCI_EN = 0b in the PRCC_BACKUP_REG0 register). This disables the internal inverter, thus reducing the power consumption to the minimum.
- Drive the RTC_XTI pin with a square signal or a sine wave.

Table 21. **Characteristics of an external slow clock input**

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{JIT} (CC)	Cycle-to-cycle jitter	—	-70	—	70	ps
t_{JIT} (per)	Period jitter	—	-70	—	70	ps
—	Variation	—	-500	—	500	ppm
T_{DUTY}	Duty cycle	—	45	—	55	%

4.4 Power-up timing sequence

Figure 6. **Power-up timing diagram**

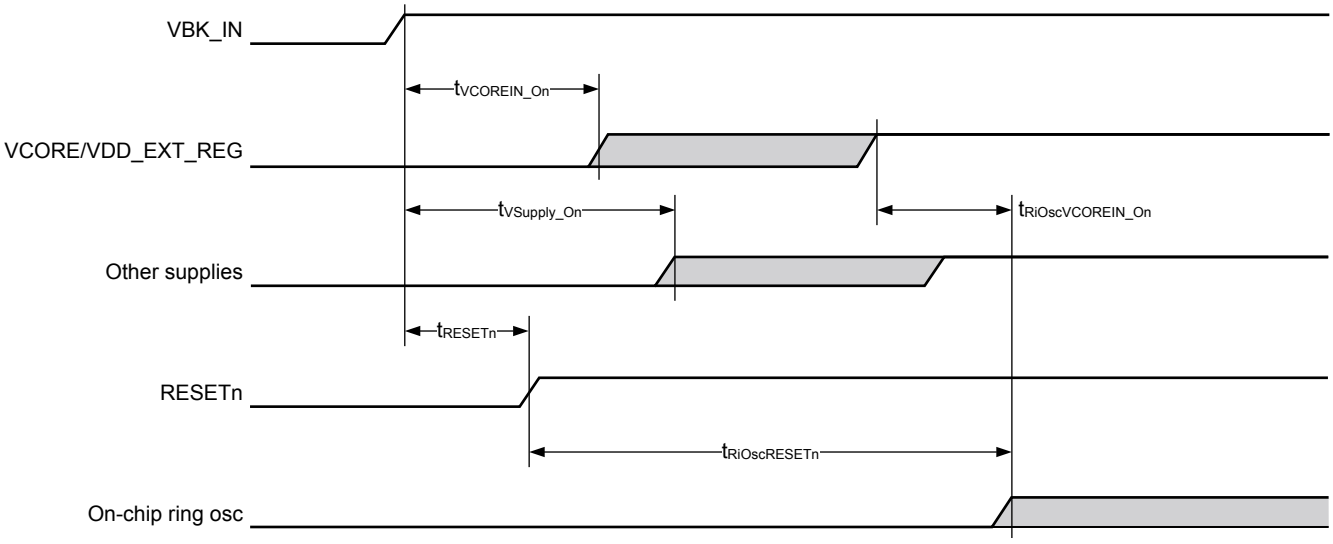


Table 22. Power-up timing data

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$t_{VCORE\_IN\_On}$	Time from the power-on of V_{BK_IN} to the power-on of V_{CORE_IN} or $V_{DD\_EXT\_REG}$	V_{BK_IN} > 1.62 V	0(1)	—	—	ms
$t_{VSupply\_On}$	Time from the power-on of V_{BK_IN} to the power-on of other supplies	V_{BK_IN} > 1.62 V	0(2)	—	—	ms
t_{RESETn}	Time from the power-on of V_{BK_IN} to RESETn going high	V_{BK_IN} > 1.62 V	4	—	—	ms
$t_{RiOscRESETn}$	Time from RESETn going high to the on-chip ring oscillator startup	V_{CORE_IN} > 1.62 V or $V_{DD\_EXT\_REG}$ > 1.14 V	0.5	—	—	ms
$t_{RiOscVCOREIN\_On}$	Time from V_{CORE} or $V_{DD\_EXT\_REG}$ applied to the on-chip ring oscillator startup	RESETn = high	0.5	—	—	ms

1. *The simultaneous power-on of V_{BK_IN} and V_{CORE_IN} or $V_{DD\_EXT\_REG}$ is allowed and tested.*
2. *The simultaneous power-on of V_{BK_IN} and other supplies is allowed and tested.*

4.5 Digital interface AC timing characteristics

Figure 7. Clock block diagram

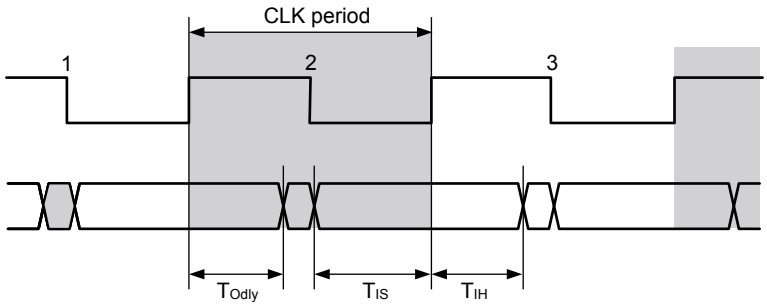


Table 23. Clock data

Specified by design.

Symbol	Comment
CLK period	Clock time period
T_{Odly}	Output data delay from the rising clock edge, unless differently specified
T_{IS}	Input data setup time to the rising clock edge, unless differently specified
T_{IH}	Input data hold time from the rising clock edge, unless differently specified

4.5.1 SQIO

Table 24. SQIO SDR mode (feedback mode)

Specified by design.

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	Clock	C_{load} 25 pF	—	—	78.5	MHz
CLK period		—	12.74	—	—	ns
CLK duty cycle		—	40	—	60	%
T_{IS}	Input	—	0.5	—	—	ns

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
T_{IH}	Input	—	2.5	—	—	ns
T_{Odly}	Output	C_{load} 25 pF	-2.5	—	2.4	ns

Table 25. SQIO DTR mode (DQS mode for flash memory read operations)

Specified by design.

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency(1)	Clock	C_{load} 25 pF	—	—	65	MHz
CLK period		—	15.38	—	—	ns
CLK duty cycle		—	40	—	60	%
T_{IS}	Input	—	0	—	—	ns
T_{IH}		—	0	—	—	ns
T_{Odly}	Output	C_{load} 25 pF	-1.25	—	1.8	ns

1. *This is the flash memory clock frequency.*

4.5.2 SPI

Table 26. SPI (controller mode)

Specified by design.

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	Clock	C_{load} 25 pF	—	—	19.625	MHz
CLK period		—	50.95	—	—	ns
CLK duty cycle		—	40	—	60	%
T_{IS}	Input	—	10	—	—	ns
T_{IH}		—	2	—	—	ns
T_{Odly}	Output	C_{load} 25 pF	2	—	10	ns

4.5.3 MSP controller mode

Table 27. MSP0 controller mode

Specified by design.

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	Clock	C_{load} 25 pF	—	—	9.8125	MHz
CLK period		—	101.9	—	—	ns
CLK duty cycle		—	40	—	60	%
T_{IS}	Input	—	10	—	—	ns
T_{IH}		—	4	—	—	ns
T_{Odly}	Output	C_{load} 25 pF	0	—	10	ns

Table 28. MSP0 target mode

Specified by design.

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	Clock	C_{load} 25 pF	—	—	9.8125	MHz
CLK period		—	101.9	—	—	ns
CLK duty cycle		—	40	—	60	%
T_{IS}	Input	—	10	—	—	ns
T_{IH}		—	4	—	—	ns
T_{Odly}	Output	C_{load} 25 pF	0	—	14.5	ns

Table 29. MSP1 target mode

Specified by design.

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	Clock	C_{load} 25 pF	—	—	9.8125	MHz
CLK period		—	101.9	—	—	ns
CLK duty cycle		—	40	—	60	%
T_{IS}	Input	—	7	—	—	ns
T_{IH}		—	4	—	—	ns
T_{Odly}	Output	C_{load} 25 pF	0	—	14	ns

4.5.4 JTAG

Table 30. JTAG characteristics

Specified by design.

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	Clock	C_{load} 25 pF	—	—	26	MHz
CLK period		—	38.4	—	—	ns
CLK duty cycle		—	40	—	60	%
T_{IS}	Input	—	5	—	—	ns
T_{IH}		—	5.5	—	—	ns
T_{Odly}	Output	C_{load} 25 pF	-3	—	15	ns

5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LFBGA81 package information

Figure 8. LFBGA81 package outline

81-ball LFBGA 8 × 8 × 1.7 mm, 0.8 mm pitch package

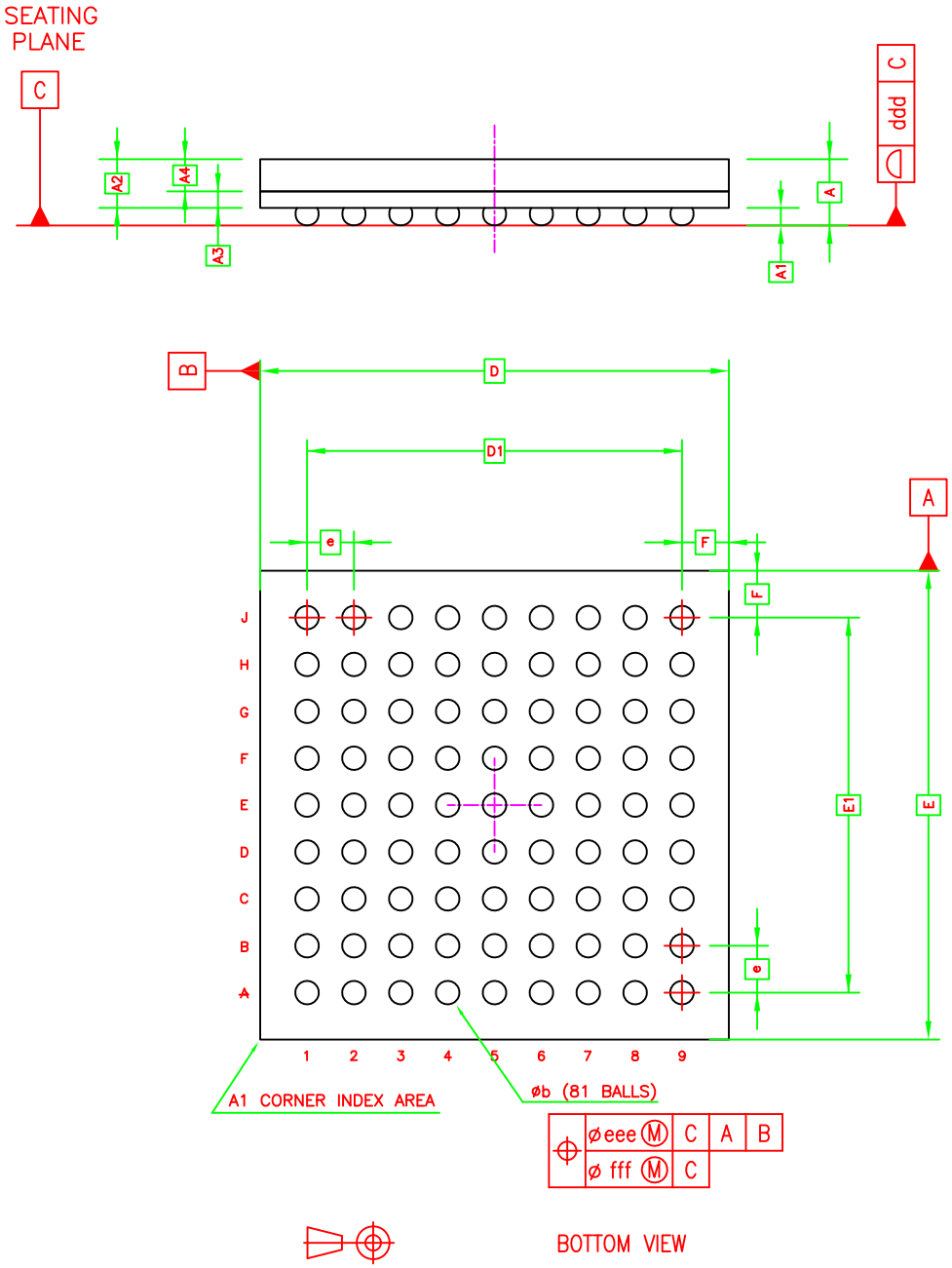


Table 31. **LFBGA81 package mechanical data**

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
A(1)	—	—	1.70
A1	0.25	—	—
A2	—	0.86	—
A3	—	0.27	—
A4	—	—	0.62
b(2)	0.35	0.40	0.45
D	7.85	8.00	8.15
D1	—	6.40	—
E	7.85	8.00	8.15
E1	—	6.40	—
e	—	0.80	—
F	—	0.80	—
ddd	—	—	0.10
eee(3)	—	—	0.15
fff(4)	—	—	0.08

1. *LFBGA stands for low-profile, fine-pitch ball grid array:*
   - *Low profile: 1.2 mm < A Max ≤ 1.7 mm / Fine pitch: e < 1.00 mm.*
   - *The total profile height (Dim A) is measured from the seating plane "C" to the top of the component.*
   - *The maximum total package height is calculated by the RSS (root sum square) methodology:*
     A Max = A1 Typ + A3 Typ + A4 Typ + √ ($A1^2$ + $A3^2$ + $A4^2$ tolerance values).
2. *The typical ball diameter before mounting is 0.40 mm.*
3. *The tolerance of position that controls the location of the pattern of the balls with respect to datums A and B. For each ball, there is a cylindrical tolerance zone eee perpendicular to datum C and located on the true position with respect to datums A and B as defined by e. The axis perpendicular to the datum C of each ball must lie within this tolerance zone.*
4. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball, there is a cylindrical tolerance zone fff perpendicular to datum C and located on the true position as defined by e. The axis perpendicular to the datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.*

5.2 Package thermal characteristics

This section describes the thermal characteristics of the device.

5.2.1 LFBGA81 thermal characteristics

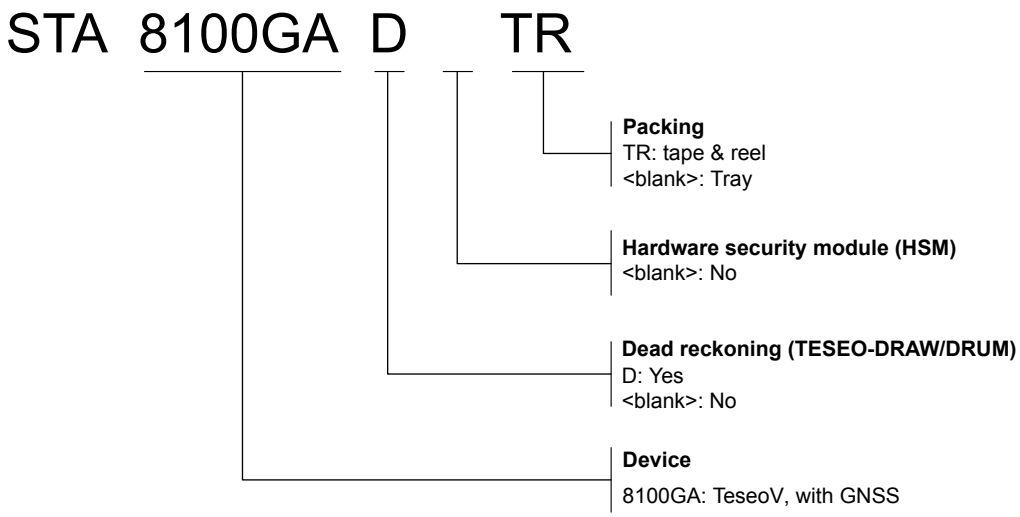
Table 32. **LFBGA81 thermal characteristics**

Symbol	Parameter	Value	Unit
T_{AMB}	Ambient operating temperature	-40 to 105	°C
θ_{JA}(1)	Thermal resistance junction-ambient	33	°C/W
Ψ_{JC}(2)	Thermal characterization parameter junction-case	3	°C/W

1. *Multilayer 2s2p as per JEDEC JESD51-2.*
2. *JESD51-8.*

6 Ordering information

Figure 9. **Ordering information scheme**



Revision history

Table 33. **Document revision history**

Date	Revision	Changes
13-May-2019	1	Initial release
29-Oct-2020	2	Cover page • Changed datasheet classification to Production data • Changed AEC-Q100 qualification to Qualified. • Removed the R in a circle superscript symbol that was inserted after “STMicroelectronics” • Added “for 85 °C maximum ambient temperature operations or 1.2V +/-5 % external voltage supply for 105 °C maximum ambient temperature operations” to bullet starting with “Main voltage domain 1.7 V to 3.6 V with LDO...” • Updated the IO-Ring 2 bullet with +/-10 % after the 3.3 V value • Removed “Hyper SPI Flash and RAM controller” • ESD voltage updated to 500V and other minor editorial changes. • Serial interface / UART updated to 3 • Removed “2x On the Fly decryptor engines” • Removed “Embedded hardware security micro enhanced” • USB2.0 full speed updated to 12 Mb/s Table 1: Power supply pins: Updated the from “Backup power may....after.” to “Backup p ower shall....after”. Table 2: Main function pins: • Updated EXT_REG_SEL, RTC_XTI and RTC_XTO’s IO voltage data • Updated footnote • Updated the text from “Input..... clock circuit.” to “If 32 kHz.....then input of.....amplifier circuit..... clock counter circuitry.” • Added a note, “If VCORE_IN is.....HIGH level,..... enter Standby mode.” Table 3: RF front-end pins: Updated Symbol name for ANTSens1 and ANTSens2 and change IO voltage for LNA_IN,LNA_OUT,RFA_IN and TCXO_IN. Table 6: Communication interface pins: Extensive update Table 7: GNSS user cases: • Updated table. • Updated note “Maximum 72 satellites tracked simultaneously.” to “Maximum 64 satellites tracked simultaneously.” Table 10: Temperature sensor: Updated Min. value and added a second footnote. Table 12: LDO on-chip regulators: updated Typ.output voltage @25C column Table 13: Absolute maximum ratings with on chip LDO voltage regulation: Updated TS max. value Table 14: Thermal data: • Updated θJA parameter and value • Updated ΨJC parameter Table 16: VDD_EXT_REG - external core power supply: updated min, typ and max values. Table 17: PMU11 - Functional specifications: Extensive update Table 18: PMU12 - Functional specifications: Extensive update Table 19: Current consumption (Tj = 125 °C): • Removed the ICORE_Dynamic row, ICC_VLNA, ICC_VPLL. • Updated test condition and Typ. value for ICC_VRFIN • Added a row for ICC_VRFIN_off • Removed IVIO1_EXT and IVIO2_IN Table 20: RF Electrical characteristics (Tj = 125 °C): Extensive update

Date	Revision	Changes
		Table 21: Electrical characteristics of digital input and output buffers: Added. Table 26: Clock data: Updated the symbol from “TIS and TIH” to “TJS and TJH” respectively. Table 34: Low speed and full speed mode: Replaced “high” with “full”. Table 48: Order codes: Replaced “tray” with “tape” Figure 1: STA8100GAS block diagram: Updated Figure 2: Device ballout: • Replaced CAN0_RX and CAN0_TX with GPIO6 and GPIO5 respectively. • Replaced SPI_CS, SPI_SI, and SPI_SO with JTAGTMS, JTAG-TDI, and JTAG-TDO respectively. • Replaced PPS_OUT, and SPI_CK with JTAG-TRSTn, and JTAG-TCK respectively. • Replaced SFC_ECS with GPIO67. • Updated TP_IF_N, TP_IF_P, and EOUT0 with TP_IF_N/ ANTSens1/ AIN0, P_IF_P/ ANTSens2/ AIN1, and PPS_OUT respectively. • Updated footnote from “Balls all have alternate..... functions A.” to “Balls all have.....registers”. Figure 4: LDO on-chip regulators dependencies: updated Figure 7: Clock block diagram: added Section 3.2: RF front end (G5RF): Updated the text from “The RF_IF chain..... 2-bit ADC.....(MAG) bit.” to “The RF_IF..... 3-bit ADC.....(MAG1, MAG0) bit”. Section 3.5.2: APB bridge 1 peripherals: Removed mail box and OTFDEC peripherals. Section 3.16: Antenna sensing: Updated section introduction paragraph. Section 3.19: Reset: Extensive update Section 4.4: RTC 32.768 kHz oscillator specifications: Added section Section 4.6: Digital interface AC timing characteristics (specified by design): Updated the section title from “Interface AC timing characteristics” to “Interface AC timing characteristics (guaranteed by design).” Section 4.6.5: USB - low speed and full speed mode: Replaced “high” with “full”. Removed sections related to Safety requirement, Hyperbus, HSM, OTP and OTFDEC.
23-Nov-2020	3	Public version on STMicroelectronics site. Updated Table 7: GNSS user cases.
15-Oct-2021	4	Following are the changes in this revision of the Datasheet: Updated all occurrences of “guaranteed by design” to “specified by design” in the document. Removed information related to SDMMC. Section : Features: • Added a bullet for Hardware Security Module (HSM). • Added a bullet for ST-DRAW. • Removed bullet for SDMMC (Secure Digital Multi Media Card Controller). Section : Description: Added a statement for security feature and TESEO-DRAW. Section 1: Overview: Updated to add statements related to HSM feature. Figure 1: STA8100GAS block diagram: Updated the block diagram and added a note. Table 6: Communication interface pins: Extensive update in the values of the table. Added footnote. Section 3.10: Watchdog Timer (WDT): Updated to add HW reset in the description. Figure 4: LDO on-chip regulators dependencies: Updated the block diagram. Table 16: VDD_EXT_REG - external core power supply: Updated Min. and Max. voltage values.

Date	Revision	Changes
		Table 17: PMU11 - Functional specifications: Removed rows for ILVDBK, ILVDCORE_BK, OLVDBK, OHVDBK, OLVDCORE_BK. Added “specified by design” for some parameters in Specification column. Table 18: PMU12 - Functional specifications: Removed rows for IVLDCORE, OLVDCORE, OHVDCORE, OLVDBK_CORE, OLVDRF, ILVDIO2, OLVDIO1 and OHVDIO1. Added “specified by design” for some parameters in Specification column. Table 19: Current consumption (Tj = 125 °C): Added a row for ICORE_functional_105. Updated information related to ICORE_Functional_85. Added a footnote. Table 22: Crystal recommended specifications: Removed footnote. Table 28: SQIO DTR mode (DQS mode for flash read): Added table. Section 6: Ordering information: Removed the table for order codes. Figure 9: Ordering information scheme: Added the diagram.
09-Oct-2024	5	In the whole document: • Replaced master/slave by manager/subordinate (AXI, AHB, DMA) or controller/target (SPI, SSP, I²C) depending on the context • minor editorial changes • restructured chapters • restructured tables • Updated package silhouette on the cover page • Added product summary and product status link to the cover page • Features – restructured content – added mention of the LFBGA81 package – added "L-band raw correction data reception" feature – removed HSM and AES accelerator features • Description: updated • Figure 2. STA8100GA ballout – replaced table by a figure – updated some ball names: A4, A5, B2, B4, B5, B9, C2, C5, C6, C9, D2, D3, D5, D6, D9, E4, G9, H4, and H5 • Table 1. Power-supply pins: – In the I/O voltage column, updated min values of V_{RFIN}, V_{RF_OUT}, V_{CORE_IN}, and V_{IO1_EXT} – V_{IO2_IN} and V_{IO1_EXT}: updated pin descriptions • Table 2. Main function pins: clarified some pin descriptions • Table 4. Memory interface (power fail-safe I/Os): removed SFC_SIO4 to SFC_SIO7 • Table 6. Communication interface pins: – added GPIO26 through GRPIO29 – J9 ball: removed function of ALT C • Section 3.4: Multiband multiconstellation baseband (G5BB) processor: – updated the list of supported Beidou signals – updated the maximum number of satellites that can be tracked simultaneously • Section 3.2: L-band raw correction data reception: added • Section 3.3: RF front end (G5RF): – updated the bands supported by the RF front end – updated the frequency of the reference clocks supported by the embedded fractional PLL • Section 3.13: GPIO: removed sentence • Section 3.14: Multitimer unit (MTU): – clarified – corrected MXTAL name (changed to TCXO) and value • Section 3.15: RTC: reorganized features

Date	Revision	Changes
		• Section 3.18: Antenna sensing: – clarified section – added reference to a dedicated application note available upon request – removed table with title "Antenna sensing current - power rising" – removed table with title "Antenna sensing current - power falling" • Section 3.20: Serial boot pins: updated • Section 3.21: Reset: updated the pad reset description • Section 3.22: Power management unit (PMU): changed RF LDO output voltage value and throughout the document • Figure 4. On-chip LDO regulator dependencies: updated • Section 4.1: Absolute maximum ratings: added introductory text • Table 11. Absolute maximum ratings – updated table title – ESDCDM: updated footnote • Table 13. $V_{DD\_EXT\_REG}$ — External core power supply: updated $V_{DD\_EXT\_REG}$ min and typ values • Table 14. Backup PMU–functional specifications: – updated table title – V_{BK_IN}: updated min value – removed "load current at deep standby mode" – removed "LDO power consumption at deep standby mode" – $V_{BK\_IN\_SLEW}$: updated max value • Table 15. Main PMU–Functional specifications: – updated table title – updated symbol for the V_{CORE_OUT} external capacitance to C_{CORE_OUT} – V_{CORE_IN}: updated min value – V_{CORE_OUT}: updated typ value and footnote – V_{IO1_EXT}: added conditions – V_{RF_IN} : updated typ value – V_{RF_OUT}: updated min value • Table 16. Current consumption: – Updated title – I_{BK_Normal}: updated conditions – $I_{BK\_DeepStandby}$ removed – $I_{BK\_Standby}$ added • Table 17. RF electrical characteristics: – updated title – Gp and NF: updated conditions – BW and ATT: updated (removed one test case) – TCXO_IN: removed min and max values • Table 18. Electrical characteristics of digital input and output buffers: V_{IL_1V8} and V_{IL_3V3}: corrected parameter description • Table 19. Recommended crystal oscillator specifications: added footnote "Specified by design" to some parameters • Table 20. Oscillator amplifier specifications: – removed second row of C_L – all values are specified by design • Table 22. Power-up timing data: updated parameter and condition columns, and added footnotes • Section 4.5: Digital interface AC timing characteristics: – removed "specified by design" from the title and added "Specified by design" as a note to all tables in the subsections • Table 25. SQIO DTR mode (DQS mode for flash memory read operations): updated note related to the clock frequency • Table 30. JTAG characteristics: updated table title • "USB - low speed and full speed mode" section removed • Figure 8. LFBGA81 package outline: added note above figure

Date	Revision	Changes
		• Moved thermal data from Section 4: Electrical specifications to Section 5.2: Package thermal characteristics • Table 32. LFBGA81 thermal characteristics: corrected symbol for "Thermal resistance junction-ambient" • Added glossary

Contents

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Glossary

AC Alternating current

ADC Analog-to-digital converter

AEC Automotive Electronics Council. Also known as CDF-AEC for Chrysler-Delco-Ford Automotive Electronics Council. Shortened to AEC.

AHB Advanced high-performance bus

AHBS Advanced high-performance bus subordinate

APB Advanced peripheral bus

AXI Advanced extensible interface

BeiDou Chinese navigation satellite-based radio navigation system

BGA Ball grid array

CAN Controller area network

CAN FD® Controller area network flexible data rate

CDM Charged device model

CMOS Complementary metal-oxide-semiconductor

CPU Central processing unit

DC Direct current

DDC Digital downconversion

DMA Direct memory access

DMAC DMA controller

DRAW Dead reckoning automotive way

DRAW Dead reckoning automotive way

DRUM Dead reckoning unplugged mode

DTR Double transfer rate

EGNOS European geostationary navigation overlay service

ESD Electrostatic discharge

eSRAM Embedded SRAM

FIFO First in, first out

FRC Free-running counter

G5BB G5 baseband correlator. ST-proprietary block part of the TeseoV family devices. It extracts positioning data from the Galileo, GPS, GLONASS, QZSS, BeiDou, and IRNSS satellite systems.

G5RF GNSS RF front end. RF ST-propietary block part of the TeseoV family devices. It supports different bands thanks to a programmable and flexible RF-IF chain driven by a fractional PLL.

GAGAN GPS-aided geo augmented navigation system. satellite-based augmentation system (SBAS) implementation by the Indian government.

Galileo EU´s global navigation satellite system

GB Gigabyte

GLONASS Russian satellite navigation system. Acronym for GLObalnaya NAvigatsionnaya Sputnikovaya Sistema (Russian). The role of the GLONASS satellite navigation system is similar to the GPS of the United States, the Galileo satellite positioning system of Europe, and the BeiDou satellite navigation system of China.

GNSS Global navigation satellite system

GPIO General-purpose input/output

GPS Global positioning system

HBM Human body model

Hi-Z High impedance

HV High voltage

HVD High-voltage detector

I/O Input/output

IC Integrated circuit

IEC International Electrotechnical Commission

IF intermediate frequency

IP Intellectual property

IRNSS Indian regional navigation satellite system, with the operational name of Navigation with Indian constellation (NAVIC).

ISO International Organization for Standardization

I²C Inter-integrated circuit

JEDEC Joint Electron Device Engineering Council

JTAG Joint Test Action Group

KB Kilobyte

LDO Low-dropout regulator

LFBGA Low-profile fine-pitch ball grid array

LNA Low-noise amplifier

LSB Least significant byte

LVD Low-voltage detector

MB Megabyte

MCU Microcontroller unit

MSAS Multifunctional satellite augmentation system

MSB Most significant byte

MSP Multichannel serial port

MTU Multitimer unit

NAVIC Navigation with Indian constellation. The Indian regional navigation satellite system (IRNSS) is an autonomous regional satellite navigation system that provides accurate real-time positioning and timing services.

NVIC Nested vector interrupt controller

OEM Original equipment manufacturer

OTP One-time programmable

PCB Printed-circuit board

PD Pull down

PLL Phase-locked loop

PMU Power management unit

PPS Pulse per second

PRCC Power, reset, and clock controller

PU Pull up

QZSS Quasi-zenith satellite system.

A Japanese satellite positioning system composed mainly of satellites in quasi-zenith orbits (QZO), but also of satellites in geostationary orbits (GEO).

RAM Random access memory

RF Radio frequency

RFA Radio-frequency amplifier

ROM Read-only memory

RSS Root sum square

RTC Real-time clock

Rx Receive/receiver/reception

SBAS Satellite-based augmentation system. It provides services for improving the accuracy, integrity, and availability of basic GNSS signals.

SD Secure digital

SDK Software development kit

SDMMC Secure digital and MultiMediaCard

SDR Single-data rate

SFC Serial flash memory controller

SoC System on chip

SPI Serial peripheral interface

SQIO Serial quad I/O

SRAM Static random-access memory

SSP Synchronous serial port

ST STMicroelectronics

TCM Tightly coupled memory

TCXO Temperature-controlled crystal oscillator

Tx Transmit/transmitter/transmission

UART Universal asynchronous receiver/transmitter

USB Universal Serial Bus

V2X Vehicle-to-everything. Qualifies wireless communication between a vehicle and any entity that may affect the vehicle, or may be affected by the vehicle. Communication system that is intended to improve road safety and traffic efficiency while reducing pollution and saving energy.

VCO Voltage-controlled oscillator

VGA Video graphics array

WAAS Wide-area augmentation system. Air navigation aid developed by the Federal Aviation Administration to augment the global positioning system.

WDT Watchdog timer

XIP Execution in place

XTAL External oscillator output