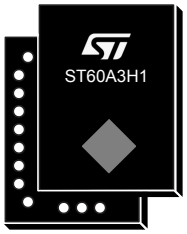
ST60A3H1

Datasheet

60 GHz V-band contactless connectivity transceiver with linear-polarization integrated antenna, and tunneling eUSB2, UART, GPIO or I²C



VFBGA23 AiP LP
(2.9 mm x 4.1 mm x 0.8 mm)

Features

- 60 GHz V-Band transceiver for short range contactless connectivity up to 480 Mbit/s
- Compact solution integrating full RF transceiver and dual-linear-polarization antenna, operating in Half-Duplex mode
- RF operational bandwidth: From 60 GHz to 61 GHz
- 42 dB typical total link budget, up to 5 cm free-space propagation loss
- eUSB2, UART, GPIO, or I²C RF tunneling
- Single 1.8 V supply
- Low power consumption (typical values):
  - eUSB2 Rx/Tx - 110/130 mW
  - UART/GPIO/I²C - 90 mW
  - Standby - 23 µW
- Optimized BOM without external matching network and clock references. A reference clock may be used at one end of the RF link to comply with specific regional regulation
- Package: VFBGA 2.9 mm x 4.1 mm x 0.8 mm, 23 balls, 0.4 mm pitch

Description

The ST60A3H1 is an RF millimeter-wave transceiver product with a dual-linear-polarization integrated antenna, operating in the 60 GHz V-band from 60 GHz to 61 GHz. The ST60A3H1 has a miniature form factor, optimized bill of materials and low-power operation. The ST60A3H1 is a high-speed RF transceiver compliant with eUSB2, UART, and I²C protocols. The transceiver module contains general-purpose input/outputs (GPIOs) that are also available in tunneling mode. The ST60A3H1 meets the requirements of applications by virtue of its compactness, low-power operation, ease of use and its innovative architecture design for optimized system bill of materials.

Applications

- Contactless test factory automation and after sales services
- Firmware Over-the-Air (FOTA) update
- Contactless data harvesting
- Life proof hole-less personal devices
- Contactless accessories
- Contactless personal equipment docking hub and data transfer
- Industrial contactless connectors
- Board-to-board connection and flex cable replacement

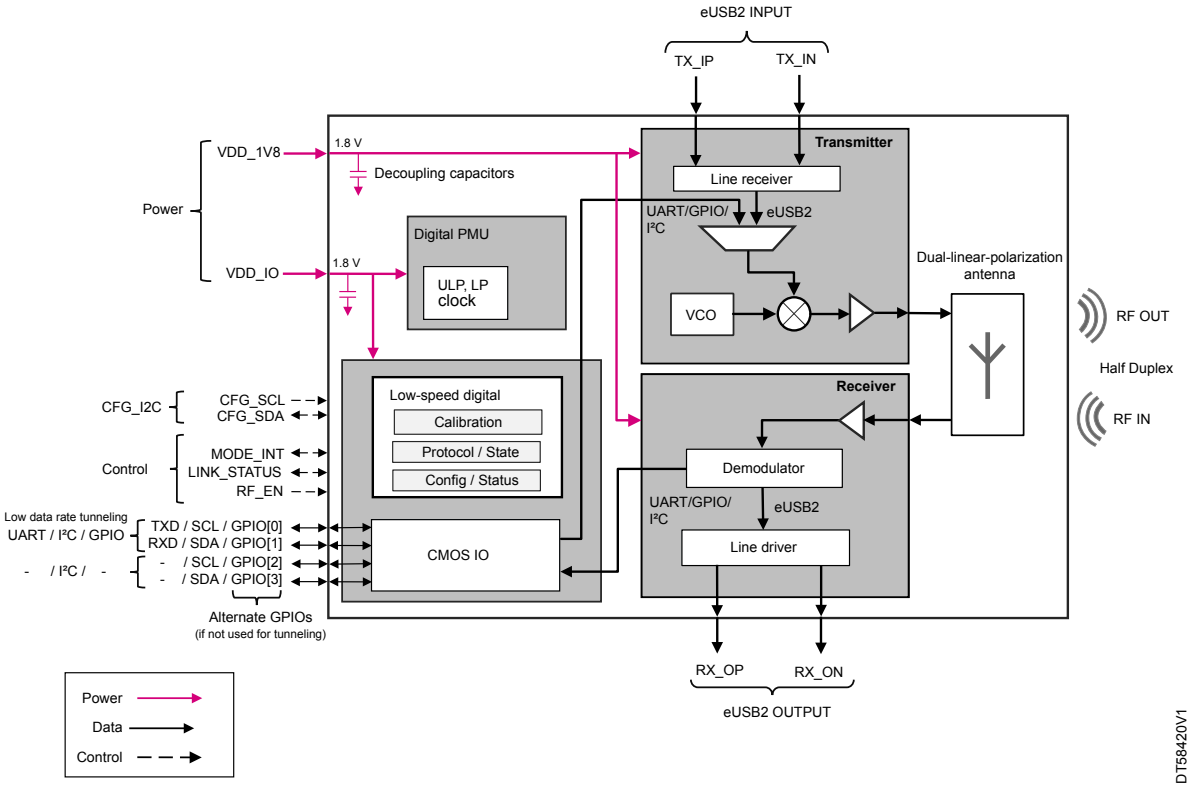
1 Introduction

1.1 Block diagram

The block diagram in Figure 1 shows a high-level view of the ST60A3H1.

For details of the pin functions by usage mode, refer to Section 2: Functional description.

Figure 1. ST60A3H1 block diagram



1.2 Acronyms and terms

Table 1. Definition of terms

Term	Definition
ABB	Analog base band
AiP	Antenna in package
BER	Bit error rate
CW	Continuous wave
CW0, CW1	Continuous wave data = 0, continuous wave data = 1
DC	Direct current
Discovery	Process of pairing two ST60A3H1 devices. Achieved during the SEEK phase of the RF_DETECT main FSM state.
EIRP	Effective isotropic radiated power
EIS	Effective isotropic sensitivity
eUSB2	Embedded USB2
FSM	Finite state machine
Full detection	Actively transmitting and listening to pair with an RF partner
FS	eUSB2 full speed
GPIO	General-purpose input/output
HS	eUSB2 high speed
I^2C	*Inter-integrated circuit* serial communication bus
Line driver	High speed circuit for transmitting the data received over the RF link
Line receiver	High speed circuit for receiving the data to be sent over the RF link
Link reset	Reset over the RF link keeping the configuration
Link training	Adjusting the RF receiver parameters to compensate for the channel characteristics
LNA	Low noise amplifier
Local	A locally programmable device partnering with an OTA-configurable device is referred to as the Local partner (see also Remote)
LP	Low power
LS	eUSB2 low speed
Mastership	Having control of OTA/RF link or protocol.
MOQ	Minimum order quantity
OTA	Over the air
OTP	One time programmable (memory)
Passive detection	Passively listening (only) to pair with an RF partner
PMU	Power management unit
POR	Power-on reset (circuitry)
Power-up reset (cold reset)	Full reset including hardware configuration
Remote	The OTA-configured device is the Remote partner (see also Local)
RRA	Remote register access
RSSI	Received signal strength indicator
SEEK	Power optimized search for an RF partner
Squelch	Suppressing a received signal when below a defined threshold level (eUSB2)

Term	Definition
ST60A3Hx	Family of ST60A3 RF millimeter-wave transceiver products with or without an integrated antenna
SW reset	Warm reset done by software through register programming
Tunneling	State of a pair of ST60A3H1 devices connected through an RF channel and seamlessly conveying data according to a specific protocol (eUSB2, UART/GPIO, or I^2C)
UI	Unit interval. UI = 2.08 ns in HS eUSB2
ULP	Ultralow power
VCO	Voltage controlled oscillator

1.3 Related documents

Table 2. Document references

Number	Reference	Title
[1]	eUSB2 v1.1	Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification.
[2]	USB v2.0	Universal Serial Bus Revision 2.0 Specification including ECNs and errata.
[3]	UTMI+ v1.0	USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Specification.
[4]	ES0650	ST60A3H1 device errata.

2 Functional description

This section details the various functional blocks of the ST60A3H1. Refer also to Figure 1. ST60A3H1 block diagram.

2.1 Overview

The ST60A3H1 is a fully integrated transceiver, with a dual-linear-polarization integrated antenna, including full transmit and receive paths, as well as digital control and power management necessary to operate the IC seamlessly into a low footprint application. The I²C configuration bus and hardware control pins enable to configure and manage the transitions of the ST60A3H1, which does not require any external RF component.

Once its RF is enabled, the ST60A3H1 enters a discovery state during which it looks for a partner. When a partner ST60A3H1 is detected, the RF link is established with optimized parameters, and the two devices enter LOW_POWER state. In this state, the locally programmable ST60A3H1 device or Local ST60A3H1 is configured by I²C. The partner ST60A3H1 device referred to as the Remote ST60A3H1 is configured either by I²C or over-the-air by the Local ST60A3H1 through Remote register access (RRA). An I²C set of commands sent to the Local device then sets the pair of ST60A3H1 devices into the desired tunneling mode (eUSB2, UART, GPIO or I²C) and data can be transferred.

The ST60A3H1 acts as a wireless repeater that seamlessly interfaces for eUSB2, UART, GPIO, and I²C protocols.

The mastership of any protocol is not correlated with the mastership (Local / Remote) of the RF link. See Figure 2 and Figure 3 below for more details.

Figure 2. ST60A3H1 pair with Local device on Host/Source/Controller side

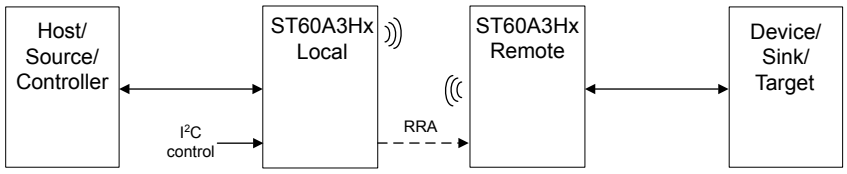
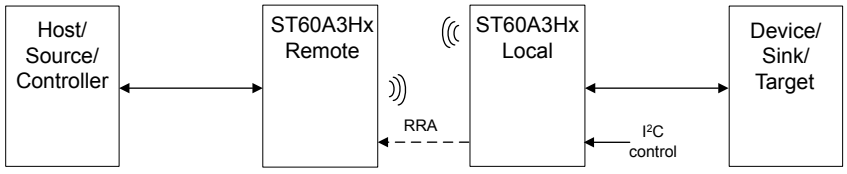


Figure 3. ST60A3H1 pair with Remote device on Host/Source/Controller side

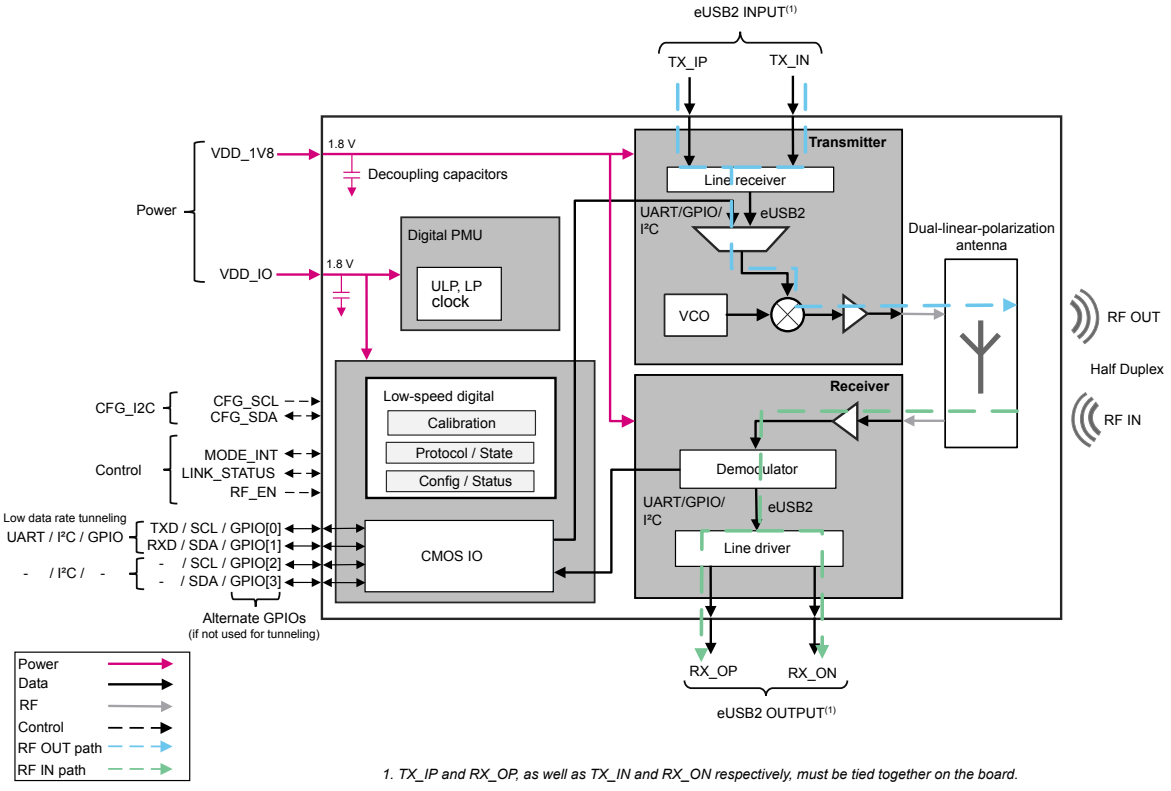


2.2 eUSB2 tunneling

eUSB2 tunneling configurations use the TX_IP, TX_IN differential pins for data transmission over the RF channel, and the RX_OP, RX_ON differential pins for data reception on the RF channel.

Figure 4 illustrates the data path in eUSB2 tunneling configurations. The four GPIOs that are not used for eUSB2 tunneling can be used as alternate GPIOs.

Figure 4. Data path in eUSB2 tunneling configurations



1. TX_IP and RX_OP, as well as TX_IN and RX_ON respectively, must be tied together on the board.

The electrical characteristics of these lines are configurable:

- DC coupled differential I/Os eUSB2
- Single ended I/Os for eUSB2 Low Speed and Full Speed.

All three eUSB2 speed rates are supported:

- Low Speed (LS) at 1.5 Mbit/s
- Full Speed (FS) at 12 Mbit/s
- High Speed (HS) at 480 Mbit/s

An ST60A3H1 pair, configured to tunnel eUSB2 traffic behaves as an eUSB2 Hybrid Repeater, as defined in appendix B of the eUSB2 specification [1]. A Hybrid Repeater refers to a device hosting an upstream eUSB2 interface and a downstream eUSB2 interface.

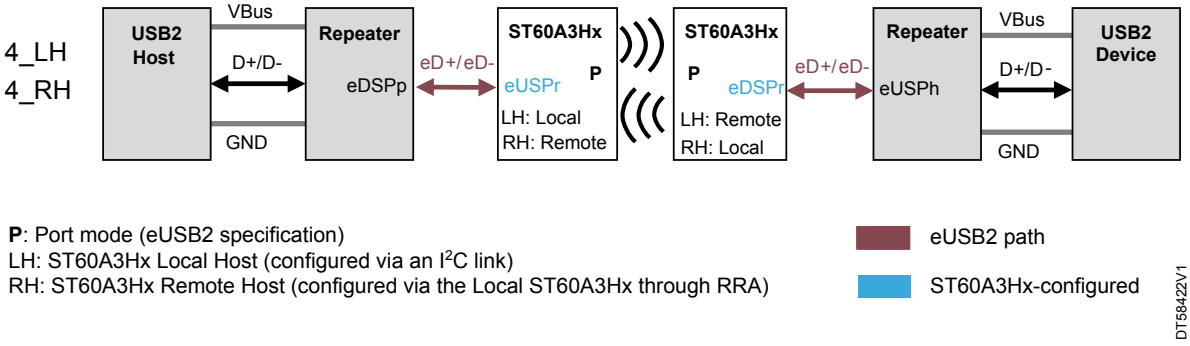
Based on the eUSB2 specification [1], a few aspects of the Hybrid Repeater setup that are worth noting are mentioned here: The ST60A3H1 is configured to support the Hybrid Repeater configuration 4, shown below with ST60A3H1 eUSB2 mode (Port only) and eUSB2 port type (eUSPr or eDSPr).

The ST60A3H1 can have two different roles:

- Local Host configured with an I²C configuration bus
- Remote Host configured over the air from the Local ST60A3H1.

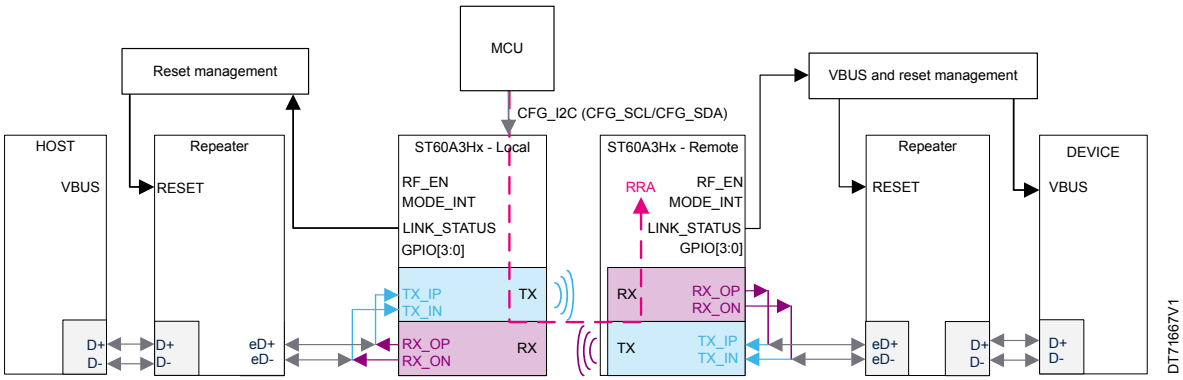
This leads to the two possible configurations 4 (4_LH and 4_RH) presented in Figure 5.

Figure 5. eUSB2 Hybrid Repeater configurations



A typical connection scenario for ST60A3H1 devices configured as an eUSB2 Hybrid Repeater is shown in Figure 6.

Figure 6. ST60A3H1 eUSB2 4_LH configuration



The main characteristics of the ST60A3H1 eUSB2 implementation are:

- A single ST60A3H1 pair is needed to implement the full eUSB2 channel.
- The ST60A3H1 supports connections to the two eUSB2 port types (eUSPr and eDSPr) as shown in the two possible configurations of Figure 5. eUSB2 Hybrid Repeater configurations.
- The ST60A3H1 implements the 1.2 V Low Speed / Full Speed DC specifications of eUSB2 release 1.1, Table 7-13, setting the supply voltage for eD+ / eD- at a nominal 1.2 V.

The electrical parameters of the High Speed I/Os are provided in Section 5: Electrical characteristics.

As part of a USB2 chain, the ST60A3H1 shows some limitations which may impact the USB2 compliance of the chain. A USB2 system that includes the ST60A3H1 must address these limitations if a USB2 certification is required. See the ST60A3H1 device errata [4] for more detailed information.

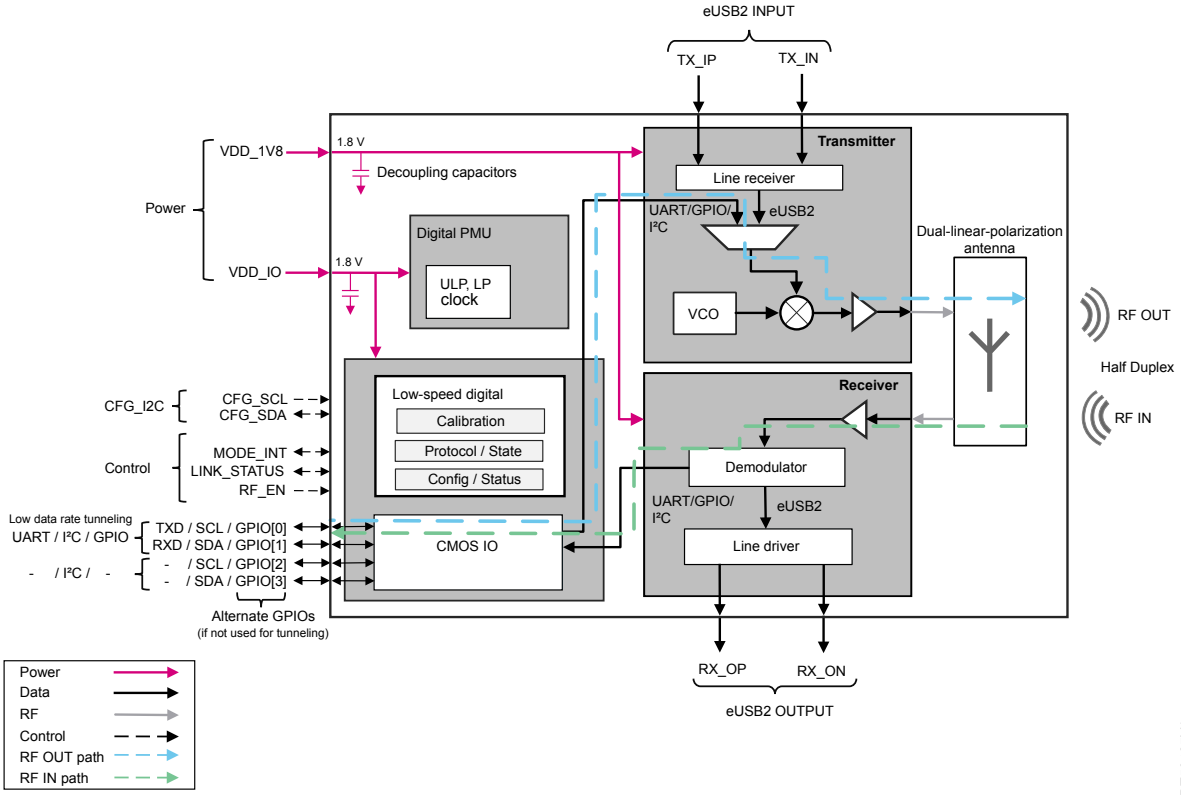
2.3 UART tunneling

All UART tunneling configurations rely on the use of CMOS I/Os: GPIO[0] for TXD and GPIO[1] for RXD. The associated logic levels are 0-1.8 V.

Two operating modes are available: Ultralow power (ULP) and Low power (LP). The ULP mode, while offering the lowest power consumption, is limited to a UART maximum data rate of 115200 bit/s, the LP mode supports data rates higher than 115200 bit/s.

The data path is shown in Figure 7. GPIO[2] and GPIO[3] that are not used for UART tunneling can be used as alternate GPIOs.

Figure 7. Data path in UART tunneling configurations

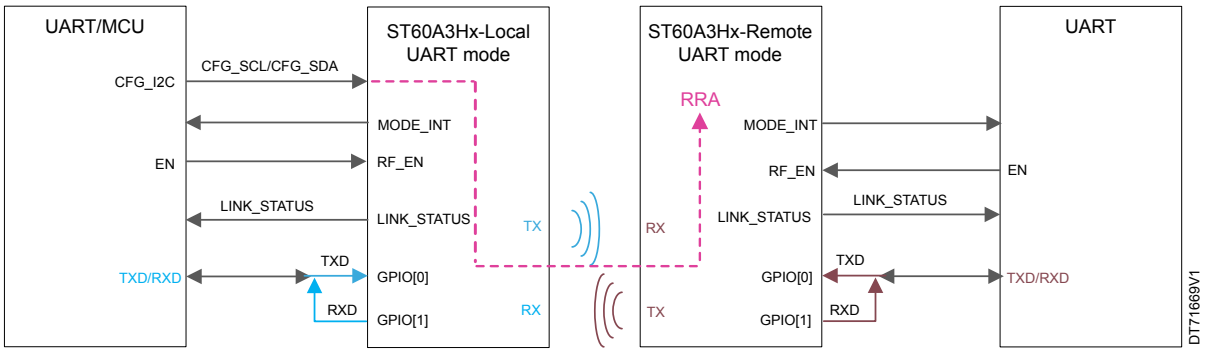


2.3.1 Half-Duplex UART

Half-Duplex UART tunneling allows UART communication supported by a Half-Duplex RF channel:

- RXD and TXD may be connected as shown in Figure 8. In such cases, RXD drive is open drain and relies on external pull-up resistor.
- It is the application responsibility to ensure that data flow is Half-Duplex.
- Data rate is limited to 6 Mbit/s in LP mode and 115200 bit/s in ULP mode.

Figure 8. ST60A3H1 Half-Duplex UART configuration



Note:

- *The Local ST60A3H1 is configured via an I²C link*
- *The Remote ST60A3H1 is configured via the Local ST60A3H1 through RRA.*

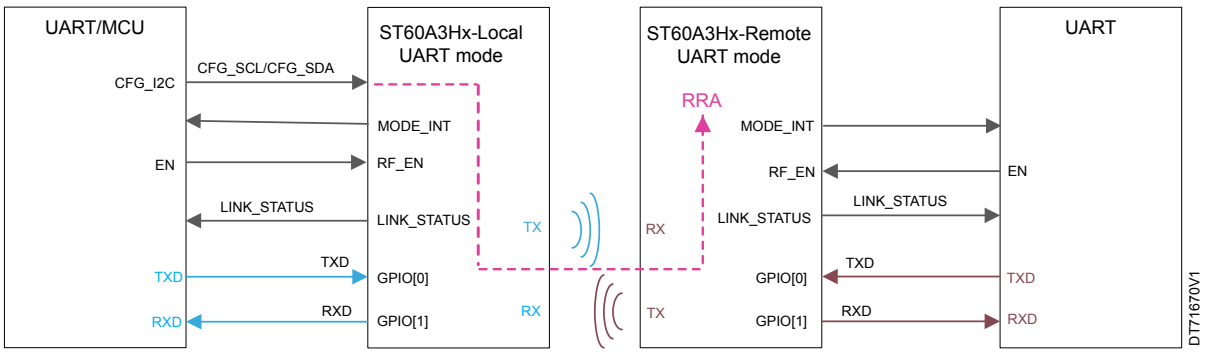
2.3.2 Full-Duplex UART

Full-Duplex UART (*dual simplex* is more appropriate) has the following main features:

- Two GPIOs are transferred in opposite directions, offering the direct possibility to plug to a 2-wire UART interface.
- Data rate is limited to 2.4 Mbit/s in LP mode and 115200 bit/s in ULP mode.

Note: In this setting GPIO[0] is always configured as input (hence connected to the TXD port of a UART interface) and GPIO[1] as output (hence connected to an RXD port of the UART interface). Their roles cannot be switched.

Figure 9. ST60A3H1 Full-Duplex UART configuration



Note:

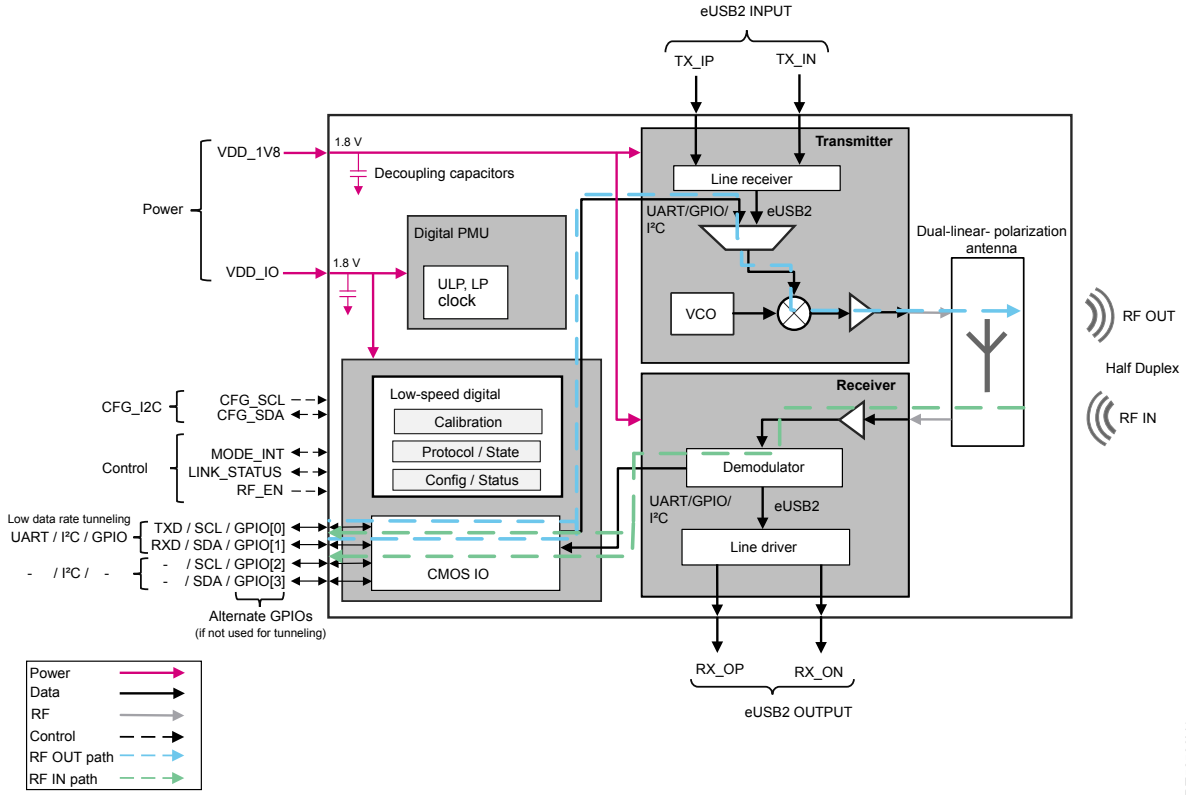
- *The Local ST60A3H1 is configured via an I²C link*
- *The Remote ST60A3H1 is configured via the Local ST60A3H1 through RRA.*

2.4 GPIO tunneling

The ST60A3H1 can be configured to tunnel one or two GPIOs over the RF channel. GPIO[0] and GPIO[1] are used for this purpose.

The data path is shown in Figure 10. GPIO[2] and GPIO[3] that are not used for GPIO tunneling can be used as alternate GPIOs.

Figure 10. Data path in GPIO tunneling configurations



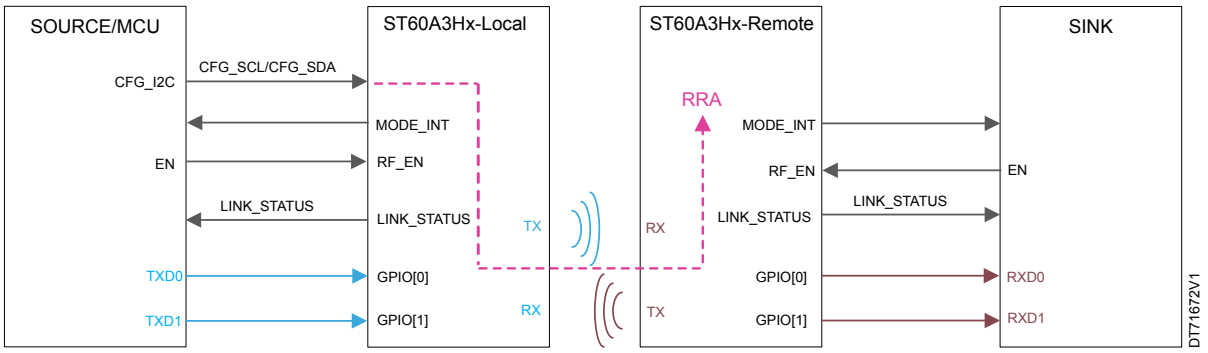
2.4.1 Single-direction GPIO tunneling

Single-direction GPIO tunneling allows data transfer through two GPIOs ***in the same direction***, as shown in Figure 11. Some differences between this configuration and the other GPIO tunneling modes are listed below:

- Up to two GPIOs can be transferred (in the same direction).
- Data modulation is optimized leading to a power-efficient solution.
- Only the LP mode is supported. The ULP mode is not available.
- There is no preferred default value, although 1 is the value at power-up reset.

The maximum data rate depends on the number of GPIOs being transferred, and whether the traffic is balanced or unbalanced in the case of two GPIOs. See Table 24. Link parameters for GPIO tunneling.

Figure 11. ST60A3H1 single-direction GPIO configuration



Note:

- *The source of the GPIO link is shown here on the ST60A3H1 Local side, though it could also be on the ST60A3H1 Remote side.*
- *The Local ST60A3H1 is configured via an I²C link.*
- *The Remote ST60A3H1 is configured via the Local ST60A3H1 through RRA.*

2.4.2 Bidirectional GPIO tunneling

LP and ULP bidirectional GPIO tunneling configurations are identical to LP and ULP Full-Duplex UART. See Section 2.3.2: Full-Duplex UART.

2.5 I²C tunneling

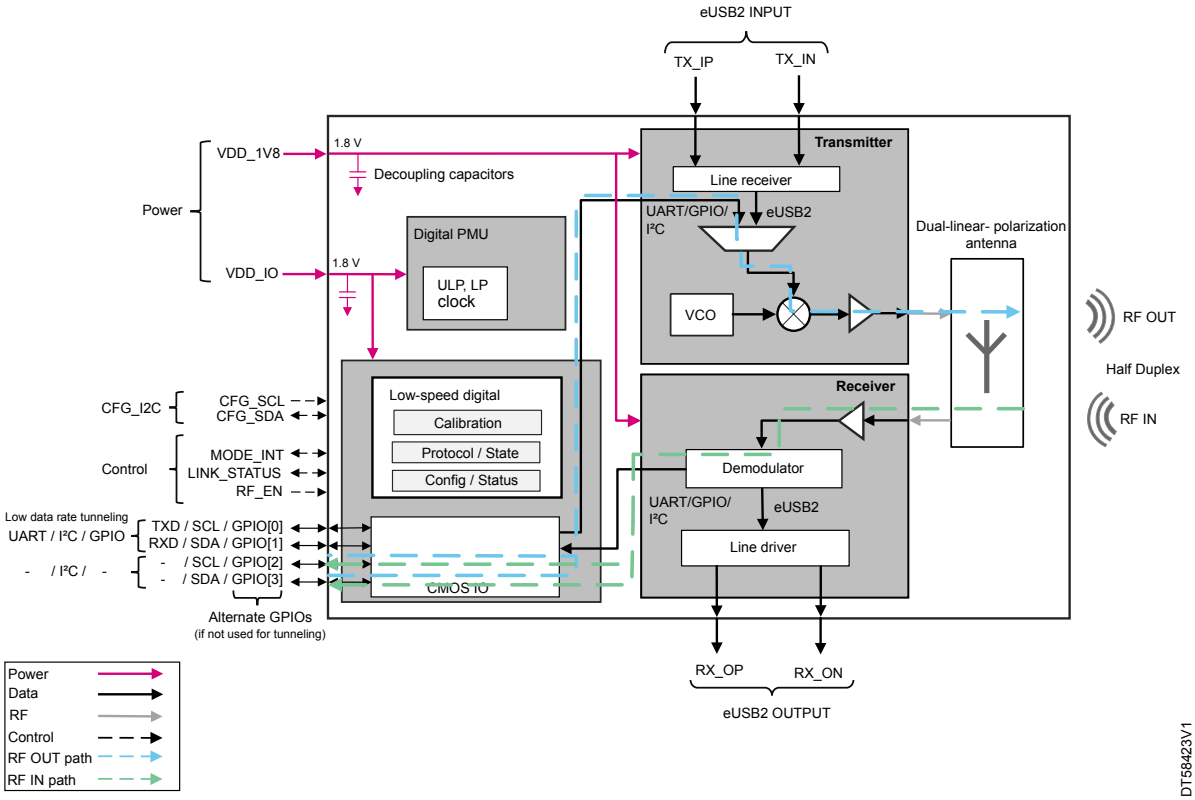
The ST60A3H1 can be configured to tunnel an I²C bus over the RF channel. This must not be confused with the I²C configuration port, which is used to configure the device, and under certain considerations, the partner ST60A3H1 device.

I²C tunneling wired interface can be multiplexed onto GPIO[0] and GPIO[1], or GPIO[2] and GPIO[3]. Note that it is possible to carry out the tunneling on GPIO[0] and GPIO[1] on one of the two devices, and on GPIO[2] and GPIO[3] on the other.

The data path is shown in Figure 12. The two GPIOs that are not used for I²C tunneling can be used as alternate GPIOs.

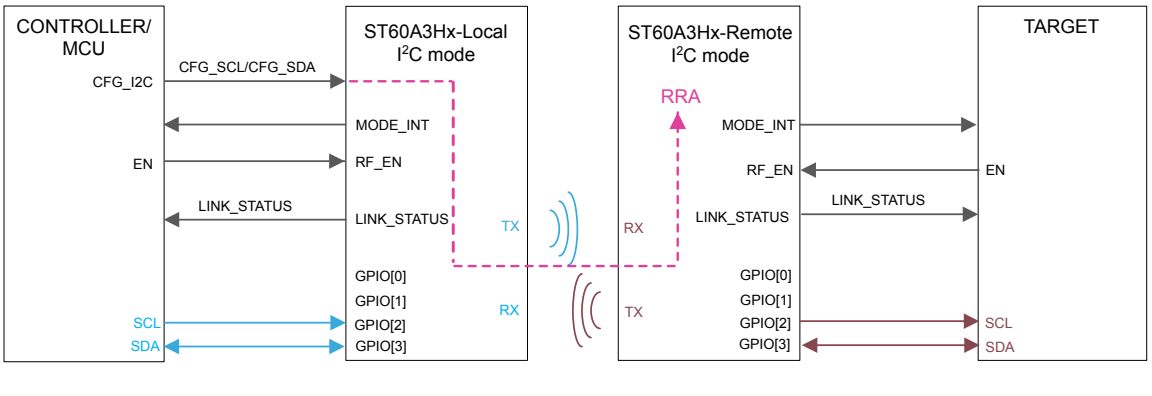
Note: Figure 12. Data path in I²C tunneling configurations and Figure 13. ST60A3H1 I²C configuration show typical configurations with GPIO[2] and GPIO[3] being selected on both devices.

Figure 12. Data path in I²C tunneling configurations



A typical configuration (Local as I²C controller) is shown in Figure 13.

Figure 13. ST60A3H1 I²C configuration



Note:

- *The Local ST60A3H1 is configured via an I²C link*
- *The Remote ST60A3H1 is configured via the Local ST60A3H1 through RRA.*

The main features of the ST60A3H1 in I²C tunneling configuration are:

- A single pair of ST60A3H1 devices implement the I²C tunnel
- Supported I²C bus speeds: Standard mode, Fast mode, and Fast mode plus at 1 Mbit/s
- 7 and 10-bit addresses
- Supports repeated start condition
- Single controller to multiple target connections:
  - The ST60A3H1 connected to the I²C controller supports a unique controller.
  - The ST60A3H1 connected to the target side can support several devices.
- The target peripheral connected to the ST60A3H1 is not allowed to stretch the clock, regardless of the bus speed.

2.6 System control and functional input/outputs

2.6.1 I/O multiplexing

The ST60A3H1 input/output multiplexing depends on the protocol in use. There can be up to four configurable alternate GPIOs identified as ALT in the Table 3. Functional I/O multiplexing. Configurable GPIOs are detailed in Section 2.6.2: Alternate GPIOs.

Table 3 lists the multiplexing of each I/O per protocol. The detailed usage of each and every implemented protocol is detailed in dedicated chapters.

Table 3. Functional I/O multiplexing

Tunneling mode	CFG_SCL	CFG_SDA	GPIO[0]	GPIO[1]	GPIO[2]	GPIO[3]	MODE_INT	LINK_STATUS	RF_EN	TX_IN, TX_IP	RX_ON, RX_OP
eUSB2	CFG_SCL(1)	CFG_SDA(1)	ALT[0](2)	ALT[1](2)	ALT[2](2)	ALT[3](2)	Interrupt	RF link status	0: OFF 1: ON	Diff and SE I/Os(3)	
UART			TXD	RXD	ALT[2](2)	ALT[3](2)				-	-
GPIO			GPIO[0]	GPIO[1]	ALT[2](2)	ALT[3](2)				-	-
I²C			SCL	SDA	ALT[2](2)	ALT[3](2)				-	-
I²C with alternate pins(4)			ALT[0](2)	ALT[1](2)	SCL	SDA				-	-

1. *Pull-up resistors must be provided externally on the I²C bus.*
2. *ALT indicates a GPIO usable for applicative purpose and configurable through I²C and OTA interface.*
3. *Differential and single-ended I/Os.*
4. *I²C tunneling can be directed to GPIO[0] and GPIO[1], or GPIO[2] and GPIO[3]. Pull-up resistors must be provided externally on the I²C tunneled bus.*

2.6.2 Alternate GPIOs

The function of each alternate GPIO is determined by register programming either through the programming interface, or through Remote programming via RRA.

Alternate GPIOs can be configured as input or output.

GPIO[2] and GPIO[3] are software controllable in all operating and configuration modes but I^2C mode with alternate pins (see Section 2.6.1: I/O multiplexing).

When not used by the functional mode, GPIOs are controlled through configuration registers.

When used by the tunneling protocol, GPIOs are directly driven by the ST60A3H1 state machine. Upon leaving the tunneling mode, GPIOs revert to the state defined by their configuration.

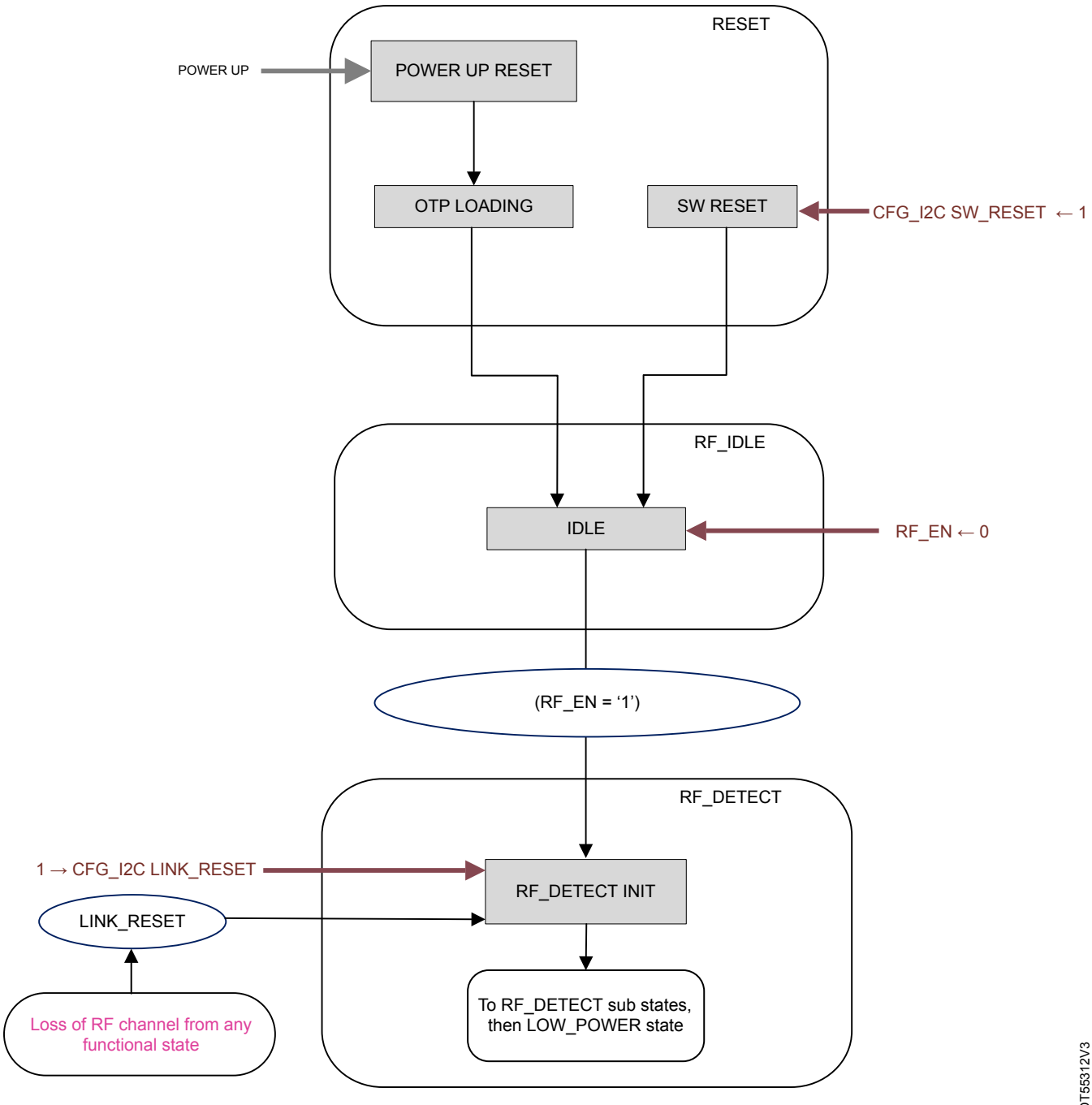
2.7 Resets

The ST60A3H1 has several reset levels in order to adapt to different application constraints and needs. The reset levels are as follows:

- Power-up or cold reset
- SW Reset (or warm reset) through register programming
- Entry into RF_IDLE state through pin RF_EN
- Link reset through register programming or RF loss

The various reset levels are detailed in the following subsections and summarized in Figure 14.

Figure 14. **ST60A3H1 reset levels**



2.7.1 Power-up or cold reset

Power-up reset (also referred to as cold reset), is the most comprehensive reset function. It configures the ST60A3H1 through the following steps:

1. Power supply is applied.
2. All registers are reset.
3. OTP memory is read back and loaded into nonresettable registers (shadow registers).
4. Register initialization.

2.7.1.1 *Supplies*

The two supplies VDD_1V8 and VDD_IO **must be tied together** on the application board.

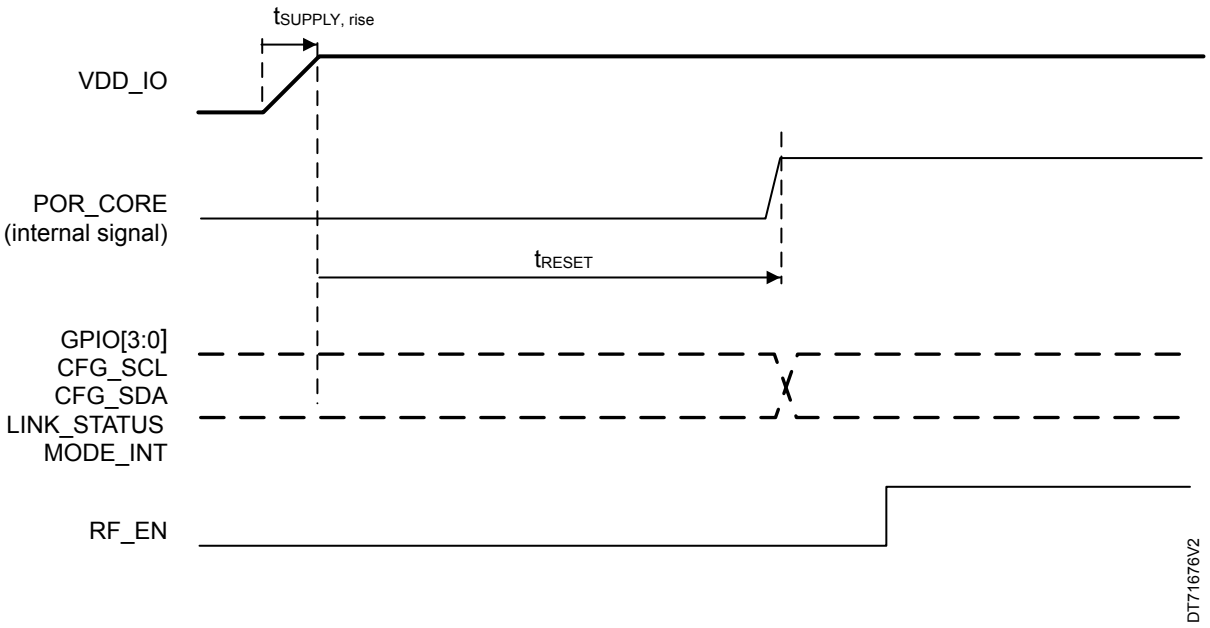
Power on triggers an internal reset after t_{RESET}. Power shutdown also triggers an internal reset. VDD_IO (or respectively VDD_1V8 since tied together) rising ($t_{SUPPLY, rise}$) and falling ($t_{SUPPLY, fall}$) must respect minimum and maximum timings, defined in Table 8. Reset, ThS and magnetic flux.

The I²C configuration interface, as well as the other I/Os except RF_EN, can be accessed at least t_{RESET} after VDD_IO has settled (see Figure 15).

The RF_EN pin is a switch that activates (or disables) the RF link. By default, its pull-up resistor feature is enabled after reset. It is described in Section 2.7.3: Entry into RF_IDLE state and can be raised t_{RESET} after VDD_IO has settled (unless it is tied to VDD_IO, see next).

Some applications require that the device remains always active. Such a requirement is fulfilled by ensuring that the RF_EN pin is tied to VDD_IO.

Figure 15. Power on reset and I/Os access



2.7.1.2 *OTP*

At power up, the OTP memory is read-back and loaded into shadow registers.

2.7.1.3 *Power-up reset*

All digital I/Os, including LINK_STATUS, are configured as input pins at power-up (refer to the note related to the LINK_STATUS pin in Section 2.8.3.3: LINK_STATUS – entry into LOW_POWER state).

In the absence of physical connections to digital I/Os on the application board, in other words, if any of the pins are left unconnected, internal pull-up and pull-down resistors ensure that the ST60A3H1 boots in a default configuration (see Table 4. Default configuration).

Table 4. Default configuration

Configuration	CFG_SCL	CFG_SDA	GPIO[0]	GPIO[1]	GPIO[2]	GPIO[3]	MODE_INT	LINK_STATUS
Default(1)	1	1	1	1	1	1	0	0

1. *Configuration with all '1' is forbidden.*

After power-up (cold) reset, the ST60A3H1 boots by default into the following configuration mode:

- Remote role
- Passive detection in RF_DETECT state

For a Local role with Full detection, the ST60A3H1 must be reconfigured while in RF_IDLE state.

2.7.1.4 *Register initialization*

On exiting cold reset, most registers are initialized to their reset value, others are initialized from shadow registers loaded from OTP.

Note: Software reset behaves similarly in this respect.

2.7.2 Software reset

The ST60A3H1 can be reset without having to perform a power-down/power-up cycle. This is referred to as *warm* or *software reset* (SW_RESET).

A software (or warm) reset can only be triggered through the I²C configuration interface. All state machines and configuration registers are reset to their default values. A software reset does not reload the content of the OTP memory (shadow registers are not reset). All other registers are reinitialized. As a result, the ST60A3H1 is reset to its default configuration mode: Remote role with Passive detection.

The software reset is triggered after the I²C transaction has completed to avoid I²C interface deadlocks.

Note: The application must not send any transaction on the I^2C configuration interface for 80 µs after a SW_RESET.

2.7.3 Entry into RF_IDLE state

RF_IDLE state is entered either from a power-up or software reset, or after setting the RF_EN pin low.

Entering RF_IDLE terminates the RF link, if any, and resets any ongoing tunneling state machine. In RF_IDLE state the I²C configuration interface is available, but no over-the-air (OTA) accesses are possible since the RF channel is disabled.

RF_IDLE state exits when the RF_EN is set high.

For devices wired as always-active (see Section 2.7.1.1: Supplies), RF_IDLE state is simply a transition state coming from power-up or software reset that is exited immediately.

Entering RF_IDLE by toggling RF_EN low resets some of the registers and forces LINK_STATUS low.

Note:

1. *If RF_IDLE state is entered by toggling RF_EN low, a wait window of at least SLEEP_TIMER time must be inserted before the next rising edge of RF_EN to ensure that RF_EN = 0 is sampled outside of any potential SLEEP phase.*
2. *The RF_EN pin has an internal pull-up resistor enabled by default. For optimal power consumption in RF_IDLE state, which is the lowest power state available when RF_EN is driven low, the pull-up resistor must be disabled through register programming.*

2.7.4 Link reset

An *RF link reset* resets all internal state machines and the corresponding status registers without affecting any configuration registers.

There are two ways to achieve an RF link reset:

- **With control registers**. This can be done in LOW_POWER or TUNNELING states. This must be done by precisely following the procedure below:
  1. Disable SLEEP_TIMER
  2. Wait (SLEEP_TIMER + 1) x 12 ms
  3. Issue the LINK_RESET
  4. Enable SLEEP_TIMER
- **Broken RF link**. The ST60A3H1 periodically checks the RF link integrity when the device is in LOW_POWER state and during idle periods in TUNNELING state. A breach in the RF connection triggers the devices to re-initialize the RF link.

Whenever a link reset occurs, the interrupt signal, EVT_LINK_DISABLED, goes high and the LINK_STATUS output pin is driven low.

Note: A SW LINK_RESET applied outside of LOW_POWER or TUNNELING states delays the effect of LINK_RESET until entry into LOW_POWER state. For instance, a LINK_RESET command while in RF_IDLE state is delayed until after RF_DETECT has completed. A new entry into RF_DETECT state then takes place.

2.8 Finite state machine

The ST60A3H1 main state machine consists of the following states:

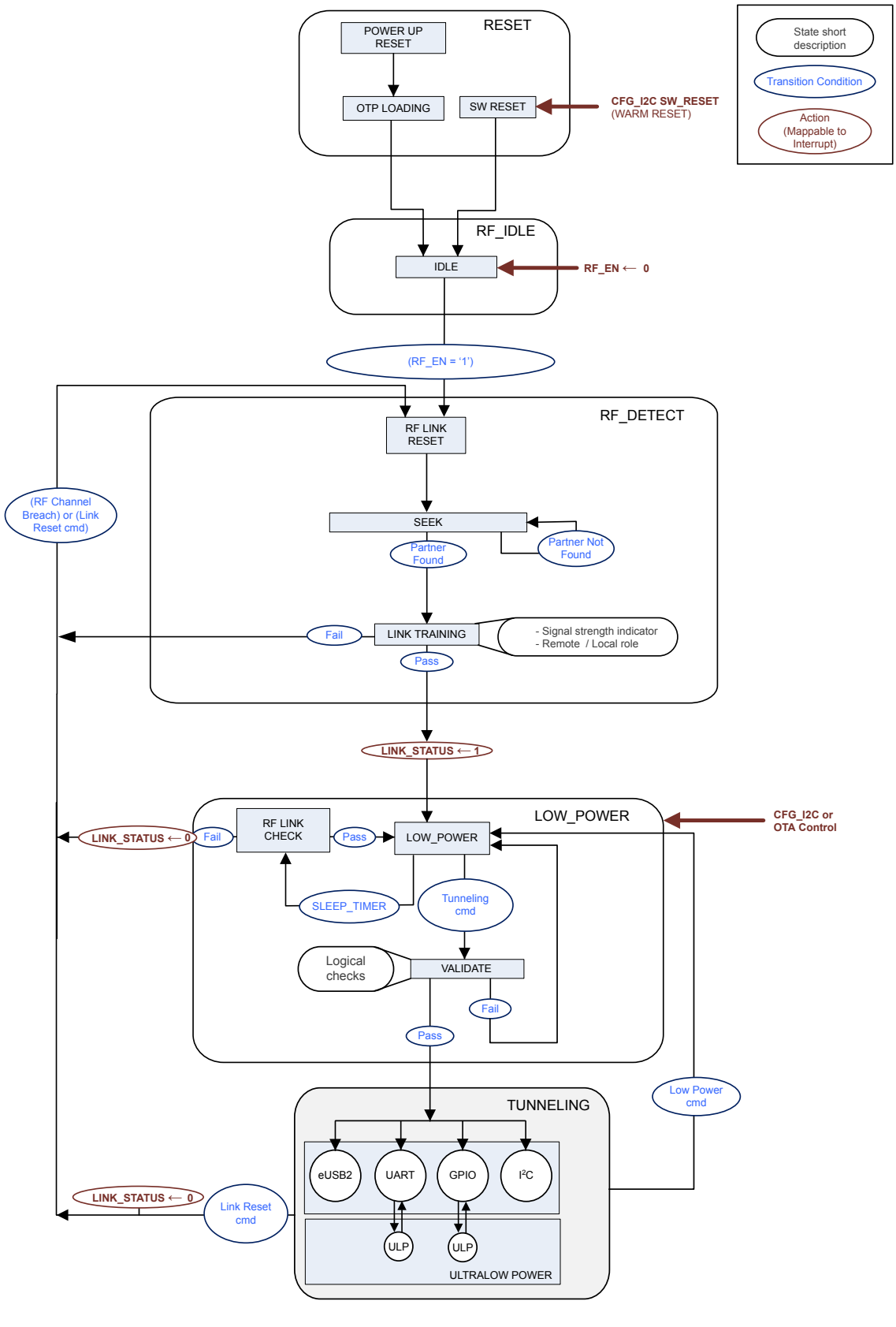
- RESET
- RF_IDLE
- RF_DETECT
- LOW_POWER
- TUNNELING states (one per supported protocol)

RESET is described in Section 2.7: Resets.

TUNNELING states are described in the sections dedicated to tunneling modes.

The state machine diagram is detailed in Figure 16.

Figure 16. **ST60A3H1 state machine**



2.8.1 RESET state

See Section 2.7: Resets for a complete description.

2.8.2 RF_IDLE state

RF_IDLE state serves the following purpose:

- The ST60A3H1 registers are fully accessible for their respective supported mode (read only, read/write or write only).
- It can be skipped by ensuring that the RF_EN pin is tied to VDD_IO (always active device). This is however an option only available for a Remote device. For a Local device, RF_EN must be controlled for configuration purposes.
- All states eventually return to RF_IDLE state when RF_EN = 0.
- Power consumption is very limited as all analog and RF blocks are disabled. Optimal power consumption is obtained by disabling the pull-up resistor on the RF_EN pin through register programming.

The transition from RF_IDLE to RF_DETECT state is ensured by setting RF_EN = 1. Refer to Section 2.7.3: Entry into RF_IDLE state for details on the RF_EN pin.

2.8.3 RF_DETECT state

RF_DETECT phases are the following:

- RF LINK RESET
  - All internal state machines are reset. Configuration registers, and possible error reports are kept unchanged.
  - If RF_DETECT is re-entered after an error such as loss of RF link, insufficient RF link quality or an error during a previous pairing attempt, the RF detection procedure is repeated indefinitely.
- SEEK
  - This is the actual power optimized search for an RF partner (see Section 2.8.3.1: SEEK phase)
  - The SEEK state loops until an RF partner has been found.
- LINK TRAINING
  - Once an RF partner has been found, LINK TRAINING is entered for optimal RF link budget.
  - The two RF partners exchange internal configuration parameters such as Remote or Local role.
  - This phase can lead to an aborted connection.

LINK_STATUS is raised on exiting RF_DETECT and entering LOW_POWER state. EVT_LINK_ENABLED replicates LINK_STATUS (see Section 3: Interrupts and errors).

2.8.3.1 SEEK phase

This section describes the procedure implemented by the ST60A3H1 when searching for an RF partner.

The schemes implemented by the ST60A3H1 for the initial discovery aim at achieving the best power consumption / connection time compromise. Whenever possible most parts of the device are switched off outside specific periods. The parameters driving the initial discovery are configurable with default values such that the average consumption during the detection phase is around a few tens of µA and the average detection time is in the order of 0.5 seconds.

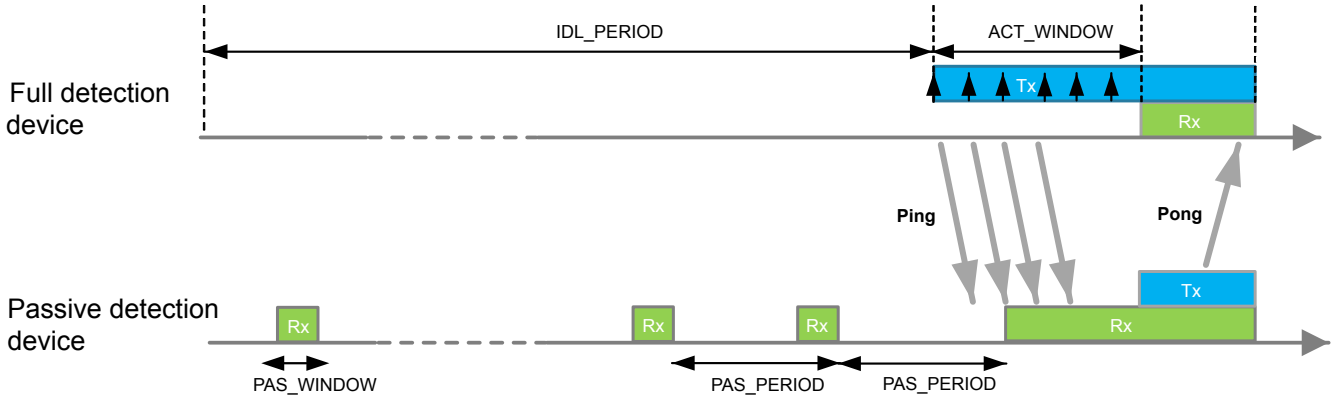
There are two ways of performing initial discovery in RF_DETECT state:

- Full detection
- Passive detection

Pairing is only possible with one device in Full Detection and the other in Passive Detection. The Passive detection is selected by default for a Remote device at power-up reset. For a Local device with Full detection, the ST60A3H1 must be reconfigured (see Section 2.7.1.3: Power-up reset).

The initial discovery is based on periodic time frames, with the aim of switching off all possible parts of the devices outside active seeking periods.

Figure 17. **Full and Passive detections**



IDL_PERIOD: Window during which no active detection takes place
ACT_WINDOW: Activity window during which Full detection device pings candidate partners
PAS_WINDOW: Window during which Passive detection device seeks for candidate partners
PAS_PERIOD: Periodicity of passive search

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Full detection

In Full detection, the ST60A3H1 alternates idle periods and active seeking periods.

During idle periods, the device cannot detect a potential RF partner. During active seeking periods, the device periodically transmits messages and listens for the possible reply of a detected RF partner at the end of the period.

- Idle periods:
  - This phase covers a time window defined as the IDL_PERIOD (1000 ms).
- Active periods:
  - The ST60A3H1 sends periodic ping messages for relatively long periods referred to as the ACT_WINDOW (125 ms).
  - The prospective partner is informed of the end of the active period. In the case of a hit, the newly found partner acknowledges the detection (pong message).

The periodicity of the Full detection scheme is equal to IDL_PERIOD + ACT_WINDOW.

Passive detection

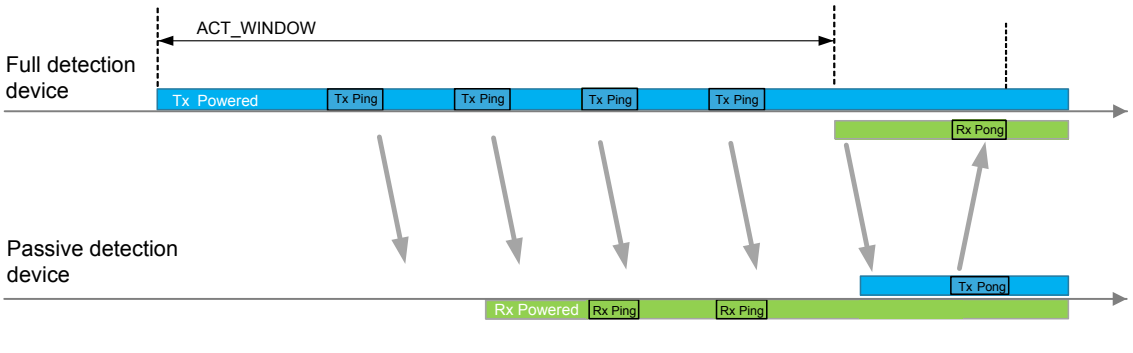
In Passive detection, the ST60A3H1 periodically turns on the RF Receiver path to detect a potential RF partner.

- Eavesdropping periods:
  - Rx is briefly turned on for a duration PAS_WINDOW (4 µs). Rx activity is repeated with a period corresponding to PAS_PERIOD (100 ms). PAS_PERIOD is set to a slightly smaller value than ACT_WINDOW to ensure that the active and eavesdropping intervals overlap.
  - If a partner is detected, the ST60A3H1 acknowledges the detection.

The ST60A3H1 is not allowed to send any ping messages. It only eavesdrops potential connecting partners and acknowledges when found. This allows for an extremely power efficient solution, provided the application ensures that the potential partner is set for Full detection.

A close-up view of the active window and actual pairing is shown in Figure 18.

Figure 18. Close-up view of pairing phase



2.8.3.1.1 Power consumption and detection time

For a given average detection time, the power consumption optimization is a tradeoff to limit the consumption of the Passive detection device, while limiting the adverse effect on the consumption of the Full detection device. This is achieved by balancing the power consumption due to activity periods (PAS_WINDOW) and idle periods (PAS_PERIOD - PAS_WINDOW) in the Passive detection device. This may be appropriate if one of the two devices has more stringent battery constraints than the other.

2.8.3.2 LINK TRAINING phase

2.8.3.2.1 Signal strength indicator

The link training phase optimizes the internal parameters of the internal receiver parameters of the two partners, with respect to the actual transmitted power and RF path loss.

Its duration is limited and expected to remain less than 200 µs.

The outcome of this phase provides an estimation of the power of the received signal, more commonly called the received signal strength indicator (RSSI). If the signal level is too small, an RSSI_ERROR interrupt is set.

Note: Insufficient signal strength during this phase may lead the communication to fail, trigger a link reset and report an RF_DETECT_ERROR.

2.8.3.2.2 Output-power temperature compensation

Link training is carried out without accounting for the actual temperature and effects on the transmitted power. When link training takes place near the limit of the operating temperature range and temperature compensation of the output power is disabled in LOW_POWER or TUNNELING states, the optimization of the receiver parameters becomes insufficiently accurate to guarantee a correct jitter and BER. To overcome this issue, the following actions must be performed (see also Section 2.10: Temperature compensation):

- Enable the output-power temperature compensation in LOW_POWER
- Before entering TUNNELING, force a LINK_RESET
- Enter TUNNELING after returning to LOW_POWER.

2.8.3.2.3 Logical checks

During the link training phase, the two ST60A3H1 devices exchange the contents of a few configuration registers to inform them of their partner's status and capability. This information embeds the control for over-the-air (OTA) transfers, also referred to as Remote or Local role.

This phase may fail in the case of conflict over the mastership of the OTA link, thus leading to RF_LINK reset and ERROR report (see Section 3: Interrupts and errors).

2.8.3.3 LINK_STATUS – entry into LOW_POWER state

Once the two partners have established the RF link, a dedicated status bit is set and the LINK_STATUS pin is raised. The link is considered up-and-ready when:

- Two partners have identified each other as a result of SEEK phase
- LINK TRAINING phase has completed successfully
- The two partners have informed each other of their role (Local, Remote) in the OTA connection, and found no incompatibility.

Two devices with the same role (two Local or two Remote devices) report an error.

Until an active tunneling mode is entered, the RF link mastership role is held by the device set for Full detection, the other device being set for Passive detection.

LINK_STATUS remains high until a disconnection is forced or detected. Nevertheless, the RF link may be breached some time before the ST60A3H1 becomes aware that the link is broken. Disconnection detection occurs:

- When failing to resume the link upon waking-up from a low power state
- When failing to receive an acknowledgement of the RF partner at intervals specified by the protocol in use in low power states (RF LINK CHECK in LOW_POWER state for instance – see Figure 16. ST60A3H1 state machine).
- When directed to disconnect by the protocol in use
- When directed to disconnect by means of the control interface (RF_EN)
- On forced LINK_RESET or SW_RESET (warm reset) through the I²C configuration interface

Successful entry into LOW_POWER state raises EVT_LOW_POWER.

LINK_STATUS de-assertion due to loss of RF signal

In RF_DETECT state, there are several retries during pairing. These retries do not affect LINK_STATUS, because LINK_STATUS remains low until the FSM reaches the LOW_POWER state.

In LOW_POWER state, LINK_STATUS is de-asserted after a maximum of SLEEP_TIMER + WATCHDOG_TIMER.

In TUNNELING state, LINK_STATUS is de-asserted after a period that depends on the implemented protocol. This is explained in Section 2.9: Sleep timer, Watchdog timer, and high-level Watchdog timer.

Note: LINK_STATUS defaults to an input pin with a weak pull-down at reset (see Section 2.7.1: Power-up or cold reset). After reset, and until an RF link is established, it is actively driven low. It is actively driven high when exiting RF_DETECT and entering LOW_POWER state. It remains high as long as the RF link is alive.

2.8.4 LOW_POWER state

LOW_POWER is the central state once an RF channel has been set, and is the entry point into any of the tunneling modes that the application supports.

LOW_POWER is particularly suitable for:

- Reading from and writing to registers of the Remote partner Over-The-Air, a feature referred to as Remote register access (RRA);
- Configuring and entering the tunneling mode.

These two important features are described respectively in Section 2.8.4.1: Over-the-air remote register access (RRA) and Section 2.8.4.5: Entry into TUNNELING state.

When no activity is required due to an RRA or a pending command to enter a tunneling mode, the RF channel enters a SLEEP sub-state with extremely efficient power consumption. The entry into SLEEP and WAKE-UP are also described in Section 2.8.4.2: SLEEP, WAKE-UP and HOUSEKEEPING phases.

2.8.4.1 Over-the-air remote register access (RRA)

It is possible to read and write the registers of the Remote RF partner over the RF link.

After partnering has occurred with another ST60A3H1, the two partnered devices exchange messages across the RF link. The messaging service also allows write or read requests to be pushed across the RF, so that the registers of the RF partner can be remotely read from and written to. RRA accesses are limited to LOW_POWER state.

In practice, write operations are performed by pushing an 8-bit address and an 8-bit data across the RF link. Read operations are performed indirectly: the requester pushes an 8-bit address across the RF and the partner ST60A3H1 replies by pushing back the 8-bit data. The software checks the completion of a write or read request by reading a Local status bit (REMOTE_BUSY, which can be mapped to EVT_RMT_DONE and can generate an interrupt – note that REMOTE_BUSY and EVT_RMT_DONE toggle on the Local device only).

The application must ensure that REMOTE_BUSY has gone low before attempting a new Remote write access. A new Remote write access while REMOTE_BUSY is high, is ignored.

Accessing register OTA opens up the following possibilities:

- Software can control the GPIO of a Remote ST60A3H1 by writing to / reading from the Remote registers controlling the GPIOs.
- Software can communicate with a Remote partner by writing to / reading from any of the eight notepad registers for any application specific purpose.
- More generally, software can control most parameters of the Remote device.

Read and write accesses to notepad registers are signaled by EVT_NOTEPAD_RD and EVT_NOTEPAD_WR respectively (see also Section 2.8.4.1.1: Interrupts and RRA).

Note:
1. *If SLEEP is enabled when an RRA access is requested, REMOTE_BUSY could remain high for SLEEP_TIMER time plus the amount of time to complete the RRA.*
2. *In the unlikely event that OTA access does not complete properly due to a loss of the RF channel, the ST60A3H1 automatically triggers a LINK_RESET.*

2.8.4.1.1 Interrupts and RRA

As already mentioned, the completion of an RRA transaction initiated over the I^2C interface on the Local device triggers EVT_RMT_DONE interrupt.

Read RRAs also raise an EVT_NOTEPAD_RD interrupt. If this event is not desired, there are two ways to circumvent the interrupt:

- If EVT_NOTEPAD_RD on the Local side is never checked by the application, it is possible to mask EVT_NOTEPAD_RD.
- If EVT_NOTEPAD_RD on the Local side is used by the application, the sequence of operations required for an RRA read can be modified with the objective of temporarily disabling EVT_NOTEPAD_RD.

2.8.4.1.2 Locally only accessible registers

Some registers exposing critical information are not readable by RRA.

Note: RRA read of such a register returns an erroneous value.

2.8.4.1.3 RRA exceptions

There are some exceptions to Remote register access:

- Locally only accessible registers as described in Section 2.8.4.1.2.
- Certain register fields should not be modified by RRA, the write being hazardous and not to be attempted.
- Some registers are dynamically updated by the FSM, therefore the read back value, whether by RRA or locally on the I^2C interface, changes over time.

2.8.4.1.4 Availability of OTA communication

Hardware-driven OTA accesses can take place during RF_DETECT (pairing phase), LOW_POWER, and TUNNELING states. The application must ensure that no concurrent register access occurs through the I^2C interface.

In normal operating conditions:

- Application-driven OTA register access is limited to LOW_POWER state
- Configuration of the Remote partner is limited to LOW_POWER state

OTA register access from the Remote device:

- The Remote device is never allowed to carry out an RRA from the I^2C configuration interface. Any attempt is ignored.

2.8.4.2 *SLEEP, WAKE-UP and HOUSEKEEPING phases*

2.8.4.2.1 SLEEP phase

In the absence of any ongoing activity over the RF channel, and provided SLEEP is enabled, the paired partners enter a SLEEP phase and thus reduce their power consumption to the bare minimum.

SLEEP is the deepest power state of the RF channel:

- All analog and RF blocks are disabled
- The low power digital clock is disabled
- An ultralow power clock (ULP Clock) and a timer are enabled

During the SLEEP phase, requests performed on the Local device through the I²C configuration interface are delayed until the device wakes-up. This concerns requests involving OTA read or writes, the tunneling command, and internal traffic ensuring integrity of the RF channel or transitions from SLEEP phase.

On entry to LOW_POWER and periodically at SLEEP_TIMER intervals while sitting in LOW_POWER, the Local device:

- Performs several pending Housekeeping tasks and expects the Remote device for the same (see Section 2.8.4.2.3: HOUSEKEEPING phase).
- OTA writes the power control register to the Remote device. This ensures coherent values of the SLEEP parameter (SLEEP enabled/disabled in LOW_POWER state).
- OTA writes SLEEP_TIMER value to the Remote device.
- Instructs the Remote device to enter SLEEP (if SLEEP is enabled).

If SLEEP is enabled, both devices reset their SLEEP_TIMER and enter SLEEP when the Remote device acknowledges the request to enter the SLEEP phase. The devices disable most of the analog and RF circuitry upon entry into SLEEP sub-state.

If SLEEP is disabled, both devices still reset their SLEEP_TIMER without effectively disabling their analog and RF circuitry. They remain idle for the duration of their respective SLEEP_TIMER. It is recommended that the desired value of the power control register be set while the Local device sits in RF_IDLE (RF_EN = 0). However updating its value is possible while the Local device already sits in LOW_POWER state.

During the SLEEP phase, LINK_STATUS remains high. LINK_STATUS goes low only if the RF link integrity engine (see Section 2.8.4.4: RF link integrity) detects a broken link.

2.8.4.2.2 WAKE-UP phase

The purpose of waking-up from SLEEP every so often is twofold:

- It reactivates the link to perform pending tasks
- It checks that the RF channel is still up and available.

On SLEEP_TIMER completion, each device wakes up independently and activates its TX and RX paths. The Local device sends ping messages while the Remote device attempts to detect ping messages and acknowledges back.

Whenever a device does not detect its RF partner within WATCHDOG_TIMER the link is declared broken, LINK_STATUS goes low and a LINK_RESET is carried out.

Due to some uncertainty between the timers of the two ends of the RF channel, the Local and Remote devices do not wake-up at the same time. This is depicted in Figure 19 and Figure 20. When a device wakes up it starts its own WATCHDOG_TIMER. If it has not resumed the connection with its partner within WATCHDOG_TIMER time, the ST60A3H1 considers that the RF Link is broken and triggers a LINK_RESET. Providing a WATCHDOG_TIMER value largely exceeding SLEEP_TIMER is recommended (defaulting respectively to 250 ms and 110 ms).

An optimization mechanism aimed at limiting the drift between the two timers, and thus optimizing the power consumption is applied (see Section 2.8.4.3: Power consumption).

Figure 19. **SLEEP and WAKE-UP phases. Local device wakes up first**

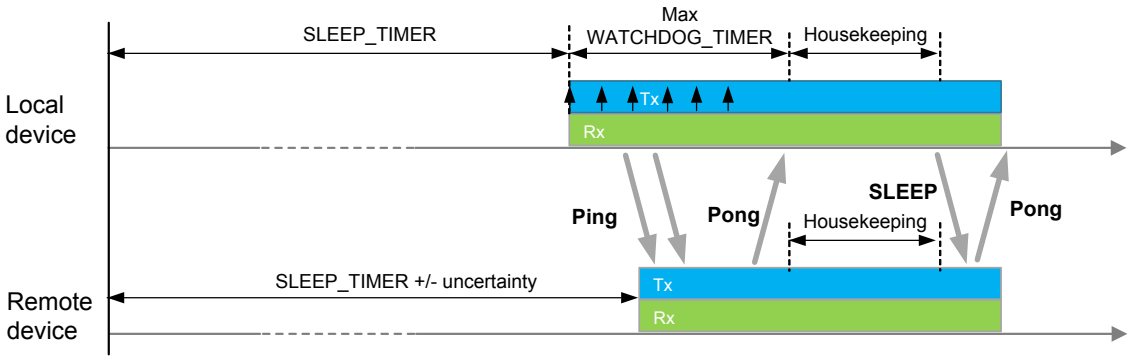
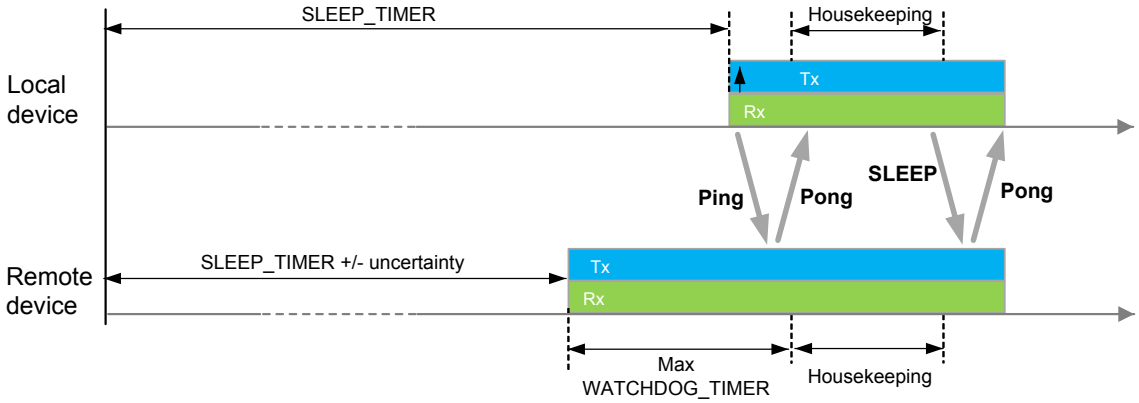


Figure 20. **SLEEP and WAKE-UP phases. Remote device wakes up first**



2.8.4.2.3 HOUSEKEEPING phase

Housekeeping tasks are:

- Pending RRA requests
- Sensing the temperature if this feature is enabled
- Handling output power temperature compensation if such tasks are enabled in LOW_POWER state.

To allow several consecutive RRA requests without risking returning to SLEEP in between each RRA, the application can disable the SLEEP feature for the duration of the RRA accesses. After the last RRA, the application must re-enable the SLEEP feature for optimal power consumption in LOW_POWER state.

Once Housekeeping tasks are completed, and only then, the Local device:

- Executes a pending tunneling command, if any
- Otherwise instructs the Remote device to return to SLEEP (if SLEEP is enabled).

2.8.4.3 *Power consumption*

The power consumption in LOW_POWER state depends on two key parameters:

- SLEEP_TIMER value
- Enabling of the temperature sensor

Clearly the device that wakes-up first consumes more than that which wakes-up last, since it must sit waiting for its partner while keeping its transmit and receive paths activated. Since it is difficult to predict which of the two partners is ready first, it makes more sense to look at the overall consumption of the two devices.

An optimization mechanism setting the emphasis on the Remote device power consumption is applied. This optimization is particularly beneficial when the SLEEP_TIMER duration has a large value of the order of 1 s or more. It optimizes the consumption of the Remote device at the slight expense of the Local device consumption.

2.8.4.4 *RF link integrity*

Two ST60A3H1 devices sitting in LOW_POWER state regularly check the integrity of the RF link. This verification is done automatically when the low power state machine is enabled and the devices periodically enter SLEEP sub-state and wake-up properly. Failing from waking up indicates a loss of the RF Channel which triggers a LINK_RESET.

The link integrity is still verified when the low power mechanism is bypassed (SLEEP disabled). The periodicity of this check is still set by the SLEEP_TIMER duration.

In order to avoid excessive occurences of LINK_RESET, the WATCHDOG_TIMER delays the effective reset of the link if no acknowledgement of a partner is detected immediately after SLEEP_TIMER duration.

2.8.4.5 *Entry into TUNNELING state*

Both ST60A3H1 devices must be programmed (Local and Remote) before entering active tunneling mode.

Programming is handled by the Local ST60A3H1.

The host connected to the Local ST60A3H1 carries out the configuration of the two devices by writing to specific registers in order to:

- Describe the tunneling configuration of the Local device:
  - The protocol that the Local partner is expected to implement
  - The role that the Local partner is expected to hold in the protocol (controller/target, source/sink, USP/DSP) including supplementary information regarding the configuration of the IC in the application
- Describe the tunneling configuration of the Remote device:
  - The protocol that the Remote partner is expected to implement
  - The role that the Remote partner is expected to hold in the protocol (controller/target, source/sink, USP/DSP) including supplementary information regarding the configuration of the IC in the application
- Trigger the tunneling command (TUNNELING_CMD). The effect of this command is to:
  - OTA copy Local configuration registers into Remote configuration registers
  - Check the validity of the configuration
  - Enter the desired TUNNELING state

Entry into TUNNELING state fails if the configurations are not compatible. This is the case in particular when protocols do not match or when directions are incompatible (such as two downstream ports connected together in eUSB2). In such a case, the two devices remain in LOW_POWER state and both trigger the interrupt EVT_LOW_POWER_ERROR.

Executing the tunneling command sets REMOTE_BUSY bit high until the command is actually executed. Completion of the command can thus be detected by interrupt if EVT_RMT_DONE is mapped as an event.

A successful entry into TUNNELING state raises EVT_TUNNELING.

2.8.5 TUNNELING state

TUNNELING state is entered from LOW_POWER state when a tunneling mode, eUSB2, UART, GPIO or I²C is activated.

See Section 2.2: eUSB2 tunneling, Section 2.3: UART tunneling, Section 2.4: GPIO tunneling, and Section 2.5: I2C tunneling for an introduction.

2.8.5.1 *RF link integrity*

In TUNNELING state, the verification of the RF link integrity depends on the protocol in use (eUSB2, UART, GPIO, or I2C).

2.8.5.2 *Return to LOW_POWER*

Returning to LOW_POWER state while in TUNNELING is achieved by:

- Ensuring there is no ongoing or upcoming traffic on the link
- Triggering the low power command (LOW_POWER_CMD) on the Local ST60A3H1

The low power command execution is delayed until the next period that the link integrity mechanism kicks in. This delay is bounded by SLEEP_TIMER duration.

Executing the low power command sets REMOTE_BUSY bit high until the command is actually executed.

It is the application's responsibility to ensure no traffic is ongoing (or if eUSB2 tunneling is active, that the link sits in SUSPEND or LS/FS idle mode) before triggering the low power command. Failing to conform to this specification may lead to unpredictable behavior.

2.9 Sleep timer, Watchdog timer, and high-level Watchdog timer

The ST60A3H1 embeds several programmable timers and watchdogs. The three main timers are the Sleep timer, the Watchdog timer (sometimes referred to as the low-level Watchdog timer) and the high-level Watchdog timer. These three timers are controlled by the SLEEP_TIMER and the WATCHDOG_TIMER.

The SLEEP_TIMER controls:

- The duration of the sleep phases in LOW_POWER state and ultralow power substates of full-duplex UART/ GPIO tunneling
- The interval at which RF link integrity is checked in LOW_POWER state, and in UART tunneling (except ULP half-duplex), GPIO tunneling or I²C tunneling

The WATCHDOG_TIMER controls:

- The time period after which a broken RF link is detected in LOW_POWER state (low-level Watchdog)
- The high-level Watchdog

Details on the usage of SLEEP_TIMER and WATCHDOG_TIMER in LOW_POWER state are provided in Section 2.9.1: Timer settings in LOW_POWER state.

2.9.1 Timer settings in LOW_POWER state

The sleep mechanism is detailed in Section 2.8.4.2: SLEEP, WAKE-UP and HOUSEKEEPING phases. For efficient power optimization, SLEEP_TIMER should be set to a relatively large value, for example 500 ms (default is 110 ms).

The low-level Watchdog timer (not be confused with the high-level Watchdog) controls the time period after which a broken RF link is detected. It is essential to ensure that WATCHDOG_TIMER is strictly higher than SLEEP_TIMER, in practice, it is highly recommended to set:

$$WATCHDOG\_TIMER > 1.2 \times SLEEP\_TIMER$$

Therefore, if SLEEP_TIMER is to be increased from its default value up to 1 s, WATCHDOG_TIMER should be increased first to follow the same ratio.

Note: SLEEP_TIMER = 500 ms, already provides good power consumption results (see Section 5.5.3: LOW_POWER parameters).

If the ST60A3H1 pair does not communicate both ways for a period of WATCHDOG_TIMER, the device triggers a LINK_RESET.

2.9.2 High-level Watchdog

The HL Watchdog is a hardware block that continuously monitors the output of the analog RF Receiver path, operating at a level above all lower level control mechanisms. The HL Watchdog relies on a counter, clocked by the ULP clock therefore always active, that is reset whenever valid activity is detected on the RF receiver path. If the HL Watchdog counter reaches its upper limit, the HL Watchdog triggers a LINK_RESET.

Note: The LINK_RESET may occur some time after the counter expiration to allow the management of interfaces and specific protocol constraints.

Internal mechanisms in LOW_POWER and TUNNELING states ensure that under normal conditions the RF link is regularly exercised. The HL Watchdog is thus a last resort mechanism to detect a broken RF link or a deadlock.

The HL Watchdog counter is initialized to zero, counting up to:

$$(WATCHDOG\_TIMER + 1) \times 8000 \text{ ULP clock cycles}$$

This corresponds to an approximate time-out duration of:

$$(WATCHDOG\_TIMER + 1) \times 80 \text{ ms}$$

The available range for time-out spans from approximately 80 ms to 20.5 s (default is 2 s).

By default, the HL Watchdog is active only when the main FSM is in the LOW_POWER and TUNNELING states but it can be disabled for debug or validation purposes.

2.9.2.1 *HL Watchdog expiration during eUSB2 tunneling*

If the HL Watchdog expires during eUSB2 tunneling:

- The high-speed I/Os are kept under the control of the eUSB2 state machine.
- If the eUSB2 line is in *connected* state, ESE1 is generated towards the Host.
- After 3 ms, LINK_RESET is asserted, interrupt signal EVT_LINK_DISABLED goes high and LINK_STATUS is driven low.

2.9.2.2 *HL Watchdog expiration during LOW_POWER state or during non-eUSB2 tunneling*

If the HL Watchdog expires during LOW_POWER state or non eUSB2 tunneling, LINK_RESET is immediately asserted, interrupt signal EVT_LINK_DISABLED goes high and LINK_STATUS is driven low.

2.10 Temperature compensation

2.10.1 Temperature sensor

In order to compensate the output power for temperature variations, the ST60A3H1 embeds a temperature sensor.

The temperature sensor is activated at regular intervals defined by TEMP_SENS_INTRVL to minimize the power consumption.

Applications that do not require any temperature sensing can disable the sensor altogether with TEMP_SENS_EN.

Table 5 lists the parameters accessible to the application that controls the temperature sensor. In practice the application must only control TEMP_SENS_EN and TEMP_SENS_INTRVL; ST60A3H1 internal state machine autonomously uses the temperature measurement for compensation.

The actual temperature in Celsius equals TEMP_DATA - 35.

Table 5. Temperature sensor control parameters

Description	Parameter	Available range
Enable / disable temperature sensing	TEMP_SENS_EN	-
Periodicity of temperature measurements in TUNNELING state	TEMP_SENS_INTRVL	4 values from 10 ms to 500 ms
Periodicity of temperature measurements in LOW_POWER state	SLEEP_TIMER(1)	-
Actual temperature in Celsius shifted by 35	TEMP_DATA	1 LSB = 1 °C +/- 1 °C accuracy at 27 °C, max +/- 3 °C at 85 °C
Measurement completion	TEMP_DATAREADY	-
Previous measurement	TEMP_DATA_PRV	-

1. *This is the normal case when SLEEP is enabled. When SLEEP is disabled, the periodicity is the minimum of SLEEP_TIMER and TEMP_SENS_INTRVL.*

2.10.2 Output-power temperature compensation

Output power varies by +/- 2 dB across the operating temperature range. Power degradation is roughly linear with increasing temperature. Compensation can be applied to overcome this power degradation.

Table 6 lists the parameters accessible to the application for output-power temperature compensation.

Table 6. Output-power temperature compensation control parameters

Description	Parameter
Enable / disable output-power temperature compensation in LOW_POWER state	PWR_TEMP_COMP_LP_EN
Enable / disable output-power temperature compensation in TUNNELING state	PWR_TEMP_COMP_TUNNEL_EN

2.10.2.1 Compensation during LOW_POWER state

This is only performed in the LOW_POWER state (as part of Housekeeping, and therefore with a periodicity dependent on SLEEP_TIMER: see Section 2.8.4.2.3) provided that PWR_TEMP_COMP_LP_EN = 1.

2.10.2.2 Compensation during TUNNELING state

This is only performed in the TUNNELING state provided that PWR_TEMP_COMP_TUNNEL_EN = 1, and is applied when the device is not communicating. Output power is adjusted at most every TEMP_SENS_INTRVL and only when the transmitter is not in use, that is:

- eUSB2: at the beginning of RX activity (start of frame) and in L2 state.
- ULP UART: when the link is idle
- All other protocols do not offer reliable opportunities to update power while in TUNNELING mode. Output-power temperature compensation can only take place in LOW_POWER state

3 Interrupts and errors

Interrupts are mapped to the MODE_INT pin.

All events and errors can be mapped onto the interrupt pin.

On a LINK_RESET, the following events are automatically cleared:

- EVT_NOTEPAD_WR
- EVT_NOTEPAD_RD (see Section 2.8.4.1.1: Interrupts and RRA)
- EVT_LINK_ENABLED
- EVT_RMT_DONE

The others are left unchanged.

Table 7. Events mappable to MODE_INT

Event name	Reported information
EVT_NOTEPAD_WR	Indicates Notepad write access
EVT_NOTEPAD_RD	Indicates Notepad read access (see Section 2.8.4.1.1: Interrupts and RRA)
EVT_LINK_ENABLED	Link is now enabled (automatically or by SW) Same logic level as LINK_STATUS
EVT_LOW_POWER_ERROR	Validation step of LOW_POWER state has failed
EVT_RMT_DONE	Remote access (RRA) done
EVT_RF_DETECT_ERROR	Error during RF Detect
EVT_LINK_DISABLED	LINK_STATUS switched from 1 to 0 due to a LINK_RESET
EVT_TEMP_ERROR	Temperature sensor overflow or error
EVT_TUNNELING	Entering TUNNELING state
EVT_LOW_POWER	Entering LOW_POWER state
RSSI_COMPLETE	RSSI is complete
RSSI_ERROR	RSSI error
EVT_PWR_COMP_ERROR	Output-power temperature compensation error

4 I²C configuration interface

The ST60A3H1 I²C configuration interface supports the I²C 100 kbit/s, 400 kbit/s and 1 Mbit/s speed rates.

Note: The ST60A3H1 I²C port does not feature any glitch filtering capability. Input and output data on the CFG_SDA pad are sampled on the clock line CFG_SCL. It is therefore mandatory that the application ensures a glitch-free CFG_SCL line.

Accessing registers through the I²C configuration interface is subject to caution:

- LOW_POWER is the state of choice for the complete configuration of a Local device and the future programming of a Remote device before entering TUNNELING state.
- Registers of a Remote device are readable through I²C when the RF link is established (LINK_STATUS=1).
- Although not recommended, registers of a Remote device are writable through I²C when the RF link is established (LINK_STATUS=1). It is the application responsibility to ensure consistency of the device configuration.

More specifically, registers should not be written to when:

- the ST60A3H1 is in RF_DETECT state
- the ST60A3H1 is in TUNNELING state, except if the write access corresponds to issuing a forced LINK_RESET or a low power command

4.1 Address selection, read and write accesses

The 7-bit device address allocated to the ST60A3H1 I²C configuration interface is fixed to 0x60. Therefore, the first byte (7-bit address and direction bit) used in transactions is:

- 0xC0 for write mode
- 0xC1 for read mode

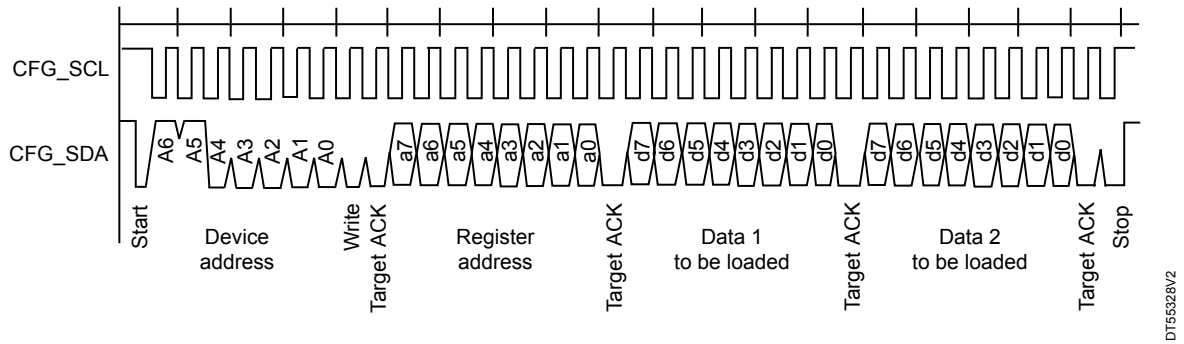
4.1.1 Write access

The byte sequence is as follows:

1. The controller sends the first byte (7-bit device address and direction bit, RW = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. The next byte is written in the internal register. Any following bytes are written in successive internal registers.
4. The transfer lasts until a stop bit is encountered.
5. The ST60A3H1, as target, acknowledges every byte transfer.

Figure 21 shows an I²C write access example with 7-bit device address set to 0x60.

Figure 21. I²C write access



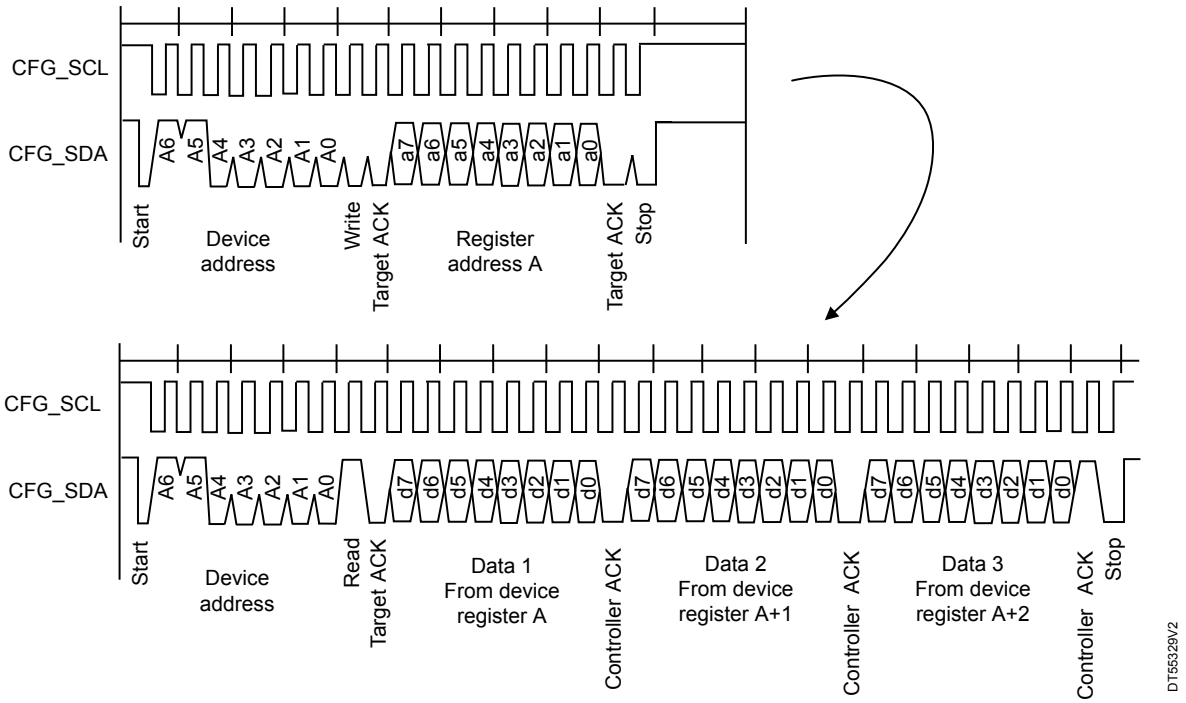
4.1.2 Read access

The byte sequence is as follows:

1. The controller sends the first byte (7-bit device address and direction bit, RW = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. This is terminated with a stop bit.
4. The controller restarts the transmission with the ST60A3H1 address and direction bit, RW = 1.
5. The ST60A3H1 acknowledges and sends the register content. If the controller acknowledge is low, the target transmits another byte which is the contents of the next address register. This continues until the controller acknowledge is high, then the transmission terminates with a stop bit.

Figure 22 shows an I²C read access example with 7-bit device address set to 0x60.

Figure 22. I²C read access



4.2 Low power and I²C access

In cases where the ST60A3H1 is in Low power mode, an I²C start wakes up the device from Low power mode, and enables an internal clock.

The internal clock is used to carry out the I²C transaction into the relevant register, and to take any action consecutive to the write access. Once the access has completed, the device returns to Low power mode.

5 Electrical characteristics

Caution: *All electrical performances are related to default or factory calibrated settings.*

All RF parameters, except for Rx blockers, are characterized in free space propagation and line of sight conditions with the ST60A3H1, which is soldered on its specifically optimized validation board. Rx blockers are characterized in conducted mode with the ST60A3H0, which is equivalent to the ST60A3H1 without the integrated antenna.

5.1 Reset, ThS and magnetic flux

Table 8. Reset, ThS and magnetic flux

Symbol	Parameter	Min	Typ	Max	Unit
t_{RESET}	Reset time after supply voltage is settled	-	-	2250	µs
t_{DWELL}	Minimum supply dwell time at ground level before rising supply voltage	-	-	10	µs
$t_{SUPPLY, rise}$	Supply rise time	50	-	1000	µs
$t_{SUPPLY, fall}$	Supply fall time	50	-	1000	µs
$ThS_{Accuracy}$(1)	Thermal sensor functionality and accuracy in the range 0 to 85 °C	-7	-	7	°C
$B_{MAX\_OP\_MAGNET}$(2)	Static magnetic flux density supported in the operational environment	-	-	10	mT
$B_{MAX\_OP\_WIRELESS\_CHARGER}$(2)	Magnetic flux density supported in the operational environment at 326 kHz/360 kHz switching frequency (wireless charger). 33 W measured on coil placed at 15 mm from the device.	-	-	200	µT
$B_{MAX\_OP\_NFC}$(2)	Magnetic flux density supported in the operational environment at 13.56 MHz switching frequency (NFC). 2.5 W measured on a coil placed at 15 mm from the device.	-	-	10	µT

1. *Calibrated at 1.8 V and 30 °C*
2. *The impact of different magnetic fields have been checked (as null or negligeable) on key parameters as well as during link operation.*

5.2 Absolute maximum ratings (AMR)

Stresses above the absolute maximum ratings listed in Table 9 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

Device use conditions are compliant with the JEDEC JESD47 qualification standard.

Table 9. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
VDD_1V8	Analog power supply	-	-	2.5	V
VDD_IO	Digital and I/O power supply	-	-	2.5	V
P_{IN}	Maximum CW input power at Rx antenna input, LNA OFF or LNA ON with dimmer Tx enabled	-	-	-4	dBm
T_{STG}	Storage temperature	-40	-	125	°C
T_J	Junction temperature	-40	-	125	°C
RH_s(1)	Storage relative humidity @ 30°C	-	-	60	%

1. *Moisture Sensitivity Level 3: 168 hours floor life (≤30°C / 60% RH) after dry pack opening at customer manufacturing.*

5.3 ESD ratings

Caution: *This is an ESD sensitive device; improper handling can cause permanent damage to the part.*

Table 10. ESD ratings

Symbol	Parameter	Conditions(1)	Min(2)	Unit
V_{ESD_HBM}	Electrostatic discharge voltage (HBM)	JS-001	+/- 1500	V
$V_{ESD\_RCDM\_GP}$	Electrostatic discharge voltage (RCDM) for pins GPIO[3:0], CFG_SDA, CFG_SCL, LINK_STATUS, RF_EN, and MODE_INT	JS-002	+/- 500	V
$V_{ESD\_RCDM\_HSO}$	Electrostatic discharge voltage (RCDM) for pins RX_OP and RX_ON	JS-002	+/- 350	V
$V_{ESD\_RCDM\_HSI}$	Electrostatic discharge voltage (RCDM) for pins TX_IP and TX_IN	JS-002	+/- 350	V

1. *For definitions of the ESD classes, see the relevant JEDEC standards, or contact STMicroelectronics customer support.*
2. *Minimum capability of the device*

5.4 Normal operating conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied.

Table 11. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD_1V8(1)	Analog power supply	1.65	1.80	1.95	V
VDD_IO(1)	Digital and I/O power supply	1.65	1.80	1.95	V
T_A(2)	Operating ambient temperature	-20	-	85	°C

1. *VDD_1V8 and VDD_IO must be tied together on the application board.*
2. *These operating conditions are applied to all parameter characterization, except $F_{shift\ carrier\ infield\ cal}$ (+/- 500 ppm) that is defined at T°cal +/- 20 °C.*

5.5 Power consumption

This section provides current consumption values for each state.

The typical values in the tables below are for supply voltages and ambient temperature, within the ranges specified in the preceding tables (see Section 5.4: Normal operating conditions).

Note: The lowest power state of the whole system is a Remote device in RF_DETECT state and a Local device in RF_IDLE state.

5.5.1 RF_IDLE parameters

RF_IDLE power consumption is optimal only if the internal pull-up on RF_EN pin is disabled. This is not the default setting (see Section 2.7.3: Entry into RF_IDLE state).

Table 12. Current consumption in RF_IDLE state (RF_EN low)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{RF_IDLE}	Current in RF_IDLE state, Local/Remote	RF_EN low, no I²C configuration traffic	-	12.5	86	µA

5.5.2 RF_DETECT parameters

The power consumption in RF_DETECT state depends on the discovery scenario chosen, as described in Section 2.8.3.1.1: Power consumption and detection time. Table 13 provides the consumption for a scenario where optimization for the Passive detection device is chosen. Contact STMicroelectronics representative if another discovery scenario is desired.

Table 13. Current consumption in RF_DETECT state

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DISCOVERY\_LOCAL}$ (1)	Current in RF_DETECT state for a Local device	Local ST60A3H1 in Full detection mode.	-	6200	8000	µA
$I_{DISCOVERY\_REMOTE}$	Current in RF_DETECT state for a Remote device	Remote ST60A3H1 waiting to be paired in Passive detection mode. Reported for passive detector based on 500 ms average search time.	-	14	88.5	µA

1. *Informative only.*

5.5.3 LOW_POWER parameters

The power consumption in LOW_POWER state depends on the state of the SLEEP_TIMER and the SLEEP period, which could be adapted to the application

Table 14 provides data for 500 ms SLEEP_TIMER. Contact ST representative for data in other configurations.

Table 14. Current consumption in LOW_POWER state

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{LOW\_POWER\_LOCAL}$(2)	Current in LOW_POWER state for a Local device	RF link @ 32 dB With SLEEP_TIMER optimization enabled (default), assuming 500 ms Housekeeping period.	-	550	800	µA
$I_{LOW\_POWER\_REMOTE}$	Current in LOW_POWER state for a Remote device	RF link @ 32 dB With SLEEP_TIMER optimization enabled (default), assuming 500 ms Housekeeping period.	-	65	170	µA

1. *Link budget figures assume line-of-sight propagation considering minimum antenna gain conditions.*
2. *Informative only.*

5.5.4 TUNNELING parameters

5.5.4.1 eUSB2 tunneling parameters

Table 15. Current consumption in eUSB2 TUNNELING state

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{eUSB2\_LSFS\_L0}$	Current in eUSB2 tunneling, 1.5/12 Mbit/s, Local/Remote	RF link @ 32 dB eUSB2 1.5/12 Mbit/s transmit/receive	-	58.0	73.5	mA
$I_{eUSB2\_HS\_L0\_T}$	Current in eUSB2 tunneling, 480 Mbit/s, Local/Remote	RF link @ 32 dB eUSB2 480 Mbit/s transmit	-	70.5	89.0	mA
$I_{eUSB2\_HS\_L0\_R}$	Current in eUSB2 tunneling, 480 Mbit/s, Local/Remote	RF link @ 32 dB eUSB2 480 Mbit/s receive	-	61.5	78.5	mA
$I_{eUSB2\_IDLE\_L0}$	Current in eUSB2 tunneling, Idle L0, Local/Remote	RF link @ 32 dB eUSB2 Idle L0 transmit/receive Assumes HS mode	-	56.0	71.5	mA
$I_{eUSB2\_SUSPEND\_L2}$	Current in eUSB2 tunneling, Suspend L2, Local/Remote	RF link @ 32 dB eUSB2 Suspend L2 transmit/receive	-	53.0	67.5	mA

1. *Link budget figures assume line-of-sight propagation considering minimum antenna gain conditions.*

5.5.4.2 Half-Duplex UART tunneling parameters

Table 16. Current consumption in Half-Duplex UART TUNNELING state

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{HD\_UART\_TND}$	Current in HD UART tunneling, no data, Local/Remote	RF link @ 32 dB 6 Mbit/s	-	48.0	67.0	mA
$I_{HD\_UART\_TD}$	Current in HD UART tunneling, with data, Local/Remote	RF link @ 32 dB 6 Mbit/s	-	49.5	72.0	mA
$I_{HD\_UART\_UTND}$	Current in HD UART ULP tunneling, no data, Local/Remote	RF link @ 32 dB 115200 bit/s	-	7.5	10.0	mA
$I_{HD\_UART\_UTD}$	Current in HD UART ULP tunneling, with data, Local/Remote	RF link @ 32 dB 115200 bit/s	-	49.5	72.0	mA

1. *Link budget figures assume line-of-sight propagation considering minimum antenna gain conditions.*

5.5.4.3 Full-Duplex UART tunneling parameters

Note: Table 17 below is also valid for bidirectional GPIO tunneling.

Table 17. Current consumption in Full-Duplex UART TUNNELING state

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{FD\_UART\_TND}$	Current in FD UART tunneling, no data, Local/Remote	RF link @ 32 dB 2.4 Mbit/s	-	48.0	67.0	mA
$I_{FD\_UART\_TD}$	Current in FD UART tunneling, with data, Local/Remote	RF link @ 32 dB 2.4 Mbit/s	-	49.5	72.0	mA
$I_{FD\_UART\_UTND}$	Current in FD UART ULP tunneling, no data, Local/Remote	RF link @ 32 dB 115200 bit/s	-	7.5	10.0	mA
$I_{FD\_UART\_UTD}$	Current in FD UART ULP tunneling, with data, Local/Remote	RF link @ 32 dB 115200 bit/s	-	49.5	72.0	mA

1. *Link budget figures assume line-of-sight propagation considering minimum antenna gain conditions.*

5.5.4.4 Single-direction GPIO tunneling parameters

Table 18. Current consumption in single-direction GPIO TUNNELING state

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{SD\_GPIO\_TND}$	Current in single-direction GPIO tunneling, no data, Local/Remote,	RF link @ 32 dB Any tunneled GPIO speed	-	48.0	67.0	mA
$I_{SD\_GPIO\_TD}$	Current in single-direction GPIO tunneling, with data, Local/Remote	RF link @ 32 dB Any tunneled GPIO speed	-	49.5	72.0	mA

1. *Link budget figures assume line-of-sight propagation considering minimum antenna gain conditions.*

5.5.4.5 I²C tunneling parameters

Table 19. Current consumption in I²C TUNNELING state

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
I_{I2C_TND}	Current in I²C tunneling, no data, Local/Remote	RF link @ 32 dB Any tunneled I²C speed	-	48.0	67.0	mA
I_{I2C_TD}	Current in I²C tunneling, with data, Local/Remote	RF link @ 32 dB Any tunneled I²C speed	-	49.5	72.0	mA

1. *Link budget figures assume line-of-sight propagation considering minimum antenna gain conditions.*

5.6 Link parameters

5.6.1 HS eUSB2 link parameters

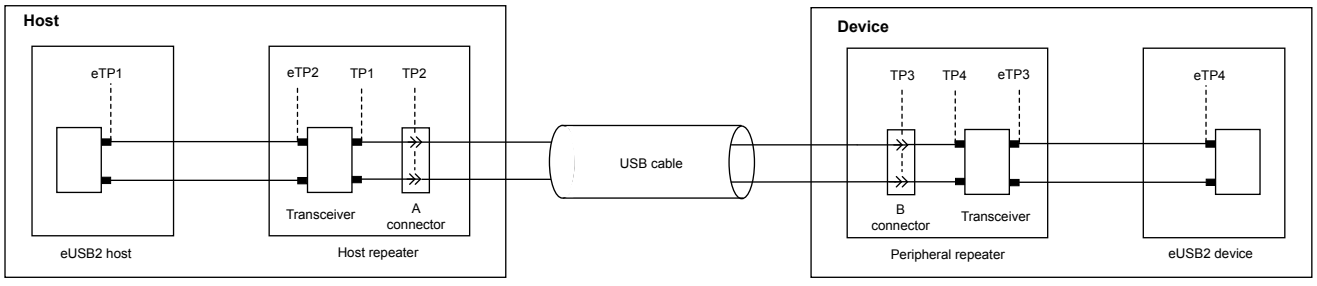
Table 20. Link parameters for High Speed eUSB2

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
TJ_{eUSB2}	Total eUSB2 jitter	For an ST60A3H1 pair with maximum path loss	-	-	212	ps
PL_{eUSB2}	eUSB2 link budget	Maximum path loss supported from Tx antenna output to Rx antenna input for TJ_{eUSB2} < 212 ps.	32	42	-	dB

1. *Link budget figures assume line-of-sight propagation.*

As detailed in Section 2.2: eUSB2 tunneling, an ST60A3H1 pair behaves as an eUSB2 Hybrid Repeater (see appendix B of the eUSB2 specification [1]). The measurement plane is reproduced in Figure 23 below (see also Figure 7-5: Measurement Plane for Repeater Mode of the eUSB2 Specification [1]).

Figure 23. Measurement plane for repeater mode



The ST60A3H1 pair is inserted either between eTP1 and eTP2 (see Figure 24 below), or between eTP3 and eTP4 (see Figure 25 below) with an insertion loss of 2 dB along the eUSB2 channel (max repeater-to-connector insertion loss from the eUSB2 specification [1]).

Figure 24. ST60A3H1 eUSB2 channel direction 1

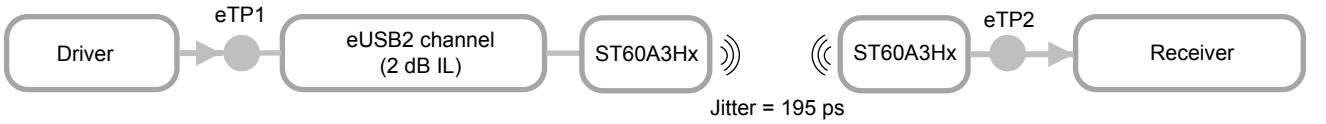
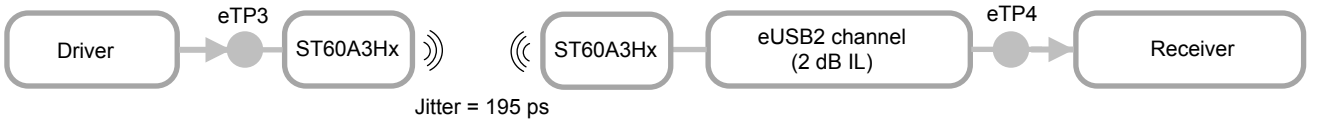


Figure 25. ST60A3H1 eUSB2 channel direction 2



The electrical characteristics for the transmitter and receiver are reported respectively in Section 5.7.2: Line receiver (TX_IP, TX_IN) and Section 5.8.2: Line driver (RX_OP, RX_ON).

Maximum number of USB hubs

The maximum number of USB hubs that can be inserted in the chain is directly linked to the number of SYNC bits consumed by the pieces of equipment between the USB Host controller and the USB Device. The USB Host controller provides 32 SYNC bits in the SOP preamble starting a USB packet. These SYNC bits participate in the clock recovery for receiving the USB packet, so some of them are lost at each entrance of an equipment on the USB chain. At the end of the USB chain, a minimum of 8 SYNC bits must remain for the USB Device. The USB v2 standard allows a maximum of 4 SYNC bits to be consumed by each hub. The ST60A3H1 pair can use a maximum of 8 SYNC bits, and a repeater behaves like a hub regarding the number of SYNC bits consumed.

Table 21. Maximum hubs and SYNC bits consumed regarding topology

Topology	Standard	Hybrid repeater configuration 4_LH / 4_RH
Max SYNC bits consumed by equipment	0 for Host controller	0 for Host controller
	4 for root hub	4 for root hub
	8 for USB Device	4 for USB to eUSB repeater
	-	8 for ST60A3H1 pair
	-	4 for eUSB to USB repeater
	-	8 for USB Device
Remaining SYNC bits	32 - 12 = 20	32 - 28 = 4
Max additional hubs	20 / 4 = 5	4 / 4 = 1

The USB port of a computer is not always connected directly to the root hub. Some computers can embed an internal hub after the root hub. In the same way, some USB Devices can embed an internal hub. Therefore, they must be considered in the maximum number of hubs supported by the hybrid repeater configuration.

5.6.2 Half-Duplex UART link parameters

Table 22. Link parameters for Half-Duplex UART (single and dual wires)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
LP_HD_UART_BR	Low power Half-Duplex UART baud rate	-	-	-	6	Mbit/s
ULP_HD_UART_BR	Ultralow power Half-Duplex UART baud rate	-	-	-	115200	bit/s

1. *Correct operation is validated with the eUSB2 link budget defined in Table 20.*

5.6.3 Full-Duplex UART link parameters

Table 23. Link parameters for Full-Duplex UART (dual wires)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
LP_FD_UART_BR	Low power Full-Duplex UART baud rate	-	-	-	2.4	Mbit/s
ULP_FD_UART_BR	Ultralow power Full-Duplex UART baud rate	-	-	-	115200	bit/s

1. *Correct operation is validated with the eUSB2 link budget defined in Table 20.*

5.6.4 GPIO link parameters

Table 24. Link parameters for GPIO tunneling

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
LP_SINGLE_GPIO_DR	Low power single GPIO tunneling data rate	-	-	-	6	Mbit/s
LP_DUAL_GPIO_UNB_DR	Low power single-direction dual GPIO tunneling data rate	Unbalanced traffic[2]	-	-	4	Mbit/s
LP_DUAL_GPIO_B_DR	Low power single-direction dual GPIO tunneling data rate	Balanced traffic	-	-	2+2	Mbit/s
LP_BIDIR_GPIO_DR	Low power bidirectional GPIO tunneling data rate	-	-	-	2.4	Mbit/s
ULP_BIDIR_GPIO_DR	Ultralow power bidirectional GPIO tunneling data rate	-	-	-	115200	bit/s

1. *Correct operation is validated with the eUSB2 link budget defined in Table 20.*
2. *The assumption is that one GPIO is almost static (less than 1 kbit/s) while the other is toggling at full speed.*

5.6.5 I²C link parameters

I/O performance and slopes refer to ST60A3H1 output characteristics.

Timings are at the output of a pair of ST60A3H1 devices, assuming that controller (or target) are at the exact limit of I²C timing specification with bus loaded as per specification.

"_target" in a parameter name indicates that it refers to a timing for a transaction from target to controller; data for a read or acknowledge. Others are related to the opposite direction; from controller to target.

Figure 26. I²C link timing diagram

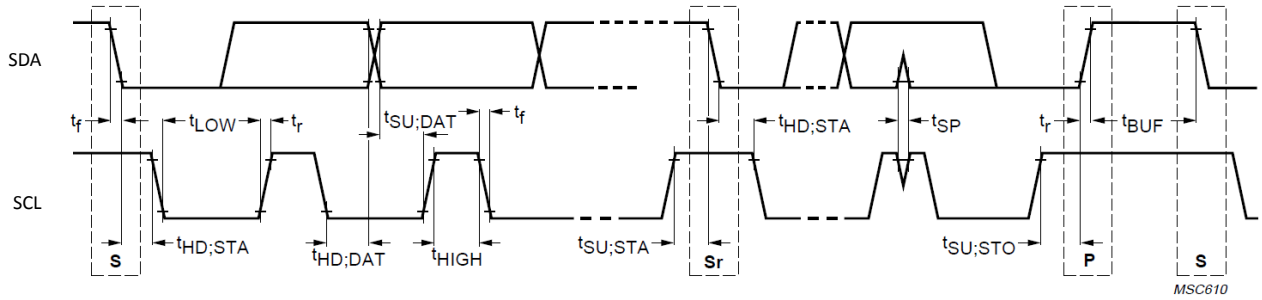


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Table 25. I²C @ 100 kHz tunneling

Symbol	Parameter[1]	Min	Typ	Max	Unit
t_{of}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ (load conditions 4 kΩ, 90 pF)	4	-	106.5	ns
$t_{HD;STA}$	Hold time (repeated) START condition	3.675	-	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	-	µs
t_{HIGH}	HIGH period of the SCL clock	3.44	-	-	µs
$t_{SU;STA}$	Setup time for a repeated START condition	3.44	-	-	µs
$t_{HD;DAT}$	Data hold time	0	-	4.06	µs
$t_{HD;DAT\_target}$	Data hold time	0	-	4.15	µs
$t_{SU;DAT}$	Data setup time	230	-	-	ns
$t_{SU;DAT\_target}$	Data setup time	-450	-	-	ns
t_r	Rise time of both SDA and SCL signals (load conditions 4 kΩ, 90 pF)	350	-	1000	ns
t_f	Fall time of both SDA and SCL signals (load conditions 4 kΩ, 90 pF)	4	-	106.5	ns
$t_{SU;STO}$	Setup time for STOP condition	3.98	-	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.14	-	-	µs
$t_{VD;DAT\_target}$	Data valid time	-	-	4.19	µs
$t_{VD;ACK\_target}$	Data valid acknowledge time	-	-	4.19	µs

1. *Correct operation is validated with the eUSB2 link budget defined in Table 20.*

Table 26. I^2C @ 400 kHz tunneling

Symbol	Parameter[1]	Min	Typ	Max	Unit
t_{of}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ (load conditions 2.2 kΩ, 90 pF)	4	-	106.5	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	-	-	No filtering	ns
$t_{HD;STA}$	Hold time (repeated) START condition	0.275	-	-	µs
t_{LOW}	LOW period of the SCL clock	1.30	-	-	µs
t_{HIGH}	HIGH period of the SCL clock	0.31	-	-	µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.31	-	-	µs
$t_{HD;DAT}$	Data hold time	0	-	1.24	µs
$t_{HD;DAT\_target}$	Data hold time	0	-	1.33	µs
$t_{SU;DAT}$	Data setup time	80	-	-	ns
$t_{SU;DAT\_target}$	Data setup time	-330	-	-	ns
t_r	Rise time of both SDA and SCL signals (load conditions 2.2 kΩ, 90 pF)	170	-	300	ns
t_f	Fall time of both SDA and SCL signals (load conditions 2.2 kΩ, 90 pF)	4	-	106.5	ns
$t_{SU;STO}$	Setup time for STOP condition	0.58	-	-	µs
t_{BUF}	Bus free time between a STOP and START condition	1.01	-	-	µs
$t_{VD;DAT\_target}$	Data valid time	-	-	1.37	µs
$t_{VD;ACK\_target}$	Data valid acknowledge time	-	-	1.37	µs

1. *Correct operation is validated with the eUSB2 link budget defined in Table 20.*

Table 27. I²C @ 1 MHz tunneling

Symbol	Parameter[1]	Min	Typ	Max	Unit
t_{of}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ (load conditions 1 kΩ, 90 pF)	4	-	81.5	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	-	-	No filtering	ns
$t_{HD;STA}$	Hold time (repeated) START condition	-0.065	-	-	µs
t_{LOW}	LOW period of the SCL clock	0.5	-	-	µs
t_{HIGH}	HIGH period of the SCL clock	0.07	-	-	µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.07	-	-	µs
$t_{HD;DAT}$	Data hold time	0	-	-	ns
$t_{HD;DAT\_target}$	Data hold time	0	-	-	ns
$t_{SU;DAT}$	Data setup time	30	-	-	ns
$t_{SU;DAT\_target}$	Data setup time	-300	-	-	ns
t_r	Rise time of both SDA and SCL signals (load conditions 1 kΩ, 90 pF)	72	-	120	ns
t_f	Fall time of both SDA and SCL signals (load conditions 1 kΩ, 90 pF)	4	-	81.5	ns
$t_{SU;STO}$	Setup time for STOP condition	0.24	-	-	µs
t_{BUF}	Bus free time between a STOP and START condition	0.31	-	-	µs
$t_{VD;DAT\_target}$	Data valid time	-	-	0.84	µs
$t_{VD;ACK\_target}$	Data valid acknowledge time	-	-	0.84	µs

1. *Correct operation is validated with the eUSB2 link budget defined in Table 20.*

5.7 Transmitter

5.7.1 RF output (RF OUT)

Table 28. Transmitter specifications

Symbol	Parameter	Min	Typ	Max	Unit
$EIRP_{mod}$	Output modulated RF power (eUSB2 HS mode) accounting for factory calibration at ambient temperature	-1	2.2	4	dBm
$EIRP_{CW}$	Output CW RF power accounting for factory calibration at ambient temperature	2.2	5.4	7.2	dBm
$F_{carrier}$	Carrier frequency – calibrated after ATE calibration	-	60.5	-	GHz
$F_{shift\ carrier}$	Tx output carrier frequency accuracy over -20 to 85 °C	-1500	-	2500	ppm

5.7.2 Line receiver (TX_IP, TX_IN)

As standards specifications may describe I/O characteristics differently, the definitions used hereafter are described in Figure 27.

Figure 27. I/O characteristics definitions

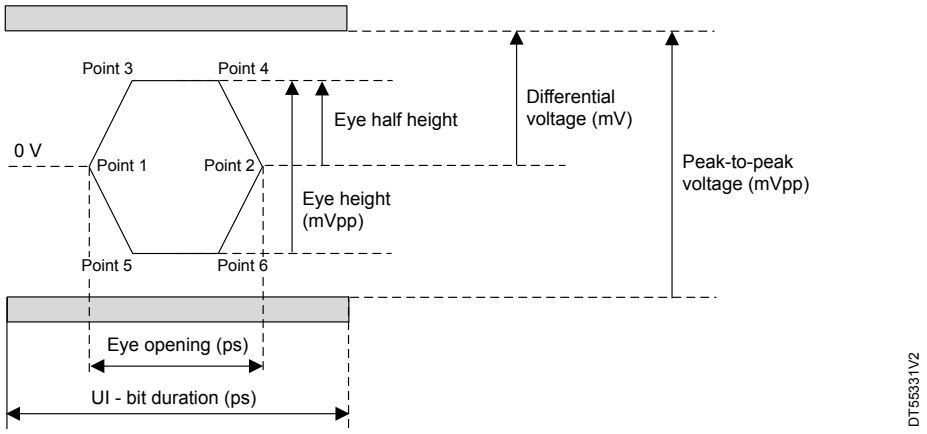


Table 29. I/O line receiver (eUSB2 differential HS)

Symbol	Parameter	Min	Typ	Max	Unit
Zi LR $_{HS\ eUSB2}$	Input impedance terminated	72	80	88	Ω
Vi Sens LR $_{HS\ eUSB2}$	Receive differential sensitivity	-	-	60	mV
Vi CmM LR $_{HS\ eUSB2}$	Common mode	120	200	280	mV
Vi SQD LR V_I $_{HS\ eUSB2}$[1]	In squelch detection level (trimmed)	52	-	111	mV
Vi SQD LR V_O $_{HS\ eUSB2}$[1]	Out of squelch detection level (trimmed)	64	-	132	mV
t_{In_SQD}	In squelch time	-	-	16	ns
t_{Out_SQD}	Out of squelch time	-	-	2	ns
CTCap LR $_{HS\ eUSB2}$	Center tap capacitance	-	-	50	pF
Eye Op LR $_{eTP1\_MASK}$[2]	Eye height	300	-	-	mV
Pt1 LR $_{eTP1\_MASK}$[2]	Eye opening - Point 1	2.6	-	-	% UI
Pt3 LR $_{eTP1\_MASK}$[2]	Eye opening - Point 3	22.6	-	-	% UI
Pt4 LR $_{eTP1\_MASK}$[2]	Eye opening - Point 4	-	-	77.4	% UI
Pt2 LR $_{eTP1\_MASK}$[2]	Eye opening - Point 2	-	-	97.4	% UI
Eye Op LR $_{eTP3\_MASK}$[3]	Eye height	300	-	-	mV
Pt1 LR $_{eTP3\_MASK}$[3]	Eye opening - Point 1	8.4	-	-	% UI
Pt3 LR $_{eTP3\_MASK}$[3]	Eye opening - Point 3	33.4	-	-	% UI
Pt4 LR $_{eTP3\_MASK}$[3]	Eye opening - Point 4	-	-	66.6	% UI
Pt2 LR $_{eTP3\_MASK}$[3]	Eye opening - Point 2	-	-	91.6	% UI

1. *Squelch levels are calibrated during production.*
2. *Measurement at line receiver input with eTP1 mask. See Figure 24. ST60A3H1 eUSB2 channel direction 1.*
3. *Measurement at line receiver input with eTP3 mask. See Figure 25. ST60A3H1 eUSB2 channel direction 2.*

Table 30. I/O line receiver (eUSB2 single-ended LS/FS)

Symbol	Parameter	Min	Typ	Max	Unit
VIL_{LR_LSFS}	Input low voltage single ended	-0.1	-	0.35 x VCC_{LD} (1)	V
VIH_{LR_LSFS}	Input high voltage single ended	0.65 x VCC_{LD} (1)	-	1.05 x VCC_{LD} (1)	V
$VHYS_{LR\_LSFS}$	Receive single-ended hysteresis voltage	0.04 x VCC_{LD} (1)	-	-	V

1. See *Table 33. I/O line driver (eUSB2 single-ended LS/FS)*.

5.8 Receiver

5.8.1 RF input (RF IN)

Table 31. Receiver specifications

Symbol	Parameter	Min	Typ	Max	Unit
RSSI_Acc $_{hir}$ (1)	RSSI accuracy high input range (-28 to -22 dBm)	-4.5	-	3.5	dB
RSSI_Acc $_{lir}$ (1)	RSSI accuracy low input range (-32 to -28 dBm)	-6.6	-	4.1	dB
RSSI_TempE$_{hir}$	RSSI temperature error. Additional residual error after RSSI readout correction (-28 to -22 dBm range).	-1.5	-	1.5	dB
FTC_DC$_{TempRange}$	Allowed temperature variation around link training temperature T_{init} for which ST60A3H1 eUSB2 jitter is guaranteed.	max (T_{init} -25; -20)	-	min (T_{init} +25; 85)	°C
RX Blocker 1dB $_{600\text{-}960M}$ (2)	Rx blocking level 600-960 MHz, LTE	-	-6	-	dBm
RX Blocker 1dB $_{1700\text{-}2025M}$ (2)	Rx blocking level 1700-2025 MHz, LTE	-	-6	-	dBm
RX Blocker 1dB $_{2300\text{-}2400M}$ (2)	Rx blocking level 2300-2400 MHz, LTE	-	-6	-	dBm
RX Blocker 1dB $_{2400\text{-}2484M}$ (2)	Rx blocking level 2400-2484 MHz with HT20 WLAN signal	-	-22	-	dBm
RX Blocker 1dB $_{2496M\text{-}2690M}$ (2)	Rx blocking level 2496-2690 MHz, B41 w/ LTE signal	-	-6	-	dBm
RX Blocker 1dB $_{3400\text{-}3600M}$ (2)	Rx blocking level 3400-3600 MHz, LTE	-	-6	-	dBm
RX Blocker 1dB $_{5.18\text{-}5.9G}$ (2)	Rx blocking level 5.18-5.9 GHz HT20 and HT80 WLAN signal	-	-22	-	dBm
RX Blocker 1dB $_{6\text{-}10G}$ (2)	Rx blocking level 6-10 GHz, LTE	-	-25	-	dBm
RX Blocker 1dB $_{24\text{-}45G}$ (2)	Rx blocking level 24-45 GHz, 5G NR	-	-6	-	dBm
RX Blocker 1dB $_{oth\ -exc}$ (2)	Rx blocking level above 45 GHz, CW. Excluding exclusion band.	-	-50	-	dBm
RX Blocker $_{ExcBand}$	Rx blocker exclusion band	57	-	64	GHz
DynR_RX $_{eUSB2}$	Input dynamic range for compliance with eUSB2 link parameters.	18 (3)	-	-	dB
Pi_RX min $_{eUSB2\ BLK}$ (4)	EIS input to meet full demodulation performance (eUSB2) in the presence of blocker.	-	-39	-33	dBm

Symbol	Parameter	Min	Typ	Max	Unit
Pi_RX min $_{eUSB2}$[4]	EIS input to meet full demodulation performance (eUSB2)	-	-40	-34	dBm

1. *Input range at nominal temperature, including process variations.*
2. *At 1 dB sensitivity degradation.*
3. *Combining DynR_RX $_{eUSB2}$ and Pi_RX min $_{eUSB2}$ leads to a maximum received level to meet eUSB2 demodulation performance of -16 dBm.*
4. *EIS input figures assume line-of-sight propagation.*

5.8.2 Line driver (RX_OP, RX_ON)

Table 32. I/O line driver (eUSB2 differential HS)

Symbol	Parameter	Min	Typ	Max	Unit
Zo LD HS $_{eUSB2\ diff}$	Output impedance	64	80	96	Ω
Vo Swing LD HS $_{eUSB2\ diff}$	Output swing range	165	200	245	mV
Vo DC CmM LD HS $_{eUSB2\ diff}$	DC Common Mode	170	-	230	mV
Eye Op LD $_{eTP4\_MASK}$[1]	Eye height	220	-	-	mV
Pt1 LD $_{eTP4\_MASK}$[1]	Eye opening - Point 1	-	-	13.8	%UI
Pt3 LD $_{eTP4\_MASK}$[1]	Eye opening - Point 3	-	-	33.8	%UI
Pt4 LD $_{eTP4\_MASK}$[1]	Eye opening - Point 4	65.2	-	-	%UI
Pt2 LD $_{eTP4\_MASK}$[1]	Eye opening - Point 2	86.2	-	-	%UI
$t_{fall\ LD\ HS\ eUSB2}$[2]	Fall time (80-20%)	100	-	-	ps
$t_{rise\ LD\ HS\ eUSB2}$[2]	Rise time (20-80%)	97.5	-	-	ps
$t_{r/f\ mm\ LD\ HS\ eUSB2}$[2]	Rise-fall mismatch	-	-	25	%

1. *Measurement at eTP4. See Figure 25. ST60A3H1 eUSB2 channel direction 2.*
2. *Standard programming.*

Table 33. I/O line driver (eUSB2 single-ended LS/FS)

Symbol	Parameter	Min	Typ	Max	Unit
VCC_{LD}	Supply voltage for eD+/eD-	1.08	1.2	1.32	V
$VOL_{LD\ LSFS\ eUSB2}$	Transmit single-ended output low	-	-	0.15 x VCC_{LD}	V
$VOH_{LD\ LSFS\ eUSB2}$	Transmit single-ended output high	0.85 x VCC_{LD}	-	-	V
$RSRC_{LD\ LSFS\ eUSB2}$	Transmit output impedance	28	-	60	Ω
$t_{fall\ LD\ LSFS\ eUSB2}$	Transmit fall time (90-10%)	2	-	6	ns
$t_{rise\ LD\ LSFS\ eUSB2}$	Transmit rise time (10-90%)	2	-	6	ns
$t_{r/f\ mm\ LD\ LSFS\ eUSB2}$	Transmit rise/fall mismatch	-	-	25	%
$RPD_{LD\ LSFS\ eUSB2}$	Pull down resistor	4	-	10	kΩ
$t_{e\_to\_U\_DJ1}$	eUSB2 to USB 2.0 repeater FS jitter to next transition	-6	-	6	ns
t_{DJ2_HR}	Repeater FS paired transition jitter in both directions.	-3	-	3	ns
t_{RJR1}	eUSBr receiver FS jitter tolerance	-15.5	-	15.5	ns
SR_TR	Transmit slew rate	144	-	528	V/µs

5.9 Control pins and GPIOs

Table 34. Control pins and GPIO DC parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD_IO	Digital and I/O power supply	1.65	1.80	1.95	V
I_{fs}	Maximum current leakage fail safe mode	-10	-	10	µA
ABS MAX	Absolute maximum rating VDD_IO	-0.5	-	2.5	V
VMAX IO	Absolute maximum rating	-0.5	-	VDD_IO+0.5	V
I_{OH1}	Output current at $V_{OH(MIN)}$, DRV0/DRV1=LL	-	-	-4	mA
I_{OH2}	Output current at $V_{OH(MIN)}$, DRV0/DRV1=LH	-	-	-6	mA
I_{OH3}	Output current at $V_{OH(MIN)}$, DRV0/DRV1=HL	-	-	-8	mA
I_{OH4}	Output current at $V_{OH(MIN)}$, DRV0/DRV1=HH	-	-	-10	mA
I_{OL1}	Output Current at $V_{OL(MAX)}$, DRV0/DRV1=LL	4	-	-	mA
I_{OL2}	Output current at $V_{OL(MAX)}$, DRV0/DRV1=LH	6	-	-	mA
I_{OL3}	Output current at $V_{OL(MAX)}$, DRV0/DRV1=HL	8	-	-	mA
I_{OL4}	Output current at $V_{OL(MAX)}$, DRV0/DRV1=HH	10	-	-	mA
V_{OH}	Output high voltage	VDD_IO-0.45	-	-	V
V_{OL}	Output low voltage		-	0.45	V
V_{IH}	Input high voltage	0.65 x VDD_IO	-	VDD_IO+0.3	V
V_{IL}	Input low voltage	-0.3	-	0.35 x VDD_IO	V
V_P	Positive going threshold voltage for Schmitt trigger operation	0.4 x VDD_IO	-	0.7 x VDD_IO	V
V_N	Negative going threshold voltage for Schmitt trigger operation	0.3 x VDD_IO	-	0.6 x VDD_IO	V
V_h	Hysteresis voltage for Schmitt trigger operation	0.055 x VDD_IO	-	0.4 x VDD_IO	V
R_{PU}	Pull-up resistor	20	-	120	kΩ
R_{PD}	Pull-down resistor	20	-	120	kΩ
Z_{FS}	Impedance fail safe mode	0.16	-	-	MΩ
V_{nL}	Noise margin at the LOW level	0.1 x VDD_IO	-	-	V
V_{nH}	Noise margin at the HIGH level	0.1 x VDD_IO	-	-	V

5.9.1 Configuration I²C

The configuration I²C block of the ST60A3H1 meets the I²C specification from NXP for Standard mode, Fast mode and Fast mode plus. The block does not however include an anti-glitch filter. For further details, see Section 4: I²C configuration interface.

5.10 Propagation delay

Table 35 provides indicative propagation delays for data transfers across an ST60A3H1 pair assuming line-of-sight propagation. The values shown do not account for propagation delays in cables and boards.

Table 35. Indicative propagation delays in tunneling

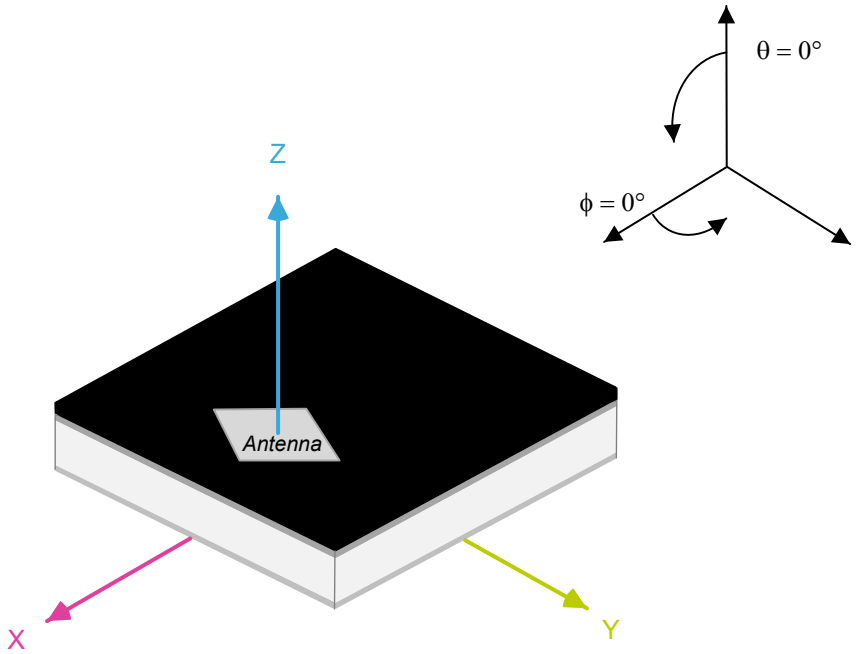
Tunneling mode	Typ	Unit
Half-Duplex UART	43	ns
ULP UART	34	µs
Single-direction GPIO	41	ns
eUSB2 LS/FS	42	ns
eUSB2 HS	< 1	UI (2.08 ns)

6 Integrated antenna characteristics

The package embeds an aperture coupled patch single antenna, with dual-linear polarization and 45° tilt, which allows the use of the same device for both sides of the link. It operates in Half-Duplex mode and features a weak back-radiation on the PCB.

Nevertheless, particular care must be taken for the PCB implementation. This is especially the case for the ST60A3H1 grounding on the board, as the antenna radiated performance can vary for different PCB implementations.

Figure 28. Antenna positioning (3D view)



The antenna's directivity is optimized along the Z axis, with an aperture opening that accommodates +/- 2 mm alignment, considering an operating range of 30 mm. Both 180° relative orientations are supported as shown in Figure 29.

Figure 29. Supported ST60A3H1 180° relative orientations

The integrated antenna broadside radiation pattern is described in Figure 30.

Figure 30. EIRP - measured 3D radiation pattern

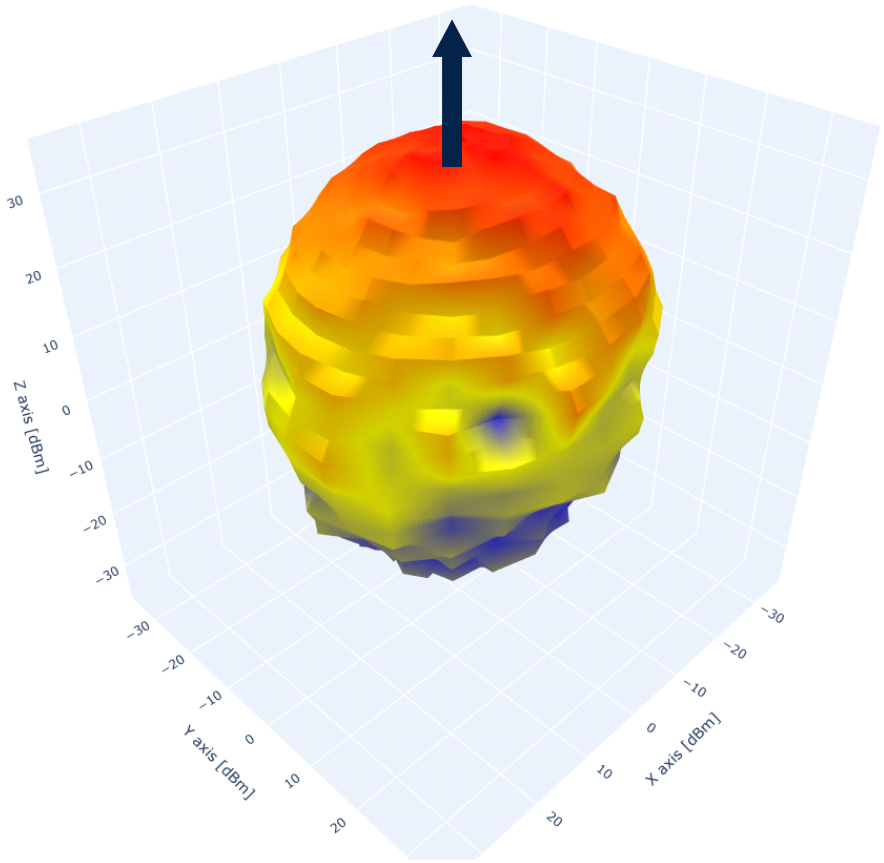


Table 36. Antenna-in-package key features

Parameter [1]	Value
Center frequency	60.5 GHz
Operational bandwidth	From 60 GHz to 61 GHz (1 GHz)
Polarization	Dual linear
Antenna number	Single antenna
Tx gain[2]	4 dBi along the Z axis
Rx gain[2]	4 dBi along the Z axis
3 dB aperture	E-Plane: +/- 55° H-Plane: +/- 45°
PCB immunity	10 dB minimum front to back ratio
XY offset	+/- 2 mm

1. *These can vary with PCB implementation.*
2. *Far-field gain established when the distance between antennas is at least 15 mm.*

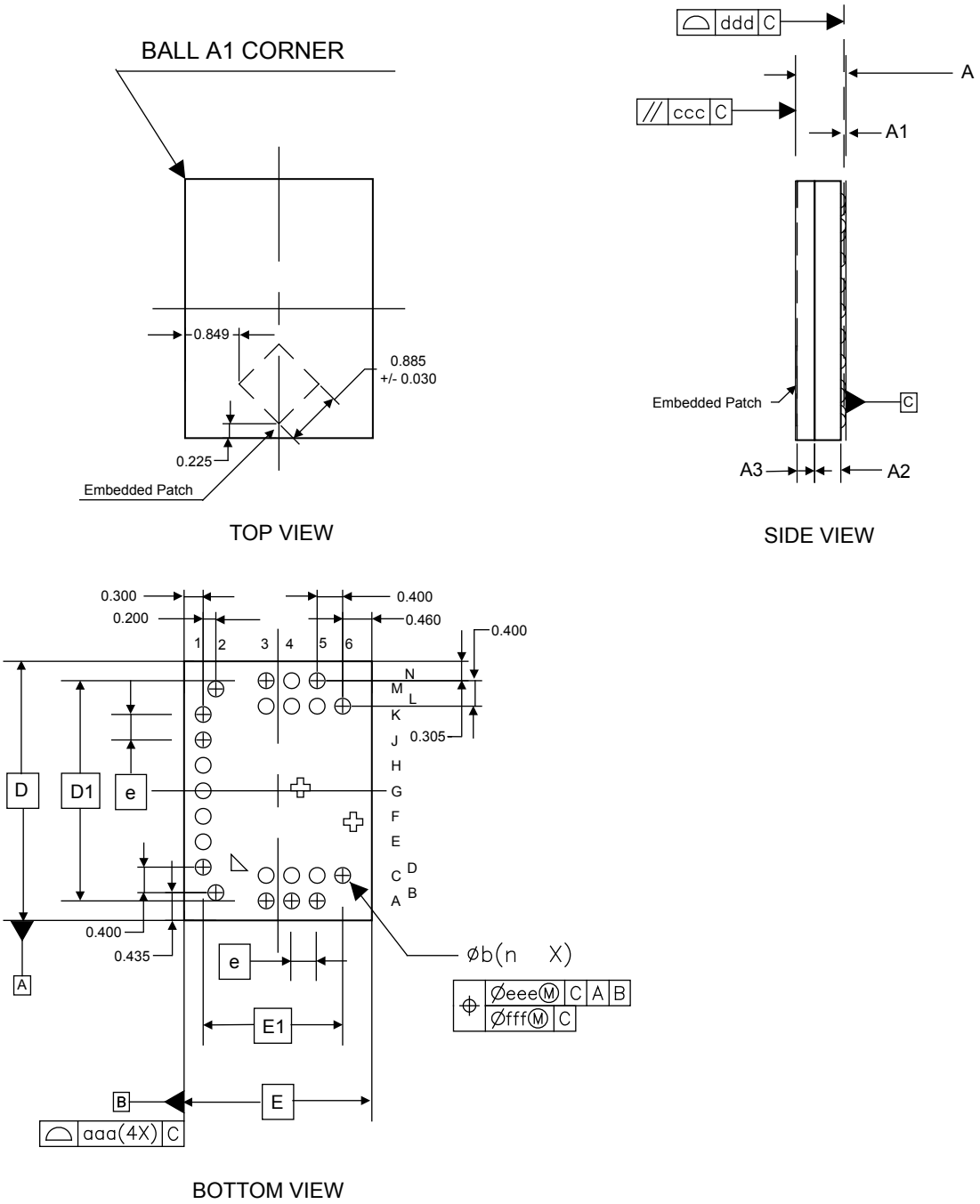
7 Package information

In order to meet environmental requirements, ST offers devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK is an ST trademark.

7.1 Package mechanical data

This package is a VFBGA (very thin profile fine pitch ball grid array) AiP (antenna-in-package) 2.9 mm x 4.1 mm x 0.8 mm, 23 balls, 0.4 mm pitch.

Figure 31. VFBGA23 AiP - outline



Note: The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.

A distinguishing feature is allowed on the bottom surface of the package to identify the terminal A1 corner. The exact shape and size of this feature are optional.

Table 37. VFBGA23 AiP - mechanical data

Symbol	Millimeters			Inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	0.746	0.792	0.838	0.0294	0.0312	0.0330
A1	0.060	0.080	0.100	0.0024	0.0031	0.0039
A2	-	0.412	-	-	0.0162	-
A3	-	0.300	-	-	0.0118	-
b	0.215	0.250	0.285	0.0085	0.0098	0.0112
D	4.020	4.070	4.120	0.1583	0.1602	0.1622
D1	-	3.460	-	-	0.1362	0.0000
E	2.900	2.950	3.000	0.1142	0.1161	0.1181
E1	-	2.190	-	-	0.0862	-
e	-	0.400	-	-	0.0157	-
aaa	-	0.050	-	-	0.0020	-
ccc	-	0.050	-	-	0.0020	-
ddd	-	0.080	-	-	0.0031	-
eee(3)	-	0.150	-	-	0.0059	-
fff(4)	-	0.050	-	-	0.0020	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *VFBGA stands for Very thin profile Fine pitch Ball Grid Array package:*
   - *Very thin profile: 0.80 < A Max ≤ 1.00 mm / Fine pitch: e < 1.00 mm.*
   - *The total profile height (Dim A) is measured from the seating plane "C" to the top of the component.*
   - *The maximum total package height is calculated by the RSS method (Root Sum Square):*
     A Max = A1 Typ + A2 Typ + A3 Typ + √ (A1² + A2² + A3² tolerance values).
3. *The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
4. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.*

Table 38. **Solder ball coordinates**

Ball location		Ball X,Y (mm)	
X	Y	X	Y
1	K	-1.1750	1.2000
1	J	-1.1750	0.8000
1	H	-1.1750	0.4000
1	G	-1.1750	0
1	F	-1.1750	-0.4000
1	E	-1.1750	-0.8000
1	D	-1.1750	-1.2000
2	M	-0.9750	1.6000
2	B	-0.9750	-1.6000
3	N	-0.1850	1.7300
3	L	-0.1850	1.3300
3	C	-0.1850	-1.3300
3	A	-0.1850	-1.7300
4	N	0.2150	1.7300
4	L	0.2150	1.3300
4	C	0.2150	-1.3300
4	A	0.2150	-1.7300
5	N	0.6150	1.7300
5	L	0.6150	1.3300
5	C	0.6150	-1.3300
5	A	0.6150	-1.7300
6	L	1.0150	1.3300
6	C	1.0150	-1.3300

Note: Coordinate 0.0 is the center of the bottom package as shown in Figure 31. VFBGA23 AiP - outline.

7.2 Package marking

The package laser marking is composed of a 2D data matrix code:

- 2D marking size: 1.95 mm x 0.9 mm
- Matrix cells: 12 x 26
- Pixel size: 75 µm

Figure 32. Package markings (top package face)

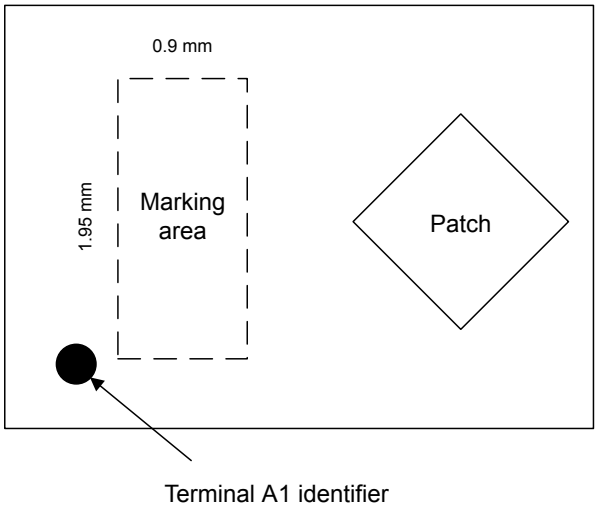


Table 39. Product identification

Product identification	Commercial product
A3H11CC3[1]	ST60A3H1C1CCEPY3 ST60A3H1C1CCEPT3

1. *Decoded data (first 8 characters)*

7.3 Thermal characteristics

The data in Table 40 refer to a multilayer board according to the JEDEC standard.

Table 40. Package thermal characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-	30.0	-	°C
T_J	Maximum junction temperature	-	42.3	-	°C
Θ_{JA}	Junction to ambient package thermal resistance(1)	-	66.6	-	°C/W
Θ_{JB}	Junction to board package thermal resistance(1)	-	41.5	-	°C/W
Θ_{JC}	Junction to case package thermal resistance(1)	-	23.8	-	°C/W
Ψ_{JB}	Thermal characterization parameter junction to board(1)	-	39.5	-	°C/W
Ψ_{JT}	Thermal characterization parameter junction to top case(1)	-	2.1	-	°C/W

1. *Refer to JEDEC standard JESD 51-12 for a detailed description of the thermal resistances and thermal parameters.*

   $T_J = T_A + \Theta_{JA} \times P_{diss}$ (in order to estimate T_J if ambient temperature T_A and dissipated power P_{diss} are known)

   $T_J = T_B + \Psi_{JB} \times P_{diss}$ (in order to estimate T_J if ambient temperature T_B and dissipated power P_{diss} are known)

   $T_J = T_T + \Psi_{JT} \times P_{diss}$ (in order to estimate T_J if ambient temperature T_T and dissipated power P_{diss} are known)

7.4 Reflow soldering conditions

There are no special requirements necessary when reflowing BGA components. As with all other SMT components, it is important that soldering profiles are checked on all new board designs. In addition, if there are multiple packages on the board, the profile must be checked at different locations on the board. The solder paste manufacturer's recommended profile should be considered and used to optimize flux activity and minimize the voiding. The recommended lead-free reflow profile is illustrated in Figure 33 and the typical parameters in Table 41.

- Ramp-to-spike profile is recommended for lead-free assembly with better wetting and less thermal exposure than traditional ramp-soak-spike profile.
- Avoid a temperature plateau around melting temperature for better accuracy.
- Thermocouples are attached through the bottom side of the board underneath the center and corner of the component BGA.
- Perform reflow optimization for the actual board or panel and refer to the solder paste supplier's recommendation.

Figure 33. **Recommended lead-free reflow soldering profile for BGA packages**

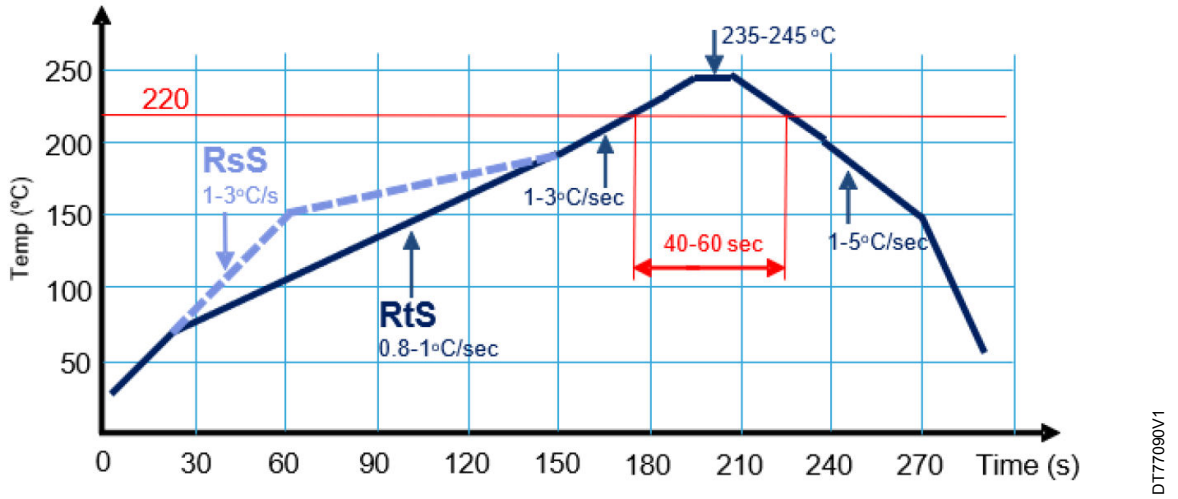


Table 41. **Typical lead-free reflow soldering profile parameters for BGA packages**

Profile	Ramp to spike	Ramp-soak-spike
Temperature gradient during preheat	Temp = 70 to 150 °C: 0.9+/-0.1 °C/s	Temp = 70 to 150 °C: 2+/-1 °C/s
Soak/Dwell(1)	N/A or Temp = 150 to 200 °C: 60+/-20 s	Soak Temp = 150 to 200 °C: 70+/-30 s
Temperature gradient during preheat	Temp = 200 to 225 °C: 2+/-1 °C/s	
Peak temperature	235 to 245 °C	
Duration above 220 °C	40 to 60 s	
Temperature gradient during cooling	-1 to -5 °C/s	

1. *Refer to solder paste supplier's recommendation.*

8 Pin list

Table 42. **ST60A3H1 pin list**

Ball	Name	Type	Description	Comments
A3	GND	Ground	Ground	-
A4	GND	Ground	Ground	-
A5	GND	Ground	Ground	-
B2	GPIO[0]	I/O	Low data rate data or alternate GPIO_0	Internal pull-up at power-up. Configured as input after reset with internal pull-up (default).
C3	VDD_1V8	Power	Analog power supply	1.8 V
C4	TX_IP	I	Tx input, positive	Analog differential or single-ended signal
C5	TX_IN	I	Tx input, negative	Analog differential or single-ended signal
C6	GND	Ground	Ground	-
D1	GPIO[1]	I/O	Low data rate data or alternate GPIO_1	Internal pull-up at power-up. Configured as input after reset with internal pull-up (default).
E1	CFG_SCL	I	Configuration I^2C bus clock after reset	Internal pull-up at power-up. Configured as input after reset with internal pull-up.
F1	CFG_SDA	I/O	Configuration I^2C data after reset	Internal pull-up at power-up. Configured as input after reset with internal pull-up.
G1	MODE_INT	I/O	Interrupt pin	Internal pull-down at power-up only. Configured as output after reset.
H1	RF_EN	I	Power-up Reset pin. RF path activation / deactivation	Internal pull-down at power-up. Configured as input after reset with internal pull-up (default).(1)
J1	LINK_STATUS	I/O	Indicates RF link status	Internal pull-down at power-up only. Configured as output after reset.
K1	GPIO[2]	I/O	Low data rate data or alternate GPIO_2	Internal pull-up at power-up. Configured as input after reset with internal pull-down (default).(2)
L3	VDD_IO	Power	Digital and I/O power supply	1.8 V
L4	RX_OP	O	Rx output, positive	Analog differential or single-ended signal
L5	RX_ON	O	Rx output, negative	Analog differential or single-ended signal
L6	GND	Ground	Ground	-
M2	GPIO[3]	I/O	Low data rate data or alternate GPIO_3	Internal pull-up at power-up. Configured as input after reset with internal pull-down (default)(2).
N3	GND	Ground	Ground	-
N4	GND	Ground	Ground	-
N5	GND	Ground	Ground	-

1. *For optimal power consumption, the internal pull-up resistor should be disabled in RF_IDLE.*
2. *Internal pull-down is removed and replaced by an internal pull-up if I^2C tunneling is enabled on this GPIO.*

9 Regulatory requirements

As an item of radio equipment operating around 60 GHz, the ST60A3H1 target is to comply with regulation requirements, depending on the geographical area it is intended to be deployed in. The ST60A3H1 aims to fulfill at least the following regulations:

- US FCC 47 CFR part-15 subpart C §15.255 frequency band 57-71 GHz
- Europe ETSI EN 305550 v2.1.0 frequency band 57-64 GHz
- Japan article 2 paragraph 1 of item 19-4-3 frequency band 57-66 GHz

The ST60A3H1 modulation is ASK; therefore the maximum output power is for bit 1 and the minimum output power is for bit 0. The ST60A3H1 implements Half-Duplex protocols, consequently when one side of the link actively transmits data (series of 0 and 1), the facing or receiving side ‘modulates’ a constant 0 and radiates a minimum power.

10 Ordering information

Table 43. **ST60A3H1 ordering information**

Commercial product	Package	Temperature range	Packing	MOQ	Availability
ST60A3H1C1CCEPY3	VFBGA 2.9 x 4.1 x 0.8 mm	Consumer -20, 85°C	Tray	2940	Production
ST60A3H1C1CCEPT3	VFBGA 2.9 x 4.1 x 0.8 mm	Consumer -20, 85°C	Tape-and-Reel	5000	Production

For further information, contact your local STMicroelectronics sales office.

Revision history

Table 44. **Document revision history**

Date	Revision	Changes
10-Dec-2024	1	Initial release.
10-Mar-2025	2	Updated: • Table 2. Document references • Section 2.2: eUSB2 tunneling • Section 5.7.2: Line receiver (TX_IP, TX_IN) • Figure 27. I/O characteristics definitions
08-Jul-2025	3	Updated: • Table 1. Definition of terms • Table 43. ST60A3H1 ordering information Added: • Table 38. Solder ball coordinates • Section 7.4: Reflow soldering conditions
13-Nov-2025	4	Updated: • Table 1. Definition of terms Modified document to use I^2C controller/target terminology.

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