

50 Mbps, half-duplex RS485 transceiver with ± 16 kV IEC 61000-4-2 contact ESD protection



SO8 4.90 mm x 3.91 mm

Maturity status link

[ST4E1651](#)

Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard.
- Half-duplex topology
- 3 V to 3.6 V supply voltage
- High speed: up to 50 Mbps data rate
- More than 64 transceivers on the bus
- Integrated protections
 - Fail-safe receiver (bus open, idle, and shorted)
 - Thermal shutdown protection
 - Bus I/O ESD protection
 - ± 16 kV IEC61000-4-2 contact discharge.
 - ± 30 kV HBM ESD
 - ± 4 kV IEC61000-4-4 class-A fast transient burst (EFT)
- -40 °C to $+125$ °C operating temperature
- Available in industry standard SO8

Applications

- Factory automation and control
- Encoders
- Building automation and safety
- Video surveillance (building, traffic monitoring)
- Backplane bus
- Grid infrastructure
- Robotics
- Motion controllers

Description

The **ST4E1651** is a low-power differential line transceiver for data transmission standard RS485 applications in half-duplex mode, compatible with 3.3 V rail power supplies, fully operating from 3 V to 3.6 V.

The **ST4E1651** operates up to 50 Mbps. It is ideal for multi-point applications over extended cable runs. It is robust to ESD transients. In particular, the bus pins support ± 16 kV IEC 61000-4-2 contact discharge. It features robust hot-swap capability during switching on and off, or during plug-in.

It is available in a standard SO8 package and operates from -40 °C up to 125 °C.

1 Pin configuration

Figure 1. Pin connections

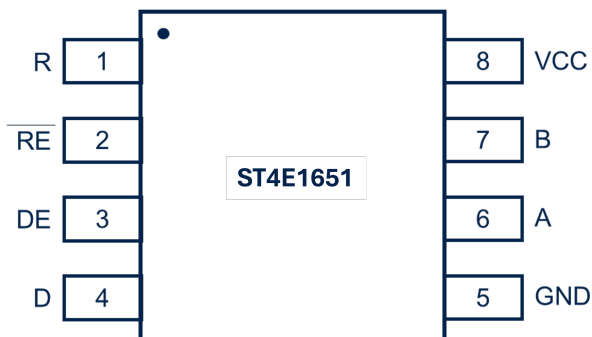


Table 1. Pin description

Name	Pin	I/O	Description
R	1	Digital output	Receiver data output
$\overline{\text{RE}}$	2	Digital input	Receiver enable input, active low
DE	3	Digital input	Driver enable input, active high
D	4	Digital input	Transmission data input
GND	5	Ground	
A	6	Bus I/O	Digital bus I/O, A
B	7	Bus I/O	Digital bus I/O, B
VCC	8	Device supply	3 V to 3.6 V supply voltage

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Device supply voltage	-0.5	7	V
	Voltage range at A and B terminals	-9	14	V
	Input voltage range at any logic pin (referred to an operating V_{CC})	-0.3	$V_{CC} + 0.3$	V
	Short-circuit duration (R, A, B) to GND	Continuous		
T_{stg}	Storage temperature	-65	150	°C

Note: All voltage values, except the differential voltage, are referred to the network ground terminal.

Table 3. ESD ratings

Symbol	Parameter	Value	Unit
ESD	IEC61000-4-2 ESD (contact discharge), bus terminals and GND	± 16	kV
	IEC61000-4-4 EFT (fast transient or burst) bus terminals and GND	± 4 (class A)	kV
	HBM, bus terminals and GND	± 30 ⁽¹⁾	kV
	JEDEC standard 22, test method A114, HBM, all other terminals	± 2	kV
	JEDEC standard 22, test method C101, (charged device model), all pins	± 1	kV

1. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Measurement for 20 A peak, 100 ns Transmission-Line Pulse (TLP), package level at room temperature.

3 Electrical characteristics

Table 4. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Device supply voltage	3		3.6	V
V _I	Input level at any bus terminal (separated or common-mode)	-7		12	V
V _{ID}	Differential input voltage	-7		12	V
I _O	Output current / driver & receiver	-70		70	mA
R _L	Differential load resistance	54	60		Ω
C _L	Differential load capacitance		50		pF
D _R	Signaling rate			50	Mbps
T _A	SO8 Operating free-air temperature	-40		125	°C

Operation is specified for internal (junction temperature) up to 155 °C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down circuit, which disables the driver output when the junction temperature reaches 170 °C.

Table 5. Thermal information

Symbol	Parameter	Min.	Typ.	Max.	Unit
R _{th-ja}	Thermal resistance, junction-to-ambient, SO8		125		°C/W

Table 6. Power dissipation

Symbol	Parameter	Test conditions	Typ.	Unit
P _D	Power dissipation, with driver and receiver enabled VCC=3.3V, T=125°C, 50% duty cycle at max signaling rate and SO8 package	Unterminated, R _L = 300 Ω, C _L = 50 pF	130	mW
		RS485-load: R _L = 54 Ω, C _L = 50 pF	131	mW

Table 7. Receiver: operating conditions ($V_{CC} = +3.0\text{ V}$ to 3.6 V , $T_A = T_{\min}$ to $T_{\max}$, unless otherwise specified. Typical values are $V_{CC} = 3.3\text{ V}$ and $T = 25\text{ }^{\circ}\text{C}$).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Receiver / DC						
V_{TH+}	Positive-going input threshold voltage	$-7\text{ V} \leq V_{CM} \leq 12\text{ V}$		-100	-10	mV
V_{TH-}	Negative-going input threshold voltage	$-7\text{ V} \leq V_{CM} \leq 12\text{ V}$	-200	-130		
V_{HYS}	Receiver differential input voltage hysteresis	Figure 12		30		
V_{OH}	Receiver high-level output voltage	$\overline{RE} = \text{GND}$, $I_{OH} = -2\text{ mA}$, ($V_A - V_B$) > 200 mV	$V_{CC}-0.2$			V
V_{OL}	Receiver low-level output voltage	$\overline{RE} = \text{GND}$, $I_{OL} = 2\text{ mA}$, ($V_A - V_B$) < -200 mV			0.2	
I_{OZ}	Receiver output high-impedance current	$0 \leq V_R \leq V_{CC}$, $\overline{RE} = V_{CC}$.	-1		1	μA
I_{OS}	Receiver output short-circuit current	$0 \leq V_R \leq V_{CC}$.	-90		90	mA
I_i	Receiver input current	$V_I = 12\text{ V}$ Figure 10		140	500	μA
	DE = GND, $V_{CC} = \text{GND}$ or $+3.3\text{ V}$	$V_I = -7\text{ V}$ – Figure 10	-400	-155		
R_{in}	Receiver input impedance	$-7\text{ V} \leq V_{inrm} \leq +12\text{ V}$	24			k Ω
Receiver/ switching characteristics						
t_r, t_f	Receiver output rise/fall time	$C_L = 15\text{ pF}$		3	6	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			20	25	ns
$t_{SK(P)}$	Receiver pulse skew, $ t_{PHL} - t_{PLH} $, $\Delta V_{in} = 1.5\text{ V}$				2.5	ns
t_{PLZ}	Receiver disable time, from low	$C_L = 15\text{ pF}$ with $1\text{ k}\Omega$		8	20	ns
t_{PHZ}	Receiver disable time, from high	$C_L = 15\text{ pF}$ with $1\text{ k}\Omega$		8	30	ns
t_{PZL}, t_{PZH}	Receiver enable time	Driver enabled $C_L = 15\text{ pF}$ with $1\text{ k}\Omega$		90	135	ns
$t_{PZH(shdn)}$	Receiver enable time from shutdown to output high	Driver disabled $C_L = 15\text{ pF}$ with $1\text{ k}\Omega$		2.4	4	μs
$t_{PZL(shdn)}$	Receiver enable time from shutdown to output low	Driver disabled $C_L = 15\text{ pF}$ with $1\text{ k}\Omega$		2.4	4	μs

Table 8. Driver: operating conditions ($V_{CC} = +3.0\text{ V}$ to 3.6 V , $T_A = T_{\min}$ to $T_{\max}$, unless otherwise specified. Typical values are at $V_{CC} = 3.3\text{ V}$ and $T = 25\text{ }^{\circ}\text{C}$).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC driver / DC						
V _{OD}	Driver differential output voltage magnitude	$R_L = 54\text{ }\Omega$, $C_L = 50\text{ pF}$	1.5			V
		$R_L = 60\text{ }\Omega$ / 375 Ω Figure 1	1.5			
		$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$				
$\Delta V_{OD} $	Change in magnitude of driver differential output voltage	$R_L = 54\text{ }\Omega$, $C_L = 50\text{ pF}$	-50		+50	mV
V _{OC(SS)}	Steady-state common-mode output voltage	Center of two 27 Ω load resistors	1	1.5	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage		-0.12		0.12	V
V _{OC(PP)}	Peak-to-peak driver common-mode output voltage			0.45		
V _{OH}	Single-ended driver output high	A or B output, I_A or $I_B = -20\text{ mA}$	$V_{CC}-0.4$			V
V _{OL}	Single-ended driver output low	A or B output, I_A or $I_B = 20\text{ mA}$			0.4	V
Driver/switching characteristics						
t_r , t_f	Driver differential output rise/fall time	$R_L = 54\text{ }\Omega$, $C_L = 50\text{ pF}$		4	6	ns
t_{PHL} , t_{PLH}	Driver propagation delay			14	20	
$t_{SK(P)}$	Driver pulse skew, $ t_{PHL}-t_{PLH} $				3	
t_{PLZ} , t_{PHZ}	Driver disable time				25	
t_{PZL} , t_{PZH}	Driver enable time	Receiver enabled			25	ns
		Receiver disabled			25	

Table 9. Input logic interface (D, DE, $\overline{RE}$): ($V_{CC} = +3.0\text{ V}$ to 3.6 V , $T_A = T_{\min}$ to $T_{\max}$, unless otherwise specified. Typical values are $V_{CC} = 3.3\text{ V}$ and $T = 25\text{ }^{\circ}\text{C}$).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{IH}	High-level input voltage		$0.7 \times V_{CC}$		V_{CC}	V
V _{IL}	Low-level input voltage		0		0.8	V
I _{in}	Input current	$V_{in} = 0$ or V_{CC}	-5		5	μA
	Input impedance on first transition (DE, $\overline{RE}$)		3		10	k Ω

Table 10. Supply current and protections: ($V_{CC} = +3.0\text{ V}$ to 3.6 V , $T_A = T_{\min}$ to $T_{\max}$, unless otherwise specified. Typical values are $V_{CC} = 3.3\text{ V}$ and $T = 25\text{ }^{\circ}\text{C}$).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current						
I_{CC}	Supply current (quiescent)	Driver and receiver enabled $DE = V_{CC}$, $\overline{RE} = \text{GND}$, no load		1.5	4	mA
		Driver enabled, receiver disabled $DE = V_{CC}$, $RE = V_{CC}$, no load		0.9	2.8	mA
		Driver disabled, receiver enabled $DE = \text{GND}$, $\overline{RE} = \text{GND}$, no Load		0.8	2.1	mA
		Driver and receiver disabled (shutdown mode) $DE = \text{GND}$, $\overline{RE} = V_{CC}$, No load		0.1	10	μA
T_{TSD}	Thermal shutdown threshold			170		$^{\circ}\text{C}$
T_{TSD_HYS}	Thermal shutdown hysteresis			13		
I_{OS}	Driver short-circuit output current	$-7\text{ V} < V_{\text{SHORT}} < +12\text{ V}$	-250		250	mA

4 Test circuits

In the schematics below, C_L includes fixture and instrumentation capacitance.

Figure 2. Driver differential output voltage with common-mode load

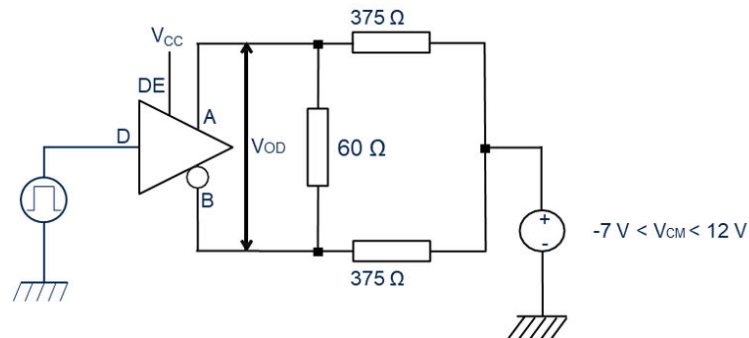


Figure 3. Driver differential and common-mode output with RS-485 load

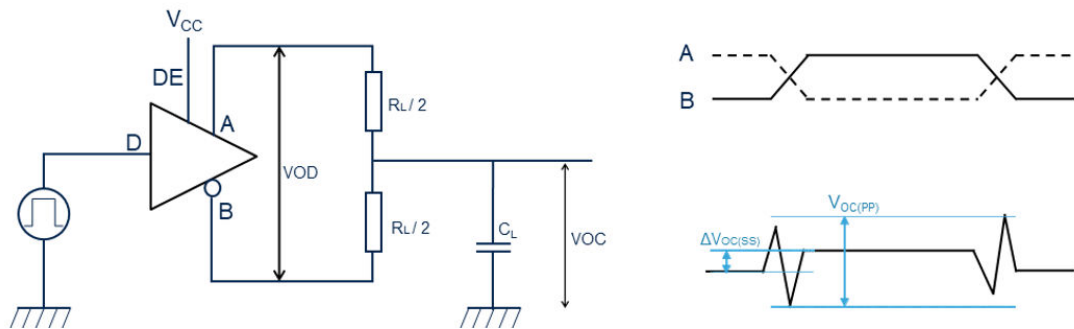


Figure 4. Driver differential output rise and fall times and propagation delays

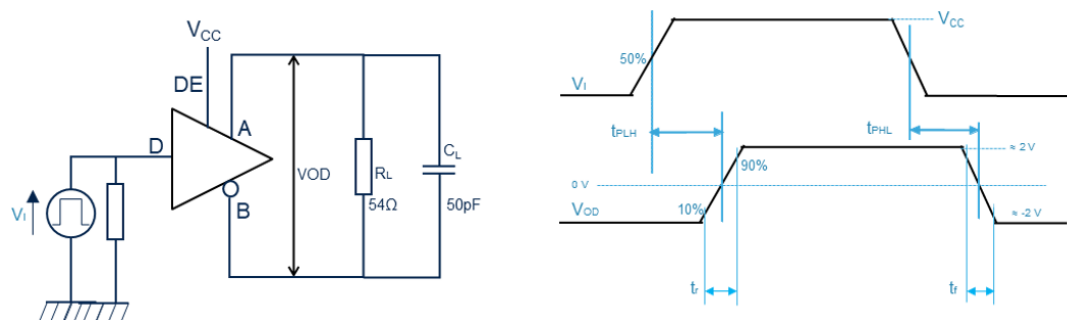


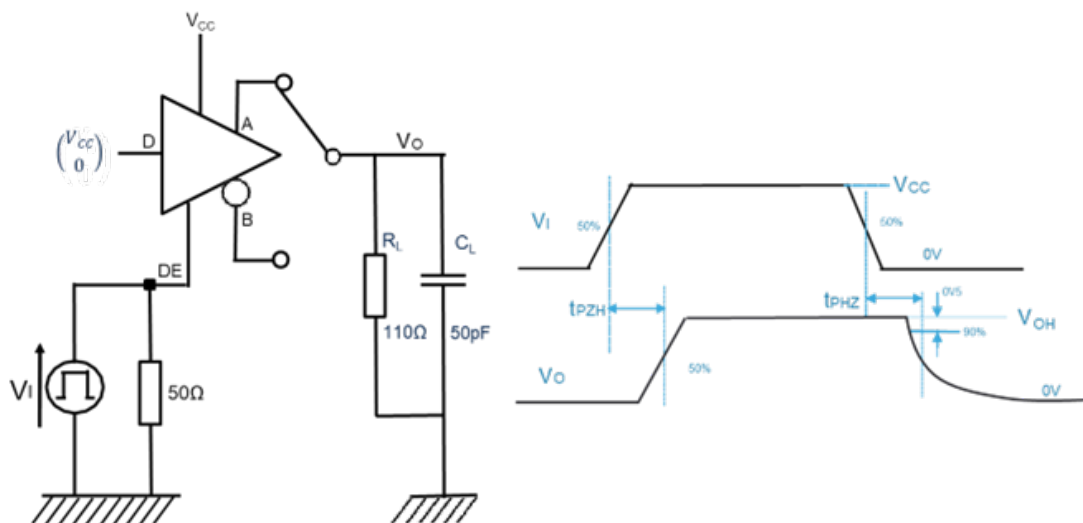
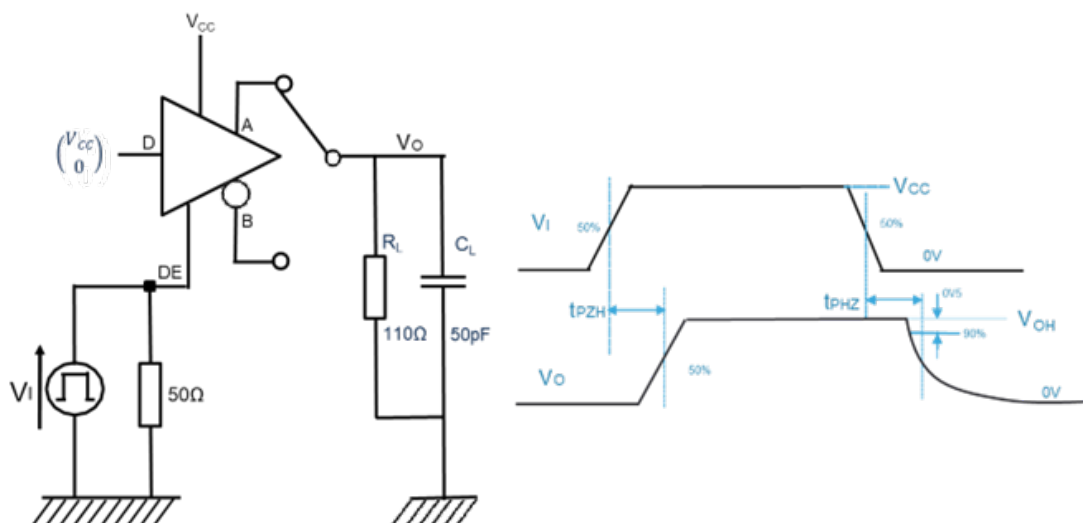
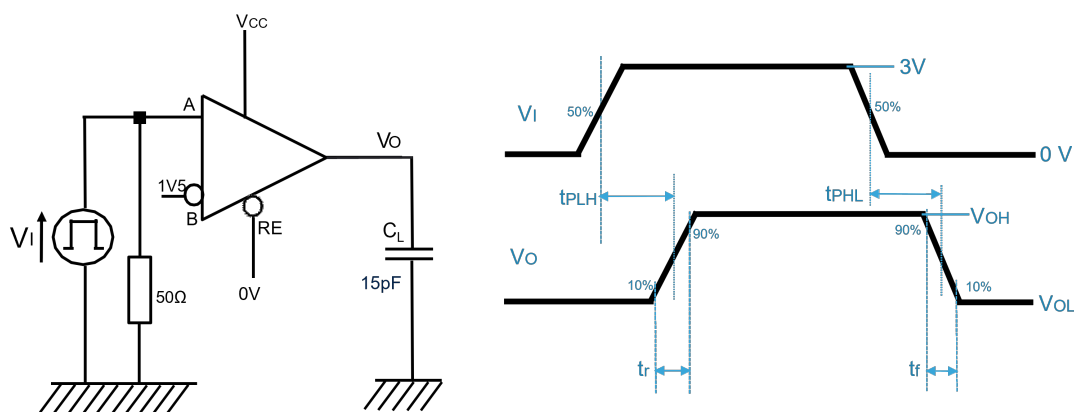
Figure 5. Driver enable and disable times with active high output and pull-down load

Figure 6. Driver enable and disable times with active low output and pull-up load

Figure 7. Receiver output rise and fall times and propagation delay


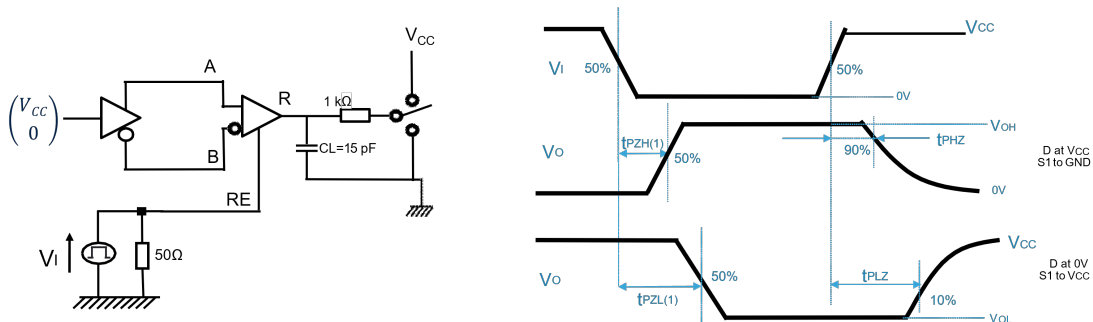
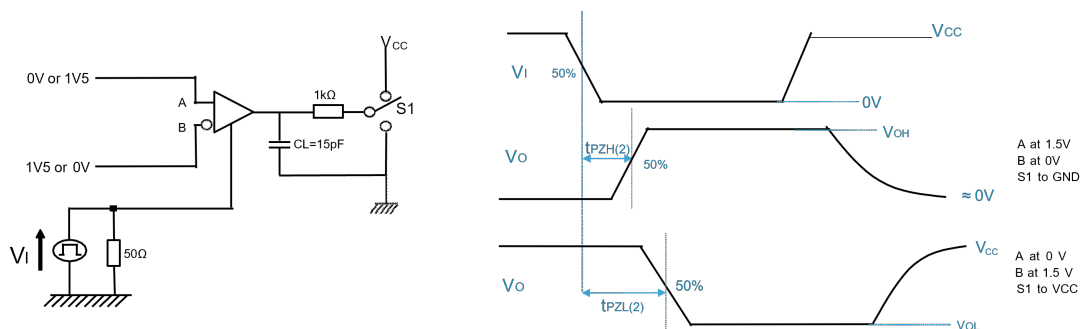
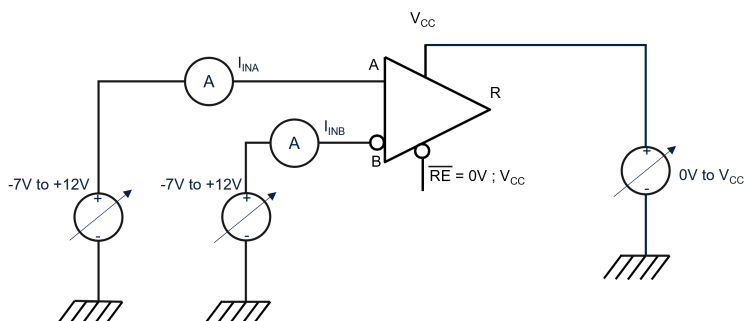
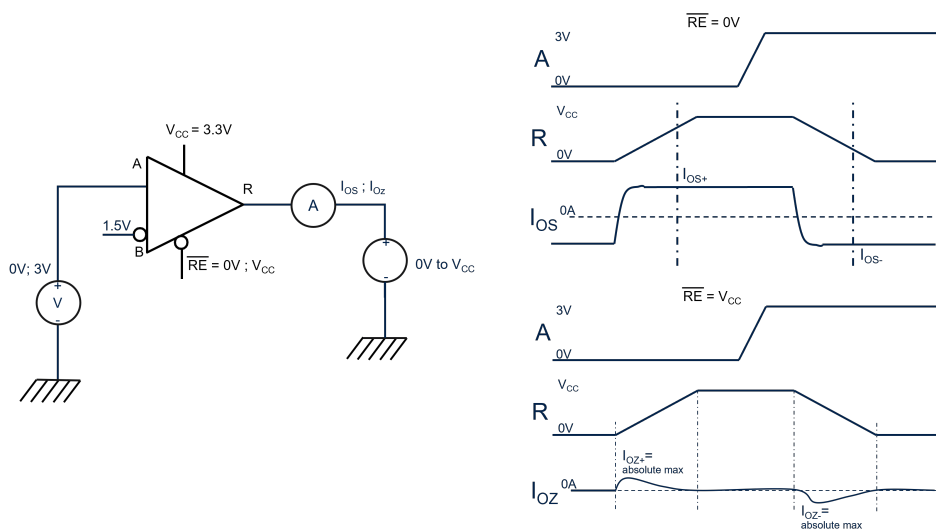
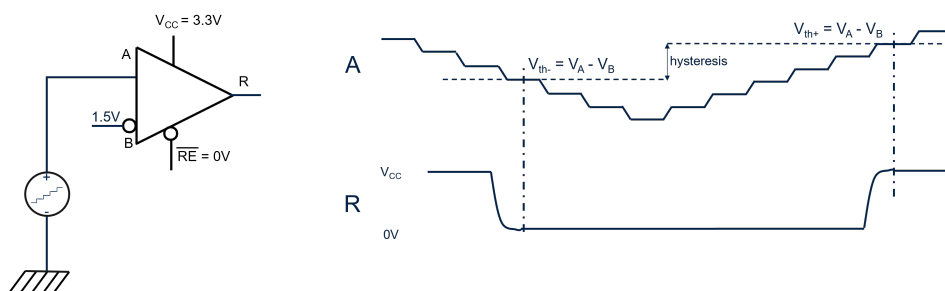
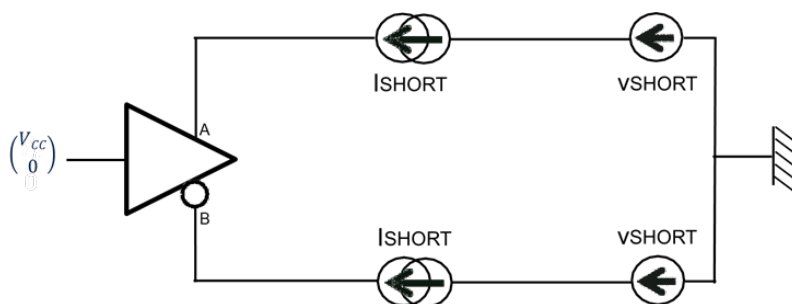
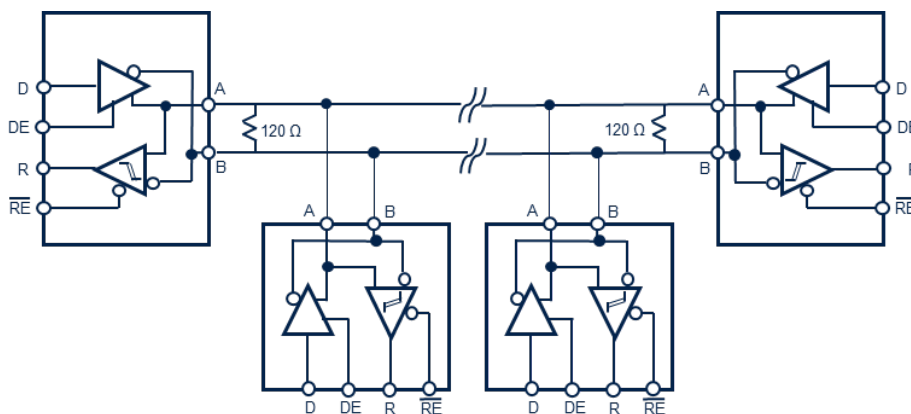
Figure 8. Receiver enable/disable times with driver enabled

Figure 9. Receiver enable/disable times with driver disabled

Figure 10. Receiver input current

Figure 11. Receiver output current


Figure 12. Receiver threshold and hysteresis

Figure 13. Short-circuit output current measurement


When one of the driver outputs is shorted to a voltage source (named V_{SHORT}) between -7 V to +12 V stabilized, the current does not exceed 250 mA and the driver is protected.

Figure 14. Typical half-duplex RS485 network


5 Typical characteristics

Figure 15. Shutdown supply current vs. temperature, DE = GND, RE = V_{CC} @ V_{CC} = 3.3 V

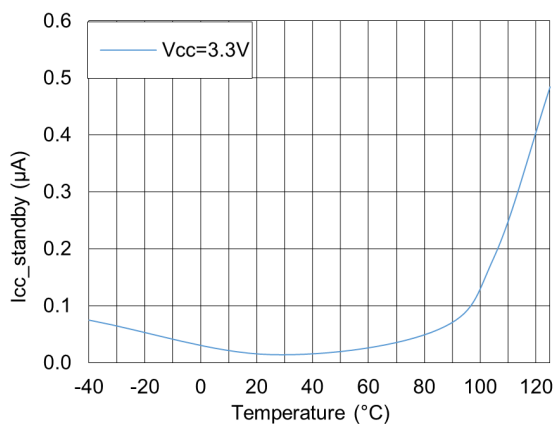


Figure 16. No-load supply current vs. temperature, DE = GND, RE = GND @ V_{CC} = 3.3 V

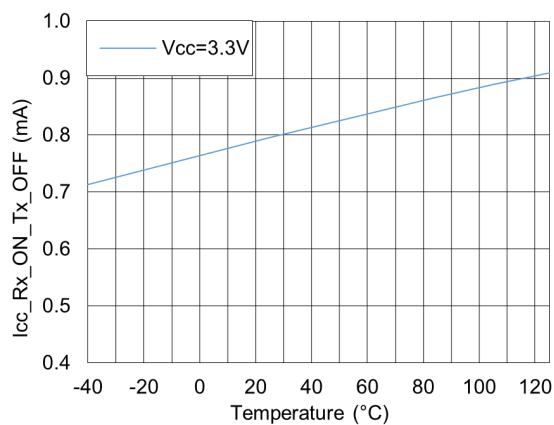


Figure 17. No-load supply current vs. temperature, DE = V_{CC}, RE = V_{CC} @ V_{CC} = 3.3 V

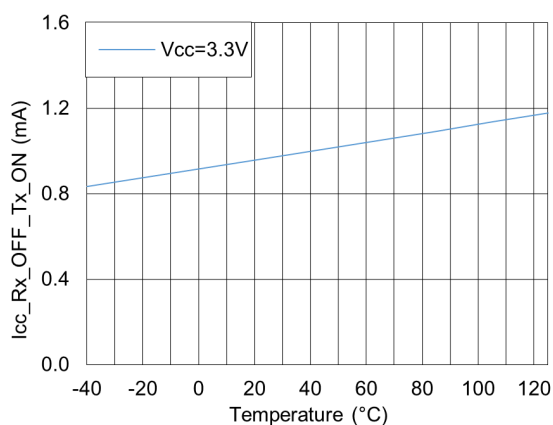


Figure 18. No-load supply current vs. temperature, DE = V_{CC}, RE = GND @ V_{CC} = 3.3 V

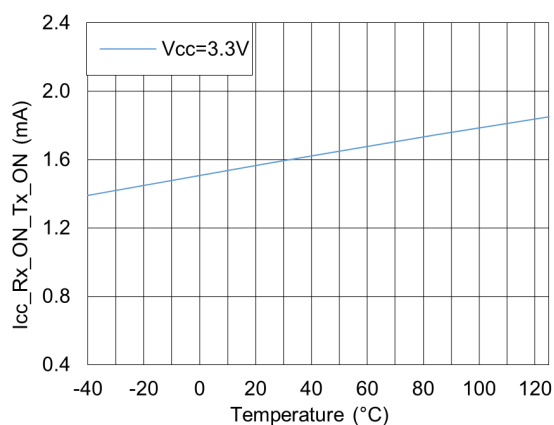


Figure 19. Driver output voltage vs. driver output current @ V_{CC} = 3.3 V

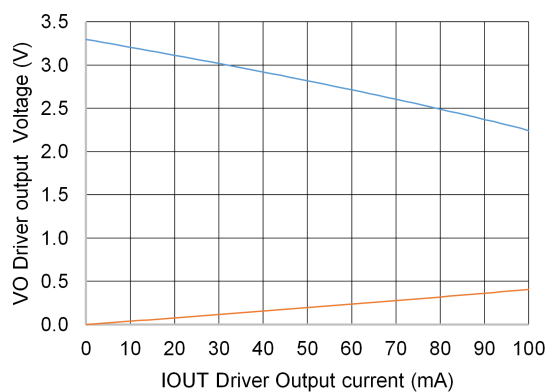


Figure 20. Driver differential output voltage vs. driver output current @ V_{CC} = 3.3 V

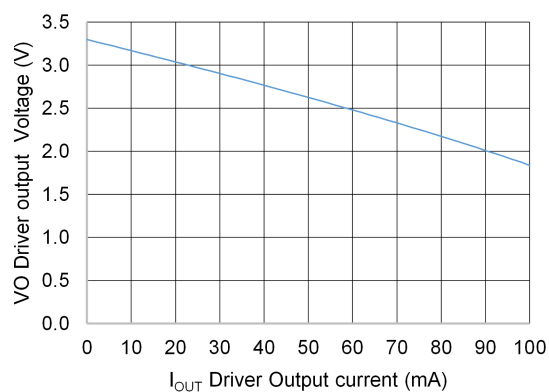


Figure 21. Driver output current vs. power supply with $R_L = 54 \Omega$

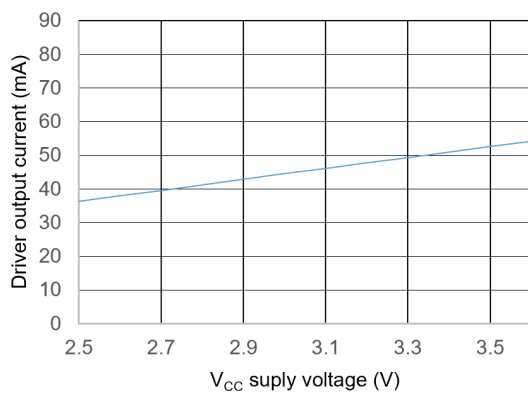


Figure 22. Differential driver output voltage vs. temperature @ $V_{CC} = 3.3 \text{ V}$

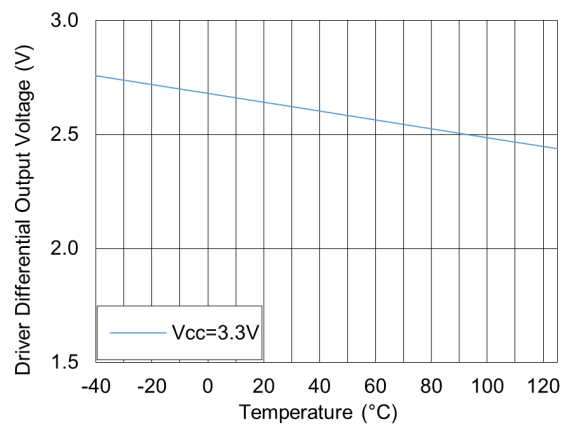


Figure 23. Driver rise time vs. temperature @ $V_{CC} = 3.3 \text{ V}$

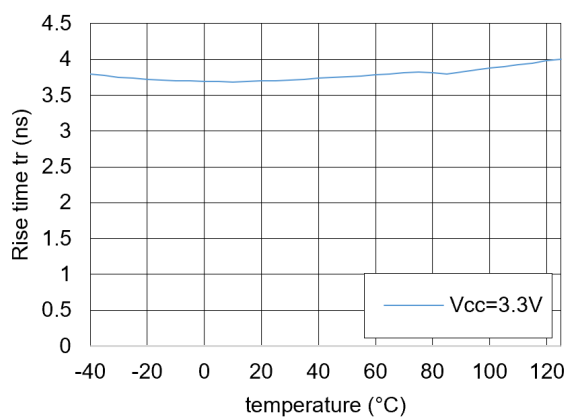


Figure 24. Receiver propagation delay vs. temperature, with $C_L = 20 \text{ pF}$ @ $V_{CC} = 3.3 \text{ V}$

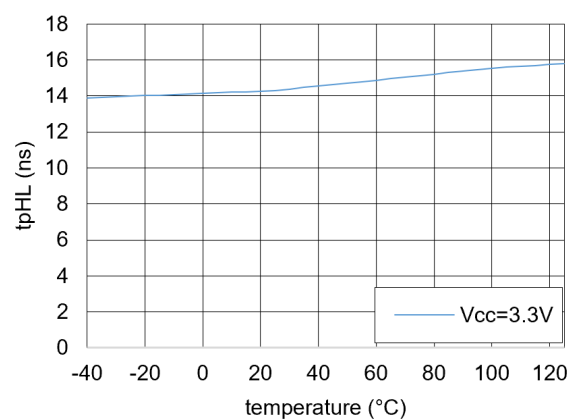


Figure 25. Driver fall times vs. temperature @ $V_{CC} = 3.3 \text{ V}$

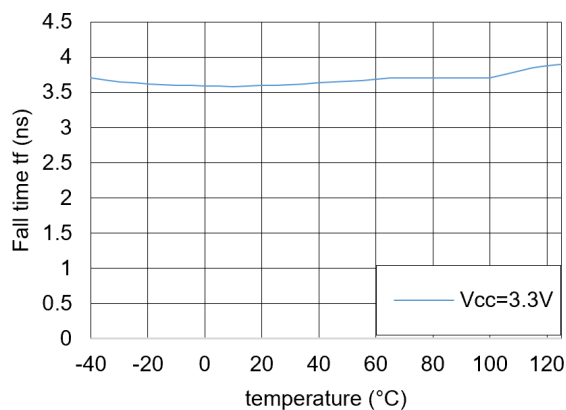


Figure 26. Driver propagation delay vs. temperature @ $V_{CC} = 3.3 \text{ V}$

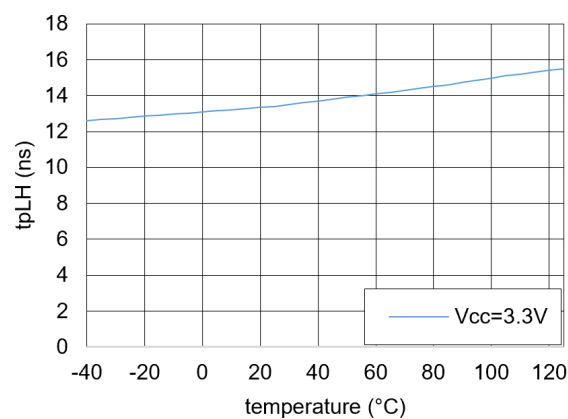


Figure 27. Supply current vs. data rate

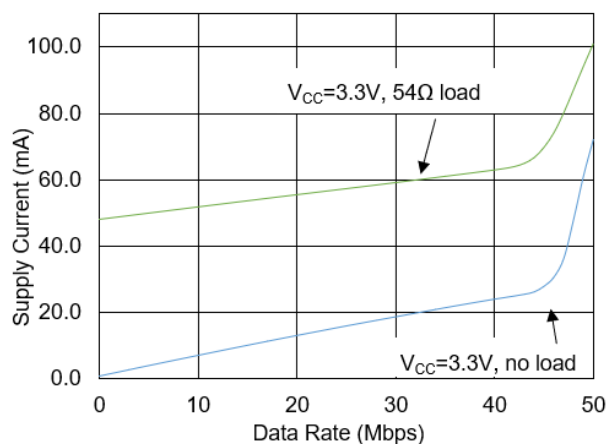


Figure 28. Receiver output vs. input @ $V_{CC} = 3.3 V$

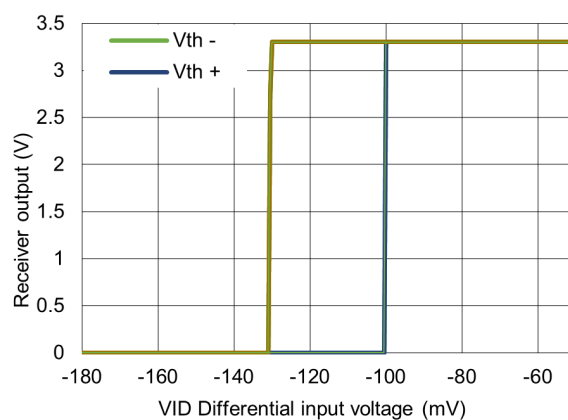


Figure 29. Receiver output. Eye diagram @ $V_{CC} = 3.3 V$, Data rate 20 Mbps, d = 100 m

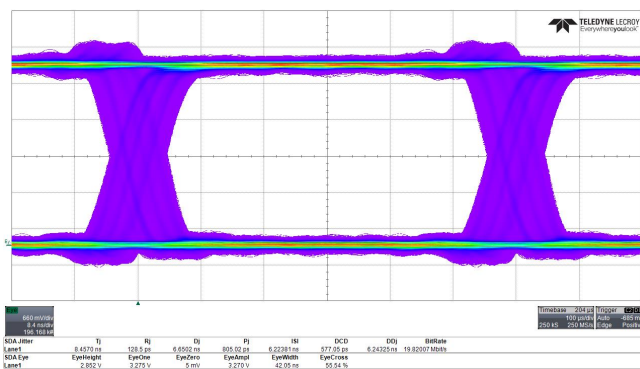
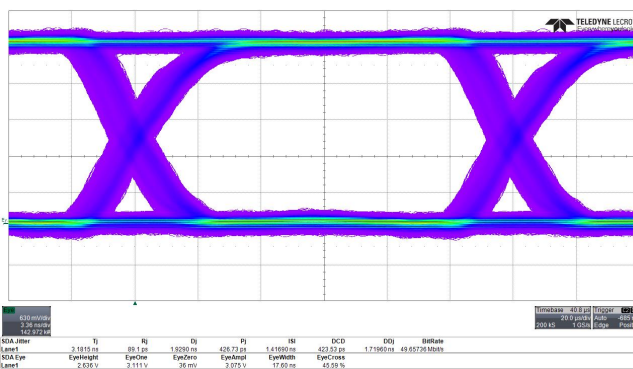


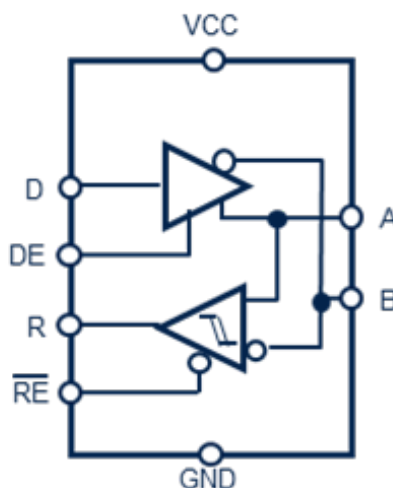
Figure 30. Receiver output. Eye diagram @ $V_{CC} = 3.3 V$ data rate 50 Mbps, d = 1 m



6 Detailed description

The ST4E1651 is a half-duplex differential RS-485 transceiver, suitable for data transmission up to 50 Mbps. The device supports up to 64 bus nodes. The receiver and driver are activated through the dedicated pins DE and $\overline{\text{RE}}$. Its functional block diagram is shown below.

Figure 31. Block diagram



Device functional modes

The ST4E1651 is designed for bidirectional data communications on multipoint bus transmission lines. Figure 14 shows a typical network application circuit. To minimize reflections, the line should be terminated at both ends with its characteristic impedance, and stub lengths should be kept as short as possible from the main line.

The various functional modes of ST4E1651 are detailed in the following function tables.

When the driver enable pin DE is high, the driver is enabled. The differential signal $V_{OD} = V_A - V_B$ follows the logic state of the signal present on input D, that is V_{OD} is positive if D is high, V_{OD} is negative when D is low.

When DE is logic low, A and B are set to high impedance, the driver is disabled, and D signal does not impact the outputs. The DE pin has an internal pull-down resistor to ground, which disables the driver by default if left open.

The D pin has an internal pull-up resistor to V_{CC} , thus when left open while the driver is enabled, output A is high and B low by default.

Table 11. Driver truth table

INPUT D	ENABLE DE	OUTPUT A	OUTPUT B	Function
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	Open	Z	Z	Driver disabled by default
Open	H	H	L	Actively drive bus high by default

When the receiver enable pin $\overline{\text{RE}}$ is logic low, the receiver is enabled. When the differential input voltage $V_{ID} = V_A - V_B$ is higher than the positive input threshold V_{TH+} , the receiver output R turns high. When V_{ID} is below the negative threshold V_{TH-} , the output R turns low. And when V_{ID} is in between the two threshold voltages, R is indeterminate.

If $\overline{\text{RE}}$ is logic high, R is high impedance, and the V_{ID} polarity and voltage do not impact it. The $\overline{\text{RE}}$ pin has an internal pull-up resistor, thus when left open, the receiver output is disabled by default.

The ST4E1651 architecture turns receiver output to fail-safe high state when the transceiver is disconnected from the bus (open), the bus lines A, B are shorted together (short), or the bus is not actively driven (idle).

Table 12. Receiver truth table

Differential input $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	Function
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	I	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	Open	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Shutdown mode

Shutdown mode is initiated when driving DE low and $\overline{RE}$ high. In this state the device draws less than 5 μA of current in all temperature and power supply conditions. Shutdown mode is entered in typically 2 μs at $V_{CC} = 3.3 V$ and an ambient temperature of 25 $^{\circ}C$.

Fail-safe receiver

The ST4E1651 has a fail-safe receiver to ensure a logic level on the bus and prevent any indeterminate state. The following conditions can be detected.

- Open bus such as a disconnected connector
- A shorted bus such as a damaged cable creating a short of the twisted pair
- An idle bus that occurs when no device on the bus is actively driving

In any of these cases, the differential receiver will drive a fail-safe logic high level so that the output of the receiver is not indeterminate.

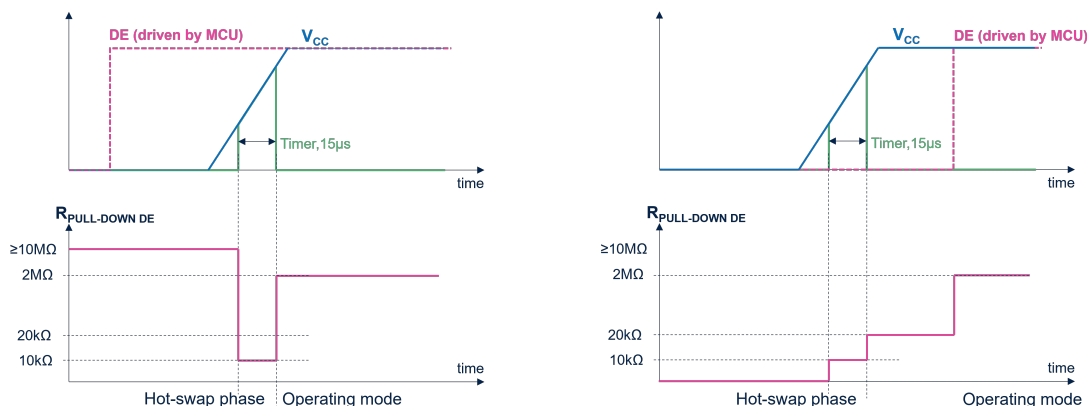
Hot-swap capability

The enable pins DE and $\overline{RE}$ are critical pins during a switch-on or plug-in phase on the RS485 bus. To prevent these pins from driving unwanted states due to possible disturbances during these steps, the ST4E1651 features an integrated hot-swap structure to avoid these potential problems.

Assuming a parasitic capacitance may be present on the board between the DE and GND nodes, or $\overline{RE}$ and V_{CC} ; when power supply rises, the MCU may drive an undetermined state on the DE and $\overline{RE}$ nodes. Depending on the input impedance on the DE and $\overline{RE}$ nodes, it can generate an unwanted signal on bus pins A, B.

A parasitic capacitance up to 100 pF is efficiently discharged with the hot-swap structure of the ST4E1651.

The new RS 485 transceiver dynamically manages the input impedance on DE and $\overline{RE}$ versus V_{CC} . A transient resistor of 10 k Ω is seen during the rising edge of the power supply, during a defined time of 15 μs typically. This allows fast discharge of parasitic capacitance, preventing any unwanted signal on the bus pins. A second typical transient resistor of 20 k Ω remains present until the V_{CC} supply is fully established. Then, the 2 M Ω pull-down resistor on DE and pull-up resistors on $\overline{RE}$ and D are connected during normal operating mode for current consumption considerations. An example is shown below for the impedance management on the DE terminal.

Figure 32. Hot-swap management with DE rising high before and after V_{CC}


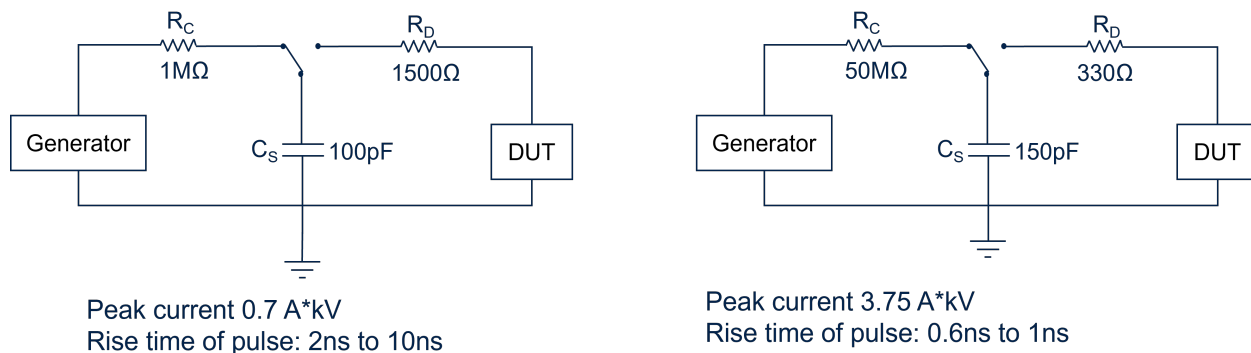
Electrostatic discharge (ESD) protection

The ST4E1651 has internal protection against Electrostatic Discharge (ESD).

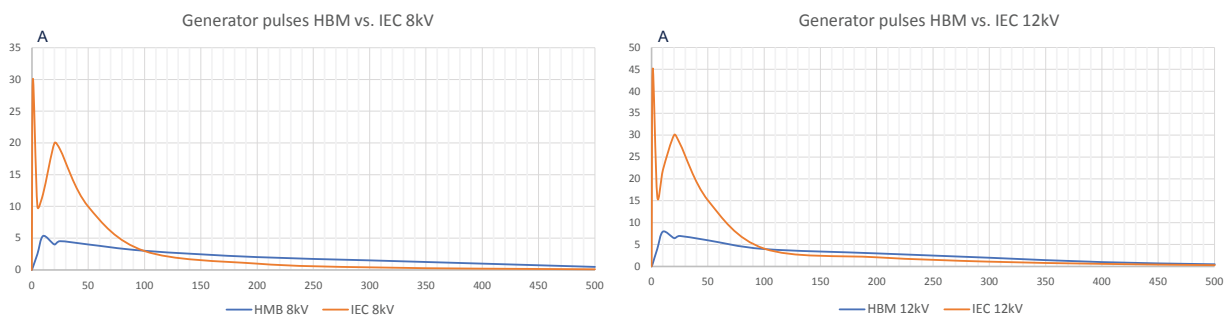
At circuit level, the ST4E1651 complies with the human body model (ANSI/ESDA/JEDEC JS-001) to guarantee robustness during the manufacturing process. All the pins of the ST4E1651 sustain 2 kV.

Because the ST4E1651 is part of a system and can be connected to its outside through the bus terminals A and B, an ESD protection is implemented on A and B to comply with the IEC 61000-4-2 standard.

The schematic below compares the simplified pulse generator between the circuit-level ESD pulse and the system-level ESD pulse.

Figure 33. HBM JEDEC (left) and IEC61000-4-2 (right) generator simplified schematics


For an equivalent ESD pulse voltage, the peak current and rise time of the pulse are much higher for the IEC61000-4-2 than for the HBM. This can be shown by the pulse diagrams below, for 8 kV and 12 kV respectively.

Figure 34. HBM JEDEC and IEC61000-4-2 waveforms comparison for different pulses


The IEC61000-4-2 standard is more severe than the HBM ESD test and significantly increases the robustness of the equipment. IEC61000-4-2 8 kV protections are commonly implemented.

The ST4E1651 increases furthermore the robustness of systems thanks to the dedicated IEC61000-4-2 16 kV protections on bus terminals A and B. There are two methods of ESD testing: contact discharge and air discharge. In the contact discharge method, the electrode of the test generator is held in contact with an exposed conductor on the Equipment Under Test (EUT). In the air discharge method, the electrode of the generator is moved from a distance towards the EUT until an arc occurs. The contact discharge offers the best reproducibility and is chosen to be the test method for IEC61000-4-2.

The ST4E1651 complies with IEC61000-4-2 16 kV contact discharge.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SO8 package information

Figure 35. SO8 package outline

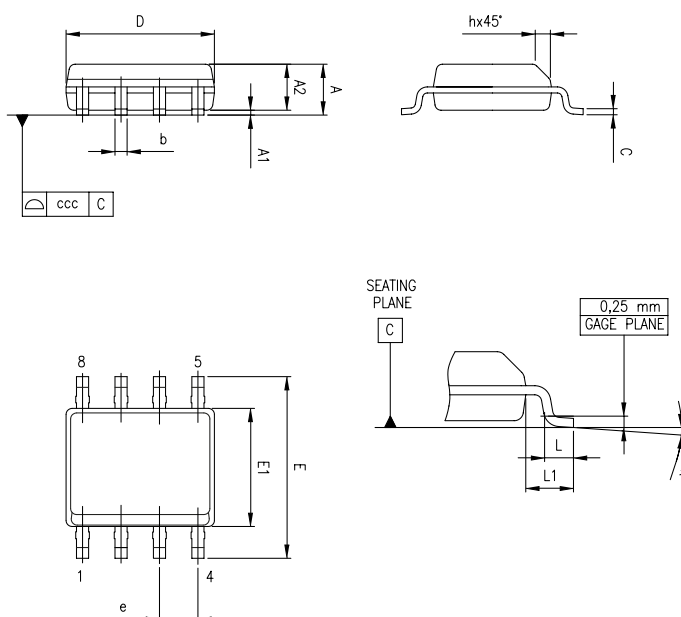
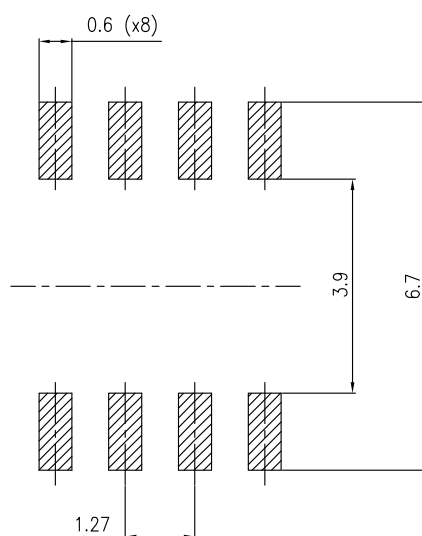


Table 13. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.04		0.010
A2	1.25			0.049		
b	0.28	0.40	0.48	0.011	0.016	0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40	0.635	1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

Figure 36. SO8 recommended footprint (mm)



8 Ordering information

Table 14. Order code

Order code	Temperature range	Package	Marking
ST4E1651IDT	-40 °C to +125 °C	SO8	O305

Revision history

Table 15. Document revision history

Date	Revision	Changes
30-Jul-2026	1	Initial release.

Contents

1	Pin configuration	2
2	Absolute maximum ratings and operating conditions	3
3	Electrical characteristics.....	4
4	Test circuits	8
5	Typical characteristics	12
6	Detailed description	15
7	Package information.....	19
7.1	SO8 package information.....	19
8	Ordering information	21
	Revision history	22

Prerelease product(s)

List of tables

Table 1.	Pin description.	2
Table 2.	Absolute maximum ratings	3
Table 3.	ESD ratings.	3
Table 4.	Operating conditions	4
Table 5.	Thermal information	4
Table 6.	Power dissipation.	4
Table 7.	Receiver: operating conditions ($V_{CC} = +3.0\text{ V to }3.6\text{ V}$, $T_A = T_{min}$ to T_{max} , unless otherwise specified. Typical values are $V_{CC} = 3.3\text{ V}$ and $T = 25\text{ °C}$).	5
Table 8.	Driver: operating conditions ($V_{CC} = +3.0\text{ V to }3.6\text{ V}$, $T_A = T_{min}$ to T_{max} , unless otherwise specified. Typical values are at $V_{CC} = 3.3\text{ V}$ and $T = 25\text{ °C}$).	6
Table 9.	Input logic interface (D, DE, $\overline{RE}$): ($V_{CC} = +3.0\text{ V to }3.6\text{ V}$, $T_A = T_{min}$ to T_{max} , unless otherwise specified. Typical values are $V_{CC} = 3.3\text{ V}$ and $T = 25\text{ °C}$).	6
Table 10.	Supply current and protections: ($V_{CC} = +3.0\text{ V to }3.6\text{ V}$, $T_A = T_{min}$ to T_{max} , unless otherwise specified. Typical values are $V_{CC} = 3.3\text{ V}$ and $T = 25\text{ °C}$).	7
Table 11.	Driver truth table	15
Table 12.	Receiver truth table	16
Table 13.	SO8 package mechanical data	19
Table 14.	Order code	21
Table 15.	Document revision history	22

List of figures

Figure 1.	Pin connections	2
Figure 2.	Driver differential output voltage with common-mode load	8
Figure 3.	Driver differential and common-mode output with RS-485 load	8
Figure 4.	Driver differential output rise and fall times and propagation delays	8
Figure 5.	Driver enable and disable times with active high output and pull-down load	9
Figure 6.	Driver enable and disable times with active low output and pull-up load	9
Figure 7.	Receiver output rise and fall times and propagation delay	9
Figure 8.	Receiver enable/disable times with driver enabled.	10
Figure 9.	Receiver enable/disable times with driver disabled	10
Figure 10.	Receiver input current	10
Figure 11.	Receiver output current	10
Figure 12.	Receiver threshold and hysteresis.	11
Figure 13.	Short-circuit output current measurement.	11
Figure 14.	Typical half-duplex RS485 network	11
Figure 15.	Shutdown supply current vs. temperature, DE = GND, $\overline{RE} = V_{CC}$ @ $V_{CC} = 3.3\text{ V}$	12
Figure 16.	No-load supply current vs. temperature, DE = GND, $\overline{RE} = \text{GND}$ @ $V_{CC} = 3.3\text{ V}$	12
Figure 17.	No-load supply current vs. temperature, DE = V_{CC} , $\overline{RE} = V_{CC}$ @ $V_{CC} = 3.3\text{ V}$	12
Figure 18.	No-load supply current vs. temperature, DE = V_{CC} , $\overline{RE} = \text{GND}$ @ $V_{CC} = 3.3\text{ V}$	12
Figure 19.	Driver output voltage vs. driver output current @ $V_{CC} = 3.3\text{ V}$	12
Figure 20.	Driver differential output voltage vs. driver output current @ $V_{CC} = 3.3\text{ V}$	12
Figure 21.	Driver output current vs. power supply with $R_L = 54\ \Omega$	13
Figure 22.	Differential driver output voltage vs. temperature @ $V_{CC} = 3.3\text{ V}$	13
Figure 23.	Driver rise time vs. temperature @ $V_{CC} = 3.3\text{ V}$	13
Figure 24.	Receiver propagation delay vs. temperature, with $C_L = 20\text{ pF}$ @ $V_{CC} = 3.3\text{ V}$	13
Figure 25.	Driver fall times vs. temperature @ $V_{CC} = 3.3\text{ V}$	13
Figure 26.	Driver propagation delay vs. temperature @ $V_{CC} = 3.3\text{ V}$	13
Figure 27.	Supply current vs. data rate	14
Figure 28.	Receiver output vs. input @ $V_{CC} = 3.3\text{ V}$	14
Figure 29.	Receiver output. Eye diagram @ $V_{CC} = 3.3\text{ V}$, Data rate 20 Mbps, d = 100 m	14
Figure 30.	Receiver output. Eye diagram @ $V_{CC} = 3.3\text{ V}$ data rate 50 Mbps, d = 1 m	14
Figure 31.	Block diagram	15
Figure 32.	Hot-swap management with DE rising high before and after V_{CC}	17
Figure 33.	HBM JEDEC (left) and IEC61000-4-2 (right) generator simplified schematics	17
Figure 34.	HBM JEDEC and IEC61000-4-2 waveforms comparison for different pulses.	17
Figure 35.	SO8 package outline	19
Figure 36.	SO8 recommended footprint (mm)	20

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