ST4E1650F

Datasheet

50 Mbps, full-duplex RS485 transceiver with ±16 kV IEC 61000-4-2 contact ESD protection

DFN10 (3 x 3 mm)

Maturity status link
ST4E1650F

Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 3 V to 3.6 V supply voltage
- High speed: up to 50 Mbps data rate
- Up to 128 bus nodes
- Receiver hysteresis of 70 mV
- Full-duplex topology
- Integrated protections
  - Fail-safe receiver (bus open, idle, and shorted)
  - Thermal shutdown protection
  - Hot swap capability
  - Bus I/O ESD protection
    - ±16 kV IEC61000-4-2 contact discharge
    - ±30 kV HBM
    - ±4 kV IEC61000-4-4 fast transient burst
- Low quiescent current in shutdown mode
- -40 °C to +125 °C operating temperature
- Available in DFN10 industry standard

Applications

- Motion controllers
- Optical network
- Building automation and safety
- Video surveillance (building, traffic monitoring)
- Backplane bus
- Grid infrastructure
- Robotics

Description

The ST4E1650F is a low-power differential line transceiver for data transmission standard RS485 applications in full-duplex mode.

The ST4E1650F operates up to 50 Mbps. It is ideal for multi-point applications in a constrained and difficult industrial environment. It is robust to ESD transients. In particular, the bus pins support ±16 kV IEC 61000-4-2 contact discharge. It features robust hot-swap capability during switching on and off, or during plug-in. The fail-safe receiver ensures a logic-high output when the inputs are shorted, open, or indeterminate. The high level of receiver hysteresis improves the noise rejection and the signal integrity.

The ST4E1650F is available in a small 3 mm x 3 mm DFN10 package and operates in a -40 °C to 125 °C temperature range.

1 Pin configuration

Figure 1. Pin connections

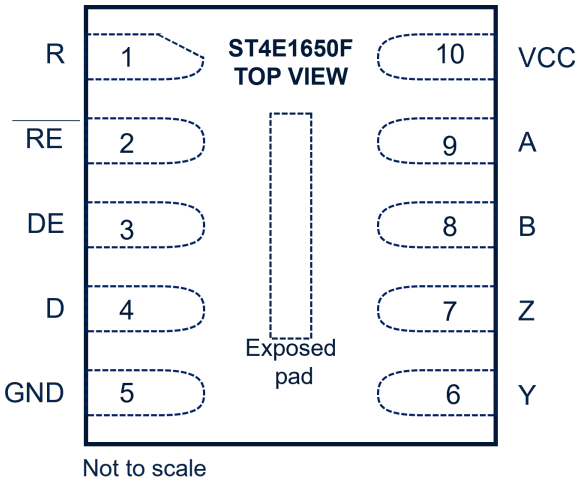


Table 1. Pin description

Name	Pin	I/O	Description
R	1	Digital output	Receiver data output
$\overline{RE}$	2	Digital input	Receiver enable input, active low (2 MΩ internal pull-up)
DE	3	Digital input	Driver enable input, active high (2 MΩ internal pull-down)
D	4	Digital input	Transmission data input
GND	5	Ground	
Y	6	Bus output	Digital bus output
Z	7	Bus output	Digital bus output
B	8	Bus input	Digital bus input
A	9	Bus input	Digital bus input
VCC	10	Device supply	3 V to 3.6 V supply voltage
EP	EP	Exposed Pad	Connect EP to ground

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Device supply voltage	-0.5	7	V
	Voltage range at A, B, Y and Z terminals	-9	14	V
	Input voltage range at any logic pin (referred to an operating V_{CC})	-0.3	V_{CC}+0.3	V
	Short-circuit duration (R, A, B, Y, Z) to GND	Continuous		
T_{stg}	Storage temperature	-65	150	°C

Note: All voltage values, except the differential voltage, are referred to the network ground terminal.

Table 3. ESD ratings

Symbol	Parameter	Value	Unit
ESD	IEC61000-4-2 ESD (contact discharge), bus terminals and GND	± 16	kV
	IEC61000-4-4 EFT (fast transient or burst) bus terminals and GND	± 4	kV
	HBM, bus terminals and GND	± 30 (1) (2)	kV
	JEDEC standard 22, test method A114, HBM, all other terminals	± 2	kV
	JEDEC standard 22, test method C101, (charged device model), all pins	±1	kV

1. *JEDEC document JEP155 states that 500 V HBM allows for safe manufacturing with a standard ESD control process.*
2. *JEDEC standard 22, test method A114, HBM (Human Boby Model), bus terminals (A, B, Y, Z), ≥ ±8 kV (limited by industrial tester capability).*

   Measurement for 20 A peak, 100 ns Transmission-Line Pulse (TLP), package level at room temperature.

3 Electrical characteristics

Table 4. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Device supply voltage	3		3.6	V
V_I	Input level at any bus terminal (separated or common-mode)	-7		12	V
IO	Output current / driver Y, Z	-70		70	mA
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
D_R	Signaling rate			50	Mbps
T_A	Operating free-air temperature	-40		125	°C

Operation is specified for internal (junction temperature) up to 150 °C. Self-heating due to internal power dissipation should be considered for each application. The maximum junction temperature is internally limited by the thermal shut-down circuit, which disables the driver outputs when the junction temperature reaches 170 °C.

Table 5. Thermal information

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{th-ja}	Thermal resistance, junction-to-ambient EP connected to ground and use of thermal vias		55		°C/W

Table 6. Power dissipation

Symbol	Parameter	Test conditions	Typ.	Unit
P_D	Power dissipation, with driver and receiver enabled V_{CC} = 3.6 V, T = 125 °C, 50% duty cycle at max signaling rate	Unterminated, R_L = 300 Ω, C_L = 50 pF	161	mW
		RS485-load: R_L = 54 Ω, C_L = 50 pF	163	mW

Table 7. Receiver: operating conditions (V_{CC} = +3.0 V to 3.6 V, $T_A = T_{min}$ to T_{max}, unless otherwise specified. Typical values are V_{CC} = 3.3 V and T = 25 °C).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Receiver / DC						
V_{TH+}	Positive-going input threshold voltage	-7 V ≤ V_{CM} ≤ 12 V		-62	-10	mV
V_{TH-}	Negative-going input threshold voltage	-7 V ≤ V_{CM} ≤ 12 V	-200	-137		
V_{HYS}	Receiver differential input voltage hysteresis	Figure 12	40	75		
V_{OH}	Receiver high-level output voltage	$\overline{RE}$ = GND, I_{OH} = - 2 mA, (VA-VB) > 200 mV	V_{CC}-0.2	Vcc-0.12		V
V_{OL}	Receiver low-level output voltage	$\overline{RE}$ = GND, I_{OL} = 2 mA, (VA-VB) < -200 mV		GND+0.05	0.2	
I_{OZ}	Receiver output high-impedance current	0 ≤ VR ≤ V_{CC}, $\overline{RE}$ = V_{CC}. Figure 11	-1		1	µA
I_{OS}	Receiver output short-circuit current	0≤ VR ≤ V_{CC}. Figure 11	-90		90	mA
I_i	Receiver input current DE = GND, V_{CC} = GND or +3.6 V	V_I = 12 V – Figure 10		108	250	µA
		V_I = -7 V – Figure 10	-200	-117		
R_{in}	Receiver input impedance	-7 V ≤ V_{incm} ≤ +12 V	48			kΩ
Receiver/ switching characteristics						
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF	1	3	6	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			37	50	ns
$t_{SK(P)}$	Receiver pulse skew, | t_{PHL}–t_{PLH}|, ΔV_{in} = 1.5 V				2.5	ns
t_{PLZ}	Receiver disable time, from low	C_L = 15 pF with 1 kΩ		14	30	ns
t_{PHZ}	Receiver disable time, from high	C_L = 15 pF with 1 kΩ		13	30	ns
t_{PZH}	Receiver enable time to output high	Driver enabled C_L = 15 pF with 1 kΩ		45	60	ns
t_{PZL}	Receiver enable time to output low	Driver enabled C_L = 15 pF with 1 kΩ		10	30	ns
$t_{PZH(shdn)}$	Receiver enable time from shutdown to output high	Driver disabled C_L = 15 pF with 1 kΩ			100	ns
$t_{PZL(shdn)}$	Receiver enable time from shutdown to output low	Driver disabled C_L = 15 pF with 1 kΩ			100	ns

Table 8. Driver: operating conditions (V_{CC} = +3.0 V to 3.6 V, T_A = T_{min} to T_{max}, unless otherwise specified. Typical values are V_{CC} = 3.3 V and T = 25 °C).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC driver / DC						
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω / 375 Ω Figure 2 -7 V ≤ VCM ≤ +12 V	1.5			V
		R_L = 54 Ω Figure 3	1.5	2.4		
		R_L = 100 Ω (RS422) V_{CC} ≥ 3.0 V	2			
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF	-70		+70	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27 Ω load resistors	1	2.43	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage		-0.12	-0.02	0.12	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage			0.9		
V_{OH}	Single-ended driver output high	Y or Z output, I_A or I_B = -20 mA	VCC-0.4			V
V_{OL}	Single-ended driver output low	Y or Z output, I_A or I_B = 20 mA			0.4	V
COD	Differential output capacitance	DE = $\overline{RE}$ = V_{CC}, f = 4 MHz		22		pF
C_{AB}	Differential input capacitance	DE = $\overline{RE}$ = GND, f = 4 MHz		10		pF
Driver/switching characteristics						
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF		4	6	ns
t_{PHL}, t_{PLH}	Driver propagation delay			13	20	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL}–t_{PLH}\|$				2	
t_{PLZ}, t_{PHZ}	Driver disable time				25	
t_{PZL}, t_{PZH}	Driver enable time	Receiver enabled			25	
		Receiver disabled			25	ns

Table 9. Input logic interface (D, DE, $\overline{RE}$): (V_{CC}= +3.0 V to 3.6 V, T_A = T_{min} to T_{max}, unless otherwise specified. Typical values are V_{CC} = 3.3 V and T = 25 °C).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		0.7 x V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{In}	Input current	3 V ≤V_{CC} ≤ 3.6 V, V_{in} = 0 or V_{CC}	-5		5	µA
	Input impedance on first transition (DE, $\overline{RE}$)		3		10	kΩ

Table 10. Supply current and protections: (V_{CC} = +3.0 V to 3.6 V, T_A = T_{min} to T_{max}, unless otherwise specified. Typical values are V_{CC} = 3.3 V and T = 25 °C).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current						
I_{CC}	Supply current (quiescent)	Driver and receiver enabled DE = V_{CC}, $\overline{RE}$ = GND, no load		2	4	mA
		Driver enabled, receiver disabled DE = V_{CC}, $\overline{RE}$ = V_{CC}, no load		1.1	2.8	mA
		Driver disabled, receiver enabled DE = GND, $\overline{RE}$ = GND, no Load		1.1	2.1	mA
		Driver and receiver disabled (shutdown mode) DE = GND, $\overline{RE}$= V_{CC}, No load		0.2	10	µA
T_{TSD}	Thermal shutdown threshold			170		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			13		
I_{OS}	Driver short-circuit output current	-7 V < V_{SHORT} < + 12 V	-250		250	mA

4 Test circuits

In the schematics below, C_L includes fixture and instrumentation capacitance.

Figure 2. Driver differential output voltage with common-mode load

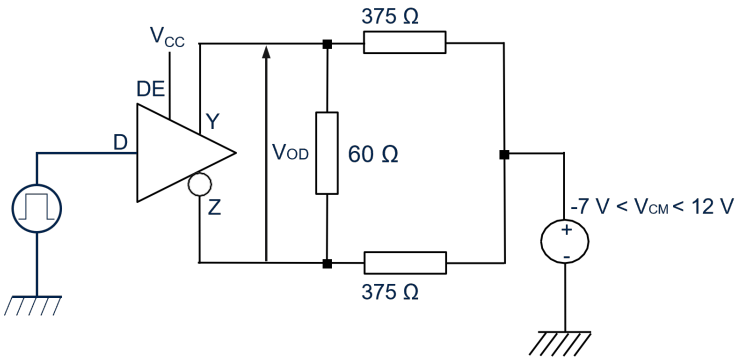


Figure 3. Driver differential and common-mode output with RS-485 load

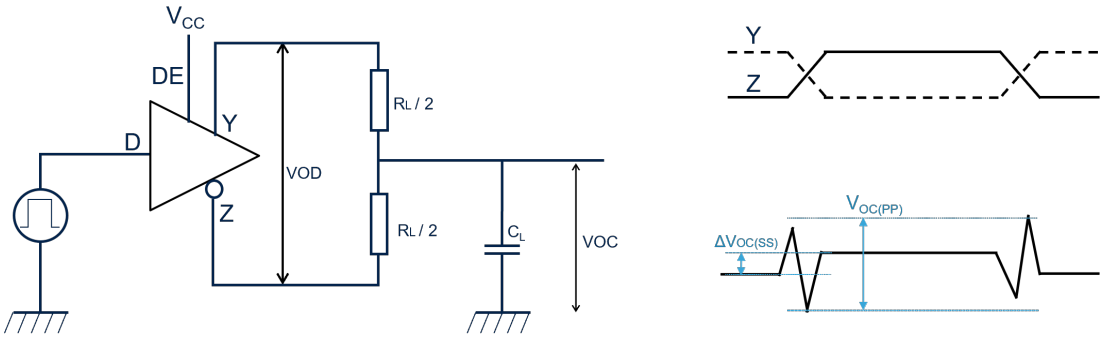


Figure 4. Driver differential output rise and fall times and propagation delays

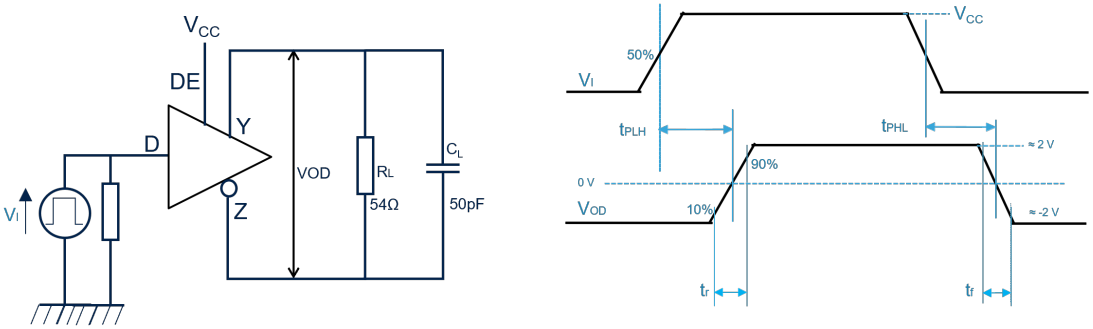


Figure 5. **Driver enable and disable times with active high output and pull-down load**

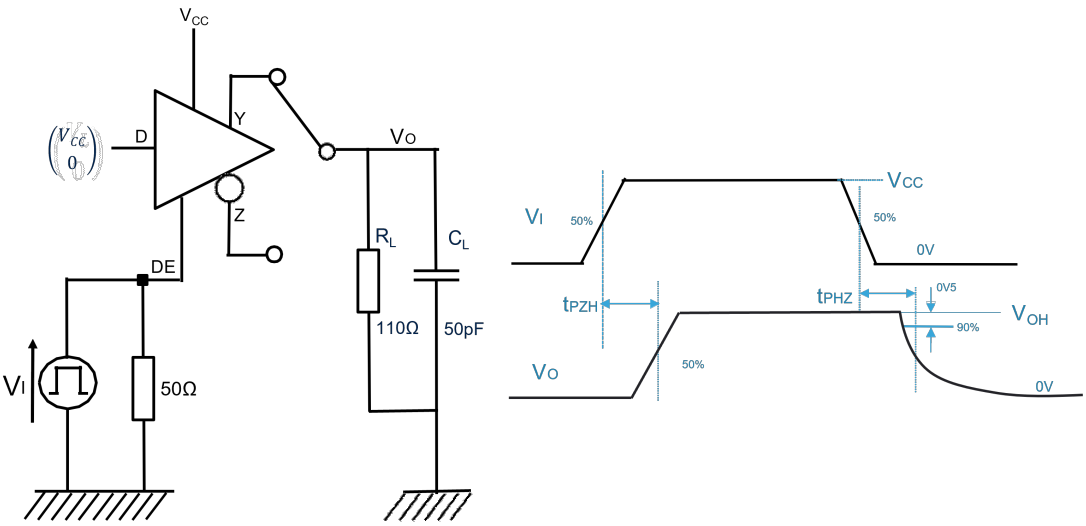


Figure 6. **Driver enable and disable times with active low output and pull-up load**

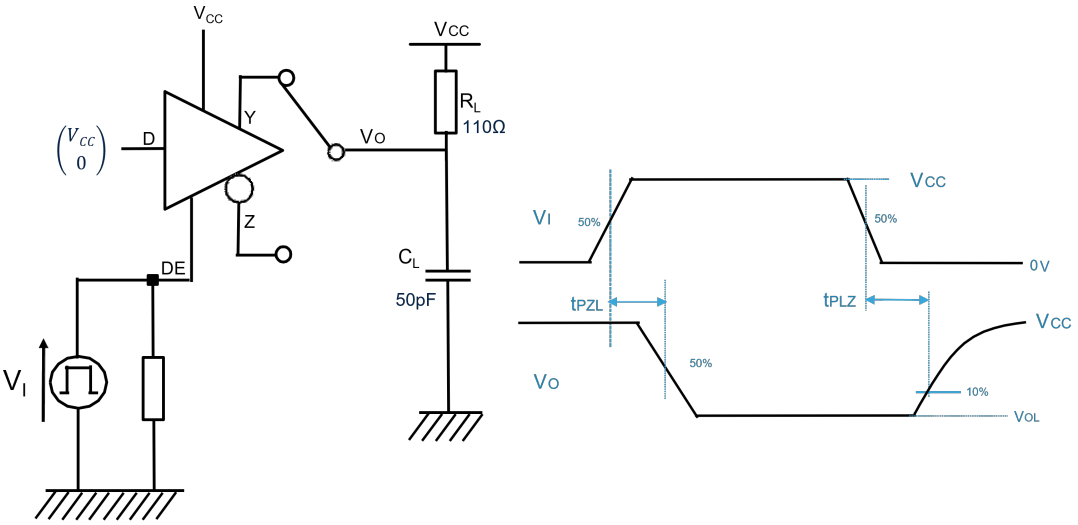


Figure 7. **Receiver output rise and fall times and propagation delay**

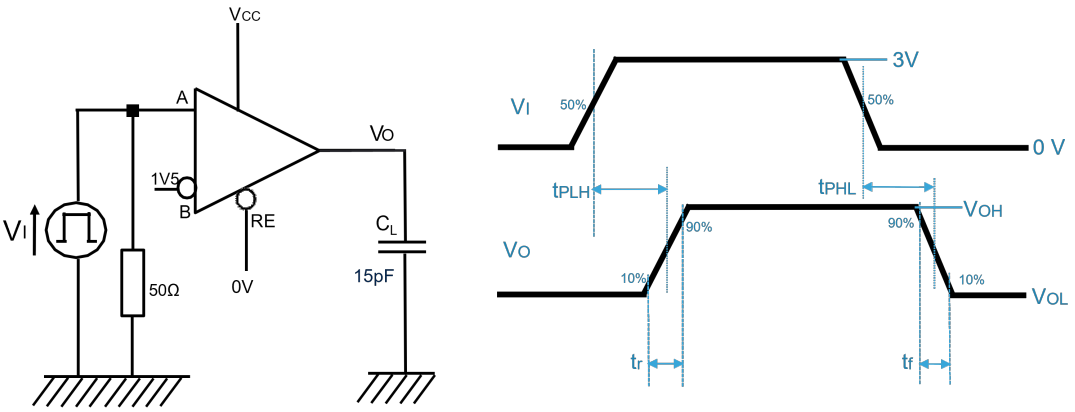


Figure 8. **Receiver enable/disable times with driver enabled**

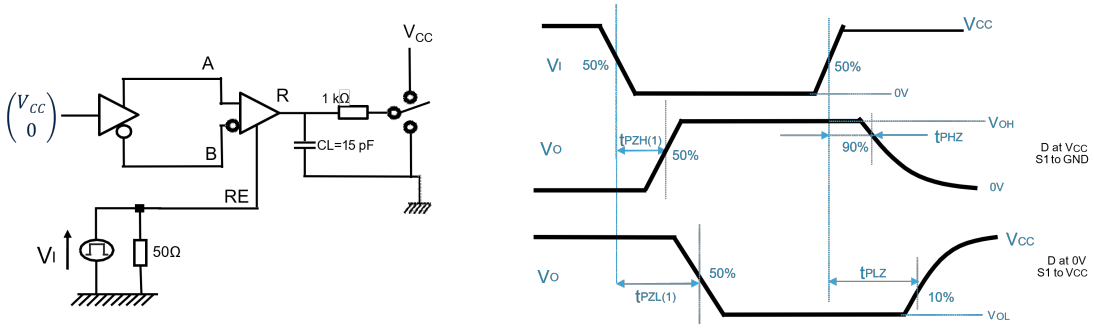


Figure 9. **Receiver enable/disable times with driver disabled**

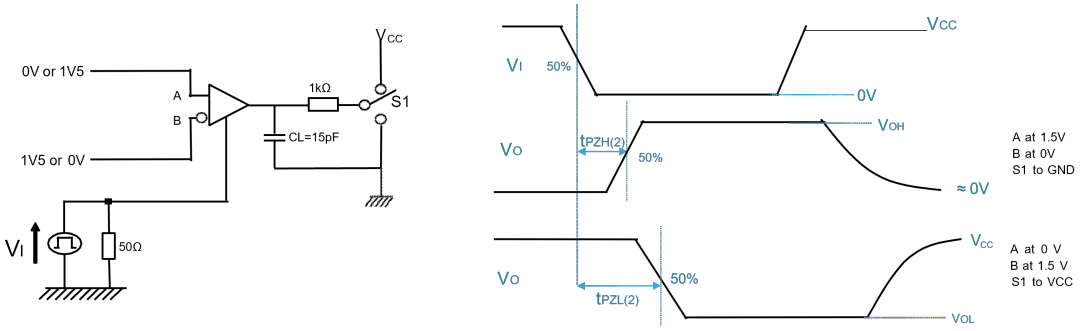


Figure 10. **Receiver input current**

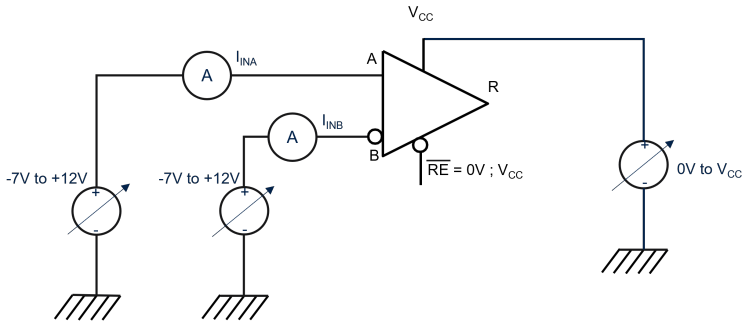


Figure 11. **Receiver output current**

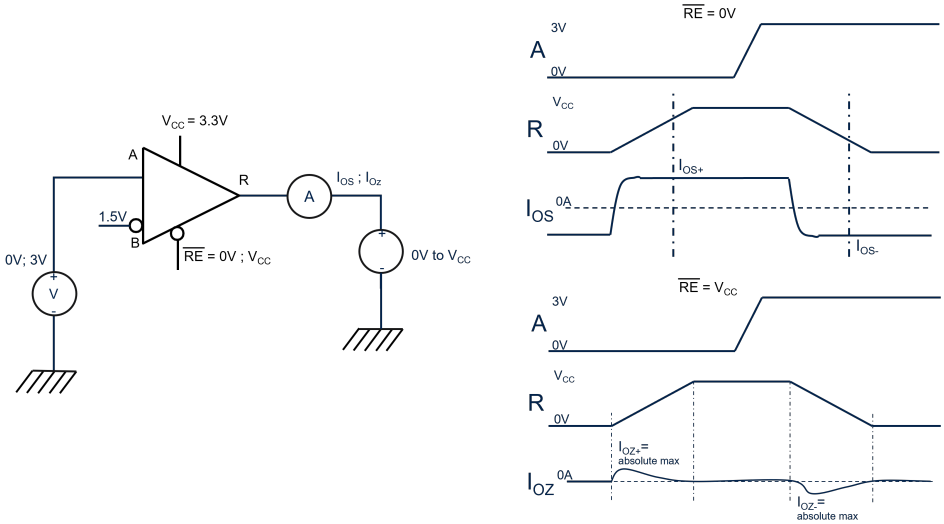


Figure 12. **Receiver threshold and hysteresis**

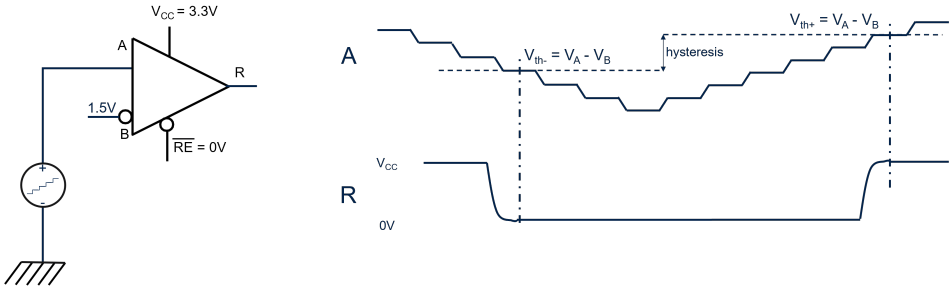
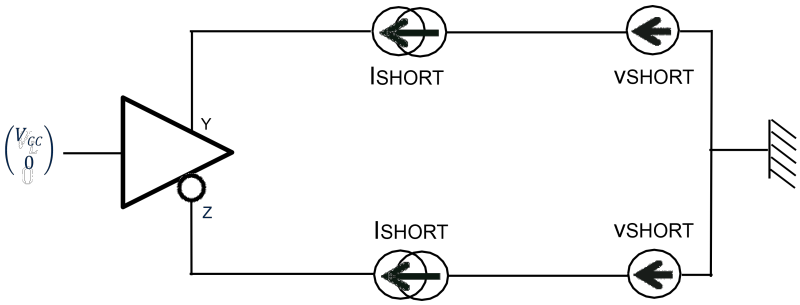
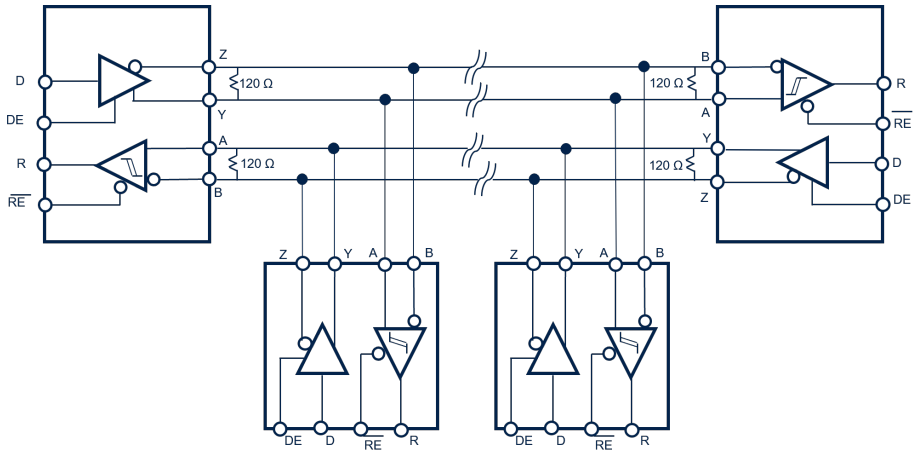


Figure 13. **Short-circuit output current measurement**



When one of the driver outputs is shorted to a voltage source (named V_{SHORT}) between -7 V to +12 V stabilized, the current does not exceed 250 mA and the driver is protected.

Figure 14. **Typical full-duplex RS485 network**



5 Typical characteristics

Figure 15. Driver output voltage vs. driver output current @ V_{CC} = 3.3 V

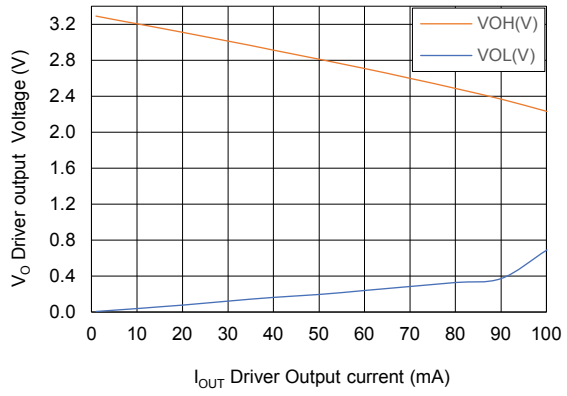


Figure 16. Driver differential output voltage vs. driver output current @ V_{CC} = 3.3 V

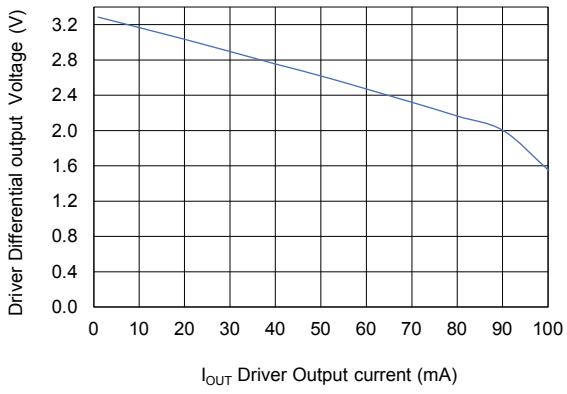


Figure 17. Receiver output vs. input @ V_{CC} = 3.3 V

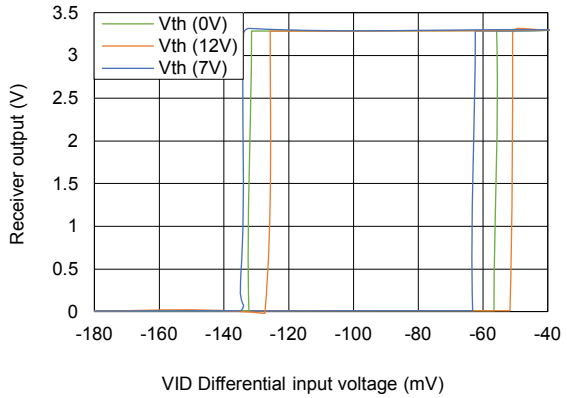


Figure 18. Driver output current vs. power supply with R_L = 54 Ω

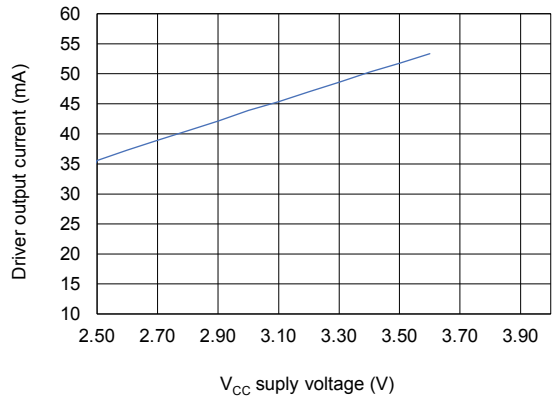


Figure 19. Supply current vs. data rate

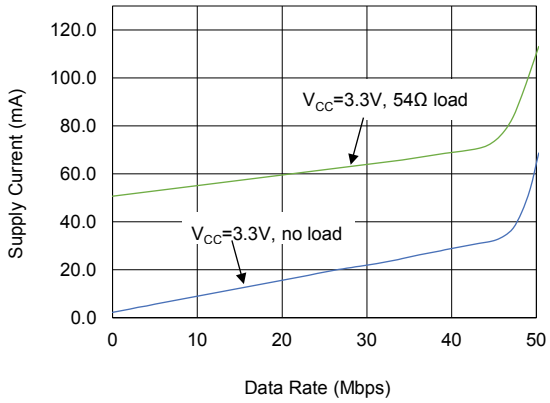


Figure 20. Shutdown current vs. temperature, DE = GND, $\overline{RE}$ = V_{CC}

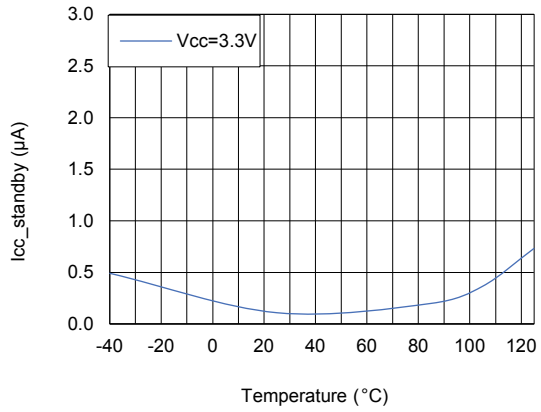


Figure 21. No-load supply current vs. temperature, DE = GND, $\overline{RE}$ = GND

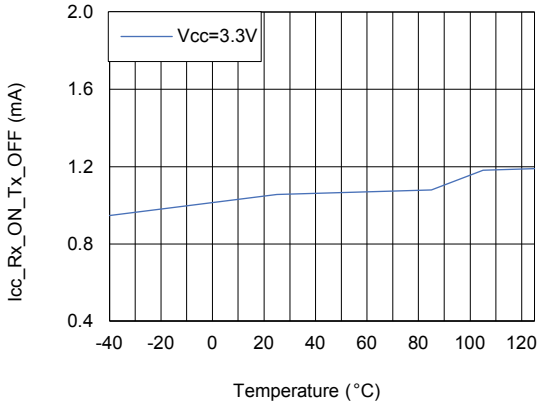


Figure 22. No-load supply current vs. temperature, DE = V_{CC}, $\overline{RE}$ = V_{CC}

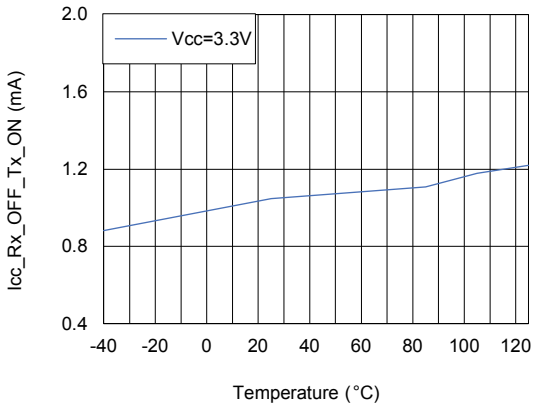


Figure 23. No-load supply current vs. temperature, DE = V_{CC}, $\overline{RE}$ = GND

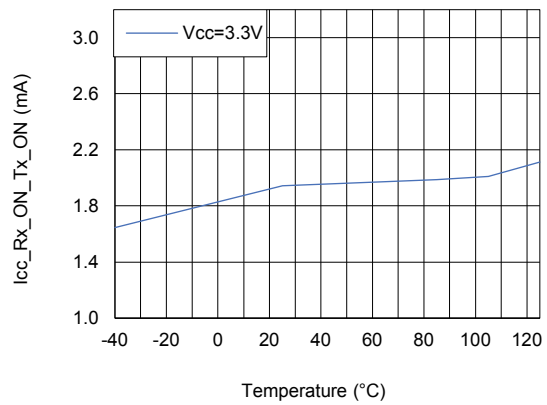


Figure 24. Differential driver output voltage vs. temperature

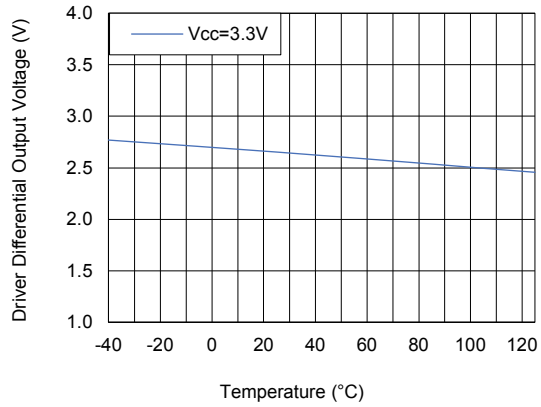


Figure 25. Driver rise and fall times vs. temperature @ V_{CC} = 3.3 V

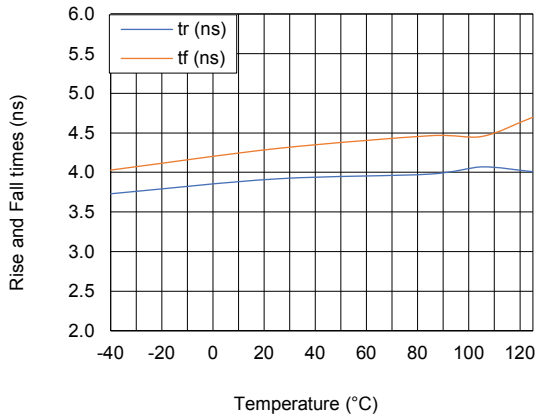


Figure 26. Driver propagation delay vs. temperature @ V_{CC} = 3.3 V

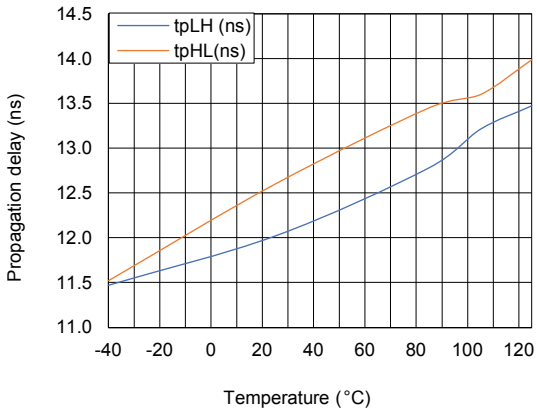


Figure 27. Receiver propagation delay vs. temperature, with C_L = 20 pF

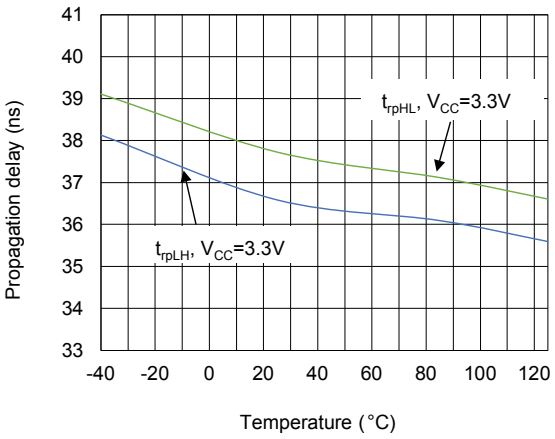


Figure 28. Eye diagram 10 Mbps short line (≤ 1 m)

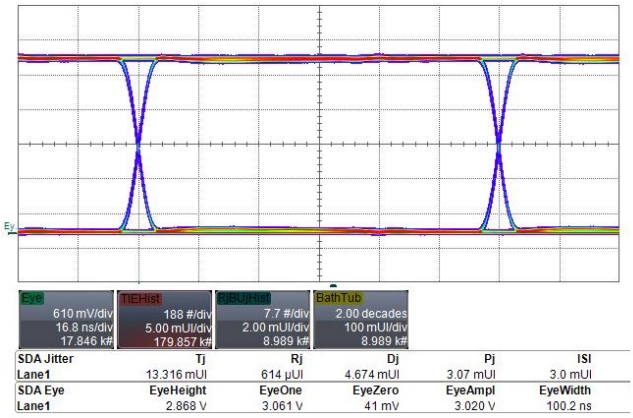
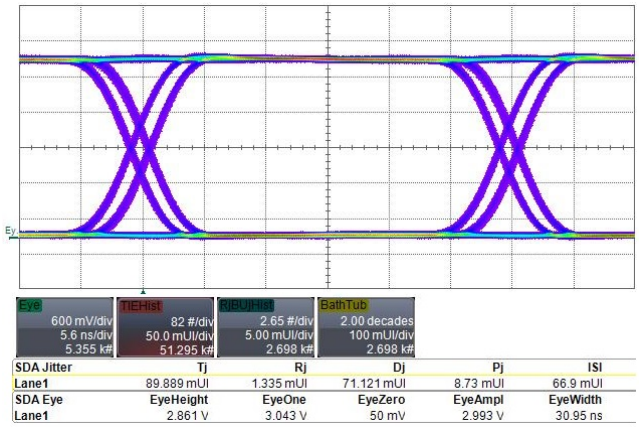


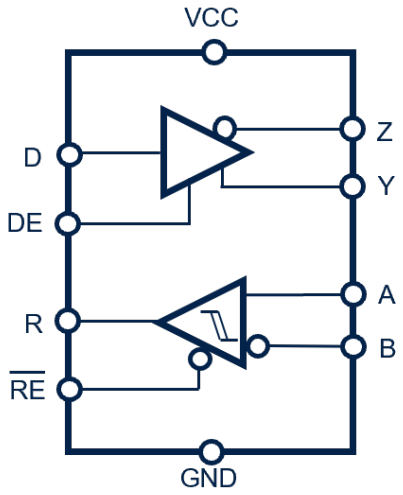
Figure 29. Eye diagram 30 Mbps short line (≤ 1 m)



6 Detailed description

The ST4E1650F is a full-duplex differential RS-485 transceiver, suitable for data transmission up to 50 Mbps. The device supports one fourth of a unit load, so up to 128 bus nodes can be set. Its functional block diagram is shown below.

Figure 30. Block diagram



Device functional modes

The various functional modes of the ST4E1650F are detailed in the following function tables.

When the driver enable pin DE is high, the driver is enabled. The differential signal $V_{OD} = V_Y - V_Z$ follows the logic state of the signal present on input D, so V_{OD} is positive if D is high, V_{OD} is negative when D is low.

In normal operating mode, the D pin has an internal 2 MΩ pull-up resistor to V_{CC}, thus when left open while the driver is enabled, output Y is high and Z low by default.

When DE is logic low, Y and Z are set to high impedance, the driver is disabled, and the D signal does not impact the outputs. In normal operating mode, the DE pin has an internal 2 MΩ pull-down resistor to ground, which disables the driver by default if left open.

Table 11. Driver truth table

INPUT D	ENABLE DE	OUTPUT Y	OUTPUT Z	Function
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	Open	Z	Z	Driver disabled by default by 2 MΩ pull-down
Open	H	H	L	Actively drive bus high by default by 2 MΩ pull-up

When the receiver enable pin $\overline{RE}$ is logic low, the receiver is enabled. When the differential input voltage $V_{ID} = V_A - V_B$ is higher than the positive input threshold V_{TH+}, the receiver output R becomes high. When V_{ID} is below the negative threshold V_{TH-}, the output R becomes low. And when V_{ID} is in between the two threshold voltages, R is indeterminate.

If $\overline{RE}$ is logic high, R is high impedance, and the V_{ID} polarity and voltage do not impact it. The $\overline{RE}$ -pin has an internal 2 MΩ pull-up resistor, thus when left open, the receiver output is disabled by default.

The ST4E1650F architecture turns receiver output to fail-safe high state when the transceiver is disconnected from the bus (open), the bus lines A, B are shorted together (short), or the bus is not actively driven (idle).

Table 12. **Receiver truth table**

Differential input $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	Function
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	I	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	Open	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Shutdown mode

Shutdown mode is initiated when driving DE low and $\overline{RE}$ high. In this state, the device draws less than 1 µA of current in all temperature and power supply conditions. Shutdown mode is typically entered within 2 µs at V_{CC} = 3.3 V and ambient temperature of 25 °C.

The ST4E1650F is designed for bidirectional data communications on multipoint bus transmission lines. Figure 11 shows a typical network application circuit. To minimize reflections, the line should be terminated at both ends with its characteristic impedance, and stub lengths should be kept as short as possible from the main line.

Fail-safe receiver

The ST4E1650F has a fail-safe receiver to ensure a logic level on the bus and prevent any indeterminate state. The following conditions can be detected.

- Open bus, such as a disconnected connector
- A shorted bus, such as a damaged cable creating a short of the twisted pair
- An idle bus, which occurs when no device on the bus is actively driving

In any of these cases, the differential receiver will drive a fail-safe logic high level so that the output of the receiver is not indeterminate.

Hot-swap capability

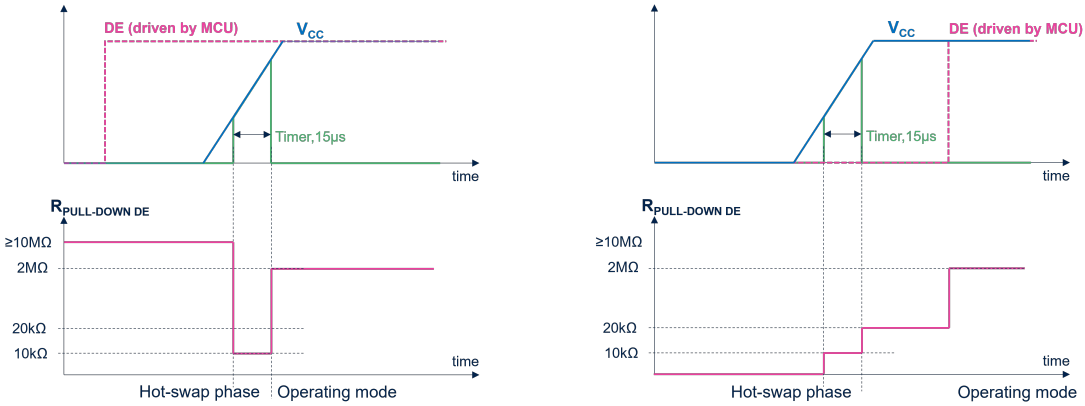
The enable pins DE and $\overline{RE}$ are critical pins during a switch-on or plug-in phase on the RS485 bus. To prevent these pins from driving unwanted states due to possible disturbances during these steps, the ST4E1650F features an integrated hot-swap structure to avoid these potential problems.

Assuming a parasitic capacitance may be present on the board between the DE and GND nodes, or $\overline{RE}$ and V_{CC}; when power supply rises, the MCU may drive an undetermined state on the DE and $\overline{RE}$ nodes. Depending on the input impedance on the DE and $\overline{RE}$ nodes, it can generate an unwanted signal on bus pins Y, Z.

A parasitic capacitance up to 100 pF is efficiently discharged with the hot-swap structure of the ST4E1650F.

The new RS 485 transceiver dynamically manages the input impedance on DE and $\overline{RE}$ versus V_{CC}. A transient resistor of 10 kΩ is seen during the rising edge of the power supply, during a defined time of 15 µs typically. This allows fast discharge of parasitic capacitance, preventing any unwanted signal on the bus pins. A second typical transient resistor of 20 kΩ remains present until the V_{CC} supply is fully established. Then, the 2 MΩ pull-down resistor on DE and pull-up resistors on $\overline{RE}$ and D are connected during normal operating mode for current consumption considerations. An example is shown below for the impedance management on the DE terminal.

Figure 31. **Hot-swap management with DE rising high before and after V_{CC}**



Electrostatic discharge (ESD) protection

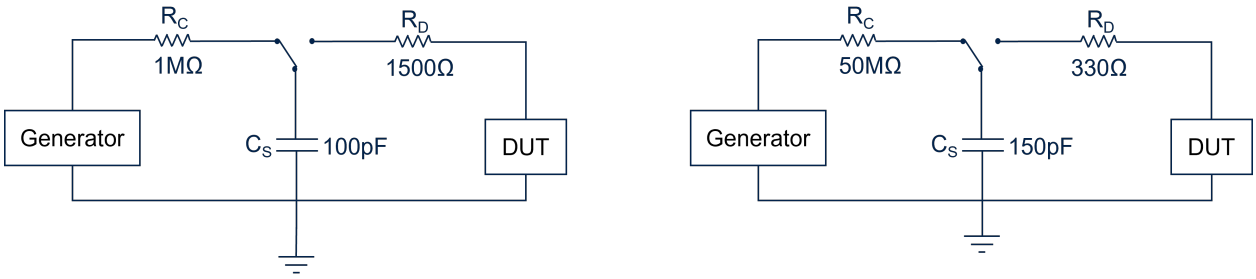
The ST4E1650F has internal protection against electrostatic discharge (ESD).

At circuit level, the ST4E1650F complies with the human body model (ANSI/ESDA/JEDEC JS-001) to guarantee robustness during the manufacturing process. All the pins of the ST4E1650F sustain 2 kV.

Because these transceivers are part of a system and can be connected to its outside through the bus terminals, an ESD protection is implemented on A, B, Y and Z to comply with IEC 61000-4-2 standard.

The schematic below compares the simplified pulse generator between the circuit-level ESD pulse and the system-level ESD pulse.

Figure 32. **HBM JEDEC (left) and IEC61000-4-2 (right) generator simplified schematics**

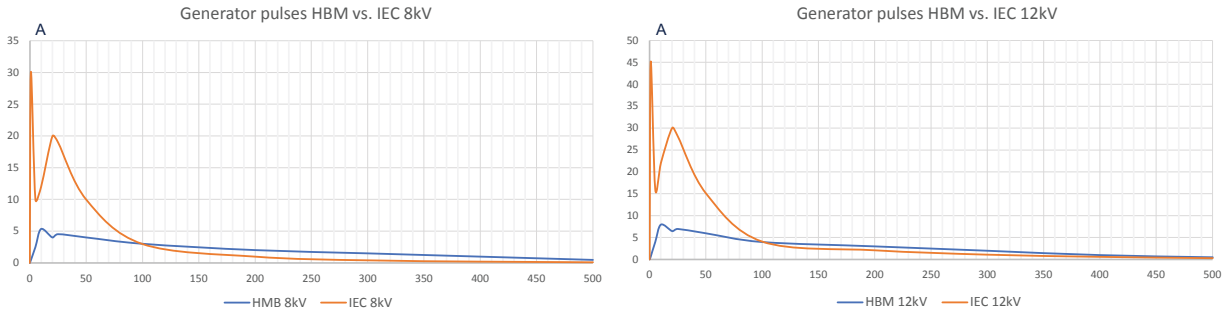


Peak current 0.7 A*kV
Rise time of pulse: 2ns to 10ns

Peak current 3.75 A*kV
Rise time of pulse: 0.6ns to 1ns

For an equivalent ESD pulse voltage, the peak current and rise time of the pulse is much higher for the IEC61000-4-2 than for the HBM. This can be shown by the pulse diagrams below, for 8 kV and 12 kV respectively.

Figure 33. **HBM JEDEC and IEC61000-4-2 waveforms comparison for different pulses**



The IEC61000-4-2 standard is more severe than the HBM ESD test and significantly increases the robustness of the equipment. IEC61000-4-2 8 kV protections are commonly implemented.

The ST4E1650F furthermore increases the robustness of systems thanks to the dedicated IEC61000-4-2 16 kV protections on bus terminals. There are two methods of ESD testing: contact discharge and air discharge. In the contact discharge method, the electrode of the test generator is held in contact with an exposed conductor on the equipment under test (EUT). In the air discharge, the electrode of the generator is moved from a distance towards the EUT until an arc occurs. The contact discharge offers the best reproducibility and is chosen to be the test method for IEC61000-4-2.

The ST4E1650F complies with IEC61000-4-2 16 kV contact discharge.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN10 (3x3 mm) package information

Figure 34. DFN10 (3x3 mm) package outline

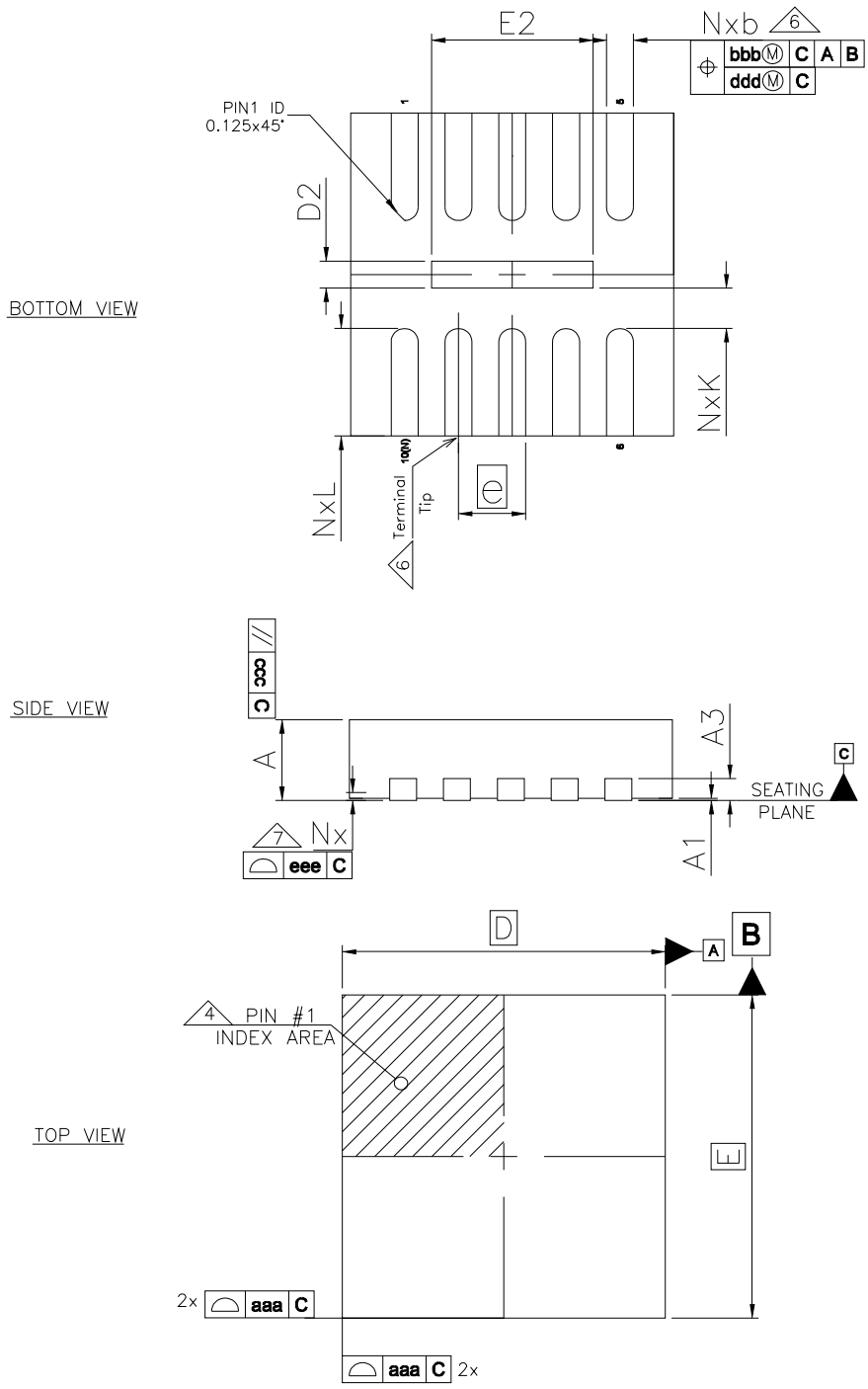
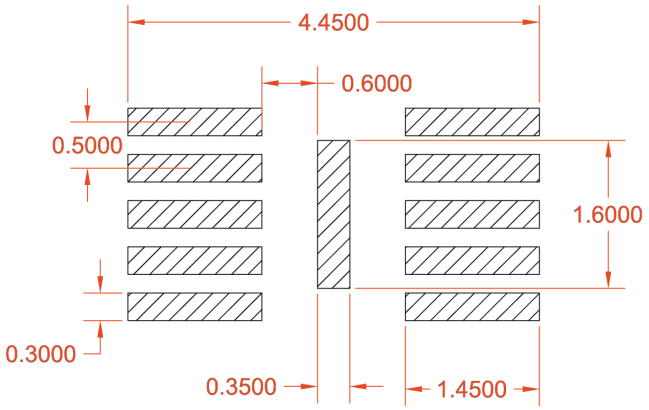


Table 13. **DFN10 (3x3 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	-	0.203 Ref.	-
b	0.20	0.25	0.30
D		3.00 BSC	
D2	0.15	0.25	0.30
E		3.00 BSC	
E2	1.40	1.50	1.60
e		0.50 BSC	
K	0.20	-	-
L	0.90	1.00	1.10
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 35. **DFN10 (3x3 mm) recommended footprint**



8 Ordering information

Table 14. **Order code**

Order code	Temperature range	Package	Marking
ST4E1650FIQT	-40 °C to +125 °C	DFN10	650F

Revision history

Table 15. **Document revision history**

Date	Revision	Changes
11-Feb-2026	1	Initial release.

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