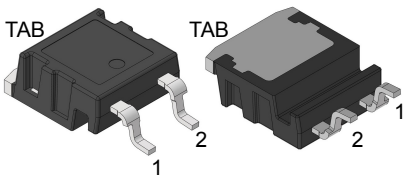
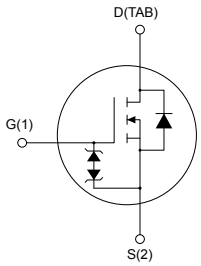
ST2H8N120K5AG

Datasheet

Automotive-grade N-channel 1200 V, 1.65 Ω typ., 6 A MDmesh K5 Power MOSFET in an H²PAK-2 HC package



H²PAK-2 HC



NG1DTS2Z

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
ST2H8N120K5AG	1200 V	2.00 Ω	6 A

- AEC-Q101 qualified
- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected
- H²PAK-2 high creepage package suitable for very high voltage application

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
ST2H8N120K5AG

Product summary[1]	
Order code	ST2H8N120K5AG
Marking	8A120K5
Package	H²PAK-2 HC
Packing	Tape and reel

1. *HTRB test was performed at 80% of $V_{(BR)DSS}$ according to AEC-Q101 rev. C. All other tests were performed according to AEC-Q101 rev. D.*

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	6	A
	Drain current (continuous) at T_C = 100 °C	3.5	
I_{DM} (1)	Drain current (pulsed)	12	A
P_{TOT}	Total power dissipation at T_C = 25 °C	165	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 6 A, di/dt ≤ 100 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$.*
3. *V_{DD} ≤ 960 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.76	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	30	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	1.3	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 100 V)	243	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1200			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1200 V			1	µA
		V_{GS} = 0 V, V_{DS} = 1200 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		1.65	2.00	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 250 kHz, V_{GS} = 0 V	-	455	-	pF
C_{oss}	Output capacitance		-	36	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(er)}$(1)	Equivalent capacitance energy related	V_{DS} = 0 to 960 V, V_{GS} = 0 V	-	23	-	pF
$C_{o(tr)}$(2)	Equivalent capacitance time related		-	56	-	pF
R_g	Intrinsic gate resistance	f = 250 kHz , I_D = 0 A	-	8	-	Ω
Q_g	Total gate charge	V_{DD} = 960 V, I_D = 2.5 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	16.2(3)	-	nC
Q_{gs}	Gate-source charge		-	3.4(3)	-	nC
Q_{gd}	Gate-drain charge		-	9.8(3)	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
3. *Baseline values from simulations.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 600 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	11	-	ns
t_r	Rise time		-	6	-	ns
$t_{d(off)}$	Turn-off delay time		-	37	-	ns
t_f	Fall time		-	22	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM} (1)	Source-drain current (pulsed)		-		12	A
V_{SD}(2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	553		ns
Q_{rr}	Reverse recovery charge		-	6		µC
I_{RRM}	Reverse recovery current		-	16		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	865		ns
Q_{rr}	Reverse recovery charge		-	8.2		µC
I_{RRM}	Reverse recovery current		-	15		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

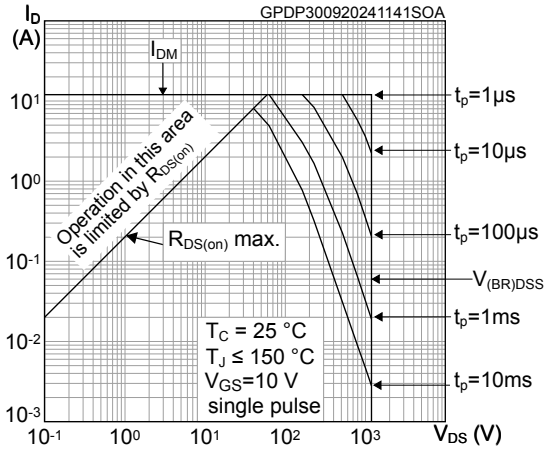


Figure 2. Maximum transient thermal impedance

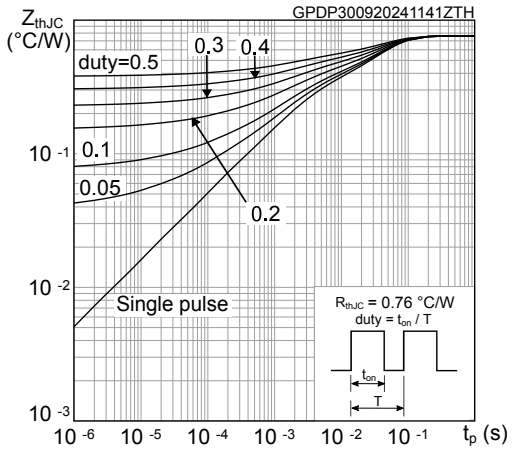


Figure 3. Typical output characteristics

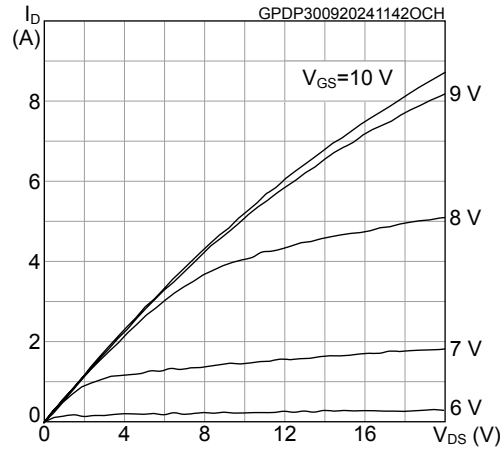


Figure 4. Typical transfer characteristics

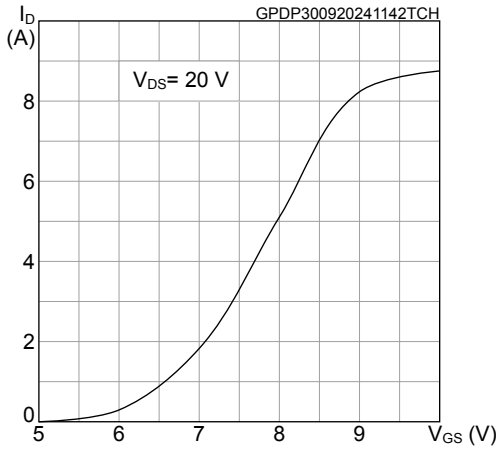


Figure 5. Typical gate charge characteristics

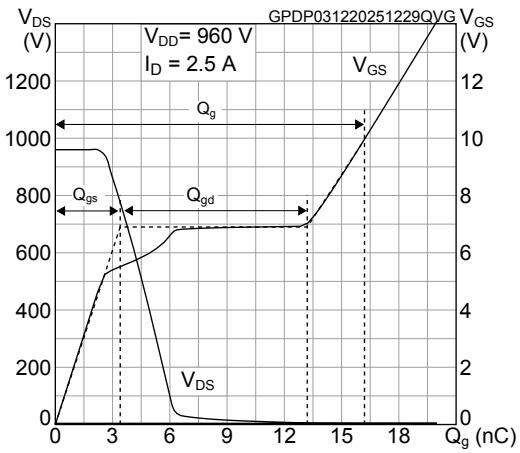


Figure 6. Typical drain-source on-resistance

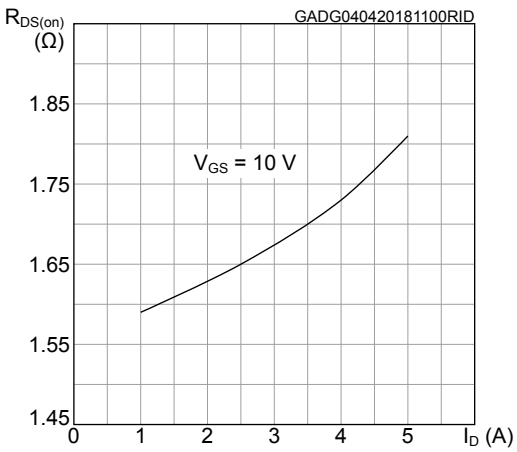


Figure 7. Typical capacitance characteristics

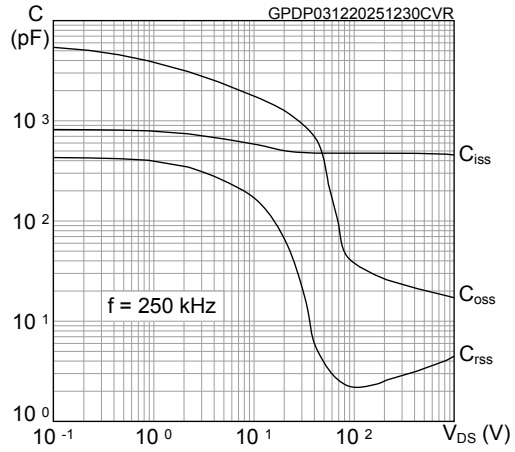


Figure 8. Normalized gate threshold vs temperature

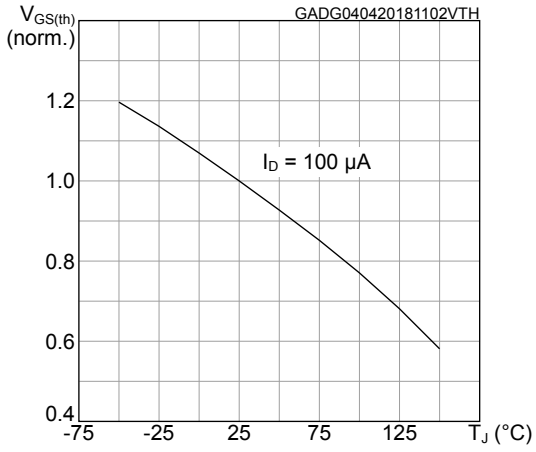


Figure 9. Normalized on-resistance vs temperature

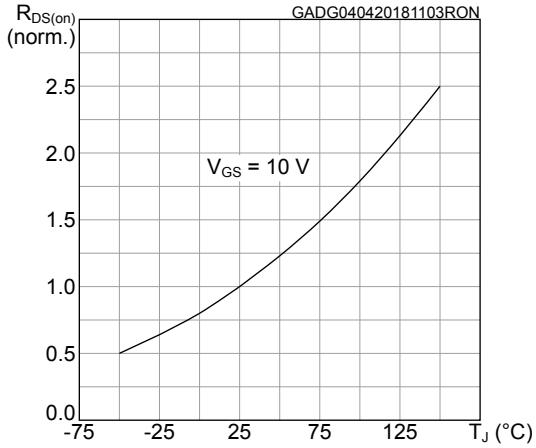


Figure 10. Normalized breakdown voltage vs temperature

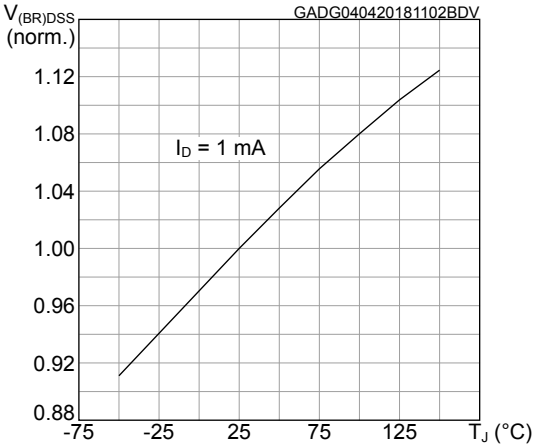


Figure 11. Typical reverse diode forward characteristics

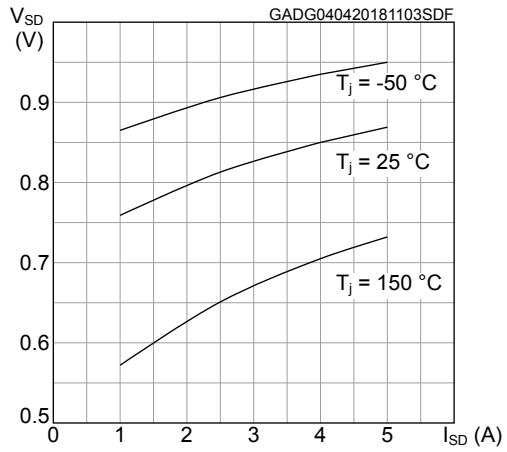


Figure 12. Maximum avalanche energy vs temperature

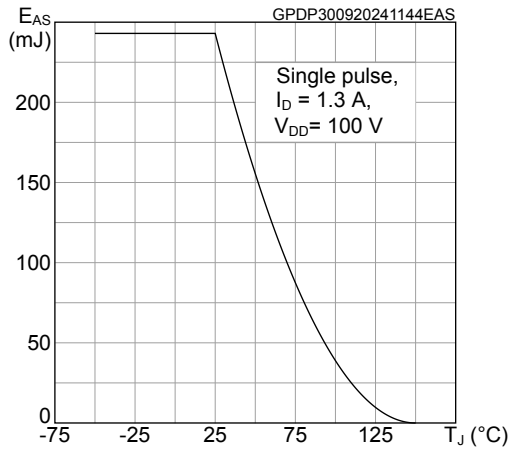
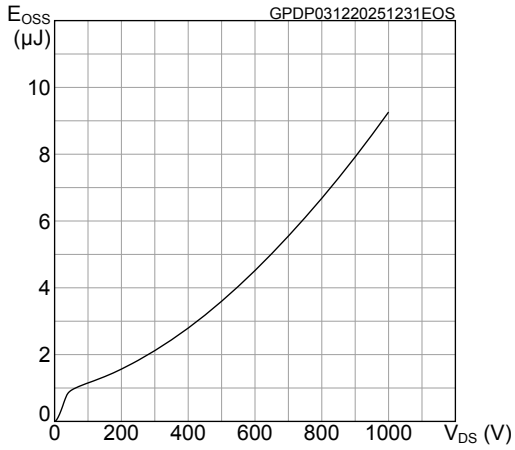


Figure 13. **Typical output capacitance stored energy**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

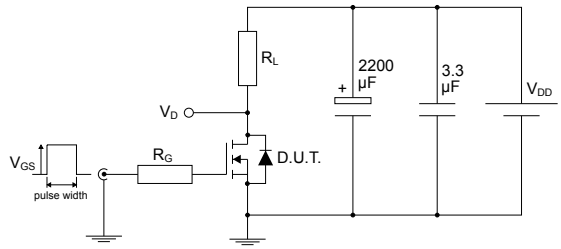


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Figure 15. Test circuit for gate charge behavior

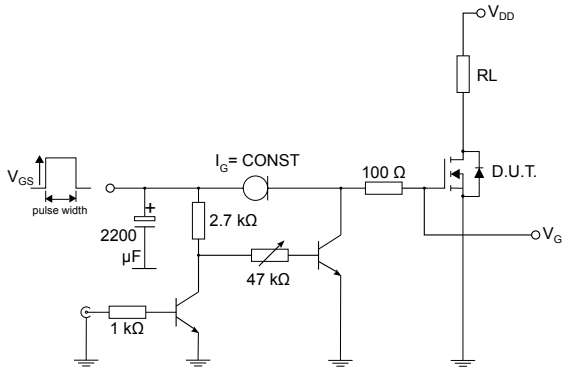

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Figure 16. Test circuit for inductive load switching and diode recovery times

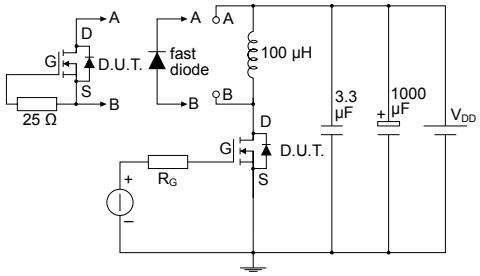

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Figure 17. Unclamped inductive load test circuit

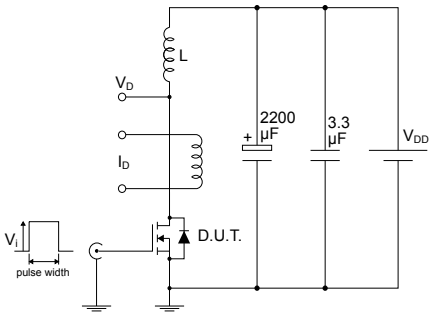

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Figure 18. Unclamped inductive waveform

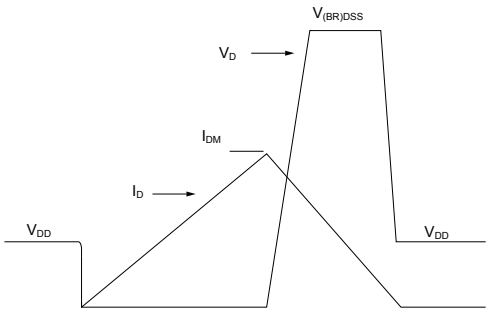

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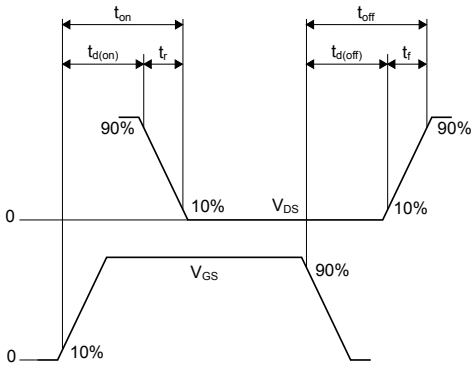
Figure 19. Switching time waveform



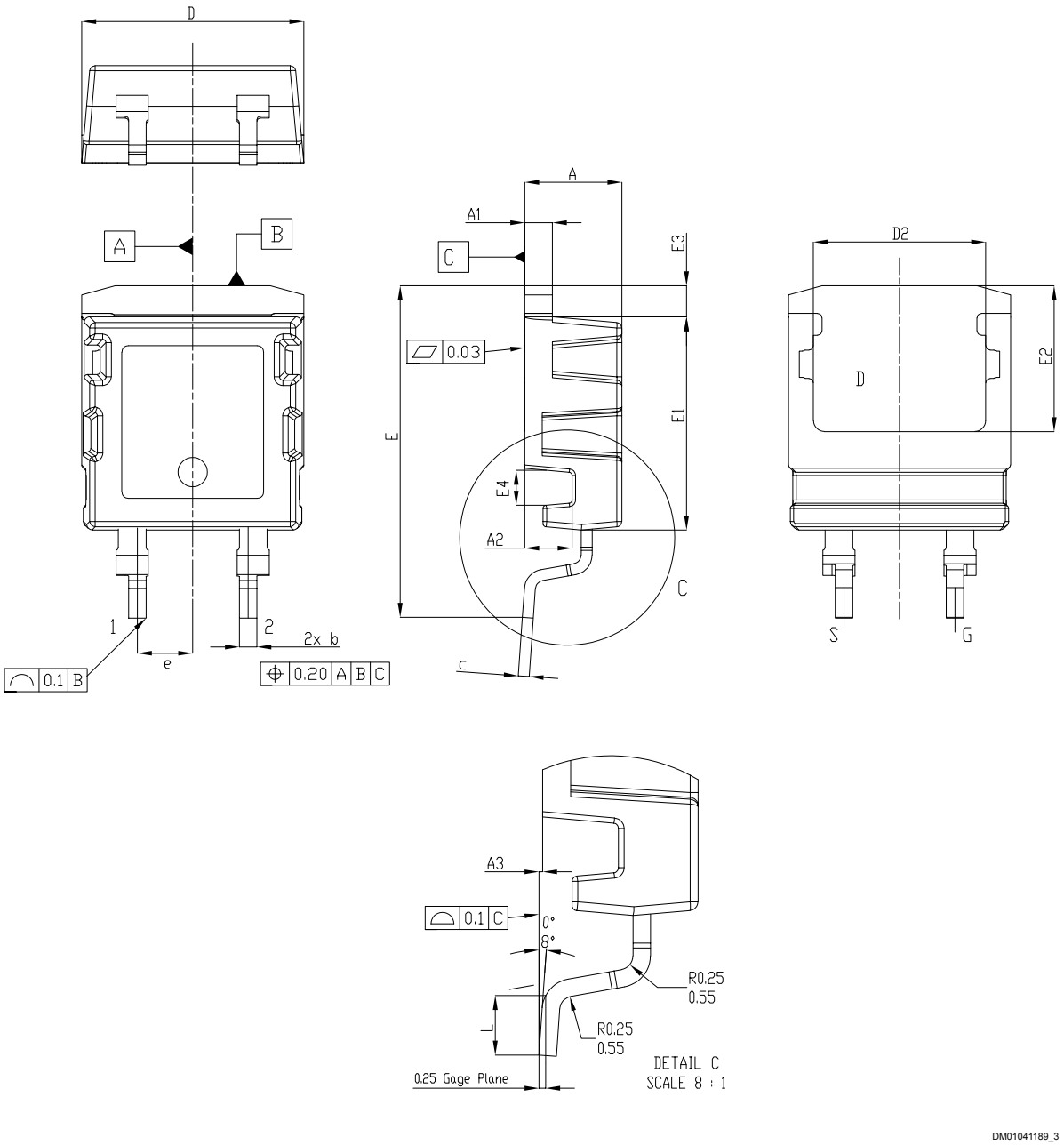
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 HC package information

Figure 20. H²PAK-2 HC package outline

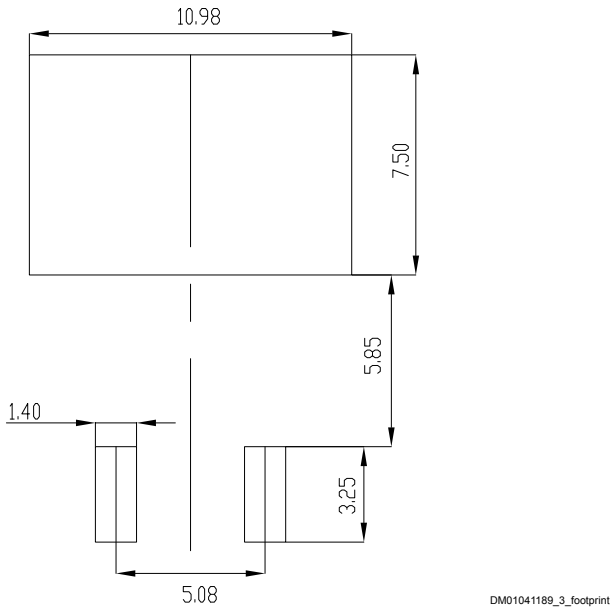


DM01041189_3

Table 8. **H²PAK-2 HC package mechanical data**

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	4.35	4.45	4.55
A1	1.25		1.40
A2	2.10		2.30
A3	0.02		0.15
b	0.75	0.80	0.90
c	0.40	0.50	0.65
D	10.00	10.20	10.40
D2	7.70	7.90	8.10
E	14.80		15.60
E1	9.60		9.90
E2	6.50	6.70	6.90
E3	1.40		1.50
E4	1.50		1.70
e		2.54	
L	1.35		2.25
Finger			
Pin 1	Gate		
Pin 2	Source		
TAB	Drain		

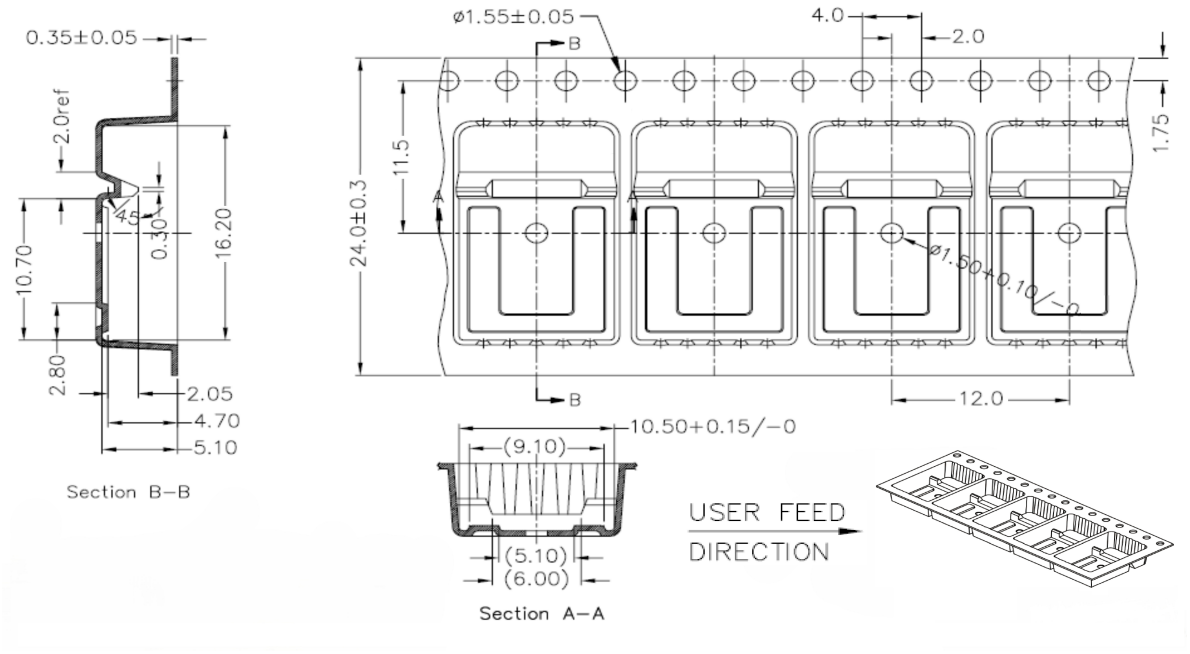
Figure 21. **H²PAK-2 HC recommended footprint**



Note: Dimensions are in mm.

4.2 H²PAK-2 HC packing information

Figure 22. **H²PAK-2 HC tape drawing**



Revision history

Table 9. **Document revision history**

Date	Revision	Changes
05-Dec-2025	1	First release.
19-Jan-2026	2	Updated Features on cover page.

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