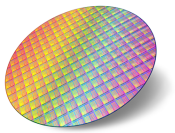
ST25TN512 ST25TN01K

Datasheet

NFC Forum Type 2 tag IC with up to 1.6 Kbits of EEPROM

UFDFPN5

(1.7 × 1.4 mm)



Wafer

Near Field Communication CERTIFIED™

Product status link
ST25TN512
ST25TN01K

Features

Includes ST state-of-the-art patented technology

Contactless interface

- Full compliancy with NFC Forum Type 2 tag and ISO/IEC 14443 type A specifications
- Power supplied by 13.56 MHz transmitter field
- Data transfer at 106 kbit/s
- Anticollision support for management of several tags in the field simultaneously
- Natively supported by Android™ and iOS™ phones
- Internal tuning capacitance 50 pF

Memory

- Up to 208 bytes (1664 bits) dedicated to user content
- Accessible by blocks of four bytes
- NFC Forum NDEF format support
- Augmented NDEF (contextual automatic NDEF message)
- 100 000 Write cycles at + 85 °C
- Data retention during 40 years at + 55 °C

Product identification and protection

- 7 bytes unique identifier
- TruST25 digital signature
- TruST25 Link
- 3-digit unique tap code
- NFC Forum T2T permanent write locks at block level

Privacy protection

- Configurable kill mode for permanent deactivation of the tag

Temperature range

- -40 °C/ +85 °C

Delivery forms

- 5-pin package ECOPACK2 (RoHS compliant)
- Bumped and sawn inkless wafer

1 Description

ST25TN512 and ST25TN01K devices are NFC Forum Type 2 tag IC with TruST25 digital signature, Augmented NDEF, and privacy features.

The RF interface is compliant with ISO/IEC 14443-2 and 14443-3 Type A standards, and NFC Forum Type 2 tag specification. Thanks to its internal tuning capacitance and harvesting of operating power from RF field provided by the NFC poller, it simply operates with an antenna and without additional component.

The embedded electrically erasable programmable memory (EEPROM) can be written with a NDEF message conforming to NFC Forum specification offering native tap with all NFC-enabled phones.

The Augmented NDEF feature allows the tag to answer dynamic NDEF message without modification of the EEPROM by the user.

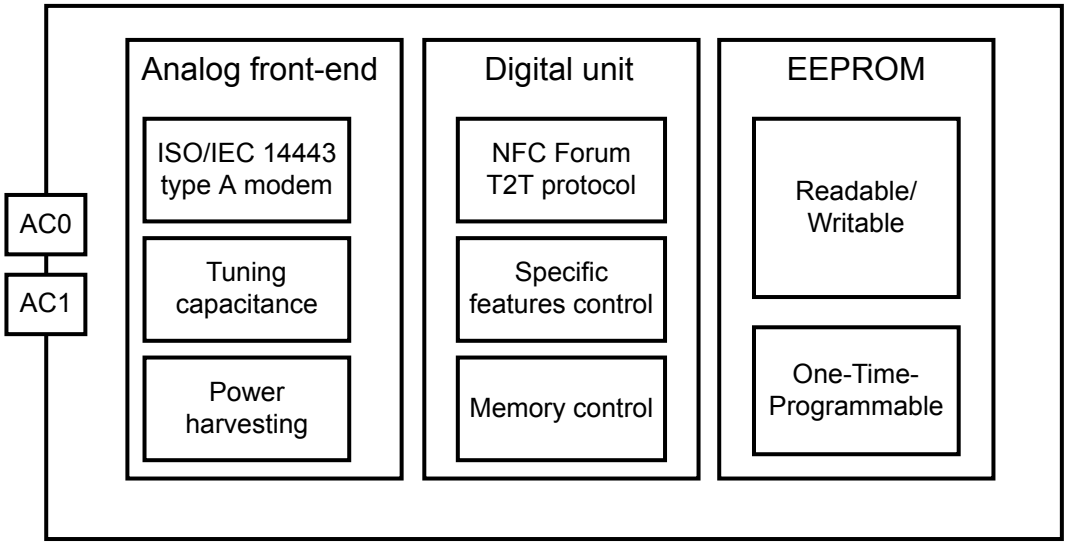
The TruST25 digital signature helps fighting against counterfeiting. TruST25 Link is a technology enabling offline NFC tag identification through reader + tag applications using ST devices.

The kill feature guarantees user privacy by permanently muting the tag with a simple software procedure.

In this document, the term ST25TN refers interchangeably to ST25TN512 or ST25TN01K.

1.1 Block diagram

Figure 1. ST25TN block diagram

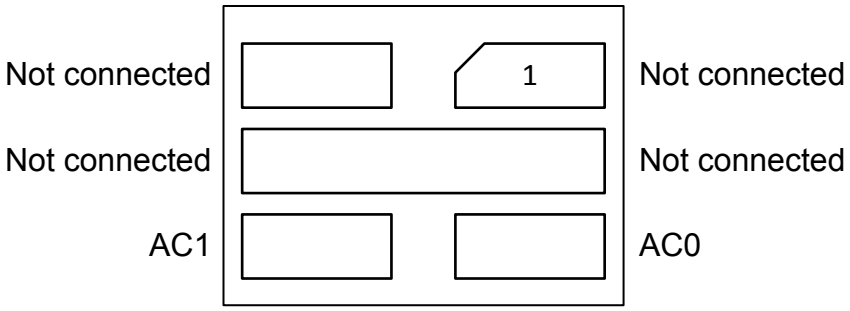


1.2 Package connections

The ST25TN is available in the following delivery forms:

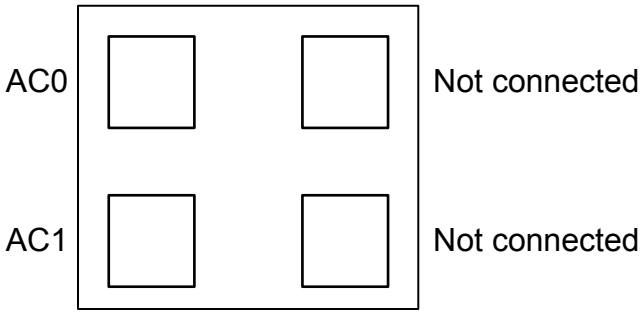
- UFDFPN5 package

Figure 2. UFDFPN5 bottom view (pads side) connections



- Bumped and sawn inkless wafer

Figure 3. Bumped wafer connection



1.3 Signal descriptions

Table 1. Signal description

Name	Description
AC0	These inputs are used exclusively to connect the device to an external coil. It is advised not to connect any other DC or AC path to AC0 or AC1. When correctly tuned, the coil is used both to power and interact with ST25TN.
AC1	
Not connected	Other pads and bumps are not connected to the internal IC.

2 Power supply

The power supply is provided exclusively by the RF field at 13.56MHz at the coil.

For proper operation, the following constraints must be met:

2.1 Power on

In accordance with ISO/IEC 14443-3, to ensure a proper boot of the RF circuitry, the RF field must be turned on without any modulation for a minimum duration t_{BOOT_RF} (see Section 8.2: RF characteristics). Before this time, the device ignores all received RF commands.

2.2 Power off

In accordance with ISO/IEC 14443-3, to ensure a proper reset of the RF circuitry, the RF field must be turned off (100% modulation) for a minimum duration t_{RF_OFF} (see Section 8.2: RF characteristics).

3 Memory overview

The memory is organized in blocks with 4 bytes per block. ST25TN01K and ST25TN512 have 64 blocks (256 bytes) always readable including both memory available for user data and memory reserved for system and configuration.

The following address space is available to standard READ/WRITE commands:

Table 2. ST25TN memory overview

Block address		Data Bytes within the block[1]			
Dec	Hex	Byte0	Byte1	Byte2	Byte3
0	00h	Device identification			
1	01h				
2	02h	Internal	SYSBLOCK	Static Lock Bytes	
3	03h	Capability container (CC)			
4 to 43[2]	04h to 2Bh[2]	User memory			
44	2Ch	Dynamic Lock area			SysLock
45	2Dh	Product identification			
46	2Eh	Augmented NDEF configuration			
47	2Fh	Kill password			
48	30h	Kill keyhole			
49 to 59	31h to 3Bh	Internal			
60	3Ch	Augmented NDEF fields			
61	3Dh				
62	3Eh				
63	3Fh				

1. *The bytes in this table are represented with the LSB on the left.*
2. *For ST25TN512, the zone of blocks address from 4 to 43 is split according to Table 3. ST25TN512 user memory.*

Table 3. ST25TN512 user memory

Block address		Data Bytes within the block			
Dec	Hex	Byte0	Byte1	Byte2	Byte3
4 to 19	04h to 13h	User memory			
20 to 43	14h to 2Bh	Reserved			

The user memory can expanded by application over other functions. More details on how to achieve it are provided in “AN5677 - Extending the user memory of ST25TN512 and ST25TN01K devices".

4 Device and product identification

ST25TN embeds several readable fields allowing the identification of the product model, version, size, and serial number.

All the fields are accessible through the standard READ command.

4.1 Device identification: unique identifier (UID)

Each ST25TN device is uniquely identified by a 7-byte Unique identifier (UID) compliant with ISO/IEC 14443-3 double-size UID.

Byte 0 of the UID is the IC manufacturer code 02h registered by STMicroelectronics according to ISO/IEC 7816-5.

Table 4. Device identification (UID)

Block address	Bits	Name	Function	Access	Factory value
0	b7-b0	UID_0	UID	READ: always WRITE: never	02h
	b15-b8	UID_1			Unique serial number
	b23-b16	UID_2			
1	b7-b0	UID_3			
	b15-b8	UID_4			
	b23-b16	UID_5			
	b31-b24	UID_6			

Table 5. BCC

Block address	Bits	Name	Function	Access	Factory value
0	b31-b24	BCC_1	Block Check Character as defined in ISO/IEC 14443-3 and NFC Forum Digital Protocol Technical Specification	READ: always WRITE: never	= 88h xor UID_0 xor UID_1 xor UID_2

4.2 Product identification: SYSBLOCK, PC, REV, KID

The product identification is done using standard READ command in the system area. To be compatible with several STMicroelectronics Type 2 tag sizes, an application must first read the value of SYSBLOCK to know the location of the system area, and then read PC/REV/KID in the system area.

Table 6. System area identification (SYSBLOCK)

Block address	Bits	Name	Function	Access	Factory value
2	b15-b8	SYSBLOCK	Block address of the beginning of the system area. To be compatible with several STMicroelectronics Type 2 tag sizes, an application must use this value plus 1 to read the product identification block.	READ: always WRITE: never	2Ch

Table 7. Product identification (PC, REV, KID)

Block address	Bits	Name	Function	Access	Factory value
"Value read in SYSBLOCK" + 1	b15-b0	PC	Product code	READ: always WRITE: never	9091h for ST25TN512 9090h for ST25TN01K
	b23-b16	REV	Product version		13h
	b31-b24	KID	Key ID used to generate TruST25 signature during manufacturing		05h

5 Device features

5.1 Capability container (CC)

The block 3 has a specific behavior conforming to NFC Forum Type 2 tag specification for capability container (CC bytes).

The content of CC bytes after manufacturing is described in Section 7: Memory content at delivery .

The modifications of CC can be prevented according to Section 5.2: Access restriction. When it is not locked the following applies:

- The bits of block 3 are one-time-programmable (OTP):
  - they can only be set to 1 and cannot be changed back to 0. Upon reception of a valid WRITE command to a block address 3, the device only sets the bits at 1, ignore the other bits and answers ACK.
- Writing into block 3 is tearing-proof:
  - even in case of tearing, the bits are never erased.

5.2 Access restriction

It is possible protect the write access of blocks with a lock mechanism. The lock is irreversible: a locked block can never be unlocked and is never writable again. The lock mechanism is compliant with NFC Forum T2T specification with some extensions providing finer grain locking options.

5.2.1 Generic lock mechanism

The blocks to lock are configured using “lock bits” of Static lock bytes, Dynamic lock area (DynLock_Area) and SysLock byte shown in Table 2. ST25TN memory overview with the memory mapping detailed in the following table.

Table 8. Memory lock bytes in memory map

Block address (hex)	Bits	Name	Function	Factory value
02h	b31-b24	STATLOCK_1	Static lock bytes to prevent modification of the beginning of memory	00h
	b23-b16	STATLOCK_2		00h
2Ch	b31-b24	SYSLOCK	System lock bits to prevent modification of the system configuration blocks	E2h
	b23-b16	DYNLOCK_2	Dynamic lock bits to prevent modification of the remaining bytes of user memory	00h
	b15-b8	DYNLOCK_1		00h
	b7-b0	DYNLOCK_0		00h

In all these bytes, each lock bit configures the write access of a given memory region. When a lock bit is set to 1, the content of the target memory region cannot be modified anymore and becomes read-only.

The lock bits are One-Time-Programmable (OTP): they can only be set to 1 and cannot be changed back to 0. Upon reception of a valid WRITE command to a block with lock bits, the device only sets the bits at 1, ignore the other bits and answers ACK.

Writing into a block with lock bits is tearing-proof: even in case of tearing, the lock bits are never erased.

The mapping of which lock bit locks which memory region is described in Table 10 and Table 9. The specificities of Static Lock bytes, DynLock_Area and SysLock byte are described in dedicated sections below.

The following table details which bit locks which block(s).

Table 9. Lock bit mapping

Locking bit		Locked Memory					
		Block number		Bytes			
Register	Bit	Hex	Dec	Byte0	Byte1	Byte2	Byte3
STATLOCK_0	b0	See Table 10. Lock bit mapping for STATLOCK_0[0:2]					
	b1						
	b2						
	b3	03h	3	CC			
	b4	04h	4	User memory			
	b5	05h	5				
	b6	06h	6				
	b7	07h	7				
STATLOCK_1	b0	08h	8				
	b1	09h	9				
	b2	0Ah	10				
	b3	0Bh	11				
	b4	0Ch	12				
	b5	0Dh	13				
	b6	0Eh	14				
	b7	0Fh	15				
DYNLOCK_0	b0	10h	16				
		11h	17				
	b1	12h	18				
		13h	19				
	b2	14h	20				
		15h	21				
	b3	16h	22				
		17h	23				
	b4	18h	24				
		19h	25				
	b5	1Ah	26				
		1Bh	27				
	b6	1Ch	28				
		1Dh	29				
	b7	1Eh	30				
		1Fh	31				
DYNLOCK_1	b0	20h	32				
		21h	33				
	b1	22h	34				
		23h	35				
	b2	24h	36				

Locking bit		Locked Memory					
		Block number		Bytes			
Register	Bit	Hex	Dec	Byte0	Byte1	Byte2	Byte3
DYNLOCK_1	b2	25h	37	User memory			
	b3	26h	38				
		27h	39				
	b4	28h	40				
		29h	41				
	b5	2Ah	42				
		2Bh	43				
SYSLOCK	b0	2Ch	44	DYNLOCK_0	DYNLOCK_1	DYNLOCK_2	SYSLOCK
	b1	2Dh	45	Product identification			
	b2	2Eh	46	ANDEF configuration			
	b3	2Fh	47	KILL_PWD			
	b4	30h	48	Kill keyhole			
DYNLOCK_2	b6	3Ch	60	ANDEF_CUSTOM			
		3Dh	61				
	b7	3Eh	62				
		3Fh	63	ANDEF_CUSTOM		ANDEF_SEP	-

5.2.2 Static lock bytes

This section describes specificities on top of the generic lock mechanism described Section 5.2.1: Generic lock mechanism.

The static lock bits are stored at block address 2, which contains both read-only and writable bits. Upon reception of a valid WRITE command for this block, the device updates only the writable bits of the block and answers ACK.

The low significant bits 0 to 2 of STATLOCK_0 are special because they allow to disable the locking of some blocks by locking the value of some STATLOCK_0 and STATLOCK_1 bits as shown in Table 10.

Table 10. Lock bit mapping for STATLOCK_0[0:2]

Locking bit		Locked memory	
Name	bit	Name	bit
STATLOCK_0	b0	STATLOCK_0	b3
	b1	STATLOCK_0	b4
			b5
			b6
			b7
		STATLOCK_1	b0
			b1
	b2	STATLOCK_1	b2
			b3
			b4
			b5
			b6
			b7

- If bit b0 of STATLOCK_0 is set to 1 and bit b3 of STATLOCK_0 is reset to 0, the block 3 (CC file) is always writable.
- If bit b1 of STATLOCK_0 is set to 1 and some bits of STATLOCK_0[7:4] or STATLOCK_1[1:0] are reset to 0, the corresponding block(s) between 4 and 9 included is always writable.
- If bit b2 of STATLOCK_0 is set to 1 and some bits of STATLOCK_1[7:2] are reset to 0, the corresponding block(s) between 0Ah and 0Fh included is always writable.

The remaining system lock bits have a granularity of 1 block: Each bit locks the value of 1 block (4 bytes) with bit b3 of STATLOCK_0 locking the value of block address 3 and so forth as described in Table 9. Lock bit mapping.

5.2.3 Dynamic lock bits

This section describes specificities on top of the generic lock mechanism described in Section 5.2.1: Generic lock mechanism.

Dynamic Lock Bits have a granularity of 2 blocks (8 bytes) per bit: Each bit locks the value of 2 blocks (8 bytes), starting at block address 10h and up to the end of the memory as shown in Table 9. Lock bit mapping.

The dynamic lock bits DYNLOCK_1[6:7] and DYNLOCK_2[0:1] that would apply to a block in the system area protected by SYSLOCK bits are ignored by the device whatever their value.

Note: For ST25TN01K: with the factory CC programming defining a T2T_Area_Size of 160 bytes, the position of the first Dynamic lock byte is the first byte after the T2T_Area. Since the granularity of dynamic lock bits matches the default granularity defined in NFC Forum Type 2 Tag specification, there is no need for a Lock Control TLV in T2T_AREA to define the position and number of dynamic lock bits.

5.2.4 System lock bits

This section describes specificities on top of the generic lock mechanism described in Section 5.2.1: Generic lock mechanism.

System lock bits have a granularity of 1 block: Each bit locks the value of 1 block (4 bytes), starting at block address 2Ch, as shown in Table 9. Lock bit mapping.

5.3 Privacy: Kill feature

It is possible to permanently kill the RF interface of the device: When the device is in KILLED state, all incoming RF commands are ignored. There is no way to revert a killed device back to normal operation.

This feature may be used to comply with GDPR or another privacy requirement.

5.3.1 Kill command

The Kill command is a Write of the kill password to the address 30h = 48.

Table 11. Kill command format

TBD	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Field	Code	Block address	Kill password				CRC_A	
Content	A2h	30h	4 bytes				2 bytes	

The Kill command may be disabled by locking the “kill keyhole” block using the locking mechanism described in Section 5.2: Access restriction.

When the Kill command is disabled (block 30h is locked), the device answers NACK0 to a WRITE command in block 30h.

When the Kill command is enabled (block 30h is not locked) and the data value in the Write command matches the kill password stored in the device, the device answers ACK and set an internal non-volatile bit “Killed” to the value 1. Then, it enters Killed state on the next and each boot as described in Figure 4. State machine.

5.3.2 Kill password

Table 12. KILL_PWD

Block address (Hex)	Name	Function	Factory value
2Fh	KILL_PWD	Kill password	00000000h

The kill password (KILL_PWD) can be freely written without password presentation unless the block is locked by corresponding SYSLOCK bit. Once corresponding SYSLOCK bit is set, the password cannot be modified anymore.

The kill password can never be read-out: Upon a READ command, the device always returns 00000000h for the bytes of block address 2Fh whatever the actual values of these bytes.

Warning: the kill password adds security only if it is locked, otherwise it can be modified without knowledge of the previous password.

5.4 Augmented NDEF

The augmented NDEF feature (ANDEF) allows the device to respond smart NDEF messages thanks to:

- Automatic insertion of a custom field such as UID
- Automatic insertion of unique tap code (UTC) without modification of the EEPROM by the user

When the feature is enabled, memory data at byte addresses ranging from ANDEF_START to ANDEF_END is replaced by the content of a virtual memory ANDEF_MEM in the response to READ command as shown in following figure

Table 13. Effect of ANDEF feature on READ data response

Block address (dec)	Block data							
	when ANDEF is disabled				when ANDEF is enabled, ANDEF_START=77, ANDEF_END=82			
	Byte0	Byte1	Byte2	Byte3	Byte0	Byte1	Byte2	Byte3
00	B0	B1	B2	B3	B0	B1	B2	B3
…	…	…	…	…	…	…	…	…
18	B72	B73	B74	B75	B72	B73	B74	B75
19	B76	B77	B78	B79	B76	**A0**	**A1**	**A2**
20	B80	B81	B82	B83	**A3**	**A4**	**A5**	B83
21	B84	B85	B86	B87	B84	B85	B86	B87
…	…	…	…	…	…	…	…	…

In the above table:

- Bx is byte x of EEPROM memory
- Ax is byte x of the virtual memory ANDEF_MEM

The values ANDEF_START and ANDEF_END depend on the ANDEF configuration as defined in Table 14. ANDEF_CFG.

- ANDEF_START = ANDEF_BLOCK * 4 + ANDEF_BYTE
- ANDEF_END = ANDEF_START + ANDEF_CUSTOM_EN * 14 + ANDEF_UTC_EN * 3 + ANDEF_SEP_EN - 1
- ANDEF_SEP_EN = 1 if both ANDEF_CUSTOM_EN is 1 and ANDEF_UTC_EN is 1, otherwise ANDEF_SEP_EN = 0

5.4.1 ANDEF configuration

The following fields configure ANDEF behavior:

Table 14. ANDEF_CFG

Block address (hex)	Bits	Name	Function	Factory value
2Eh	b5-b0	ANDEF_BLOCK	Block address for the beginning of ANDEF_MEM	0Fh
	b7-b6	RFU	-	0
	b8	ANDEF_CUSTOM_EN	1b: ANDEF_CUSTOM is appended in ANDEF_MEM 0b: ANDEF_CUSTOM is not appended in ANDEF_MEM	0
	b9	RFU	-	0
	b10	ANDEF_UTC_EN	1b: ANDEF_UTC is appended in ANDEF_MEM 0b: ANDEF_UTC is not appended in ANDEF_MEM	0
	b13-b11	RFU	-	0
	b15-b14	ANDEF_BYTE	Byte number into ANDEF_BLOCK for the beginning of ANDEF_MEM	0

ANDEF feature is disabled when both ANDEF_CUSTOM_EN and ANDEF_UTC_EN are reset to the value 0.

ANDEF_CFG is always readable.

Modifications of ANDEF_CFG can be prevented according to Section 5.2: Access restriction.

5.4.2 ANDEF custom

Table 15. ANDEF_CUSTOM

Block address (hex)	Bits	Name	Function	Factory value
3Ch-3Eh	b31-b0	ANDEF_CUSTOM	Field inserted in ANDEF_MEM when ANDEF_CUSTOM_EN is 1	ASCII coding of the device UID in hexadecimal representation
3Fh	b15-b0			

ANDEF_CUSTOM is initialized at factory with ASCII coding of the device UID in hexadecimal representation. Consequently, several ST25TN with the same content in T2T_AREA can answer different NDEF messages, each one with a device-specific content.

ANDEF_CUSTOM is always readable.

Modifications of ANDEF_ CUSTOM can be prevented according to Section 5.2: Access restriction.

Since memory is not locked at manufacturing, it is possible to replace the ANDEF_CUSTOM with another custom message.

5.4.3 ANDEF unique tap code

ANDEF_UTC is an ASCII value generated once every time the device is powered.

The value is unique to each user tap of the tag, and predictable.

The size of ANDEF_UTC is 3 bytes.

A typical usage of UTC is to embed it in the URI record of a NDEF message. In this case, when a user taps the tag with a smartphone, its web browser natively opens a URL including the unique tap code, which can be processed as an element of tag authentication by the web server.

More details on ANDEF_UTC are provided in “AN5628 – Unique tap code for ST25TN512 and ST25TN01K devices". Contact your STMicroelectronics sales office to get this document.

5.4.4 ANDEF separator

A separator is inserted between ANDEF_CUSTOM and ANDEF_UTC when both ANDEF_CUSTOM_EN and ANDEF_UTC_EN are set to 1. The value of this separator can be customized by writing ANDEF_SEP described in the following table.

Table 16. ANDEF_SEP

Blocks address (Hex)	Bits	Name	Function	Factory value
3Fh	b23-b16	ANDEF_SEP	Field inserted in ANDEF_MEM when both ANDEF_CUSTOM_EN = 1 and ANDEF_UTC_EN = 1	78h ASCII code of ‘x’

ANDEF_SEP is always readable.

Modifications of ANDEF_ SEP can be prevented according to Section 5.2: Access restriction.

5.5 TruST25 digital signature

ST25TN supports the TruST25 digital signature feature, which allows the user to verify the authenticity of the device, thanks to a unique digital signature.

TruST25 solution encompasses secure industrialization processes and tools deployed by STMicroelectronics to generate, store, and check the signature in the device.

More details on TruST25 digital signature are provided in “AN5660 – TruST25 digital signature for ST25TN512 and ST25TN01K devices". Contact your STMicroelectronics sales office to get this document.

5.6 TruST25 Link

TruST25 Link is based on a patented technology enabling offline NFC tag identification through reader and tag applications using ST devices.

More details on the TruST25 Link are provided in AN6296. Contact your STMicroelectronics sales office to get this document.

6 Device operation

6.1 NFC Type 2 tag overview

NFC Type 2 tag specification is based on NFC-A technology specification which is aligned with ISO/IEC 14443-2 and 14443-3 Type A. Since both specifications use different wording for the same concept, both wordings are often provided in this document. For example "SAK/SEL_RES" designates ISO/IEC 14443 "SAK" and its NFC Forum equivalent "SEL_RES".

The tag (also named PICC) always waits to receive a command from an initiator (named Poller or PCD) before sending a response.

Commands are transmitted using OOK (100% ASK) modulation of a 13.56MHz carrier wave transmitted by the Poller. Responses are transmitted using retro-modulation of the same carrier wave.

Both commands and responses are transmitted at 106kbps.

Type 2 tags and Type 4 tags share the same activation, anticollision and selection process allowing one-to-one communication in presence of several tags.

Type 2 tags are distinguished from Type 4 tags by their SAK/SEL_RES response to ATQA/SEL_REQ command.

ST25TN512 and ST25TN01K SAK value is described in section “SAK/SEL_RES” response.

On top of the communication protocol, Type 2 tag specification defines

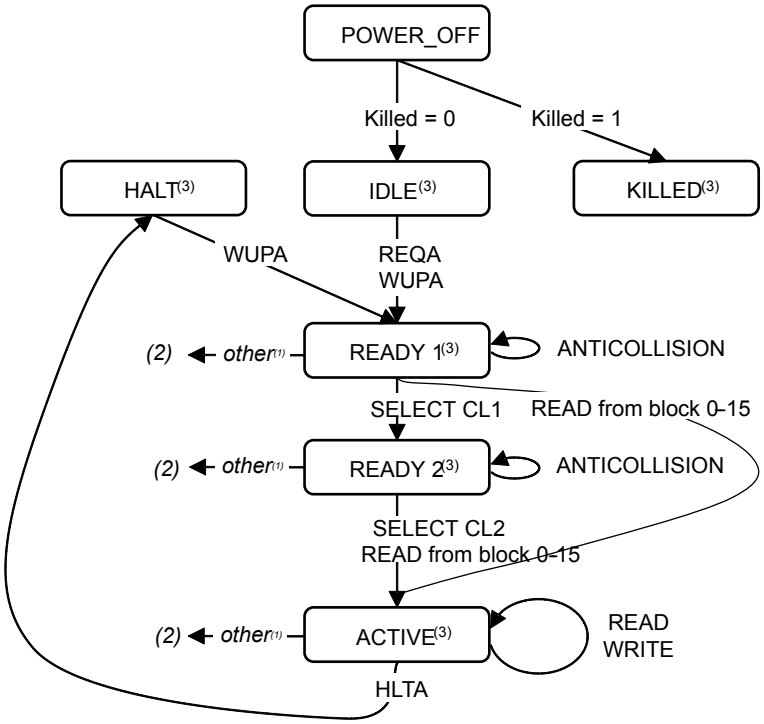
- some commands to access directly the memory,
- a memory layout,
- a memory lock mechanism,
- and memory content to layout a NDEF.

ST25TN implements the commands, the memory layout, and the memory lock mechanism. The memory content is managed by application.

6.2 State machine

ST25TN follows the following state machine, compliant with ISO/IEC 14443-3 type A anticollision and select sequences and NFC Forum T2 tag specification. The equivalence between ISO/IEC 14443 command names and NFC Forum command names is provided in Table 17. Commands overview.

Figure 4. State machine

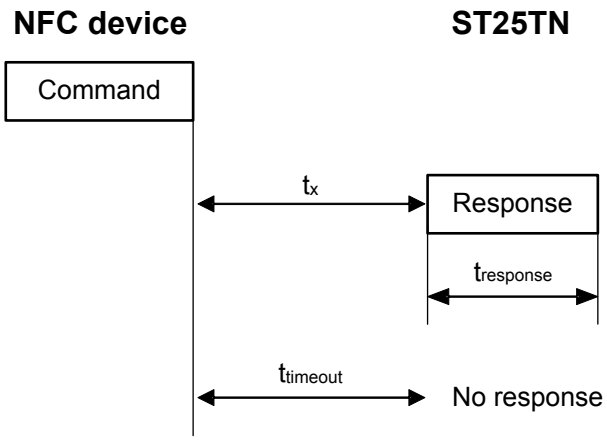


(1) “other” includes any erroneous command for which the device answers NACK.
(2) The device returns in HALT state if it was previously in HALT state after POWER_OFF state, otherwise it returns to IDLE state.
(3) In all states, the device returns to POWER_OFF state when it is not powered anymore.

6.3 Timings

The timing of commands is provided in each command section, rounded at 1 µs, using the following generic representation with drawing not to scale:

Figure 5. Generic representation of command timing



- t_x is the time between the end of the command and the beginning of the response. It is not FDT
- $t_{response}$ includes SOF and EOF of the response
- $t_{timeout}$ is equal to the maximum value of t_x

ISO/IEC 14443-3 and NFC Forum digital specification define the frame delay time (FDT) starting at the end of the last pulse of the command such that:

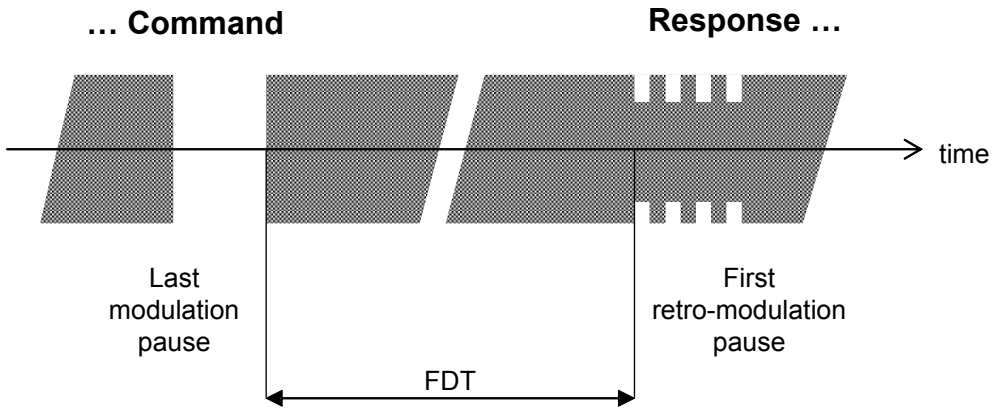
- FDT = $(n_{FDT} * 128 + 84) / f_c$ in case the last bit of the command is a logic '1'

and

- FDT = $(n_{FDT} * 128 + 20) / f_c$ in case the last bit of the command is a logic '0'

where f_c is the frequency of the carrier wave and 'n_{FDT}' is an integer.

Figure 6. Frame delay time (FDT)



The values of t_x, $t_{response}$, $t_{timeout}$ and n_{FDT} are provided for each command with its description.

6.4 Commands

6.4.1 Commands overview

Table 17. Commands overview

Type	Name		Code	Function
ISO/IEC 14443-3 Type A and NFC Forum NFC-A technology	SENS_REQ	REQA	26h(1)	Device initialization, anticollision, and selection
	ALL_REQ	WUPA	52h(1)	
	SDD_REQ_CL1	Anticollision CL1	93h xxh	
	SEL_REQ_CL1	Select CL1	93h 70h	
	SDD_REQ_CL2	Anticollision CL2	95h xxh	
	SEL_REQ_CL2	Select CL2	95h 70h	
	SLP_REQ	HLTA	50h 00h	
NFC Forum Type 2 tag	READ		30h	Read 4x Blocks of data
	WRITE		A2h	Write 1x Block of data

1. *Code on 7 bits.*

The commands used for device initialization, anti-collision and selection are described in ISO/IEC 14443-3 for Type A and alternatively in NFC Forum Digital specification for NFC-A technology.

Other commands supported by the device are described hereafter.

6.4.2 READ

Figure 7. READ command outline

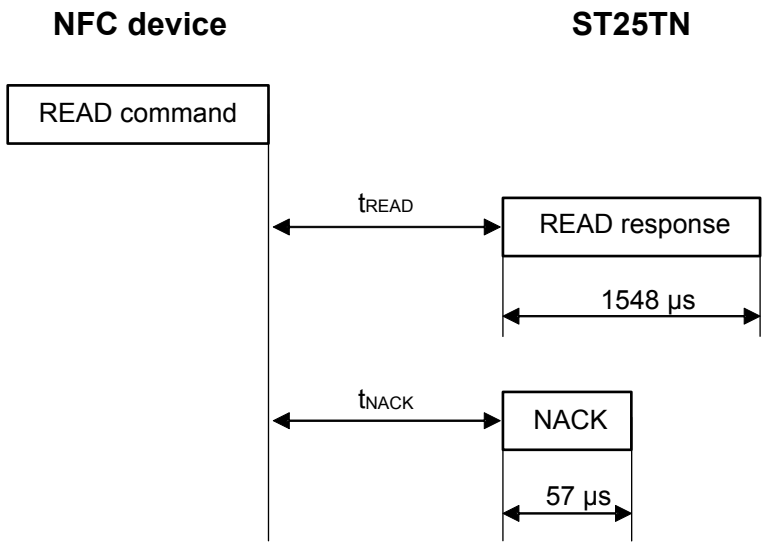


Table 18. READ command format

Byte	1	2	3	4
Field	Command code	Block address	CRC_A	
Content	30h	1 byte	2 bytes	

- Block address is the address of the first block to read.

- CRC_A is Cyclic redundancy check defined in NFC Forum digital specification for NFC-A technology.

The following responses may be issued upon reception of a READ command code:

Table 19. Possible responses to the READ command

Condition upon reception of READ command code	Response
Wrong number of bytes of payload	No response
Parity or CRC_A error	NACK1 (see Section 6.5.2: NACK response)
Block address is outside the valid address range. ST25TN valid address range is [0;3Fh] = [0;63]	NACK0 (see Section 6.5.2: NACK response)
Successful read	READ response

Table 20. READ response format

Byte	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Field	DATA																CRC_A	
Content	16 bytes																2 bytes	

- DATA is the content of 16 bytes of memory starting from the block address requested in the command. For example upon reception of the command “30h, 00h“, the bytes of blocks 00h, 01h, 02h and 03h are returned.
- DATA may differ from the content of addressed memory in the following cases:
  - ANDEF feature described in Section 5.4.1: ANDEF configuration is enabled
  - The content of blocks “KILL_PWD” (2Fh) and “Kill keyhole” (30h) can’t be read-out and are replaced with value 00h
- CRC_A is Cyclic Redundancy Check defined in NFC Forum digital specification for NFC-A technology.

If a command READ is received while the device is in state READY1 or READY2, the following specific behavior apply:

- The valid block address range is limited to [0:15]
- DATA in response roll-over to the content of block 0 after the block 15.
- The normal content of memory is always returned even if ANDEF is enabled in this region.

Table 21. READ timings

Symbol	Typical	Max	Unit
t_{READ}	70.5	4734	µs
t_{NACK}	-	4734	µs
$n_{FDT, READ}$	9	501	-

The timings showed in Figure 7. READ command outline and Table 21. READ timings are explained in Section 6.3: Timings.

6.4.3 WRITE

Figure 8. **WRITE command outline**

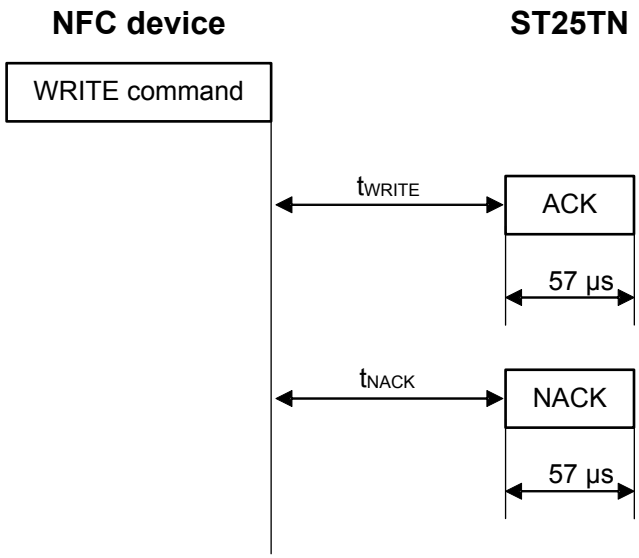


Table 22. **WRITE command format**

Byte	1	2	3	4	5	6	7	8
Field	Command code	Block address	DATA				CRC_A	
Content	A2h	1 byte	4 bytes				2 bytes	

- Block address is the address of the block to modify.
- DATA is the data to write.
- CRC_A is Cyclic Redundancy Check defined in NFC Forum digital specification for NFC-A technology.

The following responses may be issued upon reception of a WRITE command code:

Table 23. **Possible responses to the WRITE command**

Condition upon reception of WRITE command code	Response
Wrong number of bytes of payload	No response
Parity or CRC_A error	NACK1 (see Section 6.5.2: NACK response)
Block address is outside the valid address range. ST25TN01K valid address range is [0-3Fh] ([0-63])	NACK0 (see Section 6.5.2: NACK response)
Block address targets a read-only block. Read-only blocks includes the system read-only blocks and the blocks locked. The only exception is the block address 2, which is always considered as writable.	NACK0 (see Section 6.5.2: NACK response)
After writing EEPROM, the hardware check if is not OK	NACK5 (see Section 6.5.2: NACK response)
EEPROM successfully written	ACK (see Section 6.5.1: ACK response

Table 24. **WRITE timings**

Symbol	Typical	Max	Unit
t_{WRITE}	4163	4734	µs

Symbol	Typical	Max	Unit
t_{NACK}	-	4734	µs
$n_{FDT, WRITE}$	443	501	-

The timings of Figure 8. WRITE command outline and Table 24. WRITE timings are explained in Section 6.3: Timings.

6.5 Standard responses

If a command has an unknown command code the device doesn't answer.

Any error with or without answer changes the device state back to IDLE or HALT as described in Figure 4. State machine.

6.5.1 ACK response

ACK response is 4 bits equal to Ah conforming to T2 Tag specification to indicate a successful operation.

6.5.2 NACK response

NACK response is 4 bits conforming to T2 Tag specification to indicate an error.

The following NACK values are used:

Table 25. NACK responses

Name	Value (4 bits)	Meaning
NACK0	0h	Invalid argument
NACK1	1h	Parity or CRC_A error
NACK5	5h	EEPROM write error

6.5.3 ATQA/SENS_RES response

Upon reception of REQA (SENS_REQ) or WUPA (ALL_REQ) command, the device issues the following ATQA (SENS_RES) response indicating a double UID size (7 bytes):

Table 26. ATQA/SENS_RES response

Byte	1	2
Field	UID size & Anticollision info	Platform information
Content	44h	00h

In little endian representation, the corresponding 16 bits value is 0x0044.

6.5.4 SAK/SEL_RES response

Upon reception of SELECT (SEL_REQ) command with complete matching UID bits, the device issues the following SAK (SEL_RES) response indicating UID complete and PICC compliant with Type 2 tag platform and not ISO/IEC 14443-4.

Table 27. SAK/SEL_RES response

Byte	1	2	3
Field	Select acknowledge	CRC_A	
Content	00h	FEh	51h

7 Memory content at delivery

ST25TN is programmed during manufacturing to comply with NFC Forum INITIALIZED state so that it is readily usable by any NFC Forum compatible device.

Augmented NDEF fields are programmed during manufacturing so that only generic configuration as described in Section 5.4.1: ANDEF configuration is required to benefit from Augmented NDEF.

Table 28. Initial memory content

Block	Byte	Name	Parameter	Value	Description
03h	0	CC_0	Magic number	E1h	Indicates that this is a T2T
	1	CC_1	Version	10h	T2T current specification
	2	CC_2	Size	08h: for ST25TN512 14h: for ST25TN01K	T2T_Area_Size = 64 bytes : for ST25TN512 T2T_Area_Size = 160 bytes : for ST25TN01K
	3	CC_3	Access condition	00h	read/write access granted
04h	0	T2T_AREA	TLV Type	03h	NDEF
	1		TLV Length	00h	Empty NDEF
	2		TLV Type	FEh	Terminator TLV
	3		TLV Type	00h	NULL TLV
…	…	…	…	…	…
3Ch	0	ANDEF_CUSTOM	Source for custom field in ANDEF_MEM	ASCII coding of hexadecimal representation of UID	Unique to each IC
…	…				
3Fh	0				
	1				
	2	ANDEF_SEP	Source for fields separator in ANDEF_MEM	78h	ASCII code of ‘x’

8 Device parameters

8.1 Maximum ratings

Stressing the device above the rating listed in Table 29 may cause permanent damage to the device. These are stress ratings only and operation of the device, at these or any other conditions above those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 29. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_A	Ambient operating temperature		- 40	85	°C
T_{STG}	Storage temperature	UFDFPN5	-65	150	°C
		Sawn Wafer(1)	15	25	
t_{STG}	Sawn wafer(1) storage duration counted from ST production date		-	9	months
T_{LEAD}	Lead temperature during soldering		(2)		°C
V_{MAX_1}	Max input voltage peak-to-peak amplitude between AC0 and AC1		-	8.5	V
V_{ESD}	Electrostatic discharge voltage on all pins Human body model of ANSI/ESDA/JEDEC JS-001-2012 with C = 100 pF, R = 1500 Ω , R2 = 500 Ω		-	2000	V

1. *Sawn wafer on UV tape kept in its original packing form.*
2. *Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.*

8.2 RF characteristics

This section summarizes the operating and measurement conditions, and the RF characteristics of the device.

The parameters in the RF characteristics table that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables.

Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 30. RF characteristics

Symbol	Parameter	Condition(1)(2)	Min	Typ	Max	Unit
f_C	Frequency of external operating field (carrier)(3)	-	13.553	13.56	13.567	MHz
$MI_{CARRIER}$	Carrier Modulation Index(3)(4)	-	90	-	100	%
t_{Boot_RF}	Time from field activation (unmodulated carrier) to the beginning of first PCD command(3)	-	-	-	1	ms
t_{RF_OFF}	Time between RF OFF and chip reset(3)	-	-	-	0.1	ms
t_1	ISO/IEC 14443-2 pause A length(3)	f_C = 13.56 MHz	$27.5/f_C$	-	$41/f_C$	µs
t_2	ISO/IEC 14443-2 pause A low time(3)	f_C = 13.56 MHz	$6/f_C$	-	t_1	µs
t_3	ISO/IEC 14443-2 pause A rise time(3)	f_C = 13.56 MHz	0	-	$17/f_C$	µs
W_t	Time from the end of WRITE command EOF to the beginning of response SOF(3)	-	-	4.16	-	ms
C_{TUN}	Input capacitance(5)	f_C = 13.56 MHz, at POR level, on wafer and T_A = room temperature	47.5	50	52.5	pF

1. *For all parameters, by default T_A = - 40 to 85 °C.*
2. *All timing characterizations were performed using "test PCD assembly 1" defined in ISO/IEC 10373-6 and a "class 1" PICC with resonance frequency at 14.2 MHz.*
3. *Evaluated By Characterization – Not tested in production.*
4. *MI = [1 - b] / [1 + b], where b is the ratio between the modulated amplitude and the initial signal amplitude.*
5. *Evaluated By Characterization – Tested in production by correlating industrial tester measure with characterization results.*

8.3 Memory characteristics

This section summarizes the operating and measurement conditions, and the memory characteristics of the device.

The parameters in the Table 31 are derived from tests performed under the measurement conditions summarized in the relevant tables.

Designers should check that the operating conditions in their circuit match with the measurement conditions, when based on the parameters mentioned.

Table 31. Memory characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{RET}	Retention time(1)	$T_A \leq 55$ °C	40	-	-	year
Cycling	Write cycles endurance(1)	T_A = - 40 °C to 85 °C	100000	-	-	cycle

1. *Evaluated By Characterization – Not tested in production.*

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

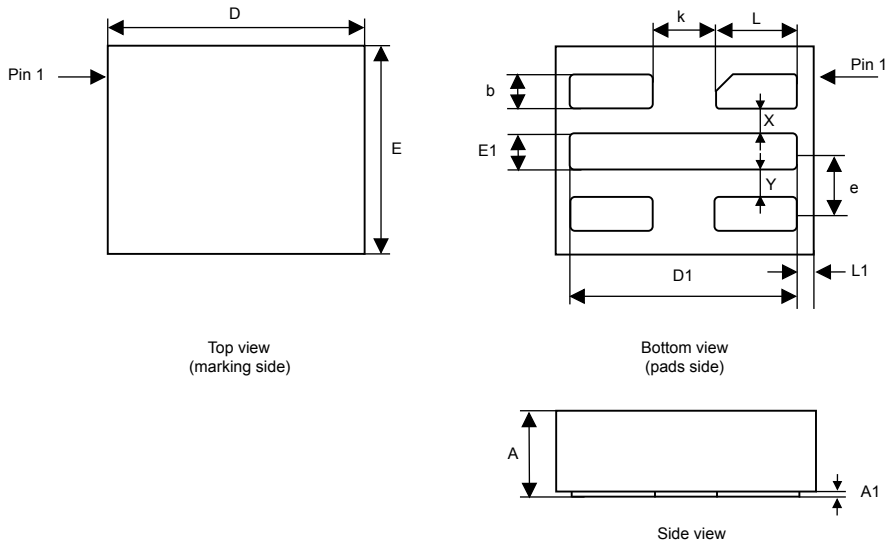
9.1 Sawn and bumped waver

Contact your STMicroelectronics sales office to get the description document.

9.2 UFDFPN5 (DFN5) package information

UFDFPN5 is a 5-lead, 1.7 × 1.4 mm, 0.55 mm thickness, ultrathin fine-pitch dual flat package.

Figure 9. UFDFPN5 - Outline



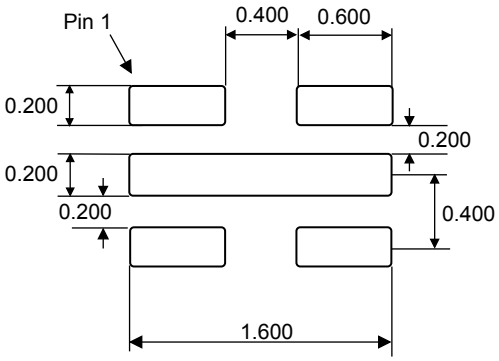
1. *The maximum package warpage is 0.05 mm.*
2. *Exposed copper is not systematic and can appear partially or totally according to the cross section.*
3. *Drawing is not to scale.*
4. *On the bottom side, pin 1 is identified by the specific pad shape and, on the top side, pin 1 is defined from the orientation of the marking. When reading the marking, pin 1 is below the upper left package corner.*

Table 32. UFDFPN5 - Mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	-	0.050	0.0000	-	0.0020
b(1)	0.175	0.200	0.225	0.0069	0.0079	0.0089
D	1.600	1.700	1.800	0.0630	0.0669	0.0709
D1	1.400	1.500	1.600	0.0551	0.0591	0.0630
E	1.300	1.400	1.500	0.0512	0.0551	0.0591
E1	0.175	0.200	0.225	0.0069	0.0079	0.0089
X	-	0.200	-	-	0.0079	-
Y	-	0.200	-	-	0.0079	-
e	-	0.400	-	-	0.0157	-
L	0.500	0.550	0.600	0.0197	0.0217	0.0236
L1	-	0.100	-	-	0.0039	-
k	-	0.400	-	-	0.0157	-

1. *Dimension b applies to the plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.*

Figure 10. UFDFPN5 - Footprint example



1. *Dimensions are expressed in millimeters.*

10 Ordering information

ST25TN part numbers are coded according to the following table:

Table 33. Ordering information scheme

Example:	ST25TN	01K	-	A	F	G	5

Device type

ST25TN = NFC Forum T2T tag

Memory size

512 = 512 bits

01K = 1280 bits

Interface

A = Antenna

Features

F = Augmented NDEF

Package

F = 75 µm ± 10 µm bumped and sawn wafer

G = 120 µm ± 15 µm bumped and sawn wafer

H = UFDFPN5

Capacitance

5 = 50 pF

11 List of acronyms

Table 34. **List of acronyms**

Acronym	Definition
ANDEF	Augmented NDEF
ASCII	American standard code for information interchange
ATQA	Answer to request, Type A
CC	Capability container
CLn	Cascade level n
CRC_A	Cyclic redundancy check for NFC-A technology
DFN	Dual flat no-lead
EEPROM	Electrically erasable programmable read-only memory
EOF	End of frame
FDT	Frame delay time
GDPR	General data protection regulation
HLTA	Halt command, Type A
IC	Integrated circuit
IEC	International electrotechnical commission
ISO	International organization for standardization
NDEF	NFC data exchange format
NFC	Near field communication
PCD	Proximity coupling device
PICC	Proximity-integrated circuit card
POR	Power-on reset
RF	Radio frequency
RFID	Radio frequency identification
RFU	Reserved for future use
SAK	Select acknowledge
SEL	Select code
SOF	Start of frame
TLV	Type length value
T2T	Type 2 tag
UFDFPN	Ultra thin fine pitch dual flat package no-lead
UID	Unique identifier
WUPA	Wake-up command, Type A

Revision history

Table 35. **Document revision history**

Date	Revision	Changes
07-Sep-2021	1	Initial release.
8-Nov-2021	2	Updated: • Features • Section 5.4.3: ANDEF unique tap code
17-Dec-2021	3	Updated: • Section 3: Memory overview • Section 5.5: TruST25 digital signature
03-Nov-2023	4	Updated: • Table 8 • Section 5.2.3
14-Oct-2025	5	Updated: • Features • Description Add: • TruST25 Link

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved