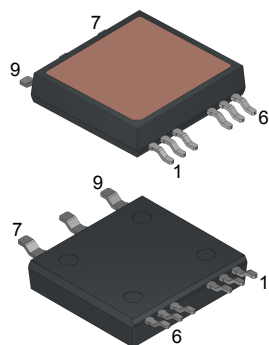
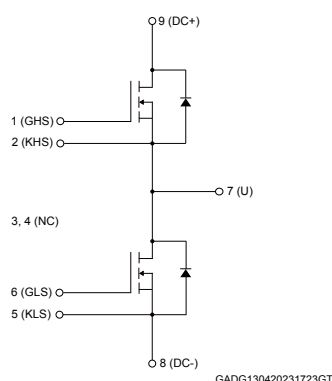


Automotive-grade ACEPACK SMIT half-bridge topology featuring 1200 V, 67 mΩ typ., 28 A SiC Power MOSFET



ACEPACK SMIT



Product status link

[SH70M12W3AG](#)

Product summary

Order code	SH70M12W3AG
Marking	SH70M12W3AG
Package	ACEPACK SMIT
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} typ.	I _D
SH70M12W3AG	1200 V	67 mΩ	28 A

- AQG 324 qualified 
- Half-bridge topology SiC MOSFET module
- 1200 V rated voltage
- Dice on direct bond copper (DBC) substrate
- SMD with insulated top side cooling
- Isolation voltage of 3.4 kVrms
- Low thermal resistance
- Package molding compound group I (CTI ≥ 600 V, 1000 Vrms in pollution degree 2)

Applications

- DC/DC converter for EV/HEV
- On board charger (OBC)

Description

The ACEPACK SMIT is a very compact surface mounted SiC MOSFET module. Thanks to the DBC substrate, the ACEPACK SMIT package provides reliable insulation, a low thermal resistance and high flexibility, enabling several configurations.

The SiC MOSFETs inside provide outstanding features, like very low on-resistance, fast switching, reduced parasitic, and robust body diode. The half-bridge association can be used to build several topologies: totem pole PFC, full, and B6 bridges.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating values)	-5 to 18	
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	28	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	20	
$I_{DM}^{(1)}$	Drain current (pulsed)	80	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	114	W
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage 50/60 Hz, $t = 60\text{ s}$)	3.4	kVrms
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{thJC}	Thermal resistance, junction-to-case	-	-	1.31	°C/W

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 1200\text{ V}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = -10\text{ to }22\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 5\text{ mA}$	1.8	3.0	4.2	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 18\text{ V}$, $I_D = 15\text{ A}$		67	78	m Ω
		$V_{GS} = 18\text{ V}$, $I_D = 15\text{ A}$, $T_J = 175\text{ }^{\circ}\text{C}$		127		

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 850\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	900	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance		-	5	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.3	-	Ω
Q_g	Total gate charge	$V_{DD} = 850\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = -5\text{ to }18\text{ V}$	-	37	-	nC
Q_{gs}	Gate-source charge		-	11	-	nC
Q_{gd}	Gate-drain charge		-	14	-	nC

Table 5. Switching energy (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	$V_{DD} = 850\text{ V}$, $I_D = 15\text{ A}$, $R_G = 10\text{ }\Omega$, $V_{GS} = -5\text{ to }18\text{ V}$	-	248	-	μJ
E_{off}	Turn-off switching energy		-	89	-	μJ
E_{tot}	Total switching energy		-	337	-	μJ

Table 6. Switching characteristics (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 850\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = -5\text{ to }18\text{ V}$, $R_G = 10\text{ }\Omega$	-	9	-	ns
t_r	Rise time		-	4.1	-	ns
$t_{d(off)}$	Turn-off delay time		-	38.5	-	ns
t_f	Fall time		-	16.5	-	ns

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

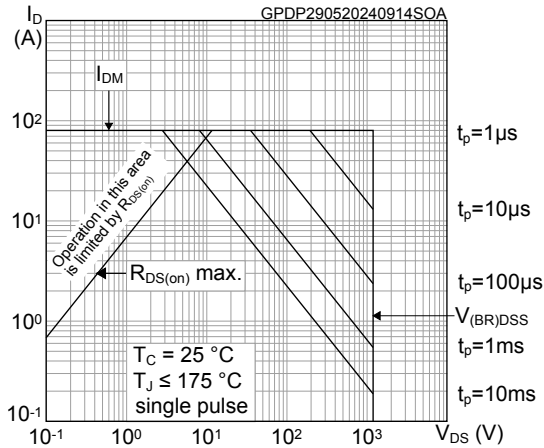


Figure 2. Maximum transient thermal impedance

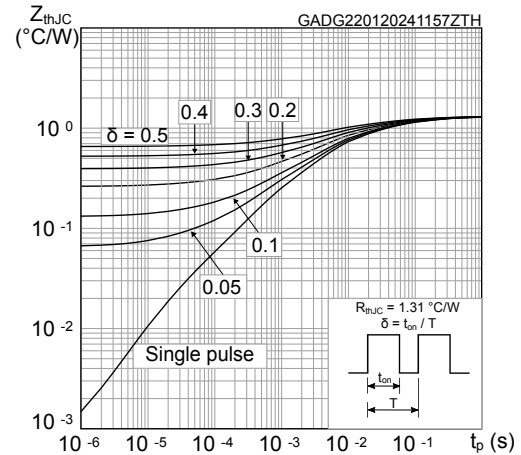


Figure 3. Typical output characteristics ($T_J = 25\text{ °C}$)

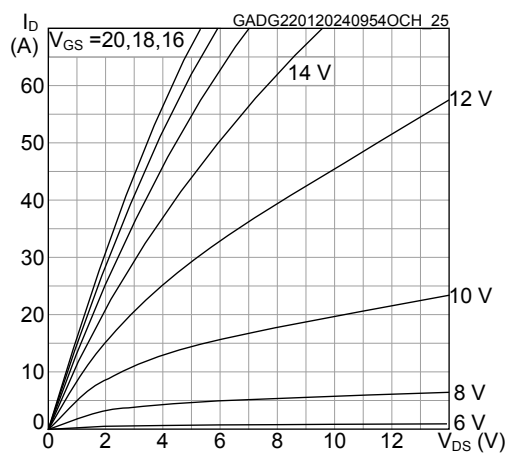


Figure 4. Typical output characteristics ($T_J = 175\text{ °C}$)

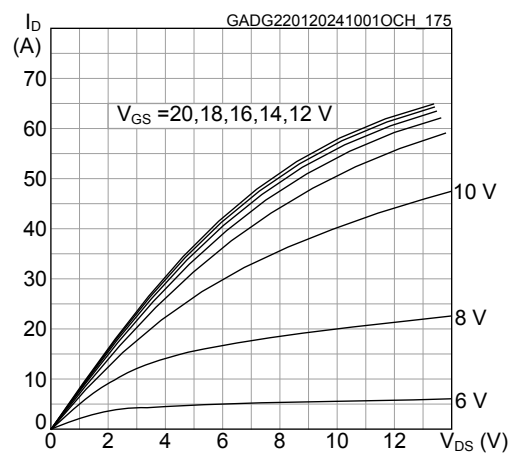


Figure 5. Typical transfer characteristics

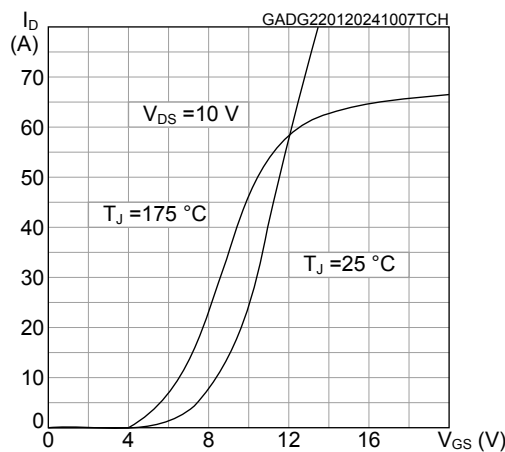


Figure 6. Total power dissipation

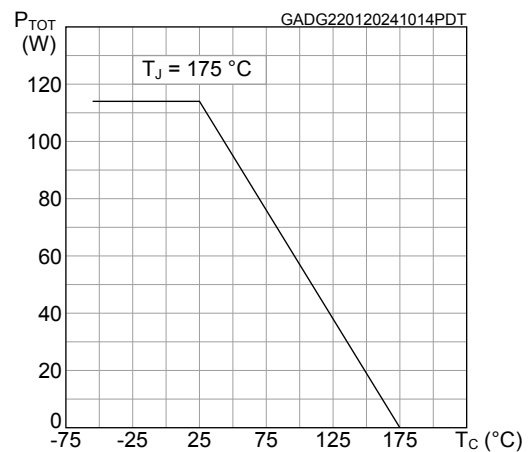


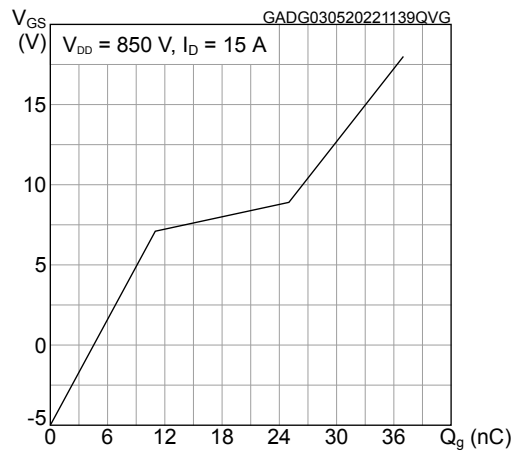
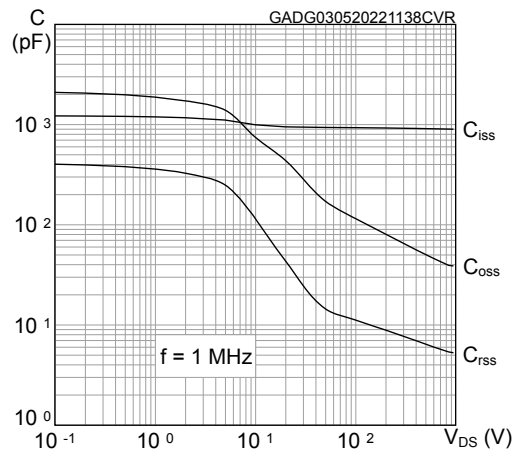
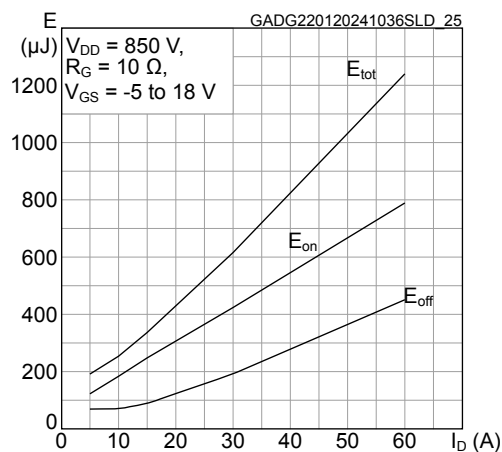
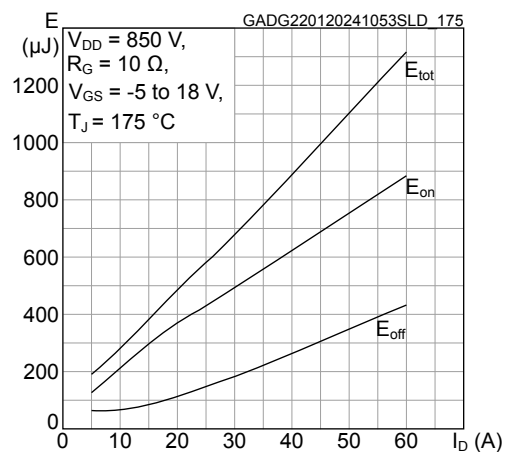
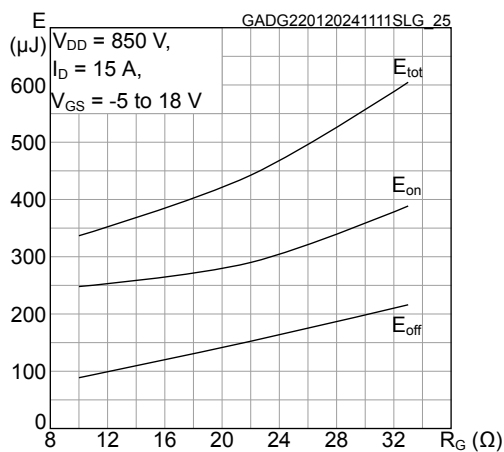
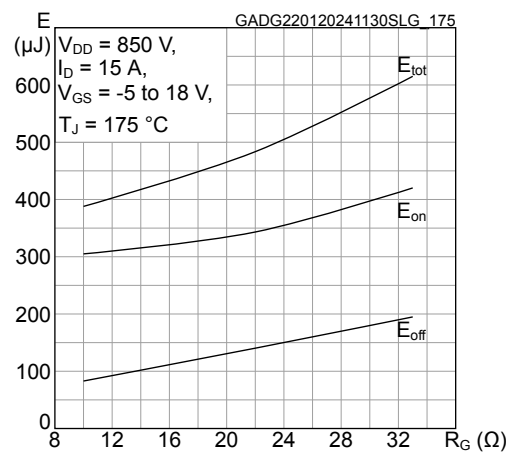
Figure 7. Typical gate charge characteristics

Figure 8. Typical capacitance characteristics

Figure 9. Typical switching energy vs drain current ($T_J = 25\text{ }^\circ\text{C}$)

Figure 10. Typical switching energy vs drain current ($T_J = 175\text{ }^\circ\text{C}$)

Figure 11. Typical switching energy vs gate resistance ($T_J = 25\text{ }^\circ\text{C}$)

Figure 12. Typical switching energy vs gate resistance ($T_J = 175\text{ }^\circ\text{C}$)


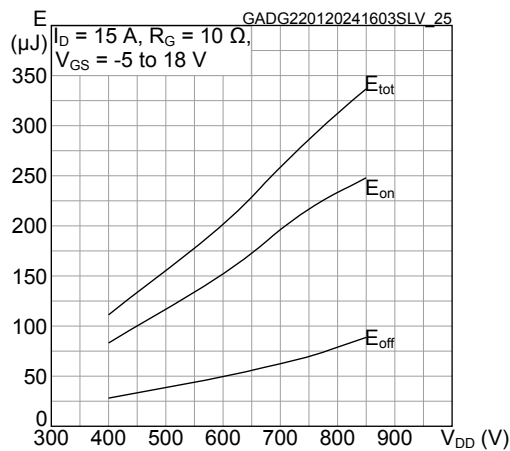
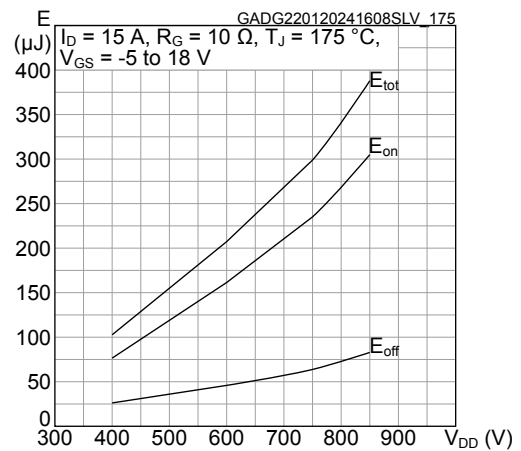
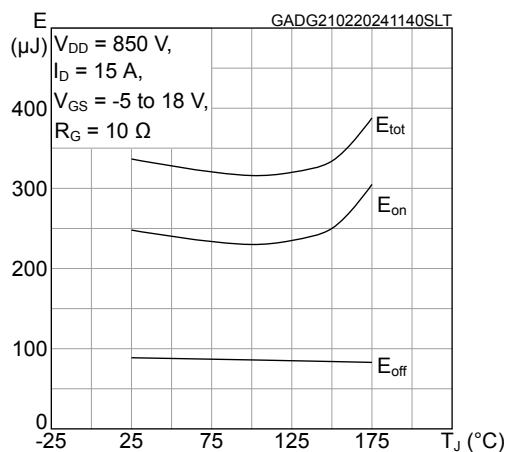
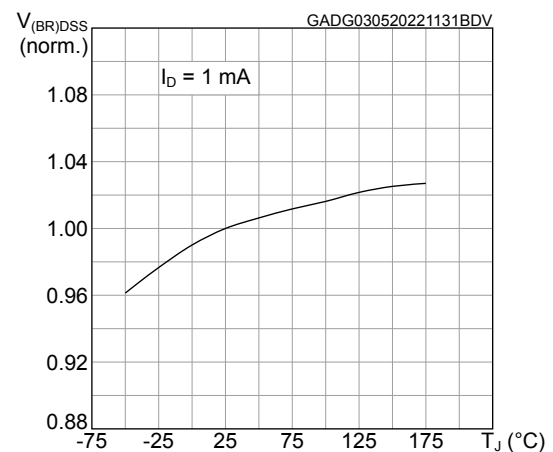
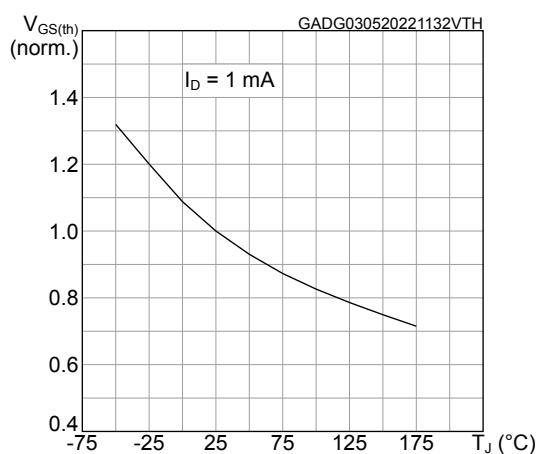
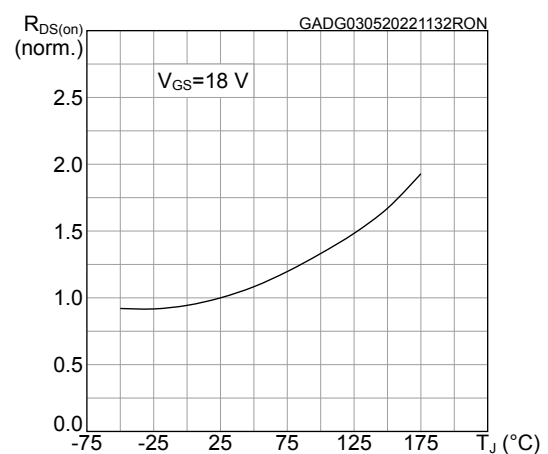
Figure 13. Typical switching energy vs supply voltage
 $(T_J = 25\text{ }^{\circ}\text{C})$

Figure 14. Typical switching energy vs supply voltage
 $(T_J = 175\text{ }^{\circ}\text{C})$

Figure 15. Typical switching energy vs temperature

Figure 16. Normalized breakdown voltage vs temperature

Figure 17. Normalized gate threshold vs temperature

Figure 18. Normalized on-resistance vs temperature


Figure 19. Typical reverse conduction characteristics
($T_J = 25\text{ }^{\circ}\text{C}$)

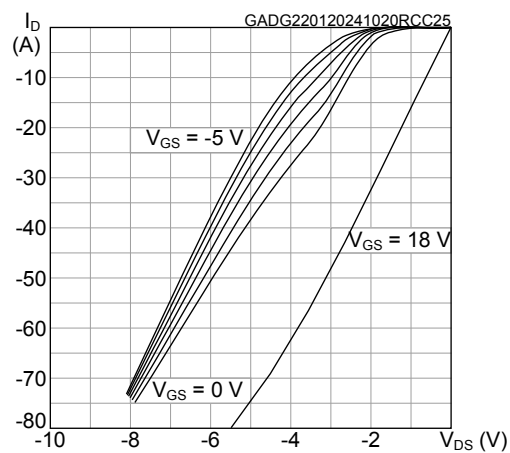
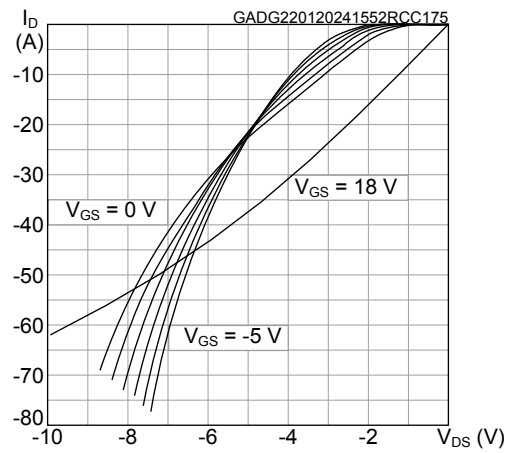


Figure 20. Typical reverse conduction characteristics
($T_J = 175\text{ }^{\circ}\text{C}$)

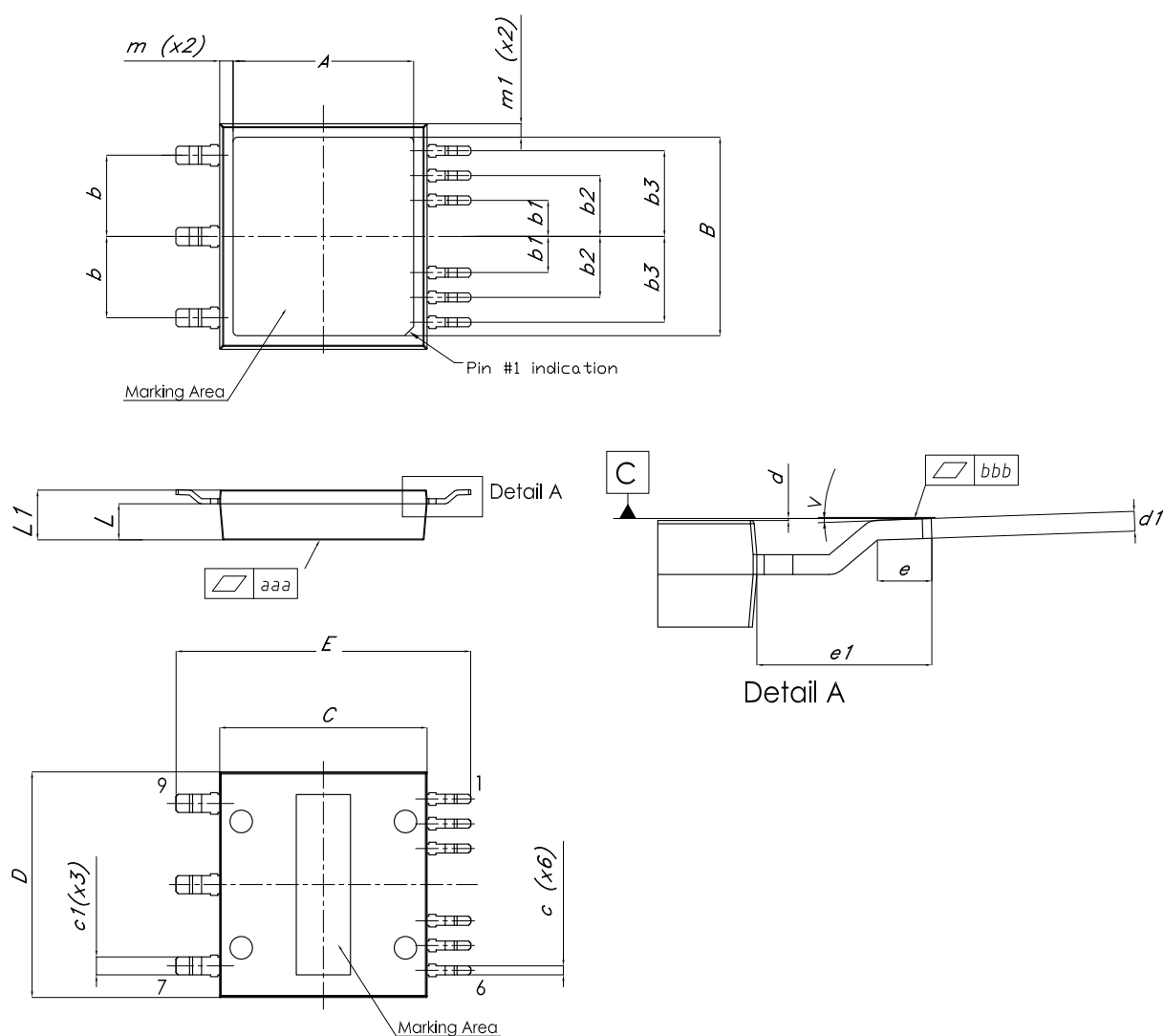


3 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 ACEPACK SMIT package information

Figure 21. ACEPACK SMIT package outline

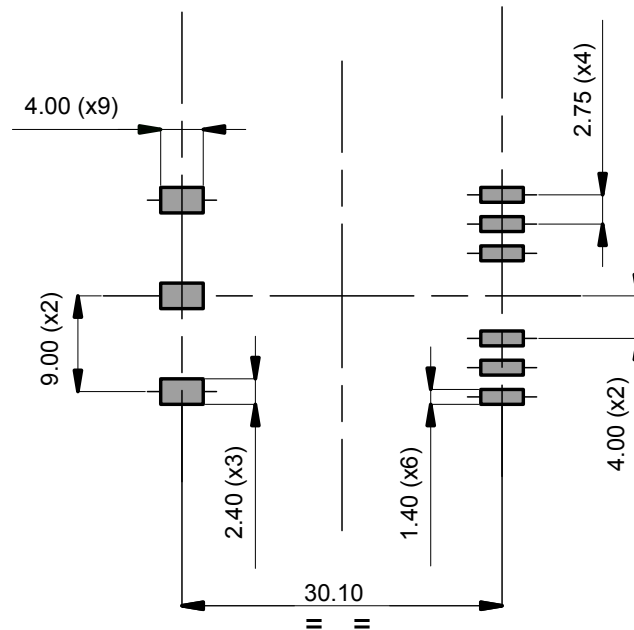


DM00447519_Rev.7

Table 7. ACEPACK SMIT package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	19.50	20.00	20.50
B	21.50	22.00	22.50
C	22.80	23.00	23.20
D	24.80	25.00	25.20
E	32.20	32.70	33.20
b		9.00	
b1		4.00	
b2		6.75	
b3		9.50	
c	0.95	1.00	1.10
c1	1.95	2.00	2.10
d	0.00		0.15
d1	0.45	0.55	0.65
e	1.30	1.50	1.70
e1	4.65	4.85	5.05
L	3.95	4.00	4.05
L1	5.40	5.50	5.60
m	1.30	1.50	1.80
m1	1.30	1.50	1.80
V	0°	2°	4°
aaa	0.01		0.05
bbb	0.00		0.10

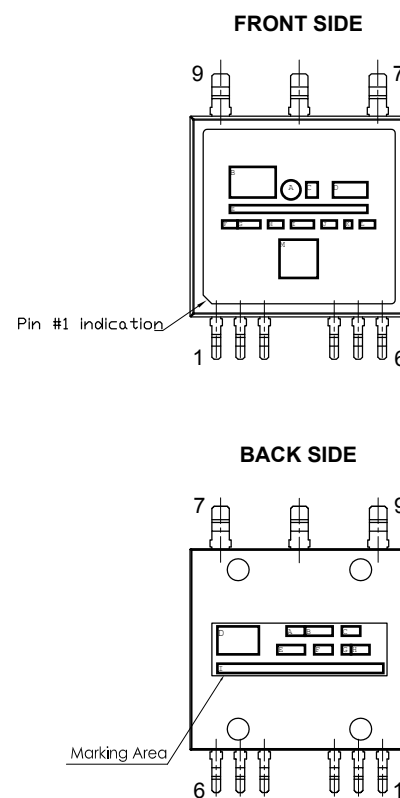
Figure 22. ACEPACK SMIT recommended footprint



DM00447519_FP_Rev.7

Note: Dimensions in mm.

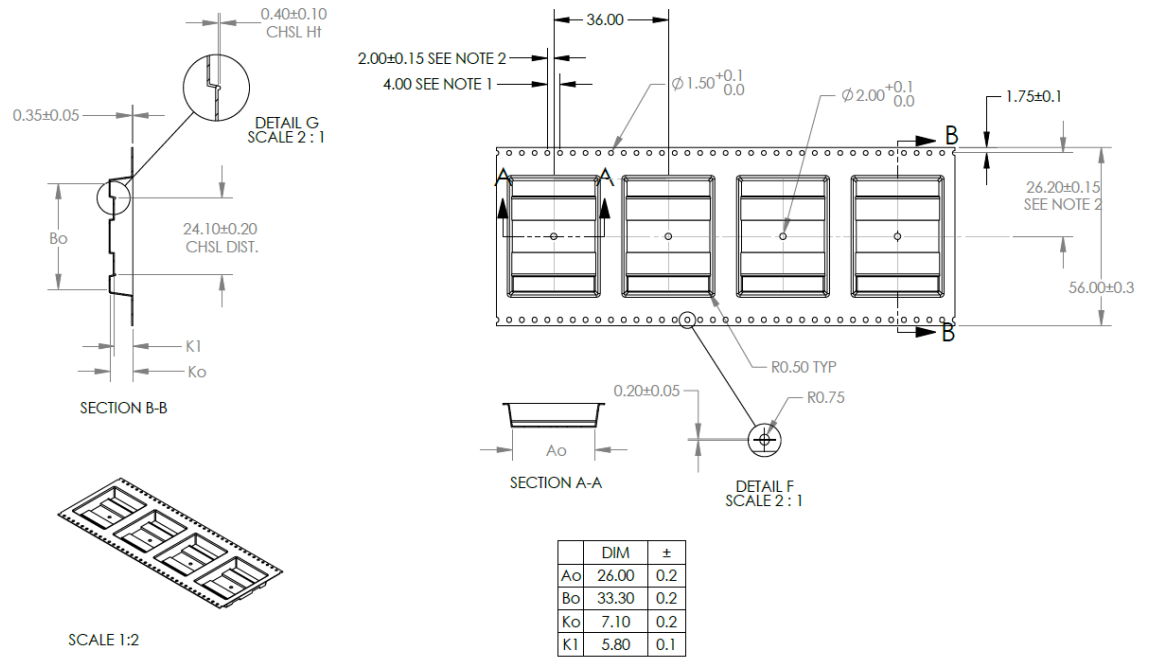
Figure 23. ACEPACK SMIT marking orientation vs pinout



DM00447519_MO_Rev.7

3.2 ACEPACK SMIT packing information

Figure 24. ACEPACK SMIT tape outline



- NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
 2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
 3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

DM00631393_Tape_Rev.1

Note: Dimensions in mm.

Revision history

Table 8. Document revision history

Date	Revision	Changes
20-Apr-2023	1	First release.
25-Jan-2024	2	Updated <i>Features</i> on cover page. Updated <i>Table 1. Absolute maximum ratings</i> , <i>Table 3. On/off states</i> , <i>Table 4. Dynamic characteristics</i> , <i>Table 5. Switching characteristics (resistive load)</i> and <i>Section 2.1: Electrical characteristics (curves)</i> .
23-Feb-2024	3	Modified I_D value on cover page. Added <i>Figure 15. Typical switching energy vs temperature</i> . Minor text changes.
06-May-2024	4	Added <i>Table 5. Switching energy (resistive load)</i> .
26-May-2024	5	Updated <i>Table 3. On/off states</i> . Updated <i>Figure 1. Safe operating area</i> .
14-Nov-2024	6	Updated <i>Table 2. Thermal data</i> .

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