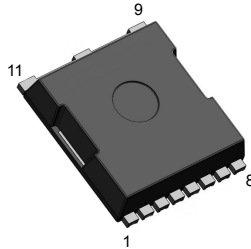
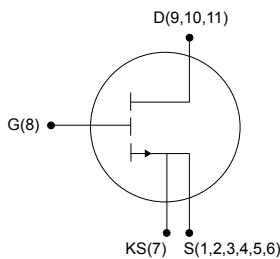


700 V, 53 mΩ typ., 26 A, e-mode PowerGaN transistor



TO-LL



G8KS7S123456D91011



Product status link

[SGT070R70HTO](#)

Product summary

Order code	SGT070R70HTO
Marking	070R70H
Package	TO-LL
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	Series
SGT070R70HTO	700 V	70 mΩ	26 A	G-HEMT

- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Kelvin source pad for optimum gate driving
- Zero reverse recovery charge
- ESD safeguard

Applications

- AC-DC converters
- DC-DC converters
- Solar inverters

Description

The **SGT070R70HTO** is a 700 V, 26 A e-mode PowerGaN transistor combined with a well established packaging technology. The resulting G-HEMT device provides extremely low conduction losses, high current capability and ultra fast switching operation to enable high power density and unbeatable efficiency performances.

1 Electrical ratings

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	700 ⁽¹⁾	V
	Drain-source voltage (transient, $t_p < 200\text{ }\mu\text{s}$)	800	
V_{GS}	Gate-source voltage	-6 to 7	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	26 ⁽²⁾	A
I_{DM}	Pulse drain current ($t_p = 10\text{ }\mu\text{s}$)	60	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	231	W
ESD	Human body model, $R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$	2	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. Recommended continuous maximum bus voltage during switching operations should not exceed 450 V.
2. Limited by design.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.54	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	56.47 ⁽¹⁾	°C/W

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}$		1	65	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}, T_J = 150\text{ }^{\circ}\text{C}$		10		
I_{GSS}	Gate-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 6\text{ V}$		110		μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 40\text{ mA}$	1.2	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 6\text{ V}, I_D = 10\text{ A}$		53	70	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 10\text{ A}, T_J = 150\text{ }^{\circ}\text{C}$		122		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}, f = 100\text{ kHz}$	-	300	-	pF
C_{oss}	Output capacitance		-	135	-	pF
C_{rss}	Reverse transfer capacitance		-	2.3	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }400\text{ V}$	-	190	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	240	-	pF
R_g	Intrinsic gate resistance	$f = 5\text{ MHz}, I_D = 0\text{ A}$	-	1.4	-	Ω
V_{plat}	Gate plateau voltage	$V_{DS} = 400\text{ V}, I_D = 10\text{ A}$	-	2.3	-	V
Q_g	Total gate charge	$V_{GS} = 0\text{ to }6\text{ V}, V_{DS} = 400\text{ V}, I_D = 10\text{ A}$	-	8.5	-	nC
Q_{gs}	Gate-source charge		-	0.7	-	nC
Q_{gd}	Gate-drain charge		-	3.6	-	nC
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$	-	0	-	nC
Q_{oss}	Output charge		-	94.7	-	nC

- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.
- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 400\text{ V}, I_D = 20\text{ A}, V_{GS} = 6\text{ V},$ $R_{G(on)} = 10\text{ }\Omega, R_{G(off)} = 2\text{ }\Omega,$ $L = 350\text{ }\mu\text{H}$	-	10	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	7	-	ns
t_f	Fall time		-	9	-	ns

Table 6. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 10\text{ A}$	-	2.4	-	V

2.1 Electrical characteristics (curves)

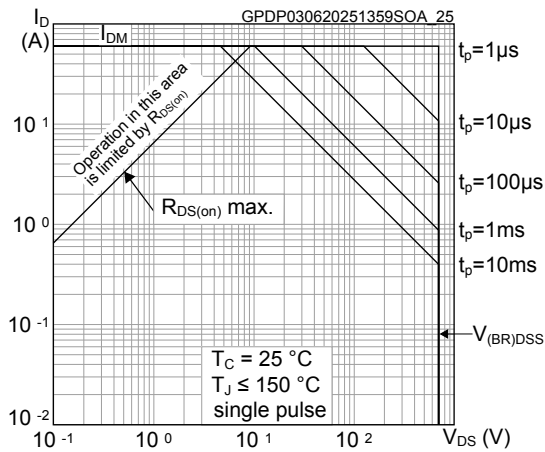
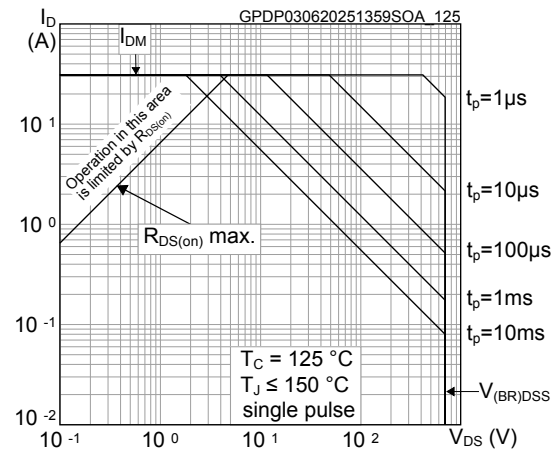
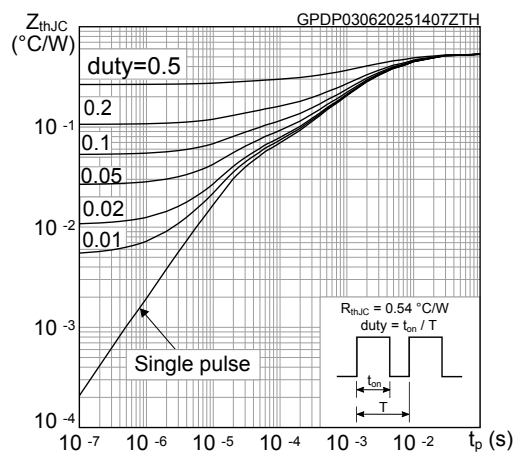
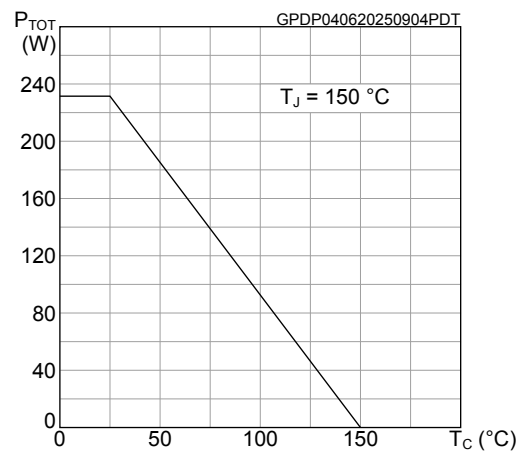
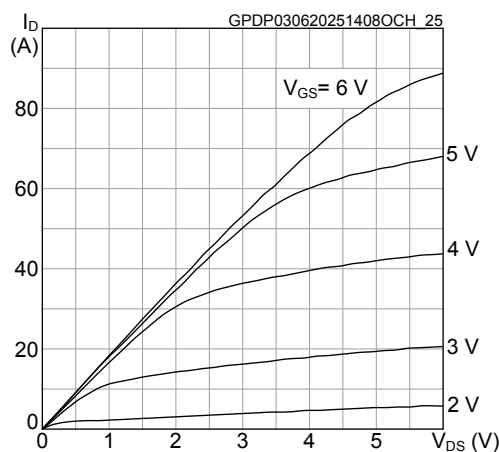
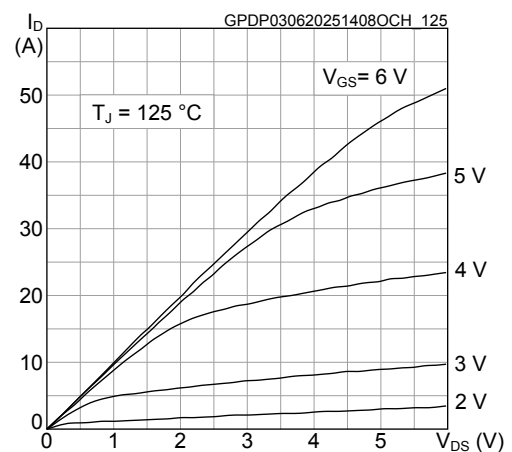
Figure 1. Safe operating area ($T_C = 25\text{ }^{\circ}\text{C}$)

Figure 2. Safe operating area ($T_C = 125\text{ }^{\circ}\text{C}$)

Figure 3. Maximum transient thermal impedance

Figure 4. Total power dissipation

Figure 5. Typical output characteristics ($T_J = 25\text{ }^{\circ}\text{C}$)

Figure 6. Typical output characteristics ($T_J = 125\text{ }^{\circ}\text{C}$)


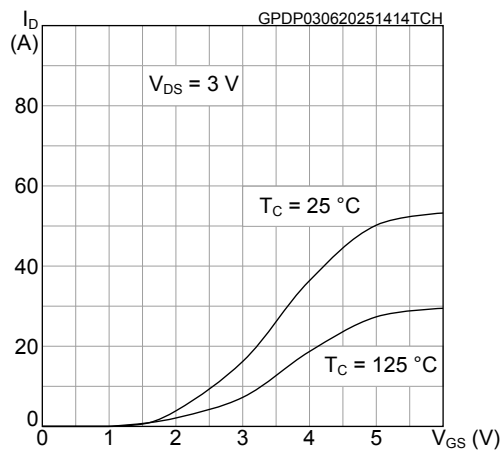
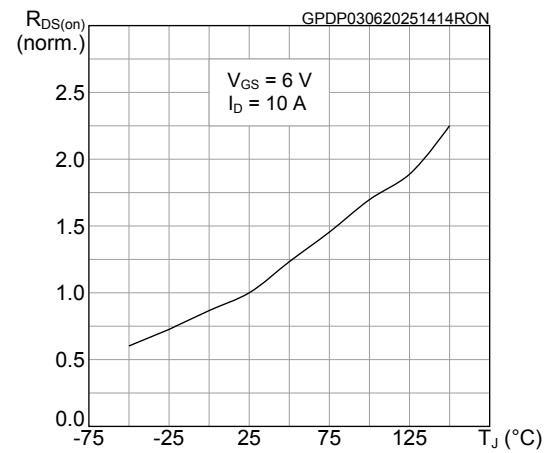
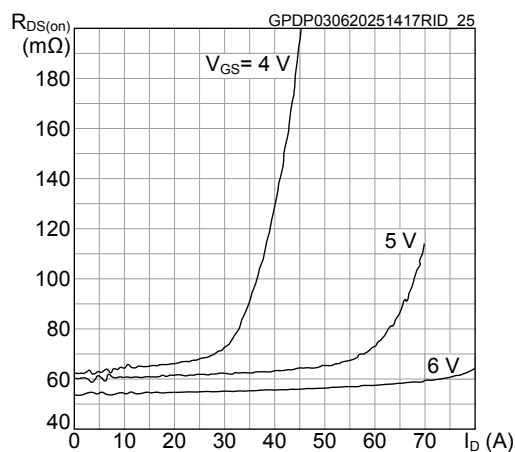
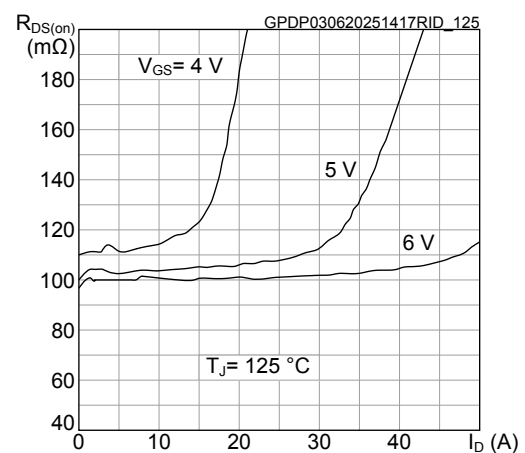
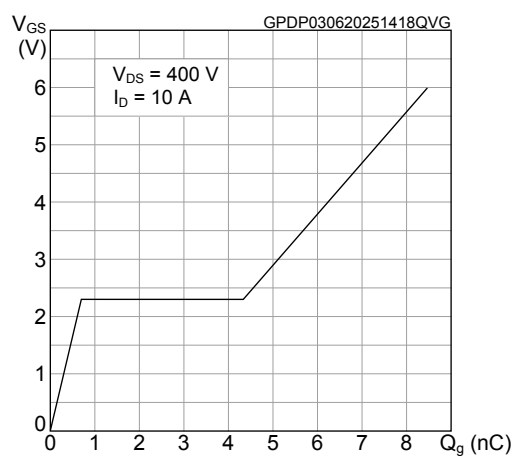
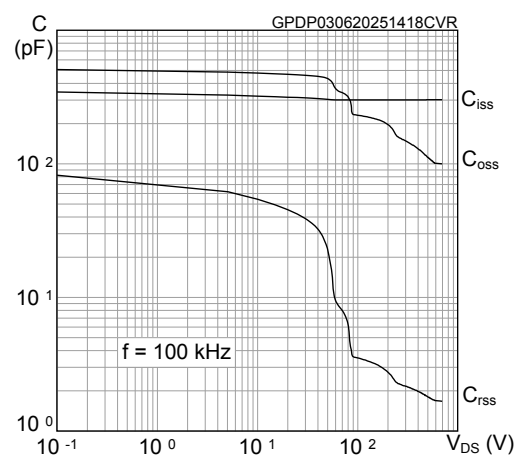
Figure 7. Typical transfer characteristics

Figure 8. Normalized on-resistance vs temperature

Figure 9. Typical drain-source on-resistance ($T_J = 25 \text{ }^{\circ}\text{C}$)

Figure 10. Typical drain-source on-resistance ($T_J = 125 \text{ }^{\circ}\text{C}$)

Figure 11. Typical gate charge characteristics

Figure 12. Typical capacitance characteristics


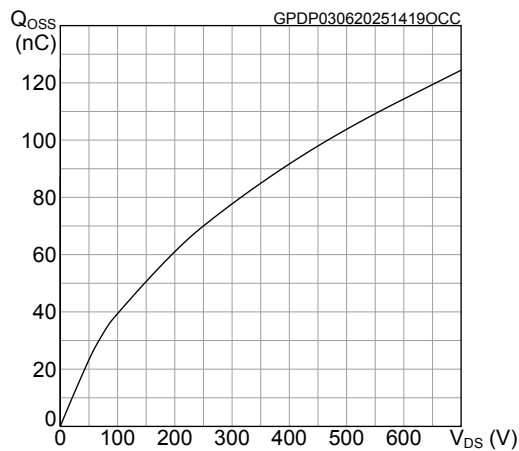
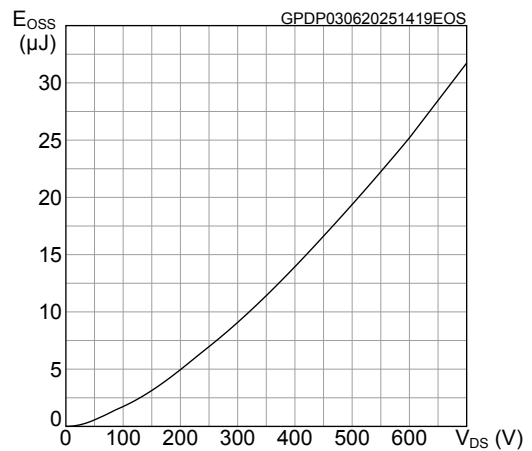
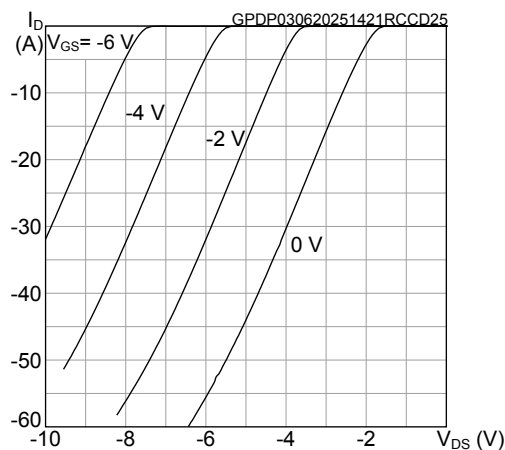
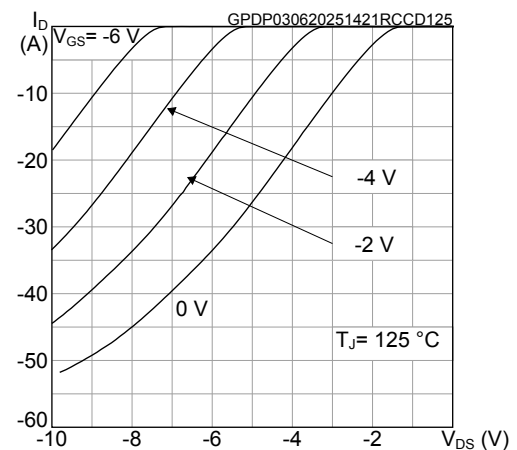
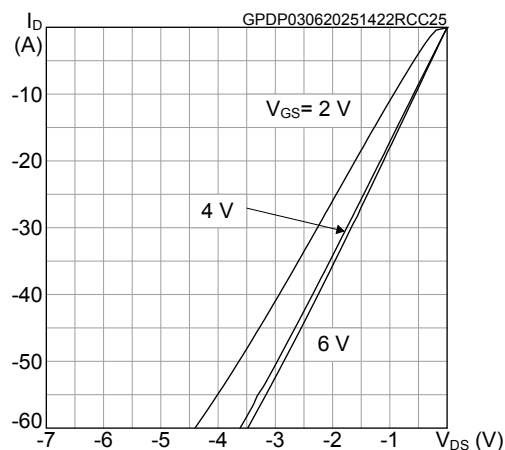
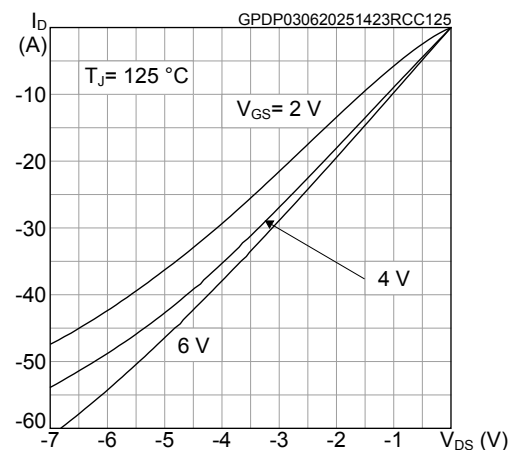
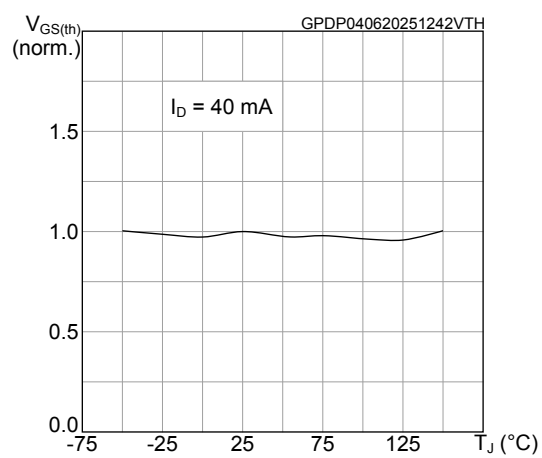
Figure 13. Typical output capacitance charge

Figure 14. Typical output capacitance stored energy

Figure 15. Typical diode reverse conduction characteristics ($T_J = 25^\circ\text{C}$)

Figure 16. Typical diode reverse conduction characteristics ($T_J = 125^\circ\text{C}$)

Figure 17. Typical reverse conduction characteristics ($T_J = 25^\circ\text{C}$)

Figure 18. Typical reverse conduction characteristics ($T_J = 125^\circ\text{C}$)


Figure 19. Normalized gate threshold vs temperature



3 Test circuits

Figure 20. Test circuit for inductive load switching times

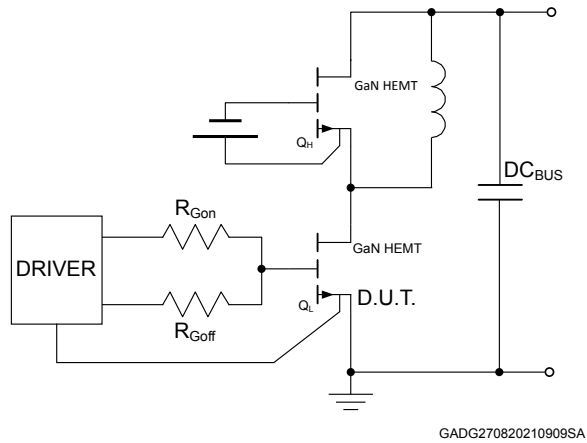
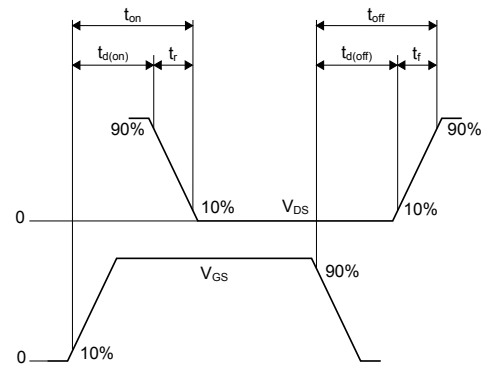


Figure 21. Switching time waveforms

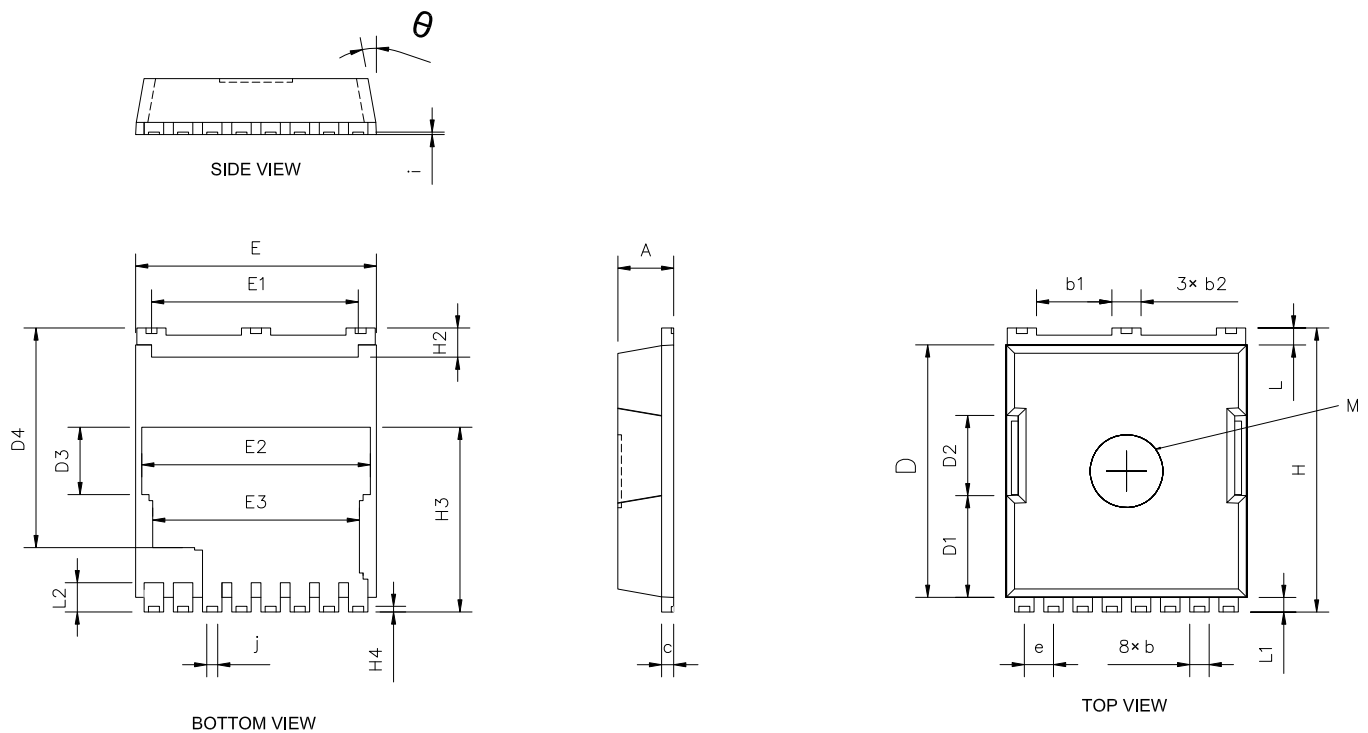


4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL for PowerGaN package information

Figure 22. TO-LL for PowerGaN package outline

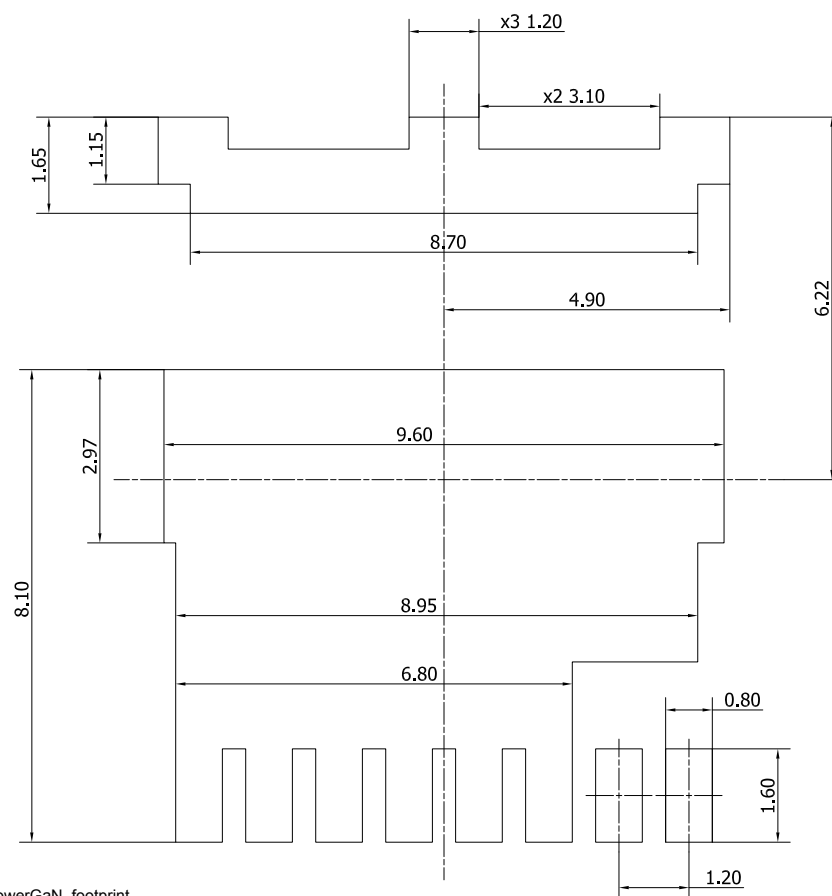


DM00276569_rev.9_PowerGaN

Table 7. TO-LL for PowerGaN mechanical data

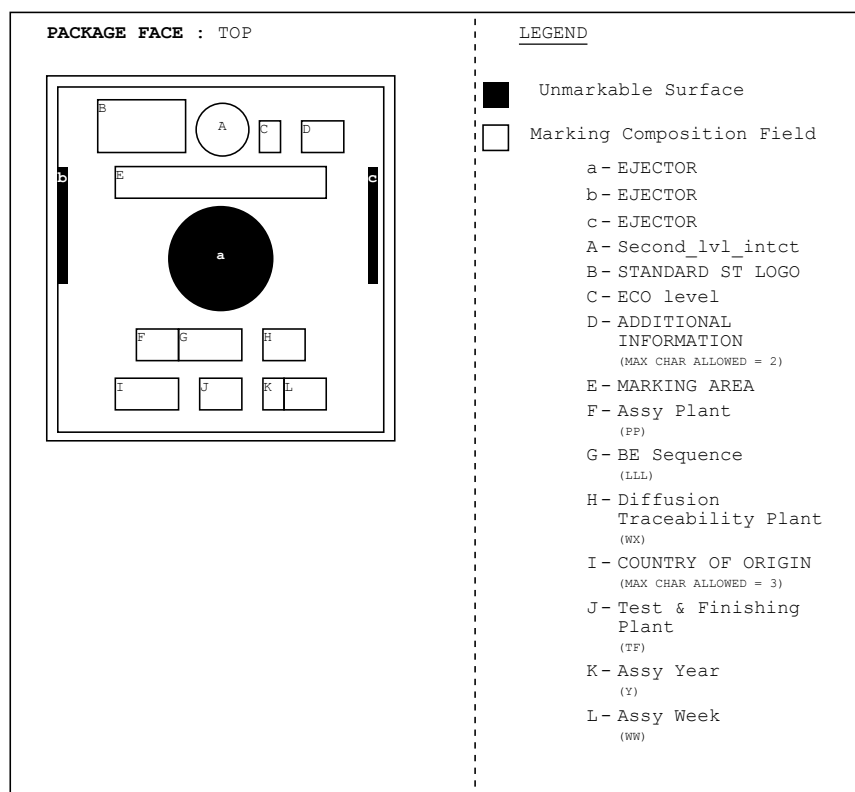
Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	3.00	3.10	3.20
b2	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.28	10.38	10.58
D1	4.18 REF		
D2	3.30 REF		
D3	2.77 REF		
D4	9.03 REF		
E	9.70	9.90	10.10
E1	8.50 REF		
E2	9.40 REF		
E3	8.50 REF		
e	1.10	1.20	1.30
H	11.48	11.68	11.88
H2	1.10	1.20	1.30
H3	7.50	7.60	7.70
H4	0.13	0.23	0.33
i	0.10		
j	0.42	0.45	0.50
L	0.50	0.70	0.90
L1	0.50	0.60	0.70
L2	1.05	1.20	1.30
M	3 REF		
Θ	10° REF		

Figure 23. TO-LL for PowerGaN recommended footprint (dimensions are in mm)



DM00276569_rev.9_PowerGaN_footprint

Figure 24. Marking composition for TO-LL for PowerGaN



DM01042834_Rev2

Engineering samples

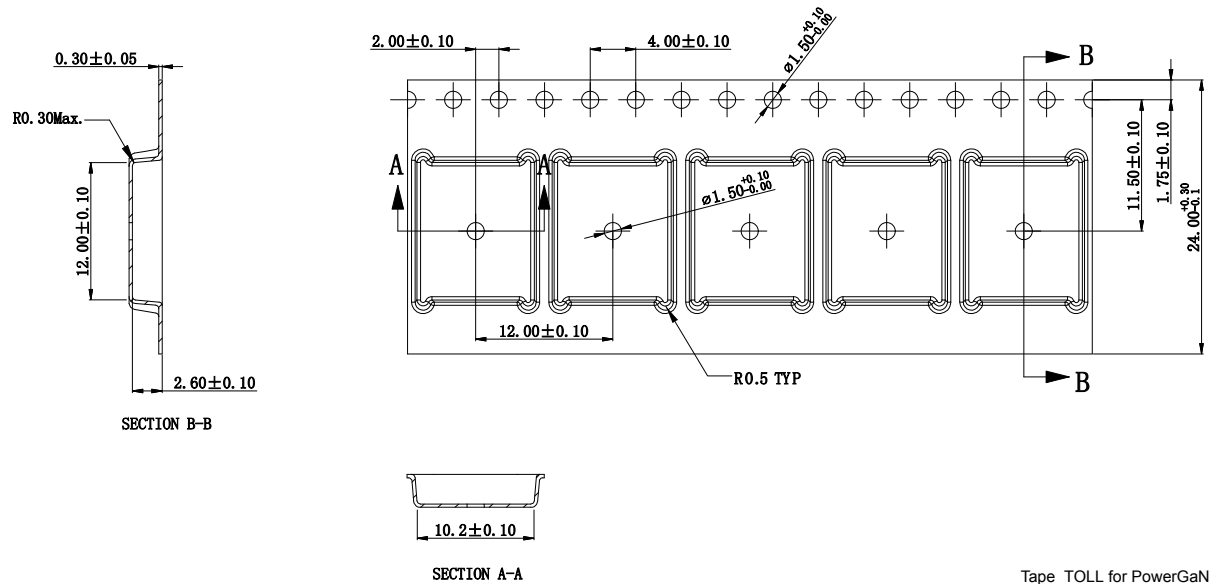
These samples are clearly identified by "ES" digits in the marking additional information field of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial samples

Fully qualified parts from ST standard production with no limitations of use or special identification marking.

4.2 TO-LL for PowerGaN packing information

Figure 25. TO-LL for PowerGaN tape (dimensions are in mm)



Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Jun-2025	1	First release.

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