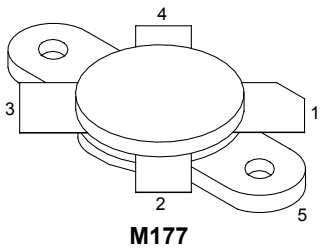
SD2933-06W

Datasheet

300 W, 50 V, 30 MHz, RF power DMOS transistor



M177

Pin connection	
Pin	**Connection**
1	Drain
2	Source
3	Gate
4	Source
5	Source

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
SD2933-06W	30 MHz	50 V	300 W	20 dB	65

- Gold metallization
- Excellent thermal stability
- Common source configuration
- P_{OUT} = 300 W min. with 20 dB gain @ 30 MHz
- Thermally enhanced packaging for lower junction temperatures

Applications

- ISM

Description

The SD2933-06W is a gold metallized N-channel MOS field-effect RF power transistor, intended for use in 50 V DC large signal applications up 150 MHz. Its special low thermal resistance package, makes it ideal for ISM applications, where reliability and ruggedness are critical factors.

STPOWER

Product status link
SD2933-06W

Product summary	
Order code	SD2933-06W
Marking	SD2933
Package	M177
Packing	Box
Base/bulk quantity	25

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	130	V
V_{DGR}	Drain-gate voltage (R_{GS} = 1 MΩ)	130	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current	40	A
P_{TOT}	Total power dissipation at T_C = 25 °C	648	W
T_{stg}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.27	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 200 mA	130			V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 50 V			100	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±500	nA
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 10 V, I_D = 250 mA	1.5		4	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 20 A			3	V
G_{FS}	Transconductance	V_{DS} = 10 V, I_D = 10 A	See Table 4. G_{FS} sort			S
C_{iss}	Common source input capacitance	V_{GS} = 0 V, V_{DD} = 50 V, f = 1 MHz		1000		pF
C_{rss}	Common source feedback capacitance			372		pF
C_{oss}	Common source output capacitance			29		pF

Table 4. G_{FS} sort

Code	Min.	Max.	Unit
C	12.00	12.99	S
D	13.00	13.99	S
E	14.00	14.99	S
F	15.00	15.99	S

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	V_{DD} = 50 V, I_{DQ} = 250 mA, f = 30 MHz	300	400	-	W
G_{PS}	Power gain	V_{DD} = 50 V, I_{DQ} = 250 mA, P_{OUT} = 300 W, f = 30 MHz	20	23.5	-	dB
η_D	Drain efficiency		50	65	-	%
VSWR	Load mismatch	V_{DD} = 28 V, I_{DQ} = 100 mA, P_{OUT} = 300 W, f = 30 MHz, all phases	3:1		-	

3 Impedance

Figure 1. Impedance data schematic

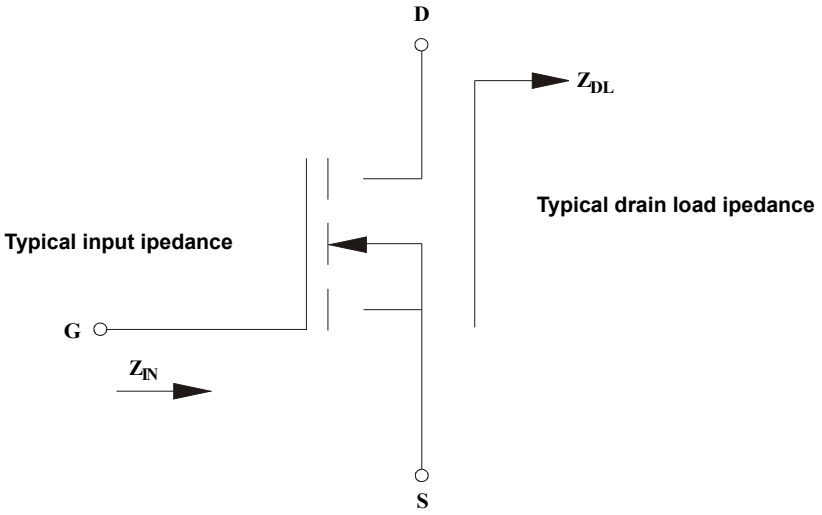


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Table 6. Impedance data

Frequency	$Z_{IN}(\Omega)$	$Z_{DL}(\Omega)$
30 MHz	1.8 - j 0.2	2.8 + j 2.3
108 MHz	1.9 + j 0.2	1.6 + j 1.4
175 MHz	1.9 + j 0.3	1.5 + j 1.6

4 Typical performances

Figure 2. Capacitance vs drain voltage

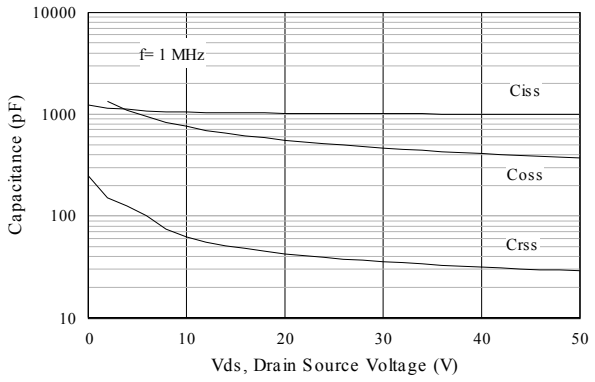

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Figure 3. Gate-source voltage vs case temperature

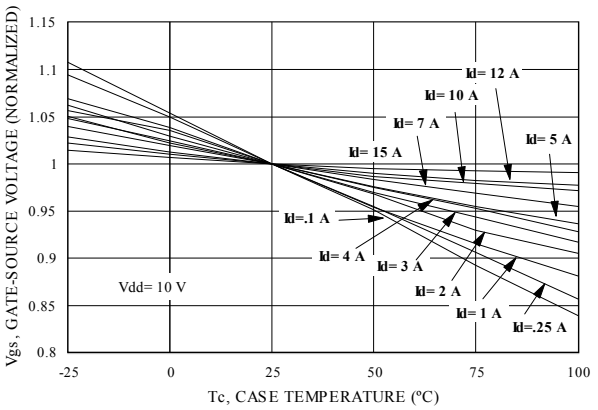

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Figure 4. Drain current vs gate voltage

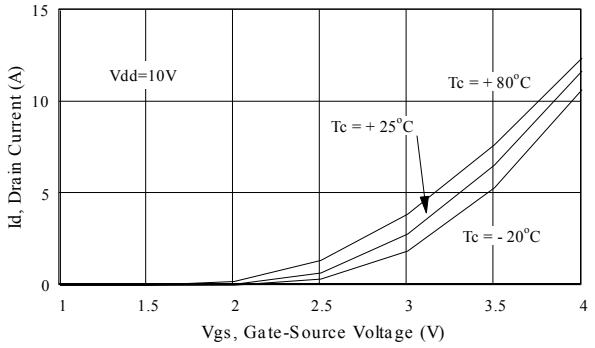

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Figure 5. Maximum thermal resistance vs. case temperature

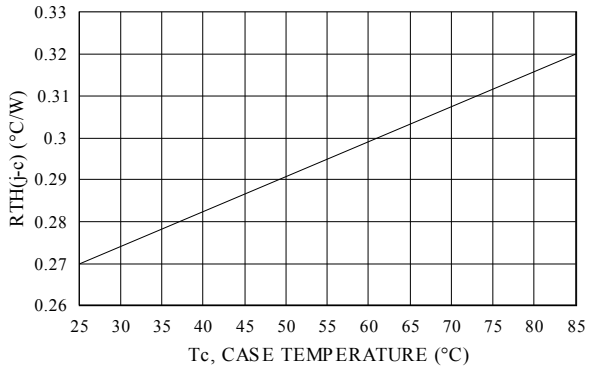

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Figure 6. Transient thermal impedance

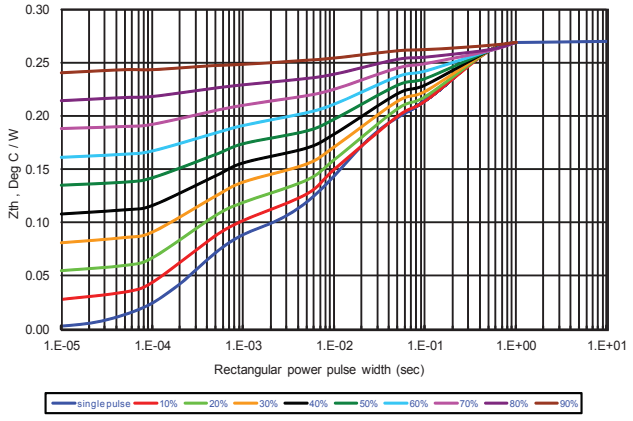

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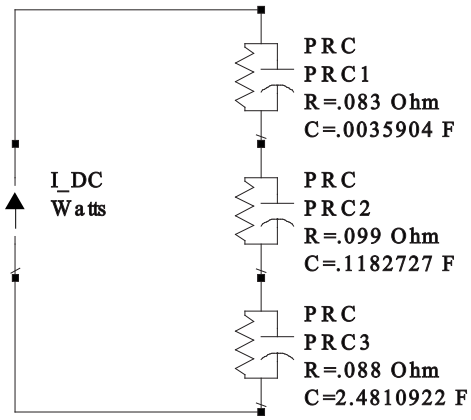
Figure 7. **Transient thermal impedance model**



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5 Typical performance (30 MHz)

Figure 8. Output power vs input power

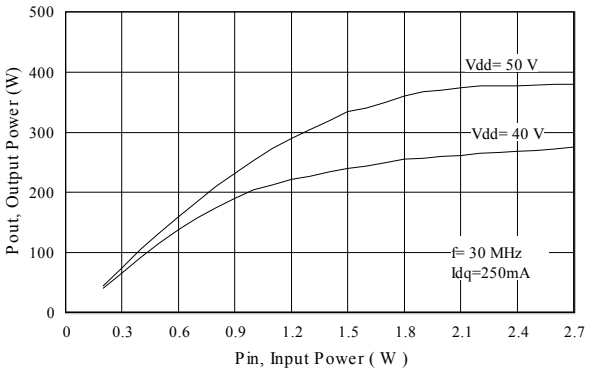

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Figure 9. Output power vs input power (at different temperature)

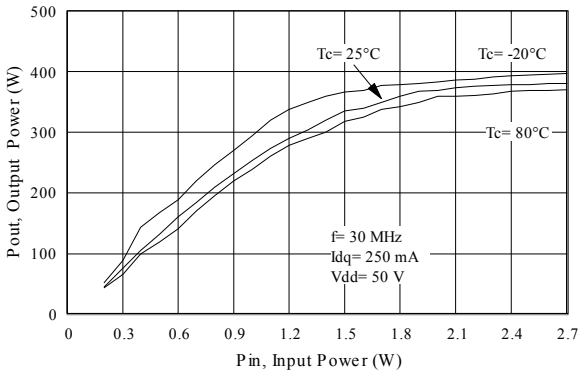

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Figure 10. Power gain vs output power

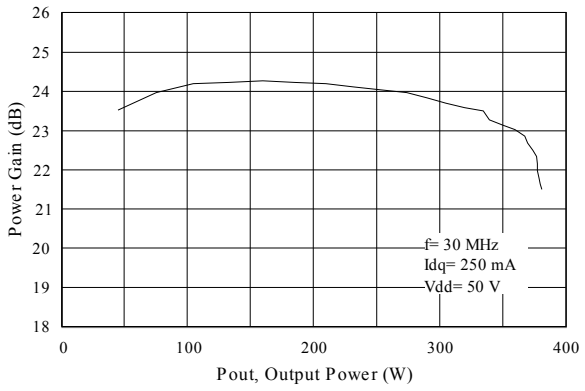

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Figure 11. Output power vs input power

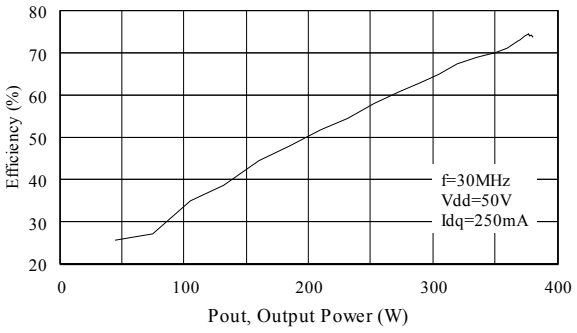

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Figure 12. Output power vs supply voltage

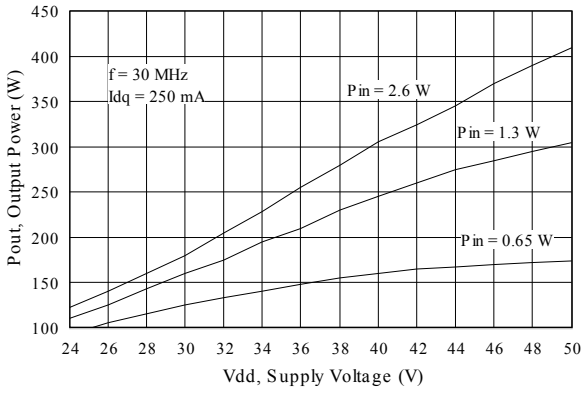

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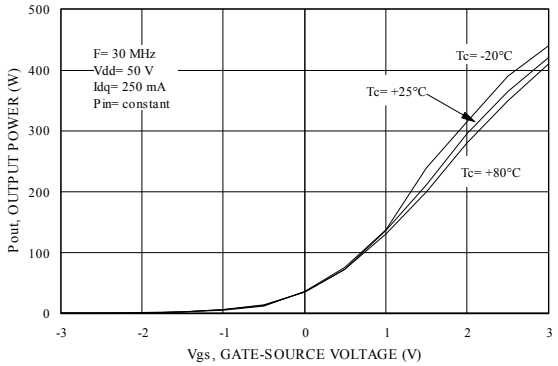
Figure 13. Output power vs gate voltage



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6 Test circuits

Figure 14. **Test circuit schematic (f = 30 MHz)**

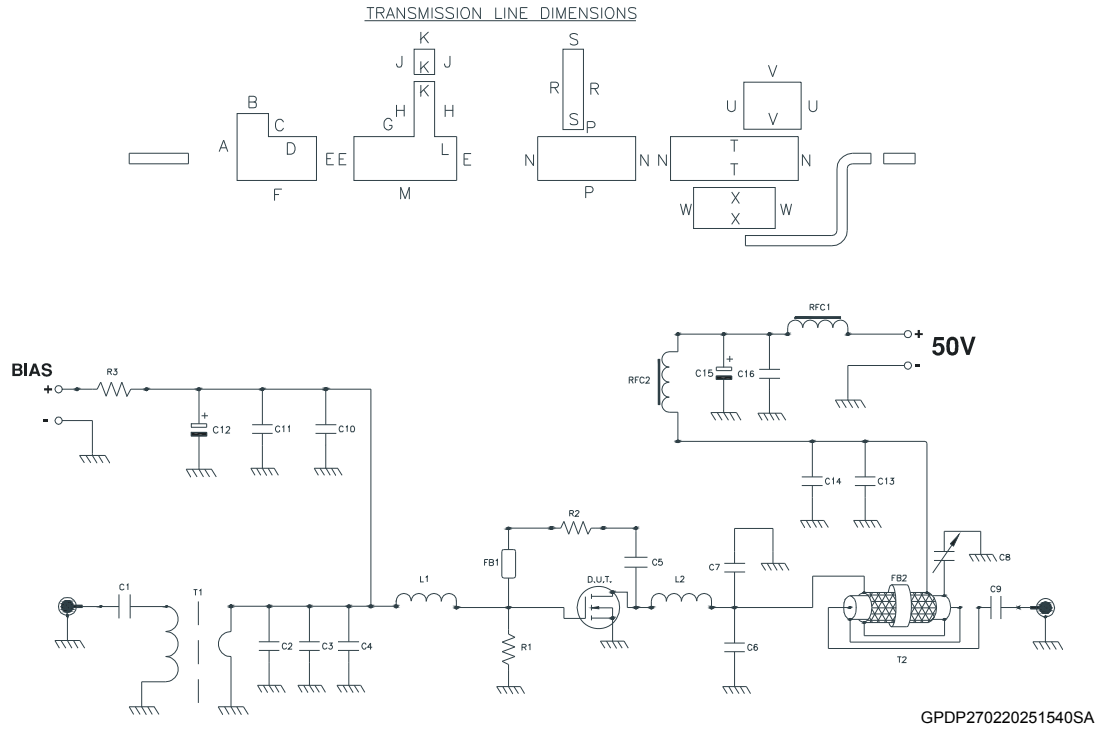


Table 7. **Component list**

Component	Description
C1, C9	0.01 mF/ 500 V surface mount ceramic chip capacitor
C2, C3	750 pF ATC 700B surface mount ceramic chip capacitor
C4	300 pF ATC 700B surface mount ceramic chip capacitor
C5, C10, C11, C14, C16	10000 pF ATC 200B surface mount ceramic chip capacitor
C6	510 pF ATC 700B surface mount ceramic chip capacitor
C7	300 pF ATC 700B surface mount ceramic chip capacitor
C8	175-680 pF type 46 standard trimmer capacitor
C12	47 mF/ 63 V aluminum electrolytic radial lead capacitor
C13	1200 pF ATC 700B surface mount ceramic chip capacitor
C15	100 mF/ 63 V aluminum electrolytic radial lead capacitor
R1, R3	1 kΩ 1 W surface mount chip resistor
R2	560 Ω 2 W wire-wound axils lead resistor
T1	HF2-30 MHz surface mount 9:1 transformer
T2	RG- 142B/U 50 Ω coaxial cable OD = 0.165[4.18] L 15”[381.00] covered with 15”[381.00] tinned copper tubular brand 13/65” [5.1] width
L1	1 3/4 turn air-wound 16 AWG ID = 0.219 [5.56] poly-coated magnet wire
L2	1 3/4 turn air-wound 12 AWG ID = 0.250 [6.34] bus bar wire
RFC1, RFC2	3 turns 14 AWG wire through fair rite toroid

Component	Description
FB1	Surface mount emi shield bead
FB2	Toroid
PCB	Ultralam 2000. 0.030” THK, εr = 2.55, 2 Oz ED CU both sides

Figure 15. 30 MHz test circuit photomaster

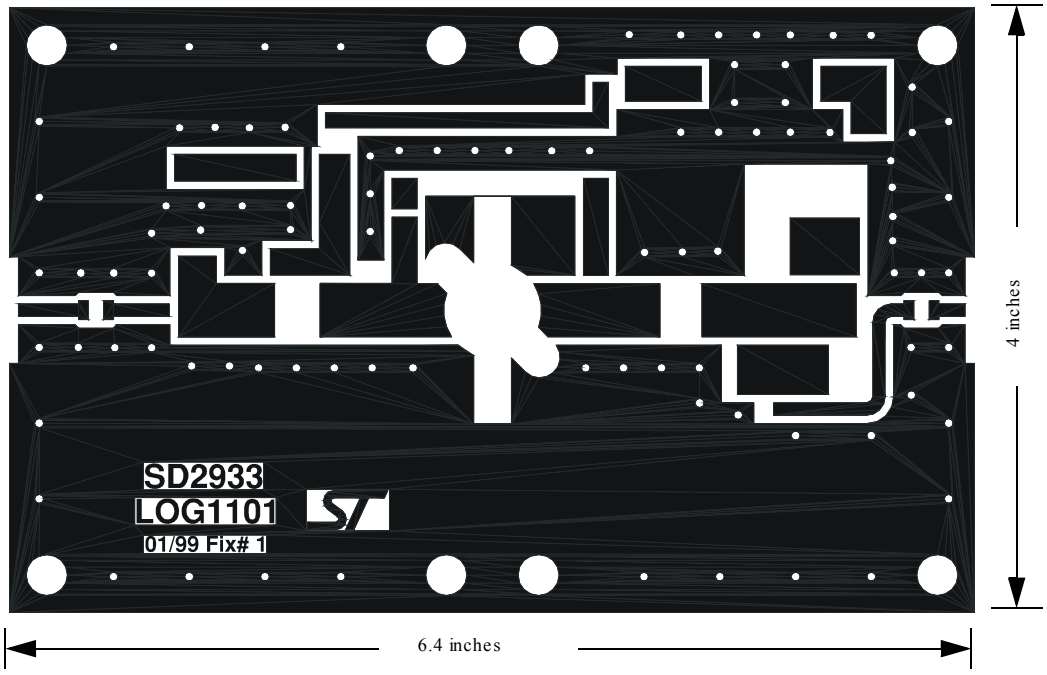
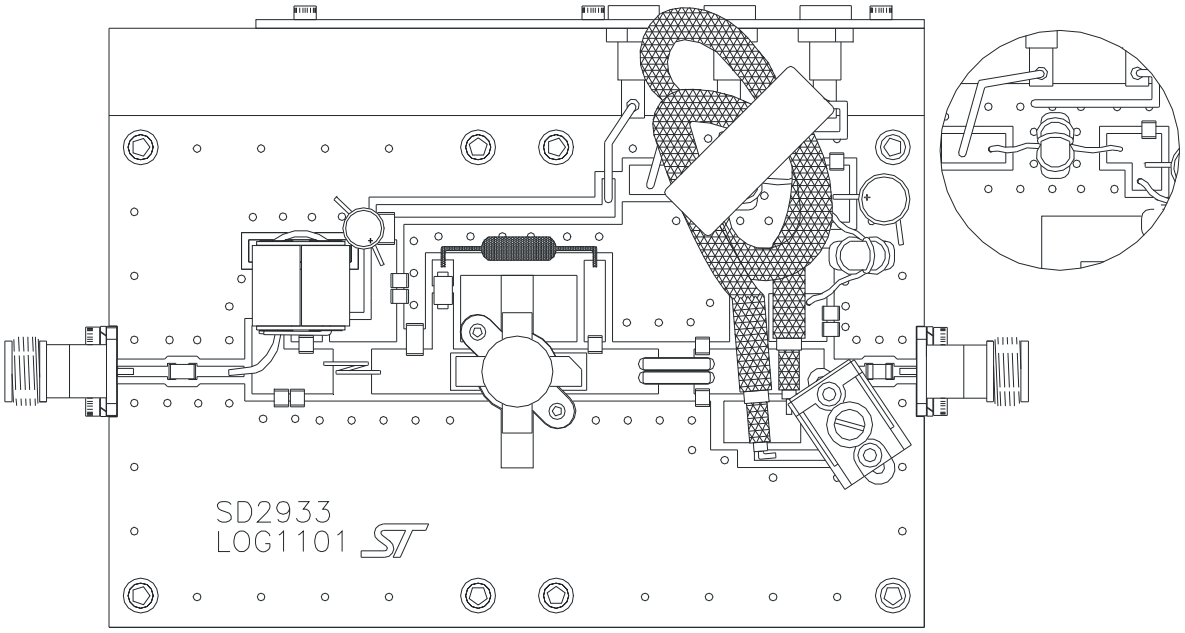


Figure 16. **30 MHz test circuit**



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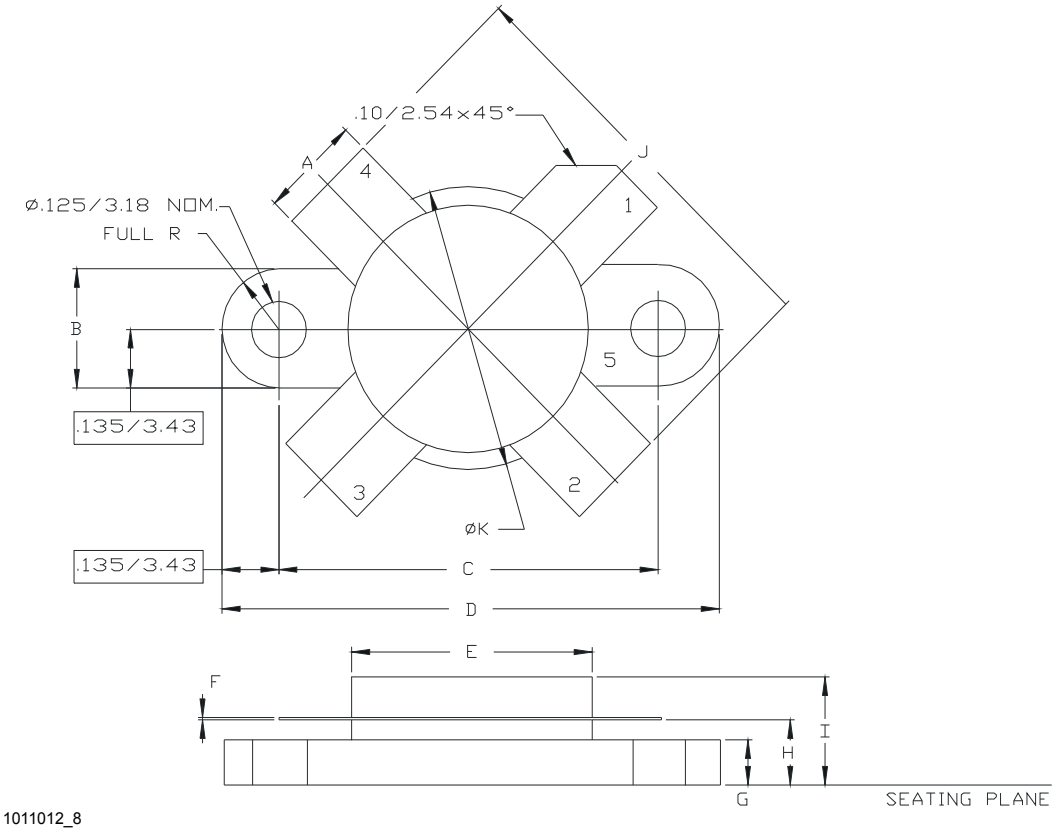
7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 M177 package information

Figure 17. M177 package outline



Note: Controlling dimensions in inches.

Table 8. **M177 package mechanical data**

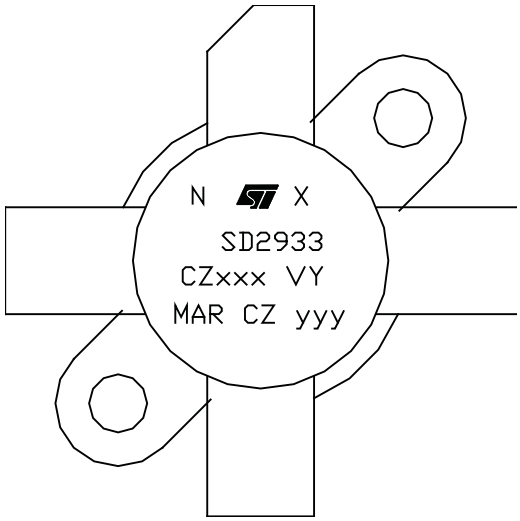
Dim.	mm		Inch	
	Min.	Max.	Min.	Max.
A	5.72	5.97	0.225	0.235
B	6.73	6.96	0.265	0.275
C	21.84	22.10	0.860	0.870
D	28.70	28.96	1.130	1.140
E	13.84	14.10	0.545	0.555
F	0.08	0.18	0.003	0.007
G	2.49	2.74	0.098	0.108
H	3.81	4.32	0.150	0.170
I		7.11		0.280
J	27.43	28.45	1.080	1.120
K	15.88	16.13	0.625	0.635

7.2 Marking, packing and shipping specifications

Table 9. Packing and shipping specifications

Order code	Packaging	Pcs per box	Dry pack humidity	V_{GS} and G_{FS} code	Lot code
SD2933-06W	Box	25	< 10 %	Not mixed	Not mixed

Figure 18. Marking layout



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Revision history

Table 10. **Document revision history**

Date	Revision	Changes
11-Mar-2025	1	First release.

Contents

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