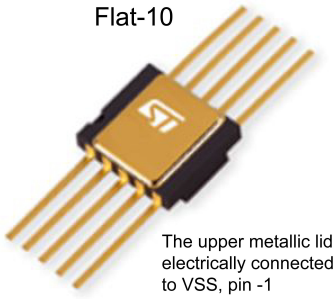
RHFOSC04

Datasheet

Rad-hard, crystal oscillator driver and divider

Flat-10



The upper metallic lid is electrically connected to VSS, pin -1

Product status link
RHFOSC04

Features

- 2.3 V to 3.6 V supply (4.8 V AMR)
- High speed:
  - Characterized from 16 MHz to 120 MHz
- CMOS output, meets JEDEC
- Divided-frequency single output
- Low power
- TTL compatible
- Enable/disable function
- Immunity to radiations:
  - 300 krad(Si) TID
  - SEL free up to 125 MeV.cm²/mg
  - SET free up to 125 MeV.cm²/mg
- SMD 5962F20207
- Mass: 0.42 g

Applications

- Oscillators for space systems

Description

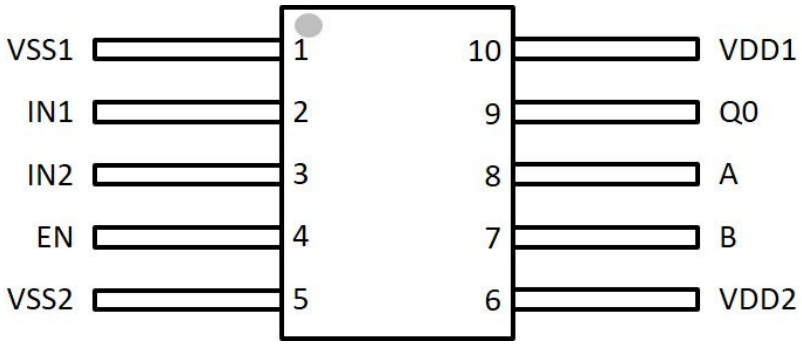
The RHFOSC04 is a crystal oscillator driver and divider. It consists of an oscillator section and 4-stage ripple-carry binary counter. The oscillator section allows the implementation of crystal oscillator circuits. The output is buffered and it is controlled by a 2-bit digital cell to deliver one among four divided frequency, from F to F/2, F/4 and F/8 frequencies. A disable function is available to set the circuit in power-down mode while keeping a high impedance output.

Designed in rad-hard rules on robust CMOS technology already proven in space, the RHFOSC04 shows an excellent stability in total-ionizing-dose (TID) up to 300 krad(Si) and it is SEL-free and SET-free up to 125 MeV.cm²/mg.

It comes in hermetic ceramic Flat-10 lead, and can operate from -55 °C to +125 °C ambient temperature.

1 General overview

Figure 1. **Pin connection**



VDD1 and VDD2 are internally connected to the die and must be externally connected to the same voltage.
VSS1 and VSS2 are internally connected to the die and must be externally connected to the same voltage.
The upper metallic lid is electrically connected to pin1 (VSS).

Figure 2. **Equivalent schematic**

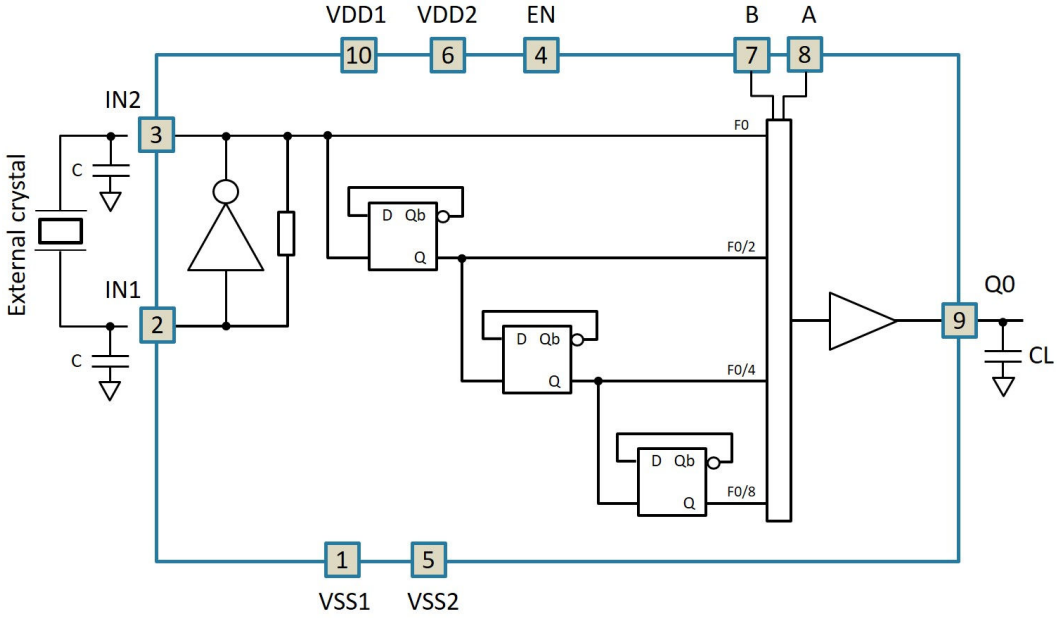


Table 1. **Truth table**

B	A	EN	Q0
0	0	1	F0
0	1	1	F0/2
1	0	1	F0/4
1	1	1	F0/8
X	X	0	High impedance

2 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 2. Absolute maximum ratings

Symbol	Parameters	Value	Units
VDD (1)	Maximum power supply between VDD and VSS	4.8	V
T_{stg}	Maximum temperature storage	-65 to +150	°C
T_j	Maximum junction temperature	+150	°C
R_{thjc}	Junction-to-case thermal resistance (Flat-10 package) (2)	22	°C/W
R_{thja}	Junction-to-ambient thermal resistance (Flat-10 package) (2)	125	°C/W
Vi	Max. voltage on any pin	-0.3 V to VDD+0.3 V	V
Ii	Max. input current at any pin	±10	mA
ESD	HBM on all pins (human body model)	2 k	V
	CDM on all pins (charged device model)	1 k	V

1. *All voltages are with respect to the network ground terminal .*
2. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on outputs.*

Table 3. Operating conditions

Symbol	Parameters	Min.	Max.	Units
VDD	Supply voltage (VDD1 and VDD2 must be connected to the same voltage)	2.3	3.6	V
VIN	Input voltage IN1 and IN2	0	VDD	V
	A, B and EN inputs	0	VDD	
T_A	Ambient temperature range	-55	+125	°C

3 Radiations

Total dose (MIL-STD-883 TM 1019):

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFOSC04 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in Table 5. DC electrical characteristics and Table 6. AC electrical characteristics apply to both pre- and post-irradiation, as follows:

- All tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID)
- The initial characterization is performed in qualification only on both biased and unbiased parts
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification

Heavy ions:

The behavior of the product, when submitted to heavy ions, is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 4. Radiations

Symbol	Characteristics	Value	Unit
TID (1)	High-dose rate (50 to 300 rad (Si) per second)	300	krad
SEL (2)	Performed at 125°C with a particle angle of 60° and a fluence of 1 x 10^7 n/cm^2 (10 millions of particles per cm²)	125	MeV.cm²/mg
	Performed at 125°C with a particle angle of 0° and a fluence of 1 x 10^7 n/cm^2 (10 millions of particles per cm²)	62	
SET (3)	Performed at 25°C	125	

1. *A total ionizing dose (TID) of 300 krad(Si) is equivalent to 3000 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latch-up.*
3. *SET: single event transient.*

4 Electrical characteristics

VDD = +2.3 V to 3.6 V, VSS = GND, enabled (EN=VDD), T_{amb} = -55 °C to +125 °C, unless otherwise specified.

Table 5. DC electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
I_{DD}	Quiescent current	IN1 and IN2 floating I_{out} = 0 (no load)		3.4	3.8	mA
I_Z	Quiescent current in disable	EN = 0 V			50	µA
I_{outZ}	Output current in disable on Q0	EN = 0 V		7	30	nA
V_{OL}	Low level output voltage on Q0	IOL = +100 µA, VDD = 2.3 V			200	mV
		IOL = +100 µA, VDD = 3.6 V			200	mV
V_{OH}	High level output voltage on Q0	IO L= +100 µA, VDD = 2.3 V	2.1			V
		IOL = +100 µA, VDD = 3.6 V	2.8			V
V_{IL}	Low level input voltage on A, B, EN inputs	VDD = 2.3 V			0.8	V
		VDD = 3.6 V			0.8	V
V_{IH}	High level input voltage on A, B, EN inputs	VDD = 2.3 V	2			V
		VDD = 3.6 V	2			V
I_{IL}	Input leakage current low on A, B, EN inputs	V_{in} = 0 V VDD= 2.3 V to 3.6 V			-0.1	µA
I_{IH}	Input leakage current high on A, B, EN inputs	V_{in} = VDD VDD = 2.3 V to 3.6 V			0.1	µA
I_{sink}	Short-circuit output current	V_{out} = VDD VDD = 2.3 V to 3.6 V		50	80	mA
I_{source}	Short-circuit output current	V_{out} = 0 V VDD = 2.3 V to 3.6 V	-80	-50		mA

VDD = +3.3 V, VSS = GND, C-load = 18 pF (see Figure 5. Phase noise, F_{clk} = 120 MHz, V_{cc} = 3.3 V), enabled (EN = VDD), Tamb = -55 °C to +125 °C, unless otherwise specified.

Table 6. AC electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
T_r	Output rise time	90%/10%, CL = 18 pF		2.2		ns
		90%/10%, CL = 2 pF		0.4		
		90%/10%, CL = 10 pF(1)	1	1.3	1.6	
T_f	Output fall time	90%/10%, CL = 18 pF		2.2		
		90%/10%, CL = 2 pF		0.4		
		90%/10%, CL = 10 pF(1)	1	1.3	1.6	
PhN	Phase noise on Q0	at 250 Hz Fclk = 16 MHz		-110		dBc /Hz
		at 170 Hz F_{clk} = 120 MHz		-100		
J_t	RMS Jitter	At 1 MHz F_{clk} = 16 MHz		4		ps
DL1	Drive level	Crystal using H1 (first harmonic), F_{clk} = 16 MHz to 25 MHz			100	µW
DL3		Crystal using H3 (third harmonic), F_{clk} = 25 MHz to 120 MHz			200	
D_{tc} (1)	Duty-cycle on Q0	F_{clk} = 16 MHz	45	50	55	%

1. *Guaranteed by design and characterization*

Figure 3. **Test circuit**

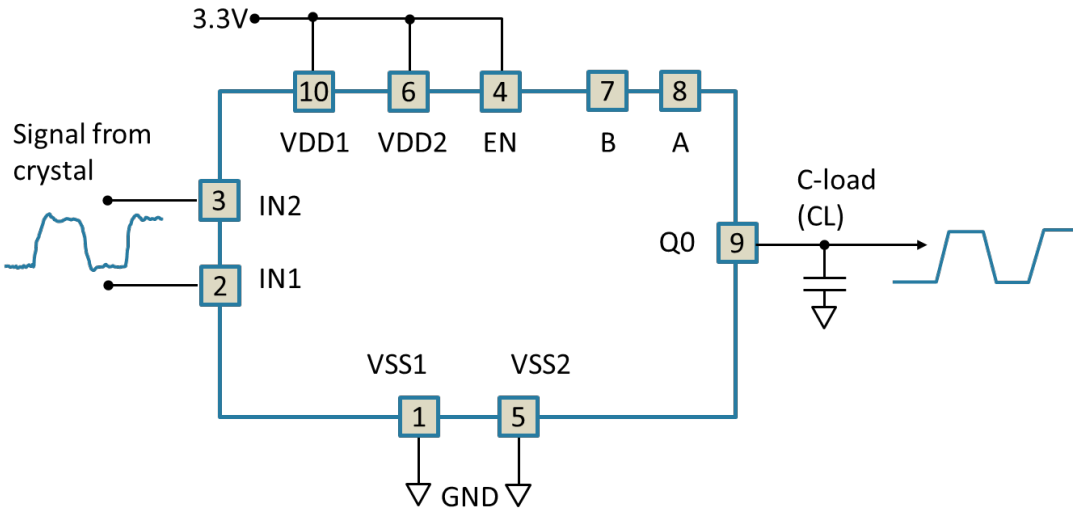
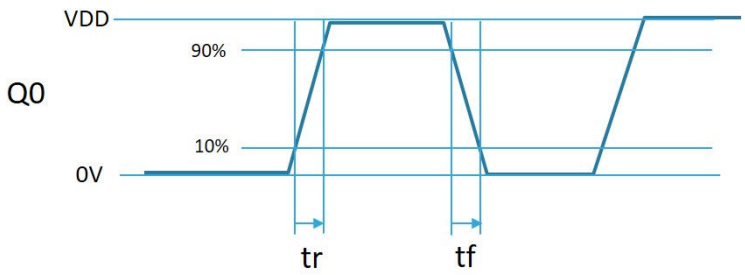


Figure 4. **Timing diagrams**



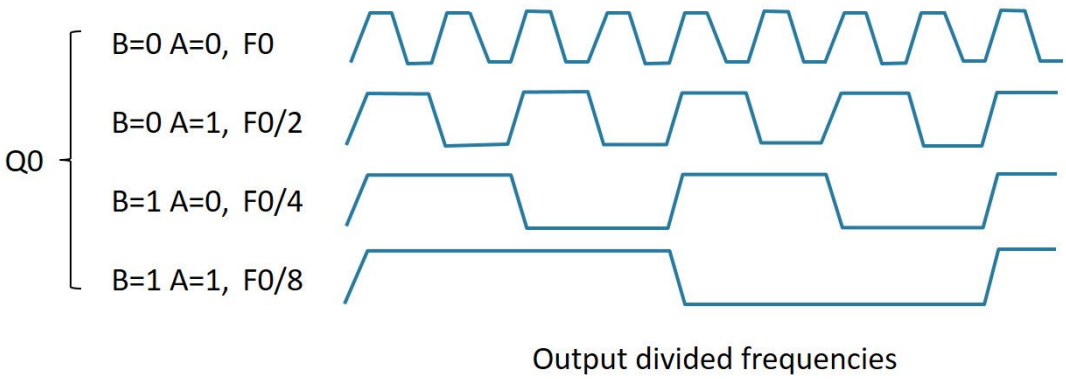


Figure 5. **Phase noise, F_{clk} = 120 MHz, V_{cc} = 3.3 V**

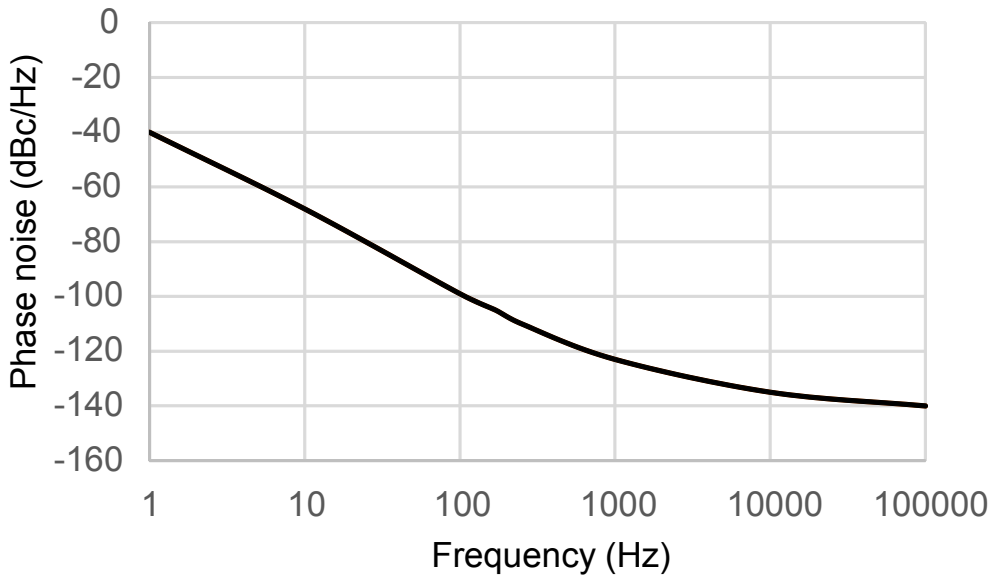


Figure 6. **Phase noise, F_{clk} = 60 MHz, V_{cc} = 3.3 V**

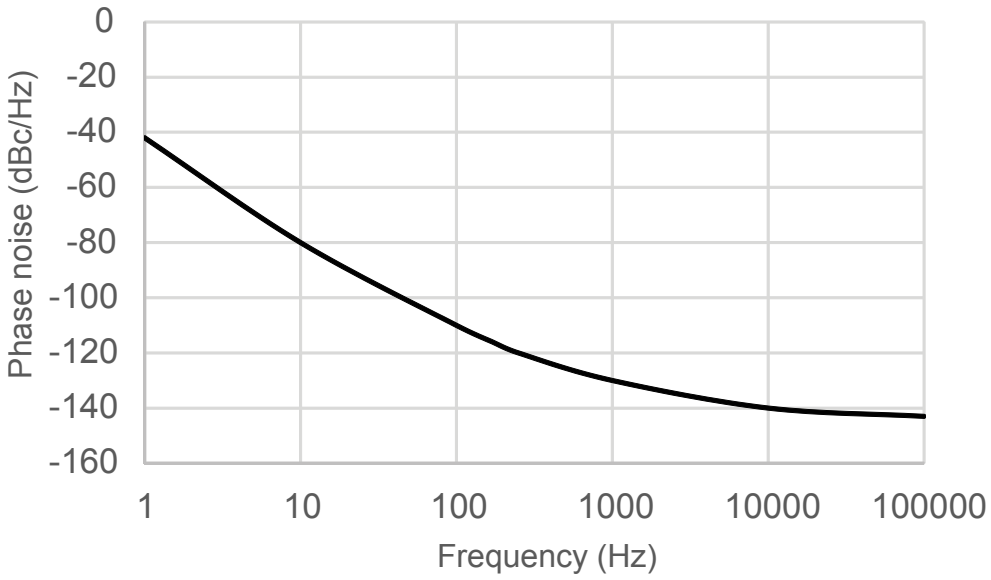


Figure 7. **Phase noise, F_{clk} = 16 MHz, V_{cc} = 3.3 V**

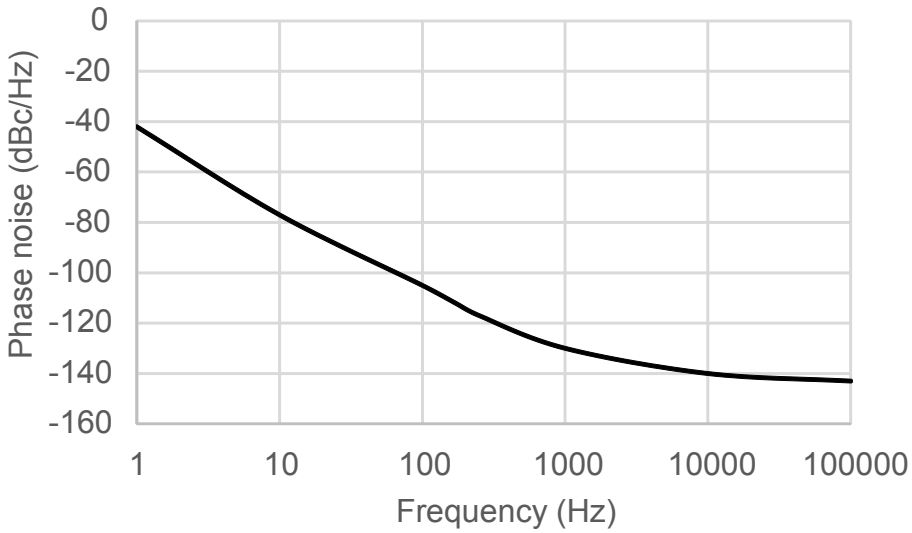
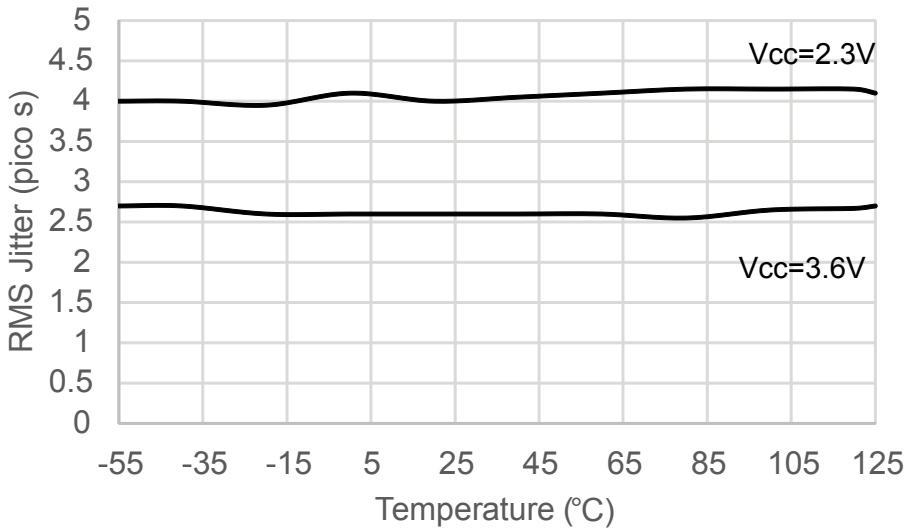


Figure 8. **RMS jitter, F_{clk} = 16 MHz**

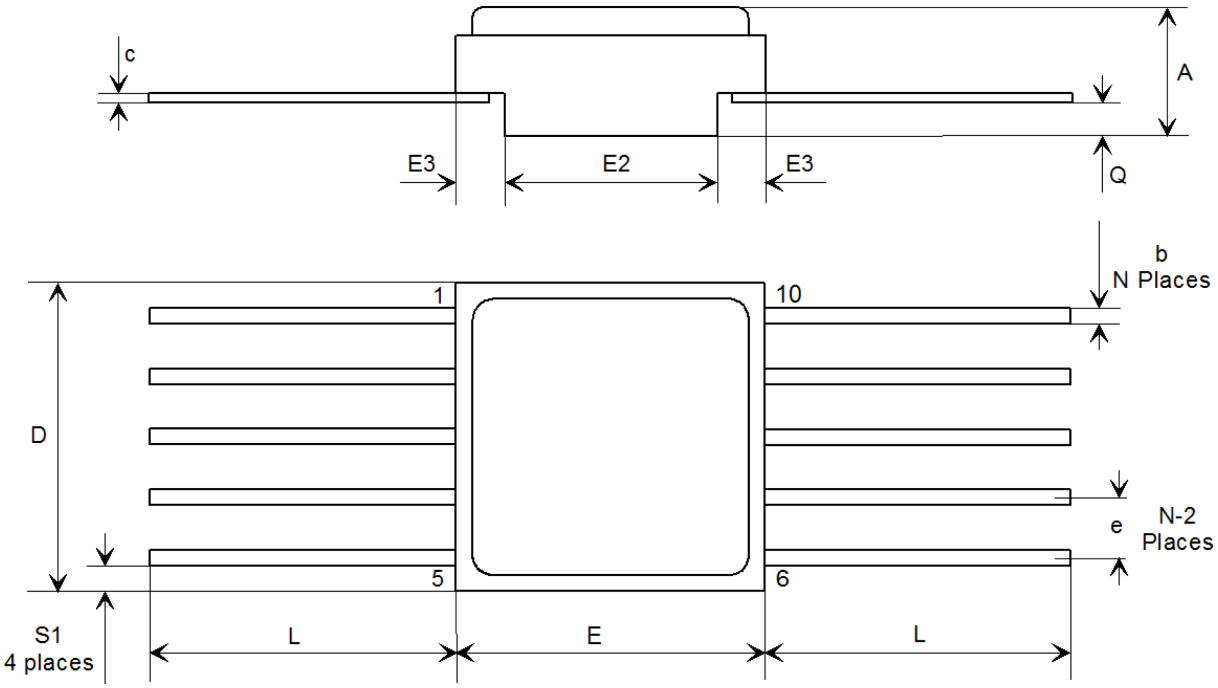


5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 Flat-10 package information

Figure 9. Flat-10 package outline



Note: The upper metallic lid is electrically connected to pin1 (VSS).

Table 7. Flat-10 mechanical data

Symbol	mm			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.26	2.44	2.62	.089	.096	.103
b	0.38	0.43	0.48	.015	.017	.019
c	0.102	0.127	0.152	.004	.005	.006
D	6.35	6.48	6.60	.250	.255	.260
E	6.35	6.48	6.60	.250	.255	.260
E2	4.32	4.45	4.58	.170	.175	.180
E3	0.88	1.01	1.14	.035	.040	.045
e		1.27			.050	
L	6.35		9.40	.250		.370
Q	0.66	0.79	0.92	.026	.031	.036
S1	0.16	0.485	0.81	.006	.019	.032
N		10			10	

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

6 Ordering information

Table 8. Ordering information

Order code	SMD	Quality level	Package	Lead finishing	Marking (1)	Packing
RH-OSC04K1	-	Engineering Model	Flat-10 (grounded lid)	Gold	RH-OSC04K1	Tray
RHFOSC04K01V	5962F20207	QML-V Flight		Gold	5962F2020701VXC	
RHFOSC04K02V	5962F20207	QML-V Flight		Solder Dip	5962F2020701VXA	

1. *Specific marking only. Complete marking includes the following:*
   - *ST logo*
   - *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
   - *Country of origin (FR = France)*

Note: Contact your ST sales office for information regarding the specific conditions for products in die form.

7 Other information

7.1 Date code

The date code (date the package was sealed) is structured as follows:

- Engineering model: 3yywwz
- Flight model: yywwz

Where:

yy = last two digits of the year, ww = week digits, z = lot index of the week

7.2 Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 9. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including: • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Reference to ST datasheet • Reference to TN1181 on engineering models • ST Rennes assembly lot ID
QML-V Flight	Certificate of Conformance including: • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Serial numbers • Group C reference • Group D reference • Reference to applicable SMD • ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 10. **Document revision history**

Date	Version	Changes
13-May-2020	1	Initial release.
13-Apr-2026	2	Changed packing from Conductive strip pack to Tray in Table 8.

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