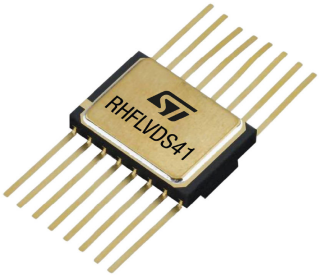
RHFLVDS41

Datasheet

Rad-hard 2.5 V quad LVDS driver



Flat-16 hermetic ceramic
(with metallic lid electrically connected to ground)

Maturity status link
RHFLVDS41

Features

- 600 Mbps typical (300 MHz)
- 2.3 V to 3.6 V power supply
- LVCMOS inputs conform to JESD80 (2.5) and JESD64-A (2.5/3.3)
- 4.8 V absolute rating
- Compliant with TIA/EIA-644 LVDS standard (point-to-point)
- 8 kV HBM on LVDS output pins
- Flow-through pinout for reduced crosstalk
- Enable/disable function with high-impedance pull-up, pull-down
- Fail-safe function on all I/Os
- Cold Spare
- LVDS output voltage: 350 mV on 100 Ω load
- Hermetic package
- Guaranteed up to 300 krad TID
- SEL immune up to 125 MeV.cm²/mg
- SET/SEU immune up to 62.5 MeV.cm²/mg
- SMD pin: 5962F25205
- Mass: 0.65 g

Applications

- High data rate communication in satellites

Description

The RHFLVDS41 is a quad, low-voltage, differential signaling (LVDS) driver specifically designed, packaged, and qualified for use in aerospace environments in a low-power and fast point-to-point baseband data transmission standard.

Operating from a 2.3 V to 3.6 V power supply, the RHFLVDS41 operates over an 100 Ω transmission media that may be printed circuit board traces, backplanes, or cables.

Designed on ST's proprietary CMOS process with specific mitigation techniques, the RHFLVDS41 achieves “best-in-class” for hardness to total ionizing dose and heavy ions.

The RHFLVDS41 can operate over -55 °C to +125 °C and it is housed in a hermetic Ceramic Flat-16 package with metallic lid electrically connected to ground.

1 Functional description

Figure 1. **Logic diagram and logic symbol (flow through pinout)**

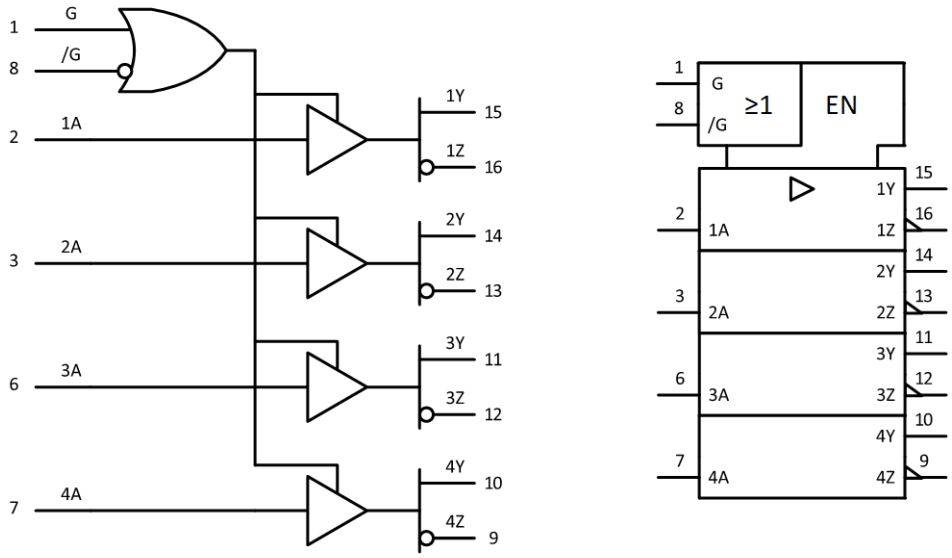


Table 1. **Truth table**

Inputs	Enables		Outputs	
nA	G	/G	nY	nZ
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
OPEN	H	X	L	H
OPEN	X	L	L	H

Note:

1. *The G input features an internal pull-up network. The /G input features an internal pull-down network. If they are floating, the circuit is enabled.*
2. *L = low level, H = high Level, X = whatever the level, Z = high impedance.*
3. *"OPEN" input: thanks to fail-safe function, nZ is forced to high level, nY is forced to low level, whatever G and /G.*

2 Pin connections

Figure 2. **Pin connections (top view). Flow-through pinout.**

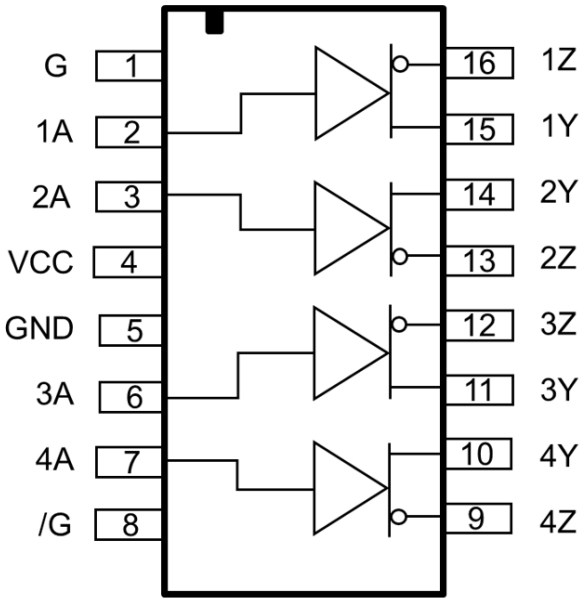


Table 2. **Pin description**

Pin number	Symbol	Name and function
2, 3, 6, 7	1A to 4A	LVCMOS inputs
15, 14, 11, 10	1Y to 4Y	LVDS outputs
16, 13, 12, 9	1Z to 4Z	
1	G	Enable
8	/G	Disable
5	GND	Ground (internally connected to the metallic lid)
4	VCC	Supply voltage

3 Maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC (1)	Maximum power supply between VCC and GND	4.8	V
VIN	LVCMOS inputs (nA, G, /G)	-0.3 to 4.8	
VOUT	LVDS outputs (nY, nZ)	-0.3 to 4.8	
Tstg	Storage temperature range	-65 to +150	°C
Tj (2)	Maximum junction temperature	150	
Rth (3)	Junction to ambient thermal resistance (Rthja)	80	°C/W
	Junction to case thermal resistance (Rthjc)	22	
ESD	HBM (human body model) on all pins, pin to pin (protections are GGMOS type, snapback behavior)	2 k	V
	HBM on LVDS outputs, versus GND (protections are SCR (silicon control rectifier) type, snapback behavior)	8 k	
	CDM: charge device model	500	

1. *All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.*
2. *Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions as per the method 5004 of MIL-STD-883.*
3. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply voltage vs. GND	2.3	3.6	V
VIN	Input voltage on LVCMOS inputs (nA, G, /G)	0	3.6 (whatever VCC)	V
Ta	Ambient temperature range	-55	+125	°C

4 Radiations

Total dose

The RHFLVDS41 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, in high-dose rate only (full CMOS technology), between 50 and 300 rad/s.

All parameters provided in Table 6 apply to both pre- and post-irradiation, as follows:

- All tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high-dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy ions:

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 5. Radiations

Symbol	Characteristics		Value	Unit
TID (1)	High-dose rate (50 to 300 rad (Si)/s)		300	krad
SEL (2)(3)	Temperature: 125 °C Fluence: 1 x 10 ions/cm² V_{CC} = 3.6 V (max. operating)	For a particle angle of 60°, no SEL observed at :	125	MeV.cm²/mg
		For a particle angle of 0°, no SEL observed at :	62.5	
SET/SEU (3)(4)	Particle angle: 0° Temperature: 25 °C Fluence: 1 x 10^7 ions/cm² V_{CC} = 2.3 V (min. operating)	No SET/SEU observed at:	62.5	

1. *A total ionizing dose (TID) of 300 krad(Si) is equivalent to 3000 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latch-up.*
3. *Fluence: number of ions on a specified area (cm²). 1x10^7 ions/cm² is equivalent to 10 million particles per cm².*
4. *SET, SEU: single event transient, single event upset.*

5 Electrical characteristics

5.1 2.5 V power supply domain

V_{CC} = 2.3 V to 2.7 V, typical values are at ambient Ta = +25 °C, min. and max. values are at Ta = -55 °C and +125 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Total enabled supply current, not switching	V_{IN} = 0 V or V_{CC}, load = 100 Ω on all channels		16	18.5	mA
I_{CCZ}	Total disabled supply current, drivers loaded or not loaded	V_{IN} = 0 V or V_{CC} G = GND, /G = V_{CC}		2.5	3	mA
V_{IH}	Input voltage high on nA, G, and /G		1.7			V
V_{IL}	Input voltage low on nA, G, and /G				0.8	V
I_{IH}	High level input current on nA, G, and /G	V_{CC} = 2.7 V, V_{IN} = 3.6 V	-10		10	µA
I_{IL}	Low level input current on nA, G, and /G	V_{CC} = 2.7 V, V_{IN} = 0	-10		10	
I_{OFF} (1)	Power-off leakage current on nA, G, and /G	V_{CC} = 0 V, V_{IN} = 2.3 V to 2.7 V	-10		10	
	LVDS outputs power-off leakage current	V_{CC} = 0 V, V_{OUT} = 2.3 V to 2.7 V	-60		60	
V_{OH}	LVDS output voltage high	R_L = 100 Ω ± 1%		1.425	1.6	V
V_{OL}	LVDS output voltage low		0.9	1.075		V
V_{OD}	Differential output voltage		250		380	mV
DV_{OD}	Change of magnitude of VOD1 for complementary output states				25	mV
V_{OS}	Offset voltage		1.125	1.25	1.375	V
DV_{OS}	Change of magnitude of V_{OS} for complementary output states				25	mV
I_{OS}	Output short-circuit current to supplies	V_{CC} = 2.7 V, V_{IN} = GND and $V_{out(-)}$ = 0 V, or V_{IN} = V_{CC} and $V_{out(+)}$ = 0 V	-9			mA
I_{OZ}	High impedance output current (disabled driver)	V_{OUT} = 2.7 V or GND	-50		50	µA
C_{IN}	Input capacitance			2.5		pF
T_{PHLD}	Propagation delay time, high to low output	R_L = 100 Ω ± 1%, C_L = 10 pF (see Figure 14)	1		2.5	ns
T_{PLHD}	Propagation delay time, low to high output		1		2.5	ns
Tr (2)	Differential output signal rise time 20%-80% (see Figure 12)	R_L = 100 Ω and prob (see Figure 13)	300		930	ps
		R_L = 100 Ω, C_L = 10 pF (see Figure 14)	400		1030	
Tf (2)	Differential output signal fall time 80%-20% (see Figure 12)	R_L = 100 Ω and prob (see Figure 13)	300		930	ps
		R_L = 100 Ω, C_L = 10 pF (see Figure 14)	400		1030	
Freq	Operating frequency	R_L = 100 Ω and prob (see Figure 13)		250		MHz
T_{SK1} (3)	Channel-to-channel skew	R_L = 100 Ω, C_L = 10 pF (see Figure 14)			400	ps

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
T_{SK2} (4)(2)	Chip-to-chip skew	R_L = 100 Ω, C_L = 10 pF (see Figure 14)			450	ps
T_{SKD} (5)	Differential skew (T_{PHLD} - T_{PLHD})				350	
T_{PHZ}	Propagation delay time, high level to high impedance output	Load and timings: refer to Figure 15			4.5	ns
T_{PLZ}	Propagation delay time, low level to high impedance output				4.5	
T_{PZH}	Propagation delay time, high impedance to high level output				4.5	
T_{PZL}	Propagation delay time, high impedance to low level output				4.5	
Cpd (6)	Power dissipation capacitance	F_{in} = 100 MHz		45		pF

1. *All pins except pin under test and V_{CC} are floating.*
2. *Guaranteed by design and characterization.*
3. *TSK1 is the maximum delay time difference between all outputs of the same device (measured with all inputs connected together).*
4. *TSK2 is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.*
5. *TSKD is the maximum delay time difference between T_{PHLD} and T_{PLHD}.*
6. *Cpd is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per circuit).*

5.2 3.3 V power supply domain

V_{CC} = 3 V to 3.6 V, typical values are at ambient Ta = +25 °C, min. and max. values are at Ta = -55 °C and +125 °C, unless otherwise specified.

Table 7. Electrical characteristics

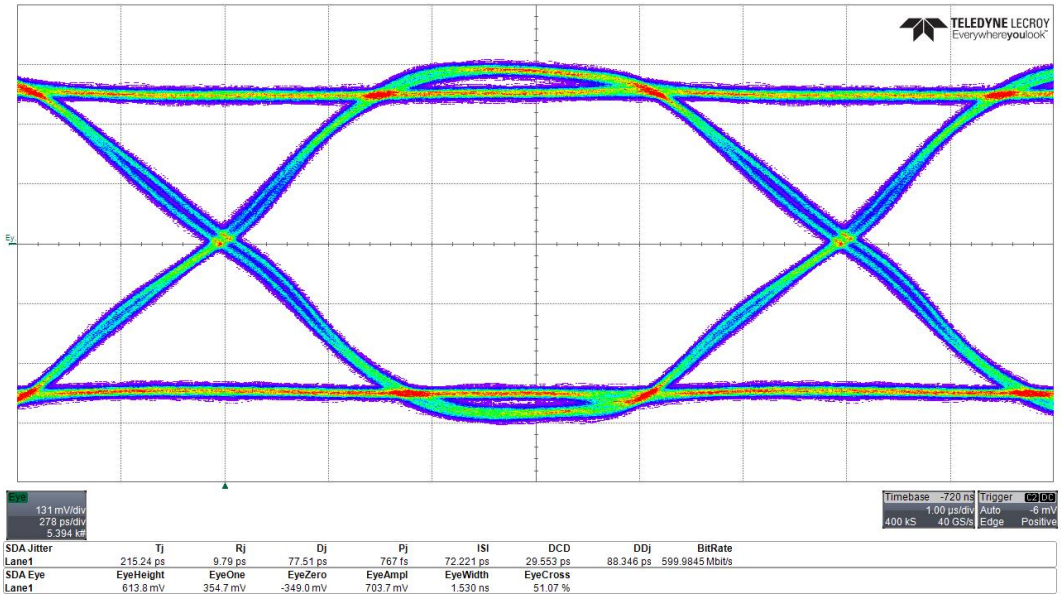
Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Total enabled supply current, not switching	V_{IN} = 0 V or V_{CC}, load = 100 Ω on all channels		17	20	mA
I_{CCZ}	Total disabled supply current, drivers loaded or not loaded	V_{IN} = 0 V or V_{CC} G = GND, /G = V_{CC}			3.5	mA
V_{IH}	Input voltage high on nA, G, and /G		2		V_{CC}	V
V_{IL}	Input voltage low on nA, G, and /G		GND		0.8	V
I_{IH}	High level input current on nA, G, and /G	V_{CC} = 3.6 V, V_{IN} = 3.6 V	-10		10	µA
I_{IL}	Low level input current on nA, G, and /G	V_{CC} = 3.6 V, V_{IN} = 0	-10		10	
I_{OFF} (1)	Power-off leakage current on nA, G, and /G	V_{CC} = 0 V, V_{IN} = 3 V to 3.6 V	-10		10	
	LVDS outputs power-off leakage current	V_{CC} = 0 V, V_{OUT} = 3 V to 3.6 V	-60		60	
V_{OH}	LVDS output voltage high	R_L = 100 Ω ± 1%		1.425	1.65	V
V_{OL}	LVDS output voltage low		0.925	1.075		V
V_{OD}	Differential output voltage		250		380	mV
DV_{OD}	Change of magnitude of VOD1 for complementary output states				25	mV
V_{OS}	Offset voltage		1.125	1.250	1.375	V

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
DV_{OS}	Change of magnitude of V_{OS} for complementary output states	R_L = 100 Ω ± 1%			25	mV
I_{OS}	Output short-circuit current to supplies	V_{CC} = 3.6 V, V_{IN} = GND and $V_{out(-)}$ = 0 V, or V_{IN} = V_{CC} and $V_{out(+)}$ = 0 V	-9			mA
I_{OZ}	High impedance output current (disabled driver)	V_{OUT} = 3.6 V or GND	-50		50	µA
C_{IN}	Input capacitance			2.5		pF
T_{PHLD}	Propagation delay time, high to low output	R_L = 100 Ω ± 1%, C_L = 10 pF (see Figure 14)	0.8		2	ns
T_{PLHD}	Propagation delay time, low to high output		0.8		2	ns
Tr (2)	Differential output signal rise time 20%-80% (see Figure 12)	R_L = 100 Ω and prob (see Figure 13)	300		600	ps
		R_L = 100 Ω, C_L = 10 pF (see Figure 14)	400		700	
Tf (2)	Differential output signal fall time 80%-20% (see Figure 12)	R_L = 100 Ω and prob (see Figure 13)	300		600	ps
		R_L = 100 Ω, C_L = 10 pF (see Figure 14)	400		700	
Freq	Operating frequency	R_L = 100 Ω and prob (see Figure 13)		300		MHz
T_{SK1} (3)	Channel-to-channel skew	R_L = 100 Ω, C_L = 10 pF (see Figure 14)			280	ps
T_{SK2} (2)(4)	Chip-to-chip skew				300	
T_{SKD} (5)	Differential skew (T_{PHLD} - T_{PLHD})				300	
T_{PHZ}	Propagation delay time, high level to high impedance output	Load and timings: refer to Figure 15			3.5	ns
T_{PLZ}	Propagation delay time, low level to high impedance output				3.5	
T_{PZH}	Propagation delay time, high impedance to high level output				3.5	
T_{PZL}	Propagation delay time, high impedance to low level output				3.5	
Cpd (6)	Power dissipation capacitance	F_{in} = 100 MHz		40		pF

1. *All pins except pin under test and V_{CC} are floating.*
2. *Guaranteed by design and characterization.*
3. *TSK1 is the maximum delay time difference between all outputs of the same device (measured with all inputs connected together).*
4. *TSK2 is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.*
5. *TSKD is the maximum delay time difference between T_{PHLD} and T_{PLHD}.*
6. *Cpd is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per circuit).*

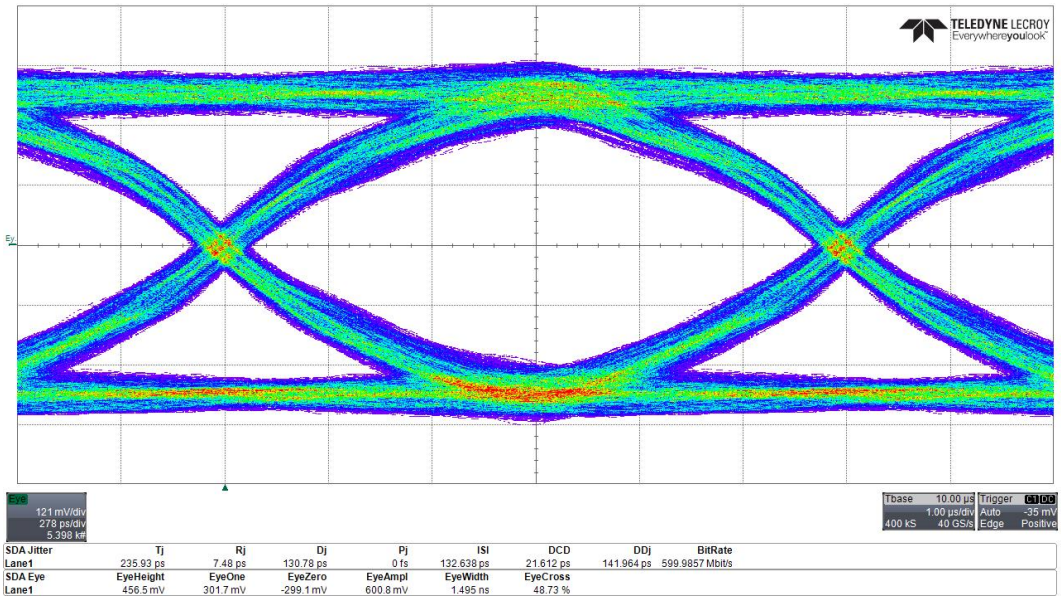
5.3 Typical performance characteristics

Figure 3. **Eye-diagram, 250 MHz, 2.5 V, 6 cm track and 100 Ω load**



SDA Jitter	Tj	Rj	Dj	Pj	ISI	DCD	DDj	BitRate
Lane1	215.24 ps	9.79 ps	77.51 ps	767 fs	72.221 ps	29.553 ps	88.346 ps	599.9845 Mbit/s
SDA Eye	**EyeHeight**	**EyeOne**	**EyeZero**	**EyeAmpl**	**EyeWidth**	**EyeCross**		
Lane1	613.8 mV	354.7 mV	-349.0 mV	703.7 mV	1.530 ns	51.07 %		

Figure 4. **Eye-diagram, 250 MHz, 2.5 V, 200 cm track and 100 Ω load**



SDA Jitter	Tj	Rj	Dj	Pj	ISI	DCD	DDj	BitRate
Lane1	235.93 ps	7.48 ps	130.78 ps	0 fs	132.638 ps	21.612 ps	141.964 ps	599.9857 Mbit/s
SDA Eye	**EyeHeight**	**EyeOne**	**EyeZero**	**EyeAmpl**	**EyeWidth**	**EyeCross**		
Lane1	456.5 mV	301.7 mV	-299.1 mV	600.8 mV	1.495 ns	48.73 %		

Figure 5. **Eye-diagram, 300 MHz, 3.3 V, 6 cm track and 100 Ω load**

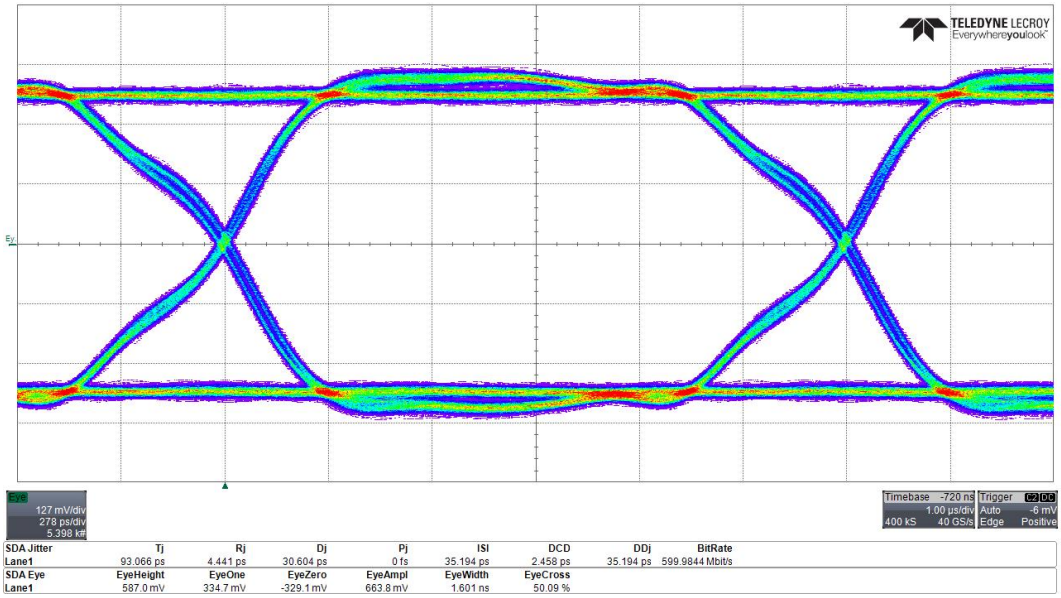


Figure 6. **Eye-diagram, 300 MHz, 3.3 V, 200 cm track and 100 Ω load**

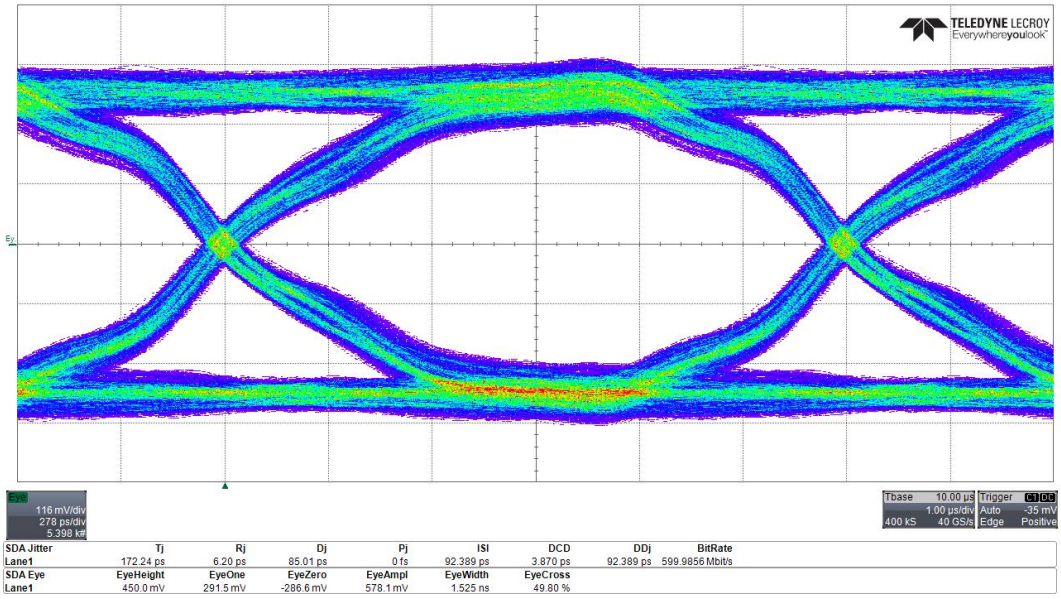


Figure 7. Jitter vs. V_{CC}

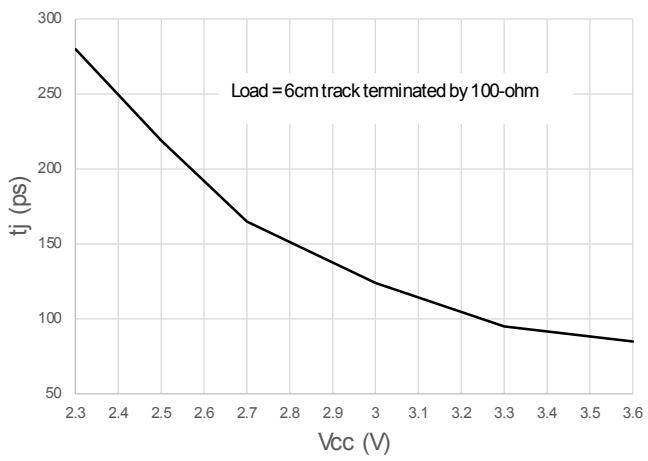


Figure 8. Output Rise/fall time vs. temperature

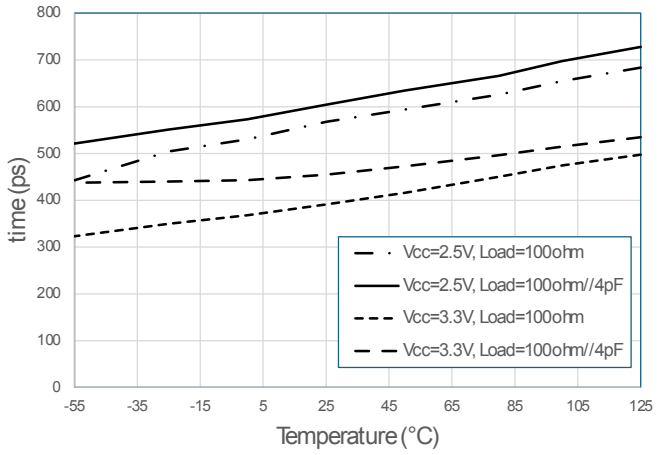


Figure 9. C_{pd} vs. temperature

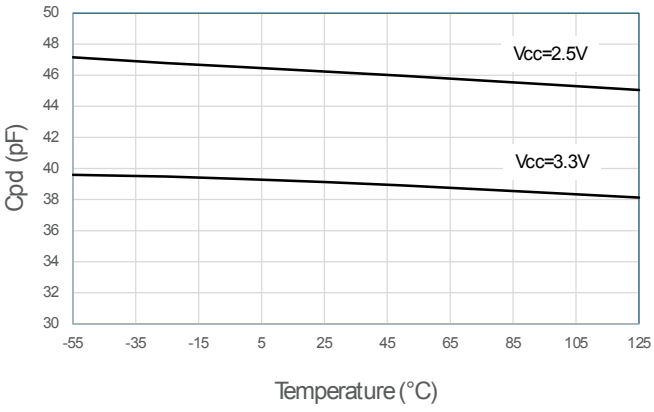
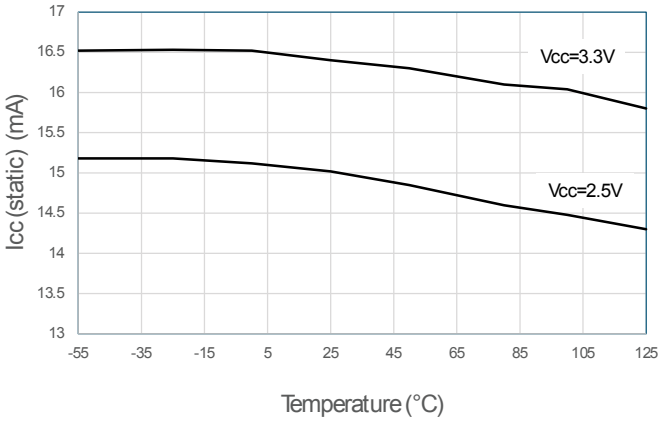


Figure 10. I_{CC} vs. temperature



6 Wave form and test circuit

Figure 11. **Voltage and current definition**

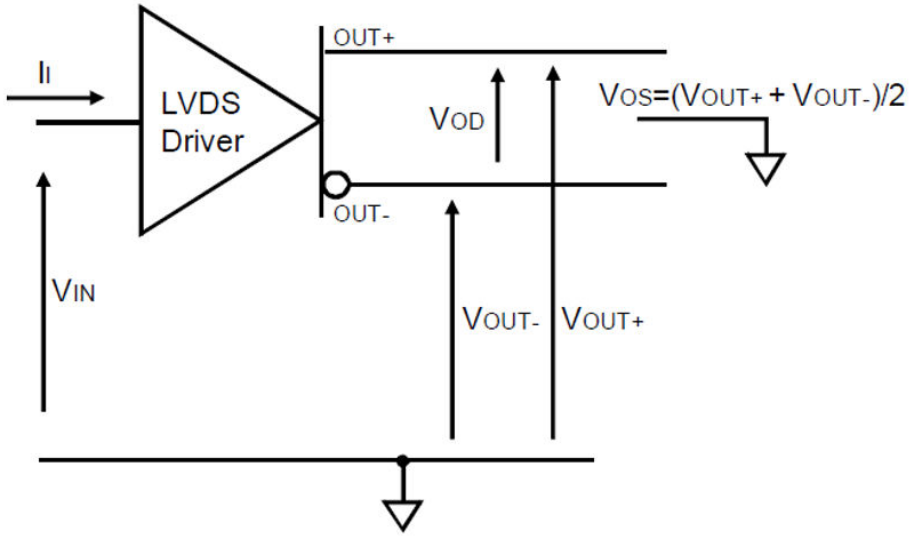
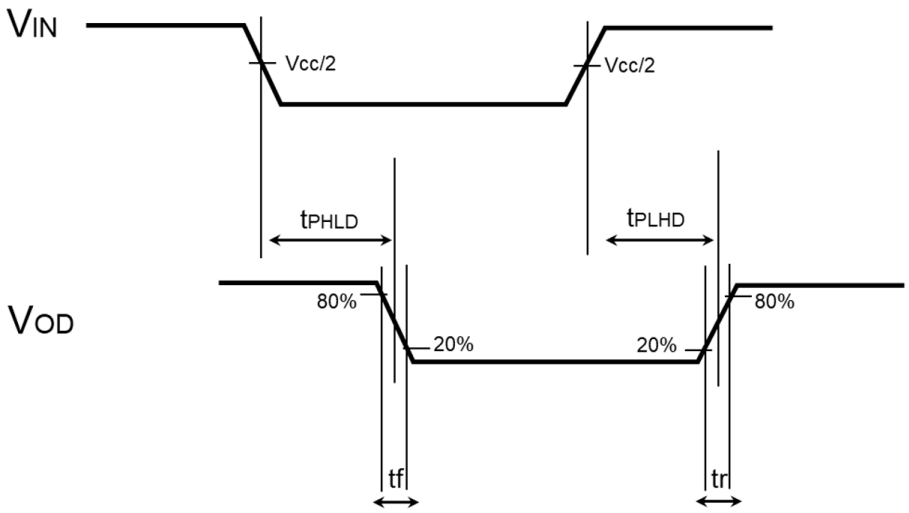


Figure 12. **Timing definitions for differential output signal**



- All input pulses are supplied by a generator with the following characteristics: Tr or Tf ≤ 1 ns, f = 1 MHz, Z_O = 50 Ω, and duty cycle = 50%.

Figure 13. **Output load A**

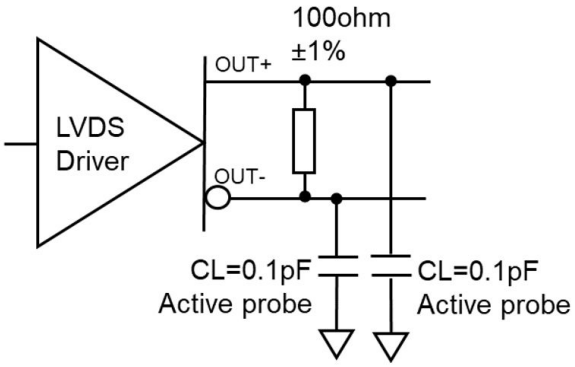


Figure 14. **Output load B**

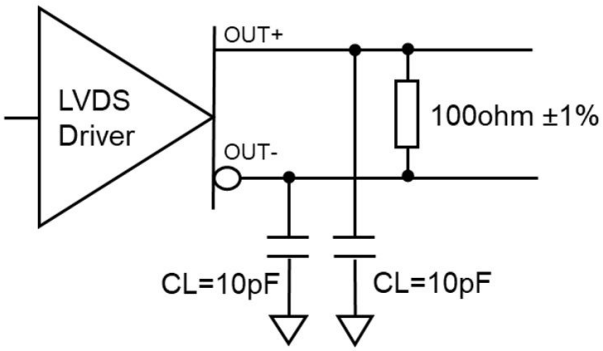
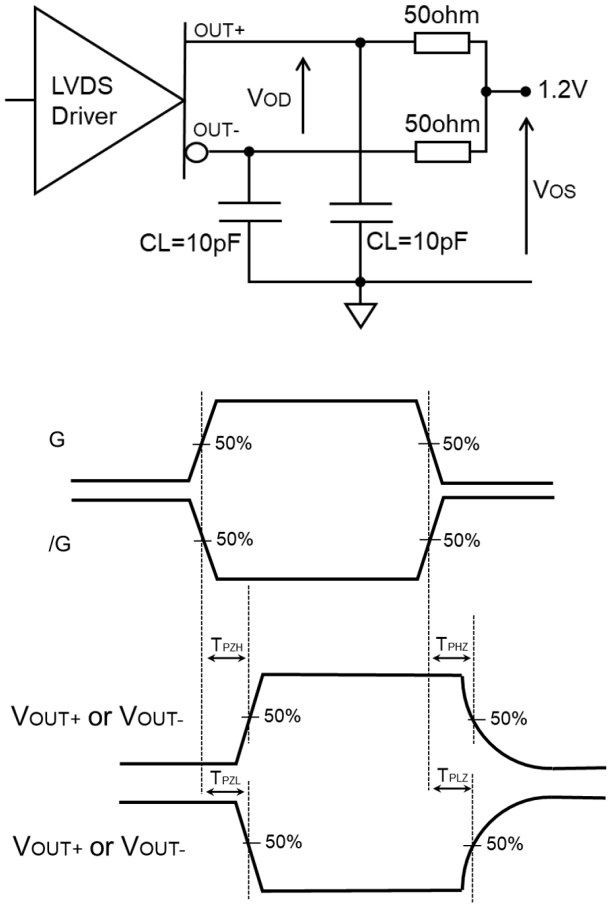


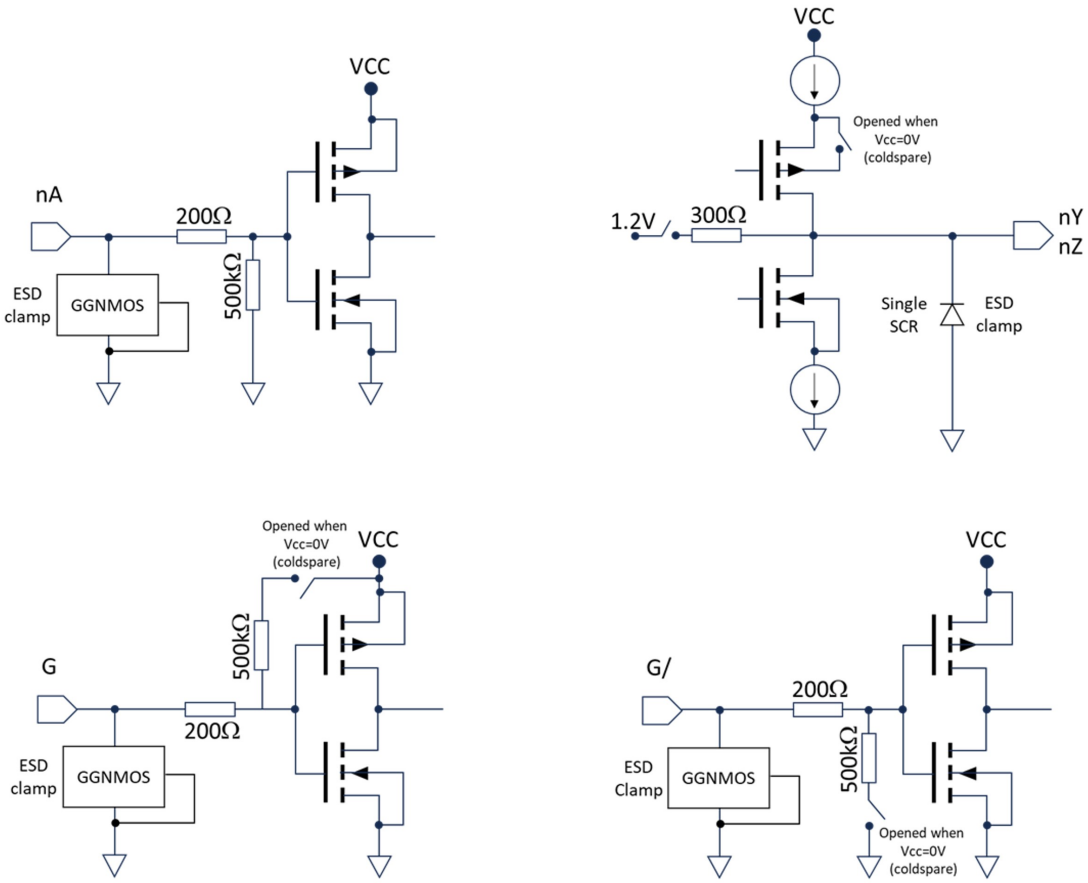
Figure 15. Enable and disable waveform



- All input pulses are supplied by a generator with the following characteristics: Tr or Tf ≤ 1 ns, frequency on G and /G = 500 kHz, and pulse width on G and /G = 500 ns.

7 I/Os specifications

Figure 16. **I/Os equivalent circuit diagram**



7.1 Cold spare

The RHFLVDS41 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (V_{CC} = GND) without affecting the bus signals or without injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and V_{CC}. ESD protection is ensured through a non-conventional dedicated structure.

7.2 Fail-safe

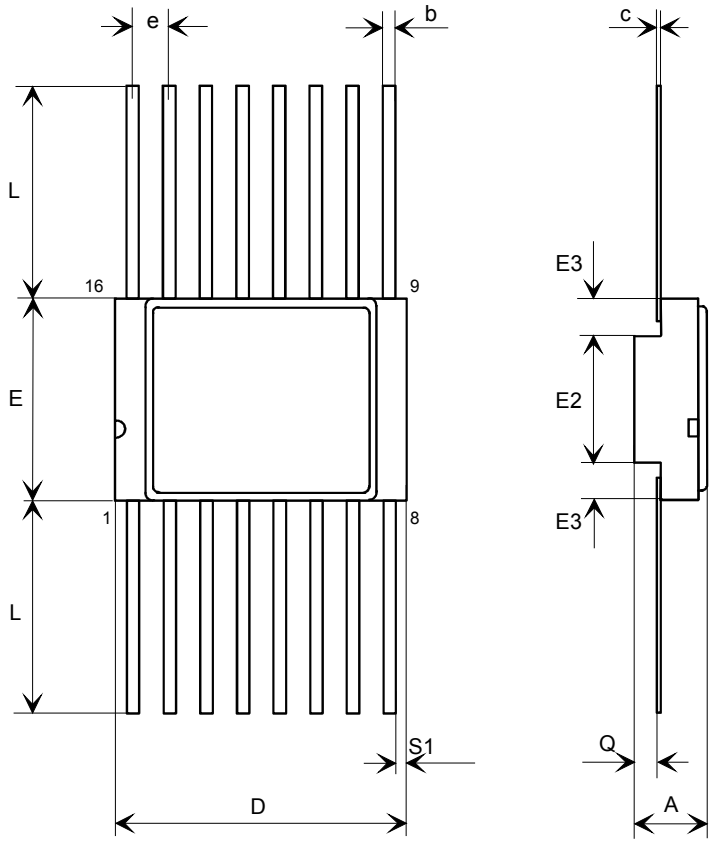
In many applications, inputs need a fail-safe function to avoid the propagation of an uncertain output state when the inputs are not connected properly. Thanks to its fail-safe function, the RHFLVDS41 forces the outputs into a stable and known logic-high state (1Y, 2Y, 3Y, 4Y to low level, 1Z, 2Z, 3Z, 4Z to high level) when the LVCMOS inputs (1A, 2A, 3A, 4A) are floating (opened). See Table 1. Truth table.

8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 Flat-16 package information

Figure 17. **Flat-16 package outline**



Note: The metallic lid is electrically connected to ground.

Table 8. **Flat-16 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.31		2.72
b	0.38		0.48
c	0.10		0.18
D	9.75		10.13
E	6.75		7.06
E3	0.76		
e		1.27	
L	6.35		7.36
Q	0.66		1.14
S1	0.13		

9 Ordering information

Table 9. Order codes

Order code	SMD [1]	Quality level	Mass	Package	Lead-finish	Marking	Packing
RH-LVDS41K1	-	Engineering model	0.65 g	Flat-16 (grounded-lid)	Gold	RH-LVDS41K1	Conductive Strip pack
RHFLVDS41K01V	5962F25205	QML-V Flight				5962F2520501VXC	
RHFLVDS41K02V					Solder Dip	5962F2520501VXA	

1. *Standard microcircuit drawing.*
2. *Specific marking only. Complete marking includes the following:*
   - *ST logo*
   - *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
   - *Country of origin (FR = France)*

Note: Contact your ST sales office for information about the specific conditions for products in die form.

10 Shipping information

Date code

The date code is structured as follows:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Engineering model: EM xyywwz

QML flight model: FM yywwz

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in Table 10 below.

The Certificate of Conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the Certificate of Conformance, is provided on a CDROM.

Note: Contact ST for details on the documentation of other quality levels.

Table 10. Product documentation

Quality level	Item
Engineering model	Certificate of Conformance including: • Customer name • Customer purchase order number • ST sales order number & item • ST part number • Quantity delivered • Date code • Reference to ST datasheet • Reference to TN1181 on Engineering Models • ST Rennes assembly lot ID
QML-V flight	Certificate of Conformance including: • Customer name • Customer purchase order number • ST sales order number & item • ST part number • Quantity delivered • Date code • Serial numbers • Group C reference • Group D reference • Reference to the applicable SMD • ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND test (1)
	SEM inspection report (2)
	X-ray plates

1. *PIND : Particle Impact Noise Detection.*
2. *SEM : Scanning Electronic Microscope.*

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
17-Dec-2024	1	Initial release.
16-May-2025	2	Updated description on the cover page, IOS1 test conditions in Table 6, Table 7, Figure 8 and Table 9. Order codes.
05-Aug-2025	3	Updated figure and features on the cover page, I_{IH}, I_{IL} and I_{OFF} test conditions in Table 6 and Table 7. Added new Section 5.3: Typical performance characteristics.

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