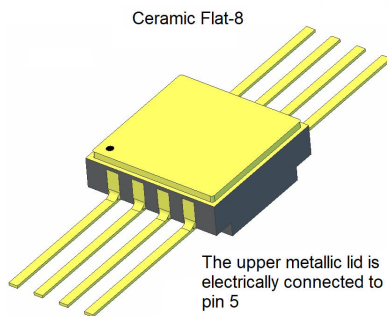


## Rad-hard 400 $\mu$ A high-speed operational amplifier



Product status link

[RHF310A](#)

### Features

- Ultra-low consumption:
  - 2 mW operating
  - 400  $\mu$ A quiescent current
- Bandwidth: 120 MHz (gain = 2)
- Slew rate: 115 V/ $\mu$ s
- Specified on 1 k $\Omega$
- Input noise: 7.5 nV/ $\sqrt{\text{Hz}}$
- 5 V power supply
- ELDRS free up to 300 krad
- SEL immune at 110 MeV.cm<sup>2</sup>/mg
- SET characterized
- SMD pin: 5962F07233
- Mass: 0.45 g

### Applications

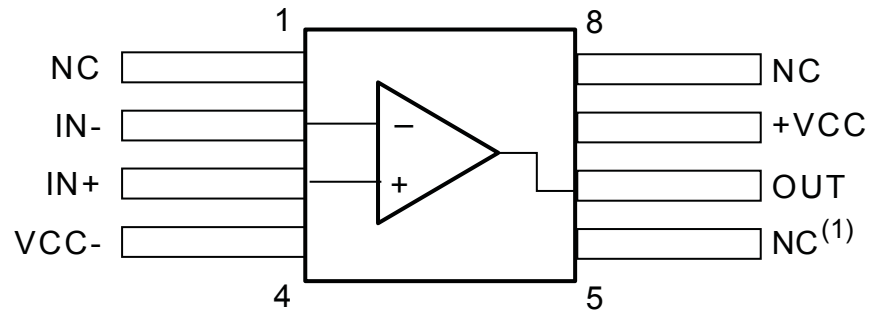
- Low-power, high-speed systems
- Communication and space equipment
- Harsh environments
- ADC drivers

### Description

The **RHF310A** device is a very low power, high-speed, single operational amplifier. A bandwidth of 120 MHz is achieved while drawing only 400  $\mu$ A of quiescent current. This low-power characteristic is particularly suitable for high-speed battery powered devices requiring dynamic performance. The **RHF310A** is mounted in a Flat-8 hermetic package.

## 1 Pin description

Figure 1. Pin connections of ceramic Flat-8 (top view)



1. The upper metallic lid is electrically connected to pin 5

## 2 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply voltage (voltage difference between $-V_{CC}$ and $V_{CC}$ pins) <sup>(1)</sup>	6	V	
$V_{id}$	Differential input voltage <sup>(2)</sup>	$\pm 0.5$		
$V_{in}$	Input voltage range <sup>(3)</sup>	$\pm 2.5$		
$T_{stg}$	Storage temperature	-65 to 150	°C	
$T_j$	Maximum junction temperature	150		
$R_{thja}$	Thermal resistance junction to ambient area	150	°C/W	
$R_{thjc}$	Thermal resistance junction to case	22		
$P_{max}$	Maximum power dissipation (at $T_{amb} = 25\text{ °C}$ for $T_j = 150\text{ °C}$ ) <sup>(4)</sup>	830	mW	
ESD	HBM: human body model <sup>(5)</sup>	Pins 1, 4, 5, 6, 7 and 8	2	kV
		Pins 2 and 3	0.5	
	MM: machine model <sup>(6)</sup>	Pins 1, 4, 5, 6, 7 and 8	200	V
		Pins 2 and 3	60	
	CDM: charged device model (all pins) <sup>(7)</sup>		1.5	kV
	Latch-up immunity		200	mA

- All voltage values are measured with respect to the ground pin.
- The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
- The magnitude of the input and output voltage must never exceed  $V_{CC} + 0.3\text{ V}$ .
- Short-circuits can cause excessive heating. Destructive dissipation can result from short circuits on amplifiers.
- Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- This is a minimum value. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
- Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	4.5 to 5.5	V
$V_{icm}$	Common-mode input voltage	$-V_{CC} + 1.5\text{ V}$ to $V_{CC} - 1.5\text{ V}$	
$T_{amb}$	Operating free-air temperature range <sup>(1)</sup>	-55 to 125	°C

- $T_j$  must never exceed 150 °C.  $P = (T_j - T_{amb}) / R_{thja} = (T_j - T_{case}) / R_{thjc}$  where  $P$  is the power that the RHF310A must dissipate in the application.

### 3 Electrical characteristics

**Table 3. Electrical characteristics for  $V_{CC} = \pm 2.5\text{ V}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
<b>DC performance</b>							
$V_{io}$	Input offset voltage		125 °C	-6.5		6.5	mV
			25 °C	-6.5	1.7	6.5	
			-55 °C	-6.5		6.5	
$I_{ib+}$	Non-inverting input bias current		125 °C			15	$\mu\text{A}$
			25 °C		3.1	12	
			-55 °C			15	
$I_{ib-}$	Inverting input bias current		125 °C			7	$\mu\text{A}$
			25 °C		0.1	5	
			-55 °C			7	
CMR	Common mode rejection ratio, $20 \log (\Delta V_{ic} / \Delta V_{io})$	$\Delta V_{ic} = \pm 1\text{ V}$	125 °C	55			dB
			25 °C	57	61		
			-55 °C	55			
SVR	Supply voltage rejection ratio, $20 \log (\Delta V_{CC} / \Delta V_{out})$	$\Delta V_{CC} = 3.5\text{ V to }5\text{ V}$	125 °C	50			dB
			25 °C	65	82		
			-55 °C	50			
PSRR	Power supply rejection ratio, $20 \log (\Delta V_{CC} / \Delta V_{out})$	$\Delta V_{CC} = 200\text{ mV}_{pp}$ at 1 kHz	25 °C		50		
$I_{CC}$	Supply current	No load	125 °C			600	$\mu\text{A}$
			25 °C		400	530	
			-55 °C			600	
<b>Dynamic performance and output characteristics</b>							
$R_{OL}$	Transimpedance	$\Delta V_{out} = \pm 1\text{ V}$ , $R_L = 1\text{ k}\Omega$	125 °C	500			k $\Omega$
			25 °C	600	1450		
			-55 °C	500			
Bw	Small signal -3 dB bandwidth on 1 k $\Omega$ load		25 °C		230		MHz
			25 °C		26		
			25 °C		120		
	Gain flatness at 0.1 dB	$V_{out} = 20\text{ mV}_{pp}$ , $A_V = 2$ , $R_L = 1\text{ k}\Omega$	25 °C		25		
SR	Slew rate <sup>(1)</sup>	$V_{out} = 2\text{ V}_{pp}$ , $A_V = 2$ , $R_L = 100\text{ }\Omega$	25 °C	90	115		V/ $\mu\text{s}$
$V_{OH}$	High-level output voltage	$R_L = 100\text{ }\Omega$	125 °C	1.5			V
			25 °C	1.55	1.65		
			-55 °C	1.5			
$V_{OL}$	Low-level output voltage	$R_L = 100\text{ }\Omega$	125 °C			-1.5	V
			25 °C		-1.66	-1.55	
			-55 °C			-1.5	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{out}$	$I_{sink}^{(2)}$	Output to GND	125 °C	70		mA
			25 °C	70	110	
			-55 °C	70		
	$I_{source}^{(3)}$	Output to GND	125 °C	60		
			25 °C	60	100	
			-55 °C	60		
<b>Noise and distortion</b>						
eN	Equivalent input noise voltage <sup>(4)</sup>	F = 100 kHz	25 °C		7.5	nV/ $\sqrt{Hz}$
iN	Equivalent positive input noise current <sup>(4)</sup>	F = 100 kHz	25 °C		13	pA/ $\sqrt{Hz}$
	Equivalent negative input noise current <sup>(4)</sup>	F = 100 kHz	25 °C		6	
SFDR	Spurious free dynamic range	$A_V = +2, V_{out} = 2 V_{pp}, R_L = 100 \Omega$	25 °C			dBc
		F = 1 MHz	25 °C		-87	
		F = 10 MHz	25 °C		-55	

1. Guaranteed by characterization of initial design release and upon design or process changes which affect this parameter.
2. See Section 3: Figure 11 for more details.
3. See Section 3: Figure 12 for more details.
4. See Section 6.3: Intermodulation distortion product.

**Table 4. Closed-loop gain and feedback components**

Gain (V/V)	+ 2	- 2	+ 4	- 4	+ 10	- 10
$R_{fb} (\Omega)$	1.2 k	1 k	150	300	100	180

## 4 Electrical characteristic curves

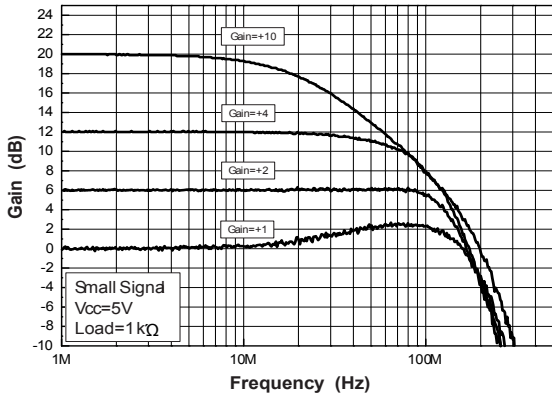
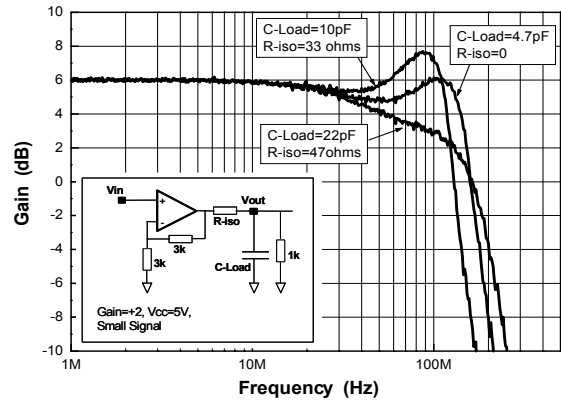
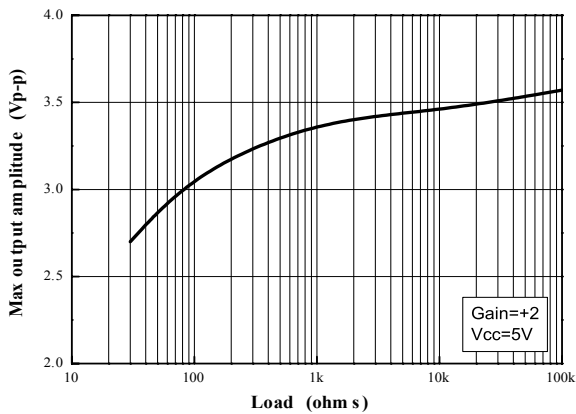
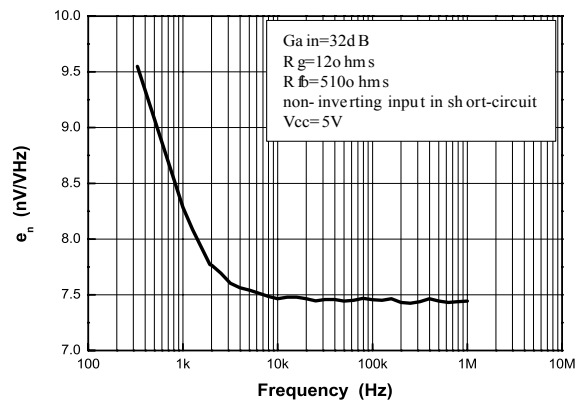
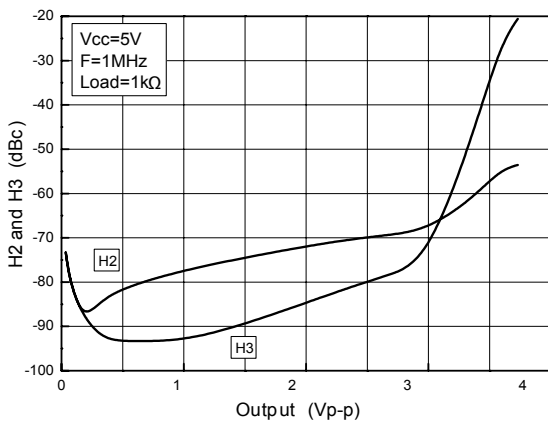
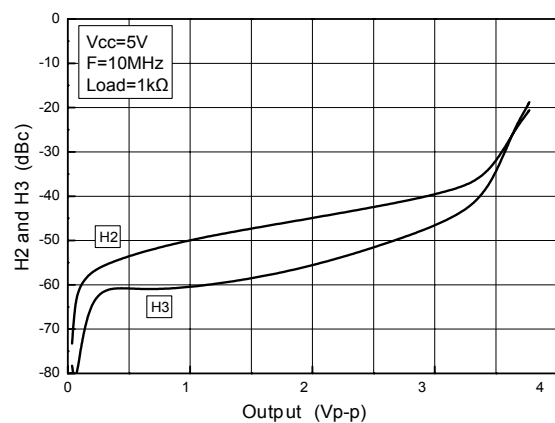
**Figure 2. Frequency response, positive gain**

**Figure 3. Frequency response vs. capa-load**

**Figure 4. Output amplitude vs. load**

**Figure 5. Input voltage noise vs. frequency**

**Figure 6. Distortion at 1 MHz**

**Figure 7. Distortion at 10 MHz**


Figure 8. Positive slew rate on 1 kΩ load

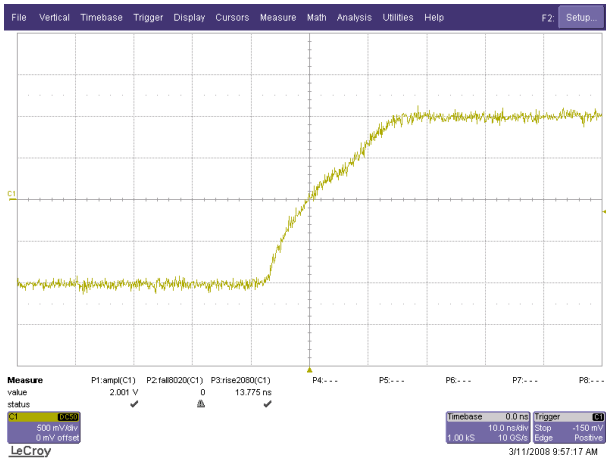


Figure 9. Negative slew rate on 1 kΩ load

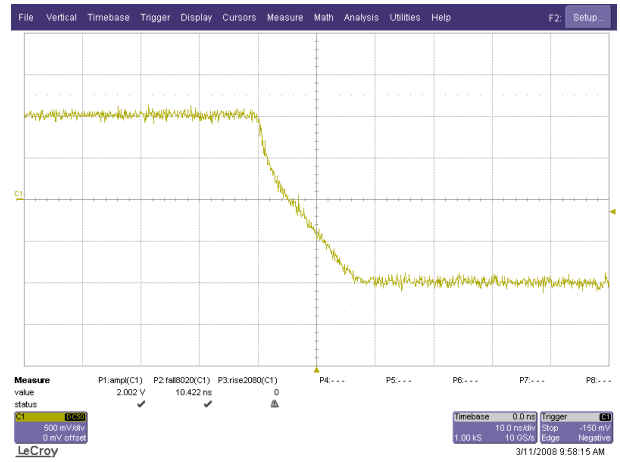


Figure 10. Quiescent current vs. V<sub>CC</sub>

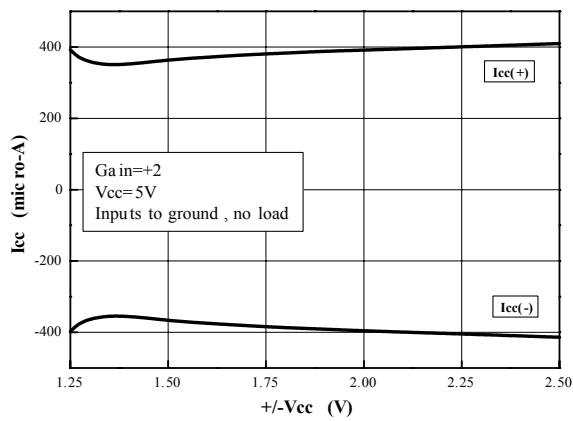


Figure 11. I<sub>sink</sub>

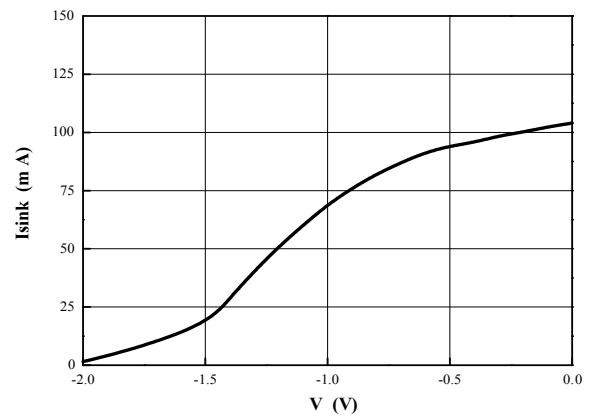


Figure 12. I<sub>source</sub>

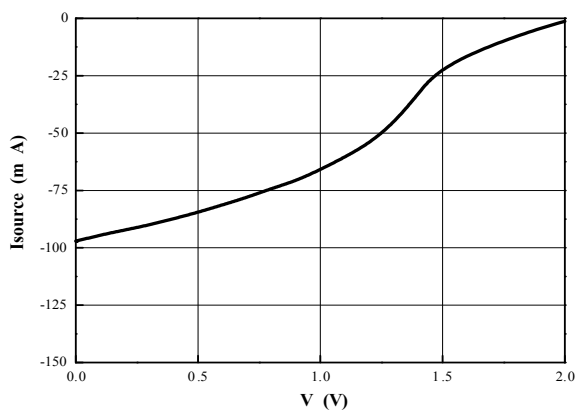


Figure 13. Bandwidth vs. temperature

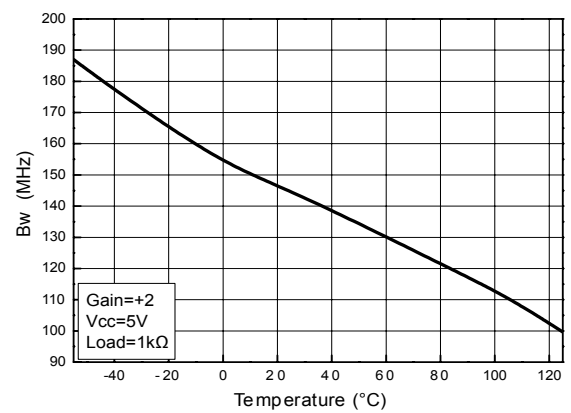


Figure 14. CMR vs. temperature

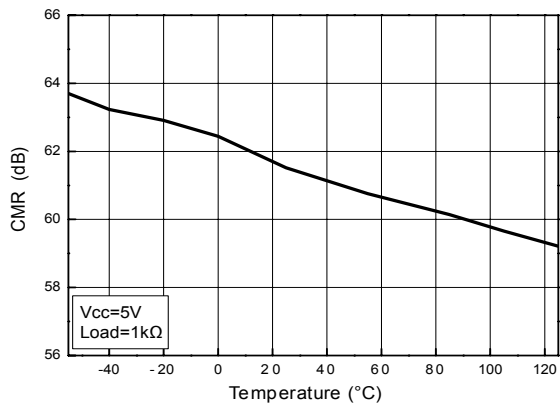


Figure 15. SVR vs. temperature

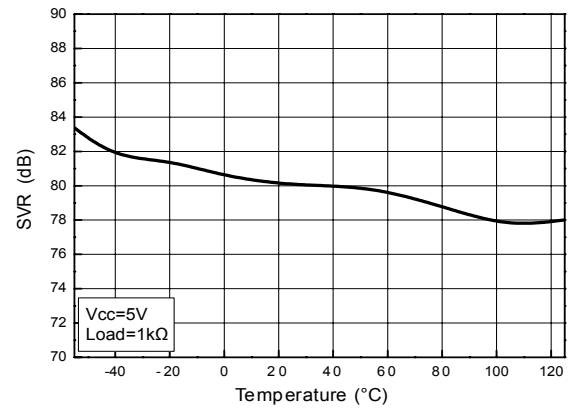


Figure 16. Slew rate vs. temperature

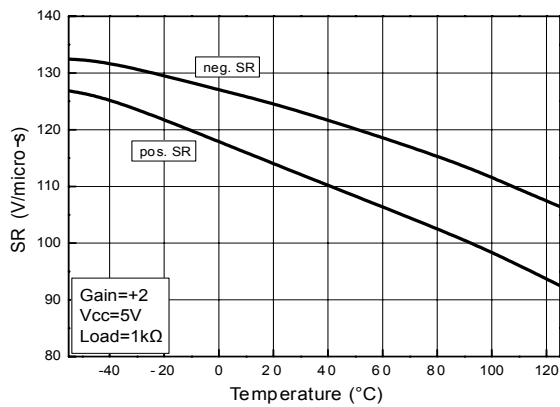


Figure 17. R<sub>OL</sub> vs. temperature

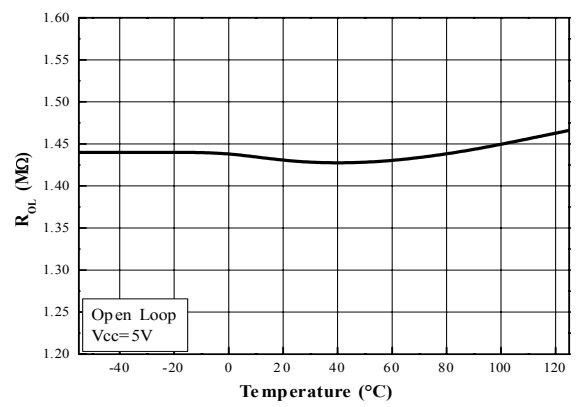


Figure 18. I<sub>bias</sub> vs. temperature

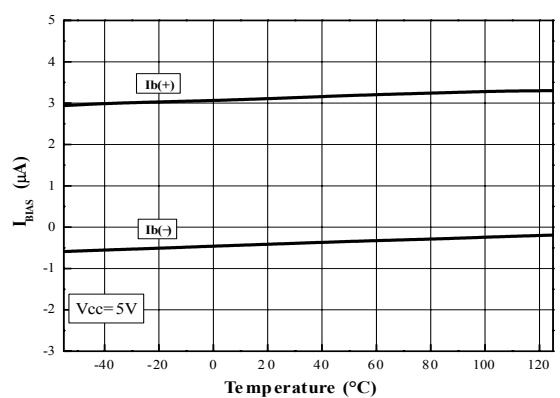


Figure 19. V<sub>IO</sub> vs. temperature

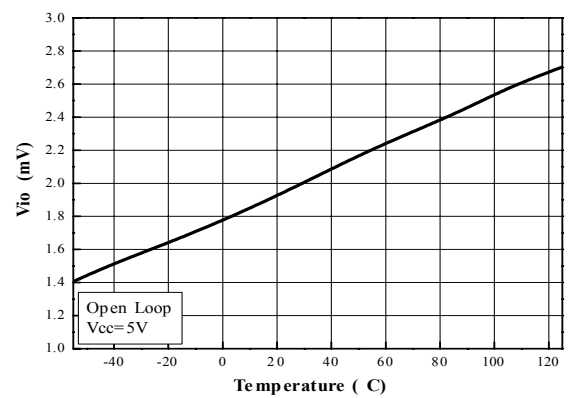


Figure 20.  $V_{OH}$  and  $V_{OL}$  vs. temperature

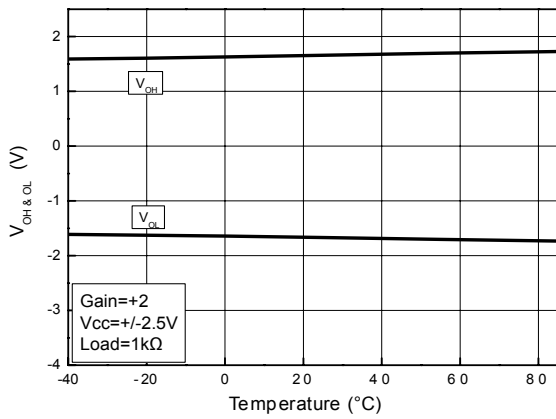


Figure 21.  $I_{out}$  vs. temperature

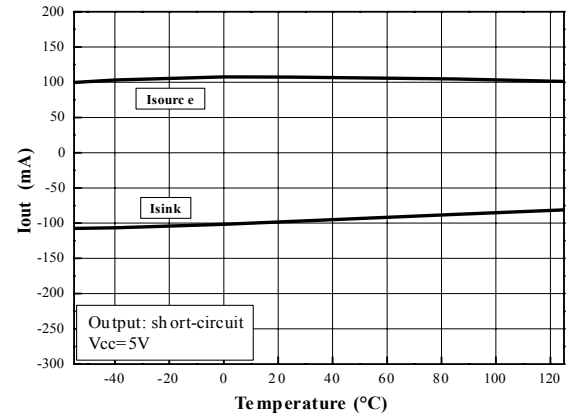
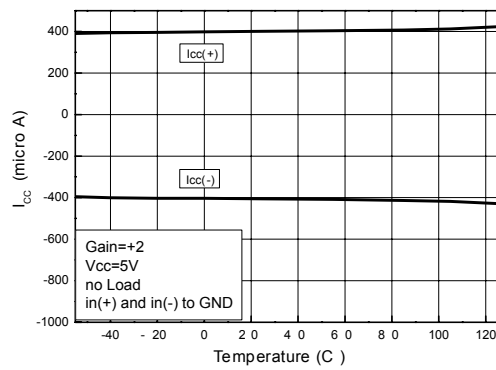


Figure 22.  $I_{CC}$  vs. temperature



## 5 Radiations

### 5.1 Introduction

Table 6 summarizes the radiation performance of the RHF310A.

**Table 5. Radiations**

Type	Features		Value	Unit
TID	High-dose rate		300	krad
	Low-dose rate		300	
	ELDRS		300	
Heavy ions	SEL immunity (at 125 °C) up to:		110	MeV.cm <sup>2</sup> /mg
	SET characterized	Inverting	No SET	
		Non-inverting	LET <sub>th</sub> = 18	MeV.cm <sup>2</sup> /mg
			$\sigma = 1.00E-06$	cm <sup>2</sup> /device
		Subtracting	LET <sub>th</sub> = 7	MeV.cm <sup>2</sup> /mg
	$\sigma = 2.00E-05$		cm <sup>2</sup> /device	

### 5.2 Total ionizing dose (TID)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 test method 1019 specification.

The RHF310A is RHA QML-V qualified, and is tested and characterized in full compliance with the MIL-STD-883 specification. It uses a mixed bipolar and CMOS technology and is tested both below 10 mrad/s (low dose rate) and between 50 and 300 rad/s (high dose rate).

- The ELDRS characterization is performed in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.
- Each wafer lot is tested at high-dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

### 5.3 Heavy ions

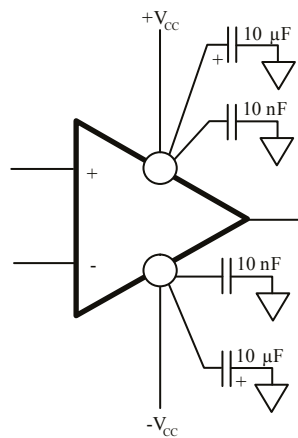
*Note: The heavy ion trials are performed on qualification lots only. No additional test is performed.*

## 6 Device description and operation

### 6.1 Power supply considerations

Correct power supply bypassing is very important for optimizing the performance of the device in high-frequency ranges. The bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than 1  $\mu\text{F}$  is necessary to minimize the distortion. For better quality bypassing, a capacitor of 10 nF can be added, which should also be placed as close as possible to the IC pins. The bypass capacitors must be incorporated for both the negative and positive supply.

**Figure 23. Circuit for power supply bypassing**



#### 6.1.1 Single power supply

If you use a single-supply system, biasing is necessary to obtain a positive output dynamic range between the 0 V and  $V_{CC}$  supply rails. Considering the values of  $V_{OH}$  and  $V_{OL}$ , the amplifier provides an output swing from 0.9 V to 4.1 V on a 1 k $\Omega$  load.

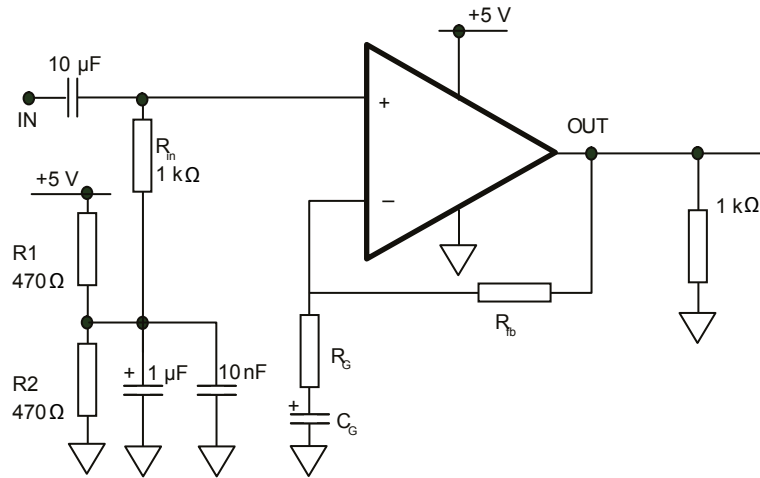
The amplifier must be biased with a mid-supply (nominally  $V_{CC}/2$ ) in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (55  $\mu\text{A}$  maximum) as 1 % of the current through the resistance divider, two resistances of 470  $\Omega$  can be used to maintain a mid-supply.

The input provides a high-pass filter with a break frequency below 10 Hz, which is necessary to remove the original 0 V DC component of the input signal and to set it at  $V_{CC}/2$ .

**Figure 24.** Figure 24 illustrates a 5 V single power supply configuration.

A capacitor  $C_G$  is added in the gain network to ensure a unity gain at low frequencies to keep the right DC component at the output.  $C_G$  contributes to a high-pass filter with  $R_{fb}/R_G$  and its value is calculated with regard to the cut-off frequency of this low-pass filter.

Figure 24. Circuit for +5 V single supply

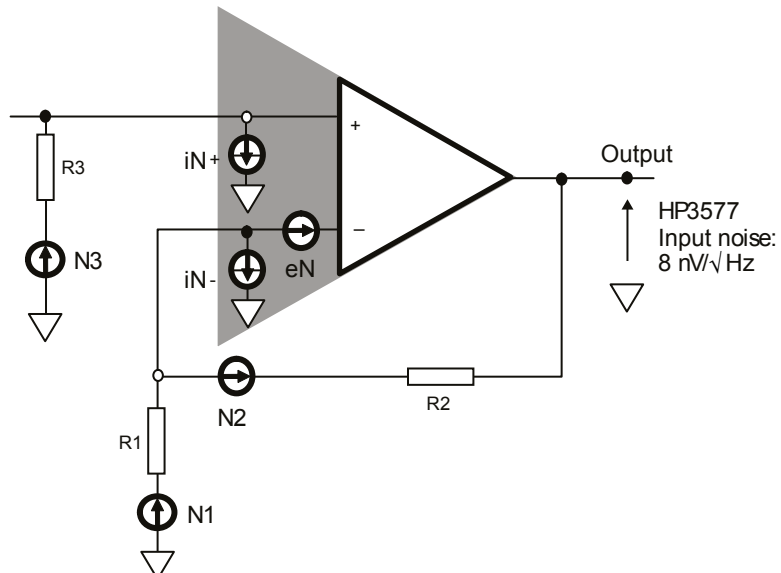


## 6.2 Noise measurements

The noise model is shown in Figure 25. Figure 25.

- $eN$ : input voltage noise of the amplifier
- $iNn$ : negative input current noise of the amplifier
- $iNp$ : positive input current noise of the amplifier

Figure 25. Noise model



The thermal noise of a resistance R is:

$$\sqrt{4kTR\Delta F}$$

Where  $\Delta F$  is the specified bandwidth, and  $k$  is the Boltzmann's constant, equal to  $1,374 \cdot 10^{-23} \text{J/}^\circ\text{K}$ .  $T$  is the temperature ( $^\circ\text{K}$ ).

On a 1 Hz bandwidth the thermal noise is reduced to:

$$\sqrt{4kTR}$$

The output noise  $eNo$  is calculated using the superposition theorem. However,  $eNo$  is not the simple sum of all noise sources but rather the square root of the sum of the square of each noise source, as shown in [Equation 1](#).

#### Equation 1

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2}$$

#### Equation 2

$$eNo^2 = eN^2 \cdot g^2 + iNn^2 \cdot R2^2 + iNp^2 \cdot R3^2 \cdot g^2 + \frac{R2^2}{R1} \cdot 4kTR1 + 4kTR2 + 1 \cdot \frac{R2^2}{R1} \cdot 4kTR3$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is shown in [Equation 3](#).

#### Equation 3

$$eNo = \sqrt{(\text{Measure d})^2 - (\text{ins trumen tation})^2}$$

The input noise is called **equivalent input noise** because it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain ( $eNo/g$ ).

After simplification of the fourth and fifth terms of [Equation 2](#), you obtain [Equation 4](#).

#### Equation 4

$$eNo^2 = eN^2 \cdot g^2 + iNn^2 \cdot R2^2 + iNp^2 \cdot R3^2 \cdot g^2 + g \cdot 4kTR2 + 1 \cdot \frac{R2^2}{R1} \cdot 4kTR3$$

### 6.2.1 Measurement of the input voltage noise $eN$

Assuming a short-circuit on the non-inverting input ( $R3 = 0$ ), from [Equation 4](#) you can derive [Equation 5](#).

#### Equation 5

$$eNo = \sqrt{eN^2 \cdot g^2 + iNn^2 \cdot R2^2 + g \cdot 4kTR2}$$

To easily extract the value of  $eN$ , the resistance  $R2$  must be as low as possible. On the other hand, the gain must be high enough.  $R3 = 0$  and gain ( $g$ ) = 100.

### 6.2.2 Measurement of the negative input current noise $iNn$

To measure the negative input current noise  $iNn$ ,  $R3$  is set to zero and [Equation 5](#) is used. This time, the gain must be lower in order to decrease the thermal noise contribution.  $R3 = 0$  and gain ( $g$ ) = 10.

### 6.2.3 Measurement of the positive input current noise $iNp$

To extract  $iNp$  from [Equation 3](#), a resistance  $R3$  is connected to the non-inverting input. The value of  $R3$  must be selected so that its thermal noise contribution is as low as possible against the  $iNp$  contribution.  $R3 = 100 \Omega$  and gain ( $g$ ) = 10.

## 6.3 Intermodulation distortion product

The non-ideal output of the amplifier can be described by the following series of equations.

$$V_{out} = C_0 + C_1 V_{in} + C_2 V_{in}^2 + \dots + C_n V_{in}^n$$

Where the input is  $V_{in} = A \sin \omega t$ ,  $C_0$  is the DC component,  $C_1(V_{in})$  is the fundamental and  $C_n$  is the amplitude of the harmonics of the output signal  $V_{out}$ .

A one-frequency (one-tone) input signal contributes to harmonic distortion. A two-tone input signal contributes to harmonic distortion and to the intermodulation product.

The study of the intermodulation and distortion for a two-tone input signal is the first step in characterizing the driving capability of multi-tone input signals.

In this case:

$$V_{in} = A \sin \omega_1 t + A \sin \omega_2 t$$

Therefore:

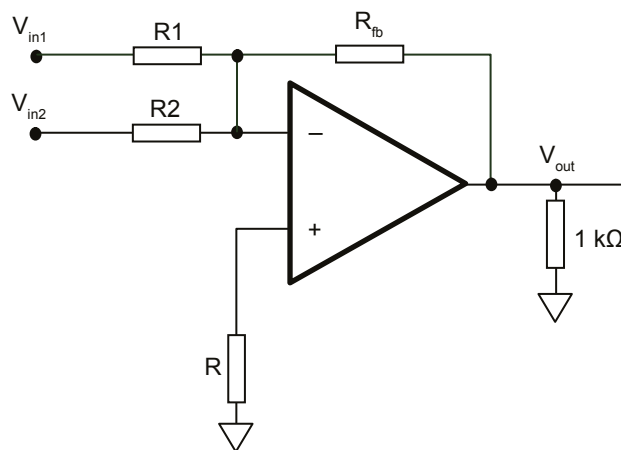
$$V_{out} = C_0 + C_1 (A \sin \omega_1 t + A \sin \omega_2 t) + C_2 (A \sin \omega_1 t + A \sin \omega_2 t)^2 \dots + C_n (A \sin \omega_1 t + A \sin \omega_2 t)^n$$

From this expression, we can extract the distortion terms and the intermodulation terms from a single sine wave.

- Second-order intermodulation terms IM2 by the frequencies  $(\omega_1 - \omega_2)$  and  $(\omega_1 + \omega_2)$  with an amplitude of  $C_2 A^2$ .
- Third-order intermodulation terms IM3 by the frequencies  $(2\omega_1 - \omega_2)$ ,  $(2\omega_1 + \omega_2)$ ,  $(-\omega_1 + 2\omega_2)$  and  $(\omega_1 + 2\omega_2)$  with an amplitude of  $(3/4)C_3 A^3$ .

The intermodulation product of the driver is measured by using the driver as a mixer in a summing amplifier configuration (Figure 26. Figure 26). In this way, the non-linearity problem of an external mixing device is avoided.

**Figure 26. Inverting summing amplifier**



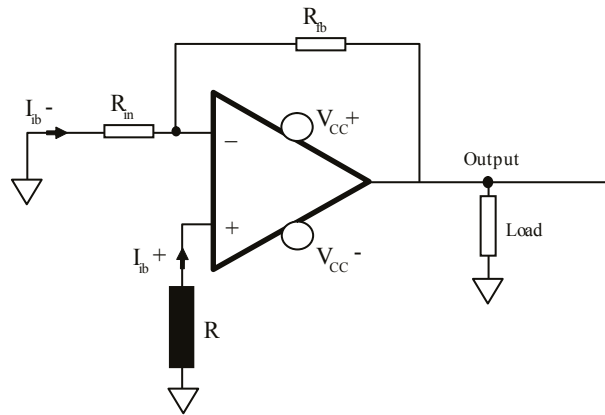
## 6.4 Bias of an inverting amplifier

A resistance is necessary to achieve good input biasing, such as resistance R shown in Figure 27. Figure 29.

The value of this resistance is calculated from the negative and positive input bias current. The aim is to compensate for the offset bias current, which can affect the input offset voltage and the output DC component. Assuming  $I_{ib-}$ ,  $I_{ib+}$ ,  $R_{in}$ ,  $R_{fb}$  and a 0 V output, the resistance R is:

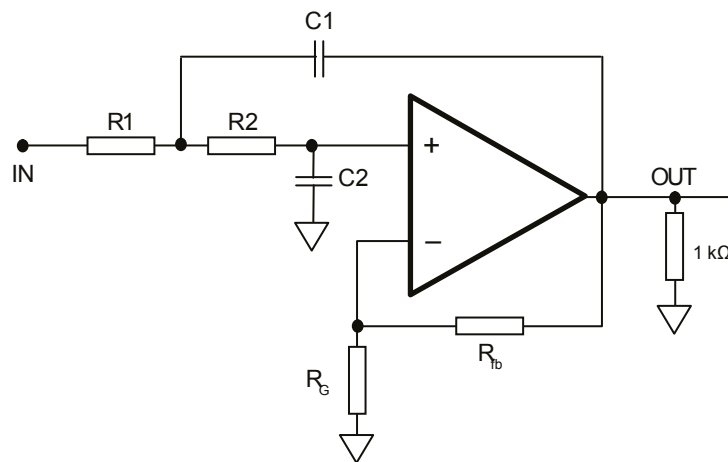
$$R = \frac{R_{in} \cdot R_{fb}}{R_{in} + R_{fb}}$$

Figure 27. Compensation of the input bias current



## 6.5 Active filtering

Figure 28. Low-pass active filtering, Sallen-Key



From the resistors  $R_{fb}$  and  $R_G$  it is possible to directly calculate the gain of the filter in a classic non-inverting amplification configuration.

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

The response of the system is assumed to be:

$$T_{j\omega} = \frac{V_{out}j\omega}{V_{in}j\omega} = \frac{g}{1 + 2\zeta \frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^2}}$$

The cut-off frequency is not gain-dependent and so becomes:

$$\omega_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

The damping factor is calculated using the following expression.

$$\zeta = \frac{1}{2} \omega_c (C_1 R_1 + C_1 R_2 + C_2 R_1 - C_1 R_1 g)$$

The higher the gain, the more sensitive the damping factor. When the gain is higher than 1, it is preferable to use very stable resistor and capacitor values. In the case of  $R_1 = R_2 = R$ :

$$\zeta = \frac{2C_2 - C_1 \frac{R_{fb}}{R_g}}{2\sqrt{C_1 C_2}}$$

Due to a limited selection of capacitor values in comparison with the resistors, you can set  $C_1 = C_2 = C$ , so that:

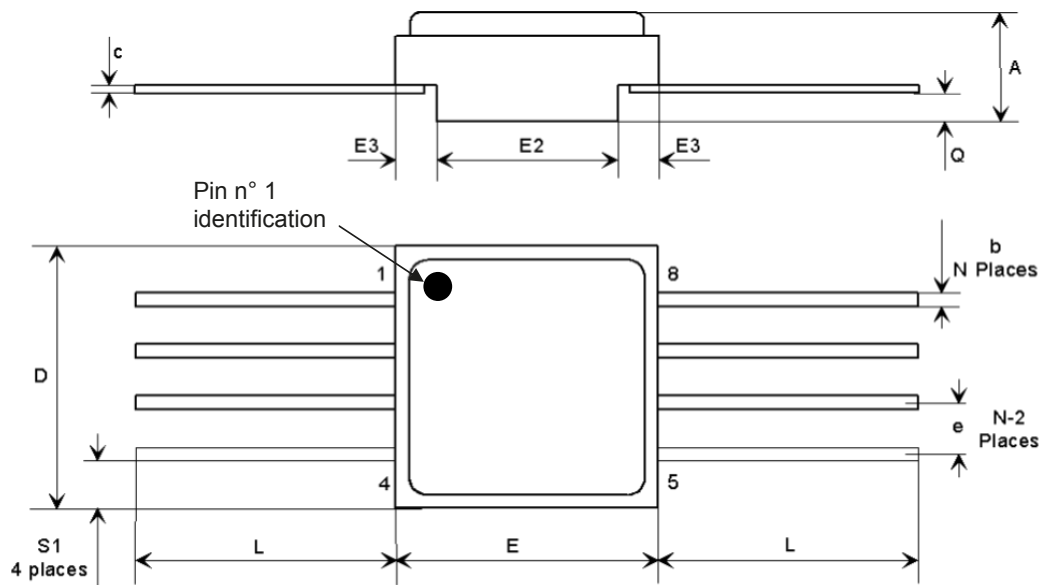
$$\zeta = \frac{2R_2 - R_1 \frac{R_{fb}}{R_g}}{2\sqrt{R_1 R_2}}$$

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.1 Ceramic Flat-8 package information

Figure 29. Ceramic Flat-8 package outline



**Note:** The upper metallic lid is electrically connected to pin 5. No other pin is electrically connected to the metallic lid nor to the IC die inside the package.

**Table 6. Ceramic Flat-8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51		7.38	0.256		0.291
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

## 8 Ordering information

**Table 7. Ordering information**

Order codes	SMD <sup>(1)</sup>	Quality level	Package	Finishing	Marking <sup>(2)</sup>	Packing
RHF310AK1	—	Engineering model	Flat-8 (lid connected to a pin)	Gold	RHF310AK1	Tray
RHF310AK01V	5962F07233	QML-V flight			5962F0723302VYC	

- Standard microcircuit drawing
- Specific marking only. Complete marking includes the following:
  - ST logo
  - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
  - Country of origin (FR = France)

### Other information

The date code is structured as shown below:

- EM xyywwz
- QML-V yywwz  
where:
  - x (EM only) = 3 and the assembly location is Rennes, France
  - yy = last two digits of the year
  - ww = week digits
  - z = lot index in the week

### Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

**Table 8. Product documentation**

Quality level	Item
Engineering model	Certificate of conformance including : Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID
QML-V Flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
26-May-2009	1	Initial release.
12-Jul-2010	2	Added Mass in Features on cover page. Added Table 1: "Device summary" on cover page, with full ordering information. Updated temperature limits for $T_{min} < T_{amb} < T_{max}$ in Table 3: "Operating conditions".
27-Jul-2011	3	Added note to the Package information section and in the "Pin connections" diagram on the cover page.
09-Jan-2015	4	Document status updated from "Preliminary data" to "Production data". Replaced package name with "Flat-8S" instead of "Flat-8" Replaced package silhouette and added marker to show the position of pin 1 on package silhouette, pinout and drawing. Features: updated Updated Table 1: "Device summary" Added Section 3: "Radiations" Added Device description and operation and updated document layout accordingly. Added Section 6: "Ordering information" Added Section 7: "Other information"
15-Mar-2016	5	Updated document layout Table 1: "Device summary": updated footnote 1, SMD = standard microcircuit drawing.
31-Mar-2017	6	Added part number RHF310A Replaced cover image Updated Features Updated Applications Updated Description Added Section 1: "Pin description" Table 2: "Absolute maximum ratings": updated $R_{thja}$ and $R_{thjc}$ values. Table 4: updated Bw and SR parameters Section 5.2: "Total ionizing dose (TID)": corrected typos Added Section 7.2: "Ceramic Flat-8 package information" Table 9: "Order codes": updated table title, removed column "EPPL", added order codes RHF310AK1 and RHF310AK01V, and updated footnotes.
13-Feb-2020	7	Removed the part number RHF310 and all its references throughout the document due to obsolete status. Updated Section 8: Ordering information.
07-Apr-2026	8	Changed packing from Strip pack to Tray in <a href="#">Section 8: Ordering information</a> .

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