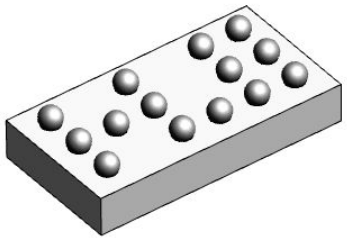
OCVPB22-14F6

Datasheet

ESD, overvoltage and overcurrent protection with charging orientation direction detection for wearables applications



WLCSP package14 bumps – pitch 400 µm
2.56 mm x 1.34 mm

Product status
OCVPB22-14F6

Features

- USB interface protection between cable and charging circuit during battery charging with:
  - Exceeds ESD IEC 61000-4-2 level 4 protection on cable side: ±15 kV contact on bridge inputs, and USB data-lines inputs
  - Detection of the polarity of the charging cable with rerouting in case of cable inversion thanks to 14 V input rectification bridge
  - Overvoltage protection (OVP) up to ± 14 V
  - Overcurrent protection (OCP) externally adjustable from 125 mA to 1.25 A
  - Controlled inrush current
  - Undervoltage lockout
  - 5 V USB 2.0 data lines protection, and multiplexer for data line polarity correction (R_{ON} = 6 Ω typical)
  - $\overline{FLAG}$ output signal (open-drain) available to inform thermal shutdown or overvoltage or overcurrent or uncompleted start-up phase
  - Proposed in 400µm pitch WLCSP package 14 bumps
  - Operating temperature from -30°C to 60°C

Benefits

- Minimal PCB footprint in wearable, mobile phone, tablet and all USB devices applications thanks to very strong integration
- High voltage protection management to give flexibility to customers to use low voltage charging circuit for power consumption and cost optimization
- USB cable inversion management

Complies with the following standards

- IEC 61000-4-2 level 4: ±15kV contact on bridge inputs and USB data-lines inputs
- JESD22-A114D level 2

Applications

- All wearable for battery charging with USB reversible connector

Description

The OCVPB22-14F6 is an integrated ESD, overvoltage and overcurrent protection with an integrated input rectification bridge to give flexibility for wearable customers to manage properly any kind of USB charging conditions with or without USB cable inversion.

Thanks to state of the art high voltage technology, ST can integrate in WLCSP package all required USB stressful high voltage and high current protection conditions (ESD, OVP and OCP) with control signals for wearable design optimization.

1 Functional description

OCVPB22-14F6 is a very integrated solution to be connected between USB cable and battery charge management chipset with very efficient protection to protect the system and the power management chipsets during battery charging.

As described herebelow , all protection functions are available to meet all stringent conditions of power supplies but also USB cable inversion:

- With 14 V input rectification bridge for polarity charging detection. Both signals (USB V_{CC} and USB datalines) are rerouted according to following rule (see Figure 2 and Table 3)

Table 1. Rectification bridge for polarity

IN_A	IN_B	USB_INC	USB_IND
V_{CC}	GND	D+	D-
GND	V_{CC}	D-	D+

- Adjustable overcurrent protection to prevent peak current to meet a wide range of wearable applications
- Overvoltage protection to properly meet battery charging voltage conditions and protecting from 14 V DC and to 20 V ringing at plug-in

Figure 1. Application block diagram

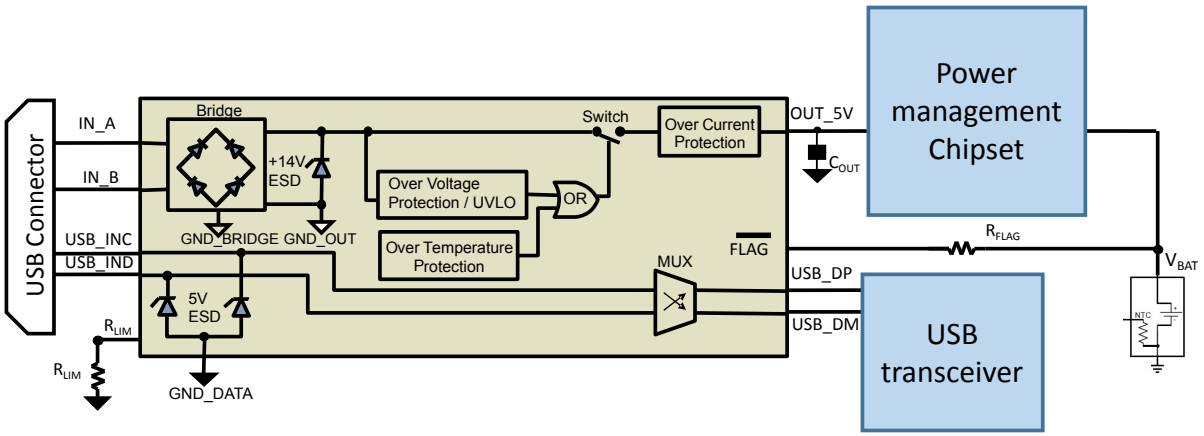


Table 2. Block diagram reference

Reference	Typical values	Comment
C_{OUT}	1 µF to 10 µF	Low ESR capacitor
R_{LIM}	From 82 Ω to 750 Ω	1% tolerance or better recommended
R_{FLAG}	100 kΩ	

Figure 2. **Functional diagram**

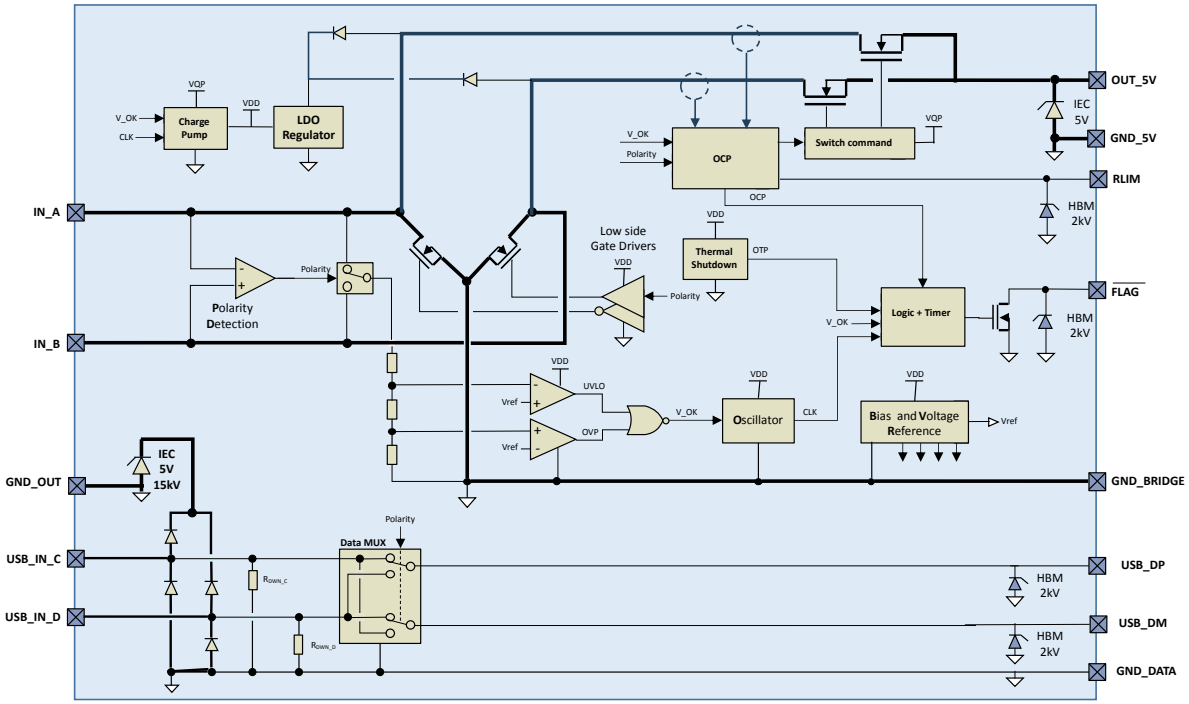


Figure 3. **Pin numbering (bump side)**

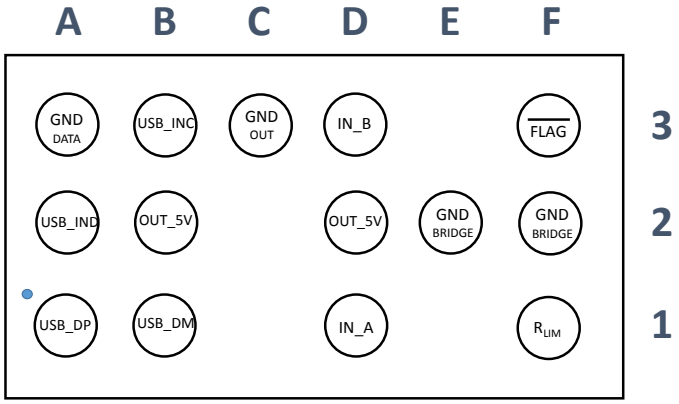


Figure 4. **Pin numbering (top view)**

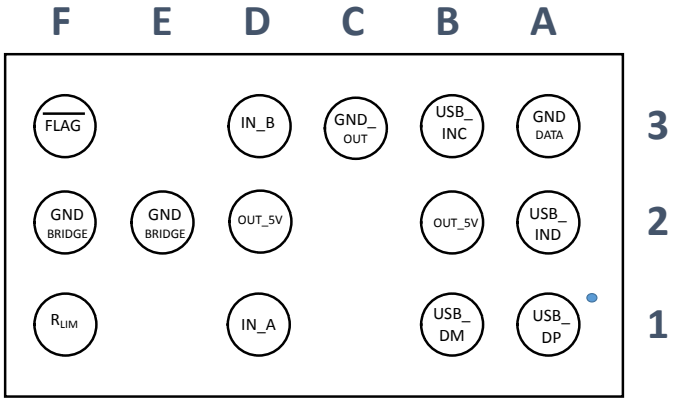


Table 3. **Pin description**

Pin	Name	Description	Pin	Name	Description
A1	USB_DP (OUT_USB_D+ DATA)	Output USB D+ dataline	B3	USB_INC	Input USB dataline USB pin 2 connector (D+ or D-)
A2	USB_IND	Input USB dataline USB pin 3 connector (D+ or D-)	D1	IN_A (USB connector V_{CC} or GND)	Input bridge rectification USB connector (V_{CC} or GND)
A3, C3, E2,F2	GND DATA GND OUT GND BRIDGE	Ground dataline Ground Output Ground bridge	D3	IN_B (USB connector GND or V_{CC})	Input bridge rectification USB connector (GND or V_{CC})
B1	USB_DM (OUT_USB_D- DATA)	Output USB D- dataline	F1	R_{LIM}	External resistor used to set current-limit threshold
B2, D2	OUT_5V	Output USB 5 V voltage charging	F3	$\overline{FLAG}$	Active-low open-drain output, asserted during overcurrent, over/under voltage and over temperature conditions

1.1 Rectification bridge description

Thanks to an input rectification bridge, polarity of the charging cable can be detected and be rerouted in case of USB cable inversion.

During steady state, current flow through power MOS of the bridge providing a low drop-out voltage.

1.2 OCP function description

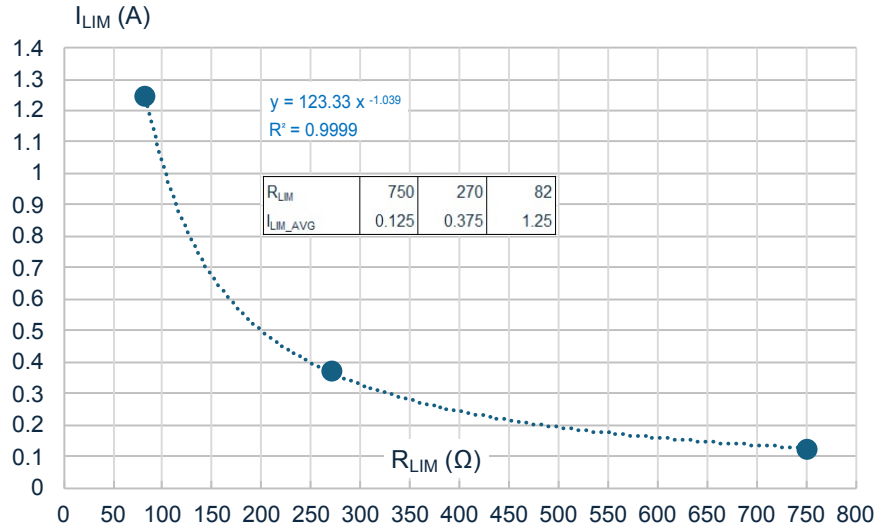
Over current protection is required to prevent any inrush current or unexpected overcurrent that could damage the system.

Current limitation of the OCP is set using an external resistor R_{LIM} (from 100 mA to 1.1 A min) to meet a wide range of wearable applications.

Typical limitation current is set at 10-15 % above targeted value as described in Table 4.

I_{LIM} versus R_{LIM} definition is described as follows:

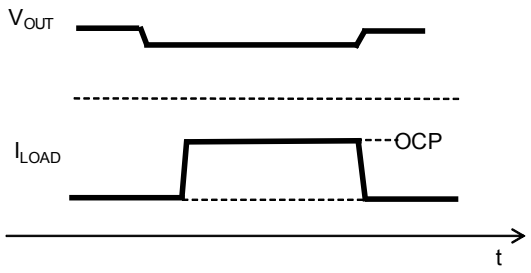
Figure 5. I_{LIM} versus R_{LIM} definition



Note: The maximum capacitance which can be attached to the output pin depends on the R_{LIM} setting, as described in Table 4.

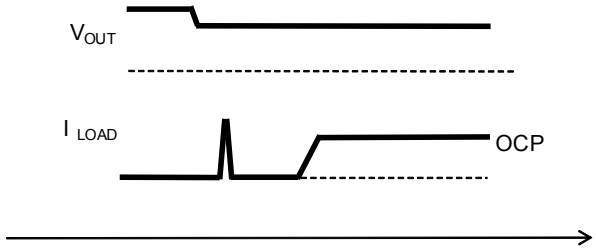
In case of slow overloading, the current is regulated at OCP level as described in Figure 6.

Figure 6. Load current regulation during slow overloading



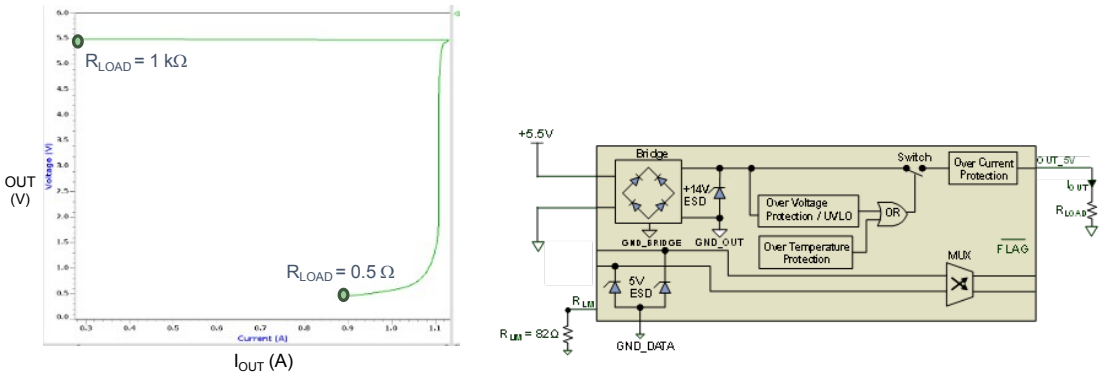
In case of fast overloading, the power-switch is switched-off in the microsecond range as described in Figure 7. Then the power-switch is slowly turned on and the load-current regulated at the OCP level.

Figure 7. **Fast overloading**



In case of fast short-circuit, the power-switch is switched-off in the microsecond. The typical over current protection transfer function is given in Figure 8.

Figure 8. **Typical over current protection transfer function**



During OCP operation, high power can be dissipated in the chip. If junction temperature reaches OTP level (135 °C), the power-switch is temporarily opened to cool the device. OCP is then re-enabled once T_j decreases by 25 °C.

Table 4. **Typical R_{LIM} settings**

R_{LIM} (Ω)	Maximum system output current (A)	OCVPB22-14F6 typical current limit (A)	Maximum output capacitor (µF)
750	0.1	0.125	1
270	0.31	0.375	3.3
82	1.1	1.25	10

1.3 OVP function description

Both undervoltage lockout and overvoltage lockout are integrated to secure correct operating voltage conditions of connected Power management chipset.

In normal charging condition, V_{IN} and V_{OUT} can vary from 4.25 V to 5.55 V.

Under 4.25 V and over 5.55 V, UVLO or OVLO are activated to disable the output (OVP switch open and FLAG set to low - to inform protection Power management chipset).

1.4 $\overline{\text{FLAG}}$ output signal

$\overline{\text{FLAG}}$ output signal (open-drain) is available to inform thermal shutdown or overvoltage or overcurrent or uncompleted start-up phase.

This signal is kept to low when product exceeds temperature conditions or voltage protection is activated or overcurrent occurs or start-up phase is still incomplete.

During normal conditions, this signal is at high level thanks to an external pull-up resistor.

2 Electrical characteristics

Table 5. Absolute maximum ratings (limiting values)

Symbol	Parameter	Test conditions	Value	Unit
V_{PP_USB}	ESD discharge on USB cable side, exceeds IEC 61000-4-2 level 4: pins D1 and D3 pins A2 and B3	Contact or air discharge pin to GND with C_{OUT}[1][2]	 ±15 ±15	kV
V_{PP_OUTPUT}	ESD discharge (all pins), HBM -JESD22-A114D, level 2	Contact or air discharge	±2	kV
V_{IN_MAX}	Max transient input voltage	IN_A to GND or IN_B to GND (test pulse < 5 min)	-0.3 to +14.0	V
V_{DATA_MAX}	Max data voltage	USB_INC, USB_INC, USB_DP and USB_DM	-0.3 to +5.5	V
V_{RLIM_MAX}, $V_{\overline{FLAG}}$ and OUT_5V	Max voltage range		-0.3 to +7	V
$I_{OUT\_MAX\_DC}$	Max DC output current on OUT_5V before OCP		1.1	A
$I_{\overline{FLAG}\_sink}$	Max sunk current through $\overline{FLAG}$ PIN		4	mA
R_{LIM}	OCP setting resistor range		82 to 750	Ω
T_{OP}	Operating temperature range		-30 to +60	°C
T_{STG}	Storage temperature range		-55 to +150	°C

1. *1 µF < C_{OUT} < 10 µF low ESR capacitor.*
2. *Maximum length between OUT_5V bump and C_{OUT} capacitor < 2 mm.*

Table 6. USB power electrical characteristic (-30 °C < T_{amb}< 60 °C, typ at T_{amb} = 25 °C and V_{IN} = 5 V unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	IN_A to GND or IN_B to GND	4.25		5.55	V
I_{Q_IN}	Supply quiescent current	$V_{INx-INy}$ = 5 V, R_{OUT} = 1 MΩ		1.25	2.5	mA
$UVLO_{OFF}$	Under-voltage lockout deactivation		3.8		4.25	V
$UVLO_{ON}$	Under-voltage Lockout		3.45		4.05	V
OVP_{ON}	Over-voltage protection		5.5		6.35	V
OVP_{OFF}	Over-voltage protection deactivation		5.45		6.2	V
$R_{ON\ High-side}$	High side ON resistance	I_{OUT} = 100 mA	50	78	130	mΩ
$R_{ON\ Low-side}$	Low side ON resistance	I_{OUT} = 100 mA	20	55	90	mΩ
I_{LIM}	Overcurrent threshold	R_{LIM} = 82 Ω, V_{OUT} = 4.75 V	1.19	1.25	1.39	A
		R_{LIM} = 270 Ω, V_{OUT} = 4.75 V	340	375	405	mA
		R_{LIM} = 750 Ω, V_{OUT} = 4.75 V	100	125	135	mA
T_{sd}	Thermal Shutdown		120	135		°C
T_{sd_hyst}	Thermal Shutdown hysteresis			20	40	°C
$V_{OL\_\overline{FLAG}}$	$\overline{FLAG}$ low state output voltage	V_{IN} = 3.6 V, I_{Sink} = 4 mA on $\overline{FLAG}$			0.4	V
$I_{\overline{FLAG}\_leak}$	$\overline{FLAG}$ leakage current	$V_{\overline{FLAG}}$ = 5 V			200	nA
T_{ON}	Activation time	From V_{IN} > $UVLO_{OFF}$ to $\overline{FLAG}$ = HIGH Z		1.2	2	ms

Table 7. USB data characteristic (-30 °C < T_{amb}< 65 °C, typ at T_{amb} = 25 °C and V_{IN} = 5 V unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DATA}	Dataline input Voltage range	USB_INC, USB_IND, USB_DP, USB_DM	-0.3		3.65	V
C_{ON}	ON capacitance	V_{DATA} = 0 V, F = 10 MHz		7.2		pF
F_C	Cut-off frequency	-3dB bandwidth (F = 10 MHz as reference) R_L = 50 Ω, C_L = 0 pF		920		MHz
		-3dB bandwidth (F = 10 MHz as reference) R_L = 50 Ω, C_L = 5 pF		614		
R_{ON_DATA}	On-Resistance	V_{DATA} = 0 V to 0.4 V, I_{DATA} = 8 mA			9.2	Ω
R_{ON_FLAT}	On-Resistance flatness	V_{DATA} = 0 V to 0.4 V, I_{DATA} = 8 mA		10		mΩ
R_{PULL_DOWN}	Pull-down resistor between IN_C,IN_D and GND			100		kΩ

Figure 9. **USB2.0 high speed 480 Mbps eye diagram (pin A1 and B1 - with OCVPB22-14F6 and no load capacitor)**

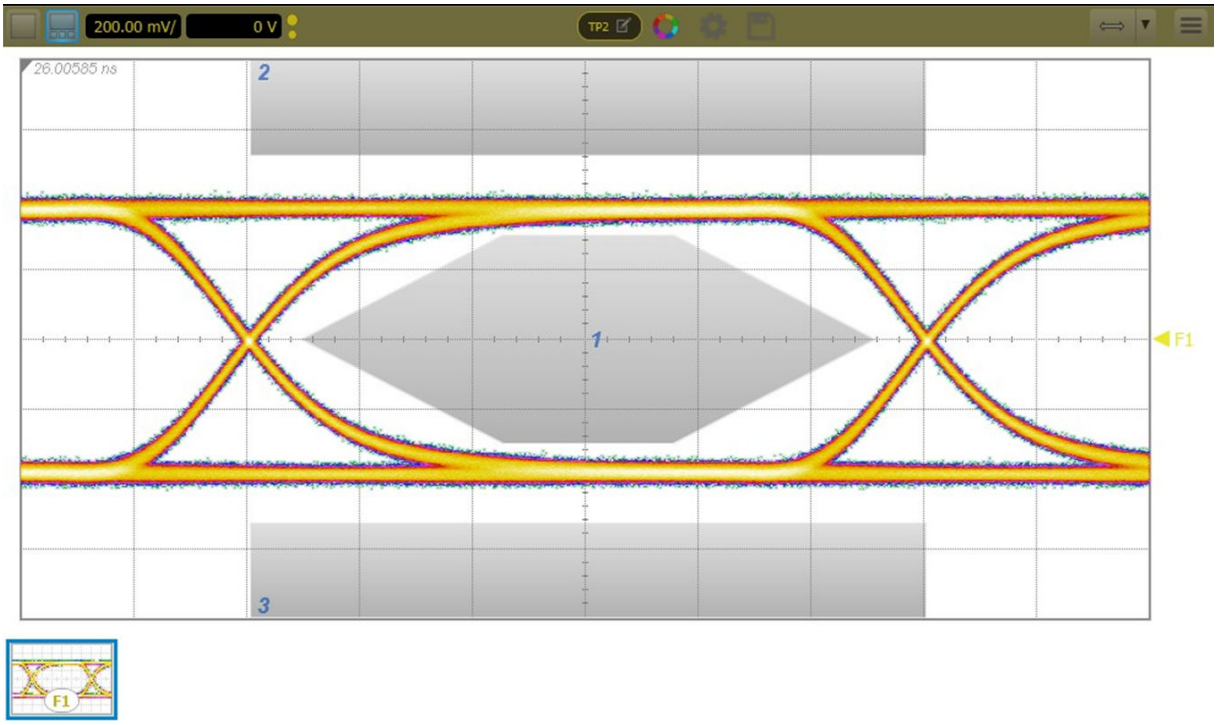
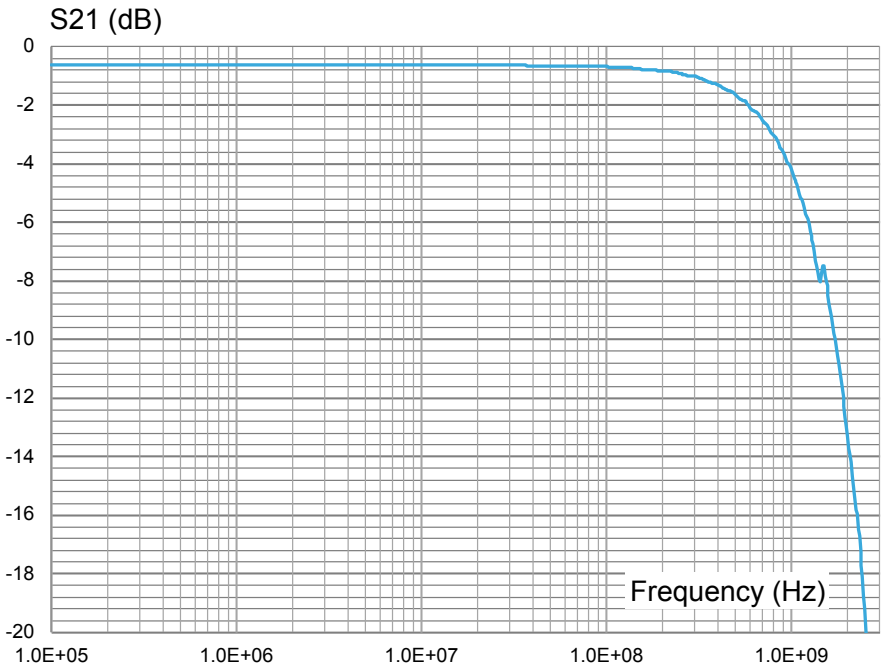


Figure 10. **S_{21} measurement (pin A1 and B1 - with no load capacitor)**

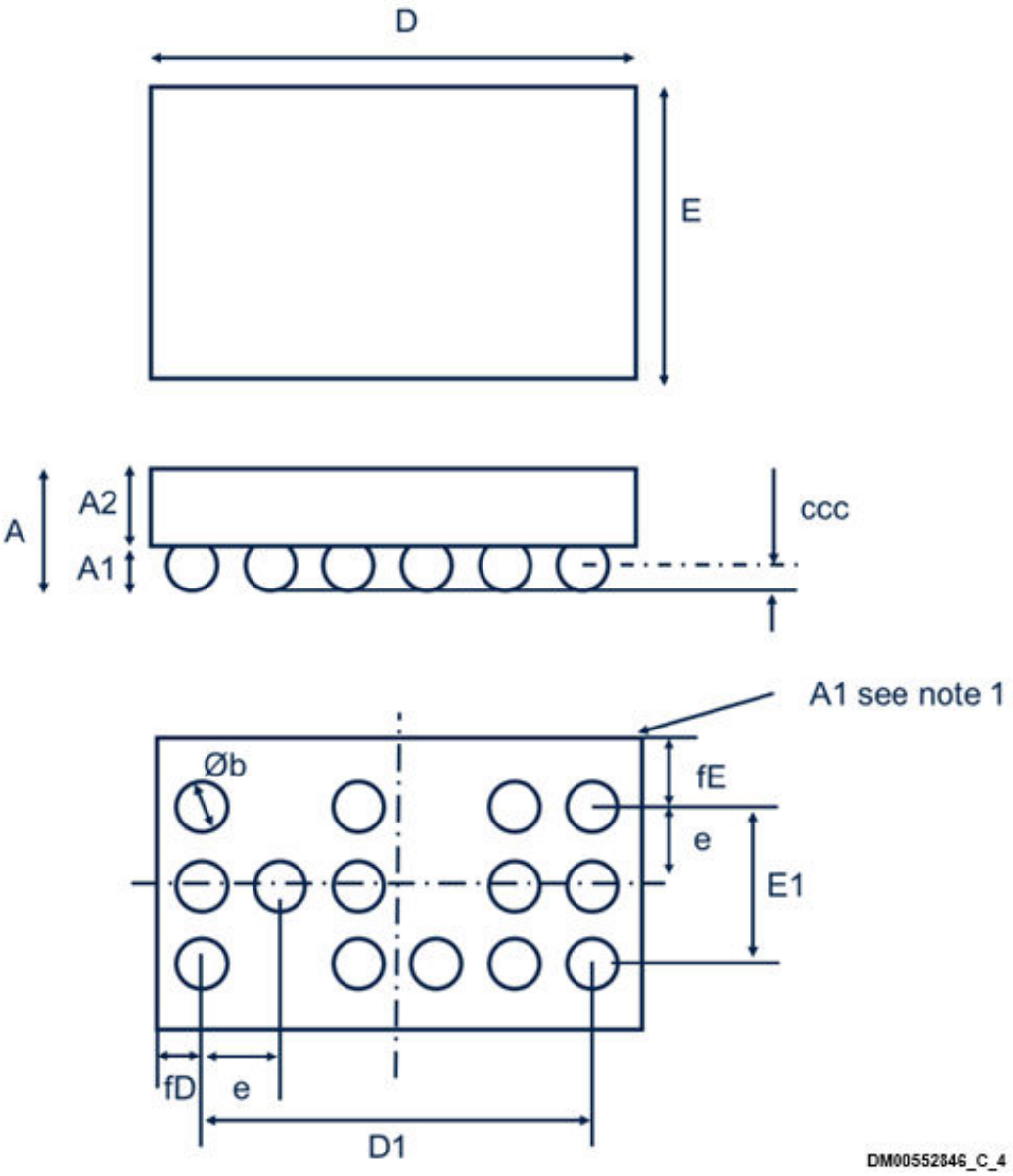


3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 WLCSP 14 bumps package information

Figure 11. WLCSP 14 bumps package outline

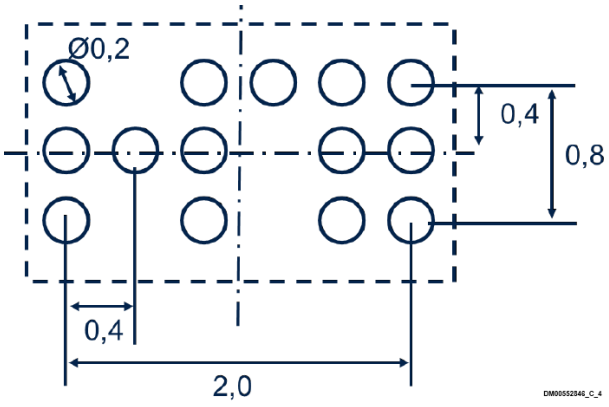


Note: The terminal A1 on the bumps side is identified by a distinguishing feature (for instance by a circular "clear area" - typically 0.1mm diameter). The terminal A1 on the backside of the product is identified by a distinguishing feature (for instance by a circular "dot" - typically 0.5mm diameter).

Table 8. **WLCSP 14 bumps mechanical data**

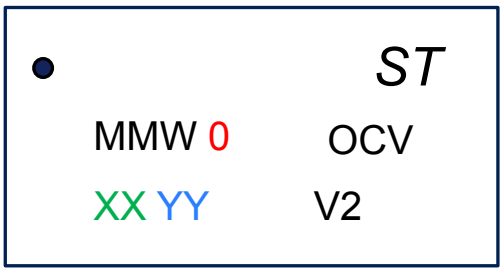
Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.540	0.580	0.620
A1	0.160	0.180	0.200
A2	0.380	0.400	0.420
b	0.205	0.230	0.255
D	2.508	2.558	2.608
D1		2.000	
E	1.294	1.344	1.394
E1		0.800	
e		0.400	
fD		0.274	
fE		0.267	
ccc			0.030

Figure 12. **Footprint dimensions (in mm)**



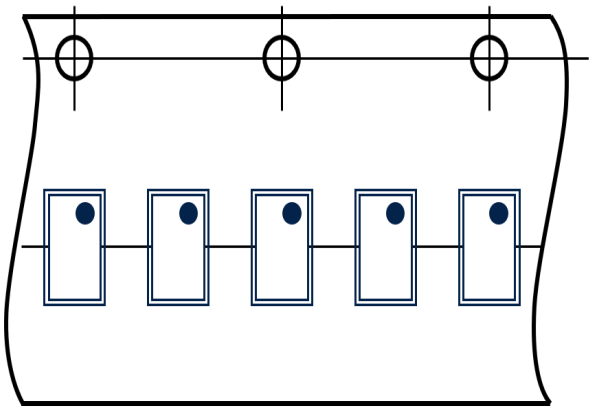
3.2 WLCSP 14 bumps tape and reel specification (all dimensions in mm)

Figure 13. Marking



MMW : lot number digits
0 : wafer number
XX : X die coordinate
YY : Y die coordinate
OCV : OCVPB series
V2 : version 2

Figure 14. Package orientation in reel



To ensure component traceability, labels are stuck on the reels and the cardboard box. The reels and the cardboard box are identified by labels including part number, shipped quantity and traceability references.

Traceability is ensured for each production lot and each shipment lot through the labeling. The trace code number printed on the labels ensures backward traceability from the lot received by the customer at each step of the process.

Trace code definition

Trace code is defined by 8 digits:

- **WX**: Assembly plant code: GK for ST Shenzhen China
- **yww**: Date code: y for year and ww for week
- **nnn**: alphanumeric sequential number

Figure 15. Labeling

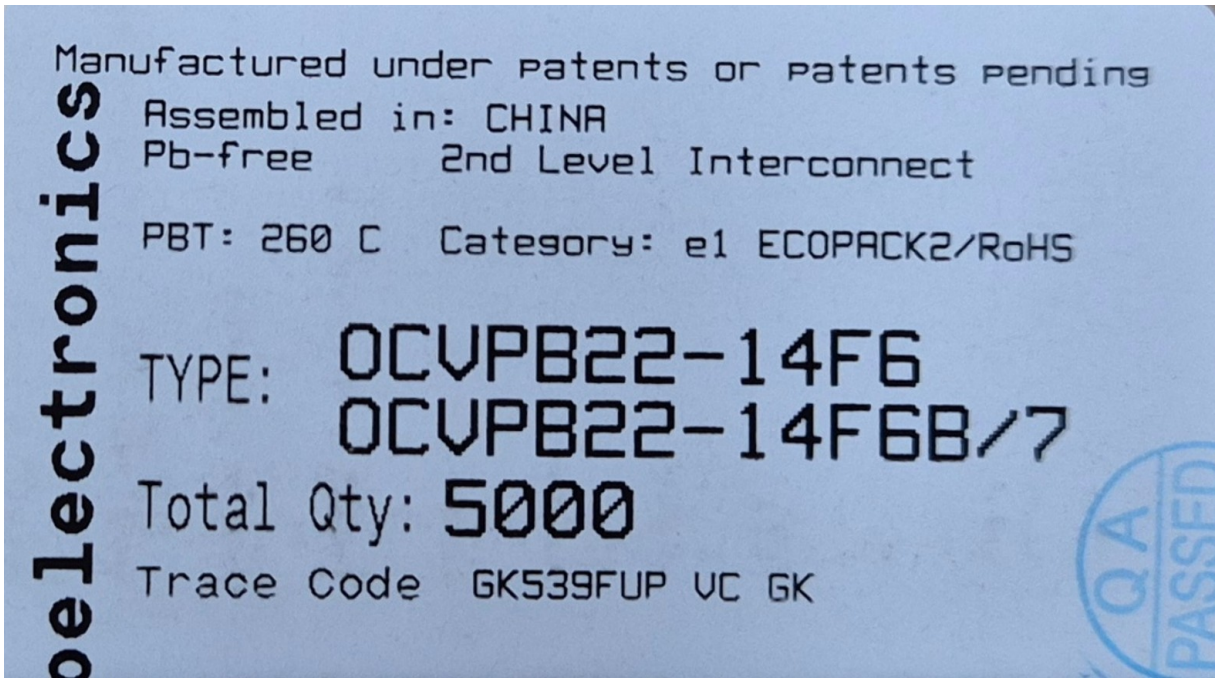
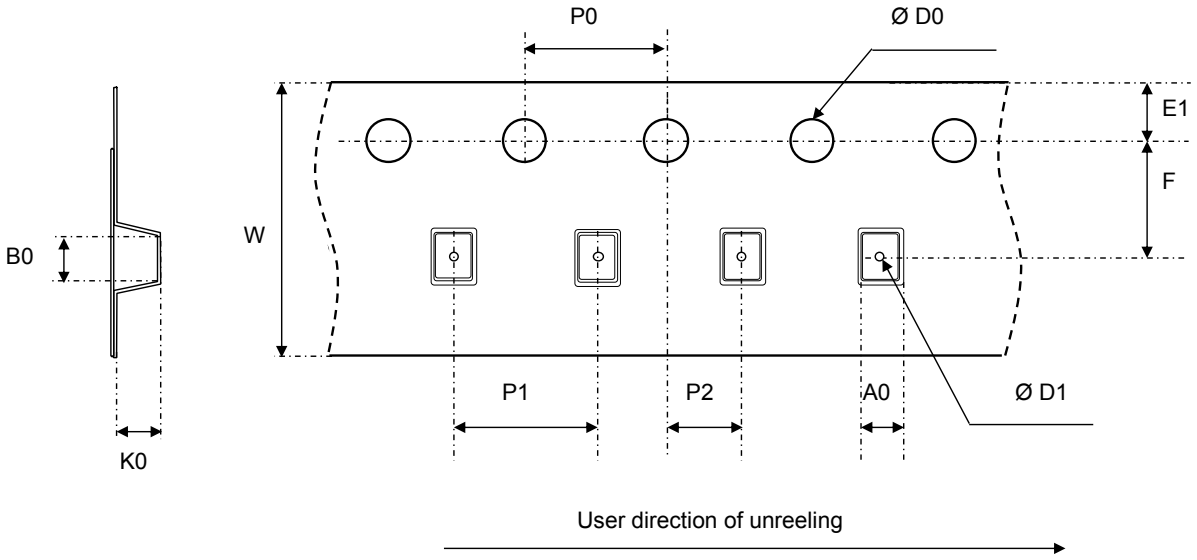


Figure 16. **WLCSP 14 bumps tape and reel specification (all dimensions in mm)**



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 9. **Tape and reel mechanical data**

Ref.	Dimensions (millimeters)		
	Min.	Typ.	Max.
A0	1.40	1.45	1.50
B0	2.61	2.66	2.71
D0	1.40	1.50	1.60
D1	0.55	0.60	0.65
E1	1.65	1.75	1.85
F	3.45	3.50	3.55
K0	0.63	0.68	0.73
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

4 Soldering assembly recommendations

4.1 PCB design recommendations for multi-bump Flip Chip

For optimum electrical performance and highly reliable solder joints, STMicroelectronics recommends the PCB design guidelines listed in Table 10.

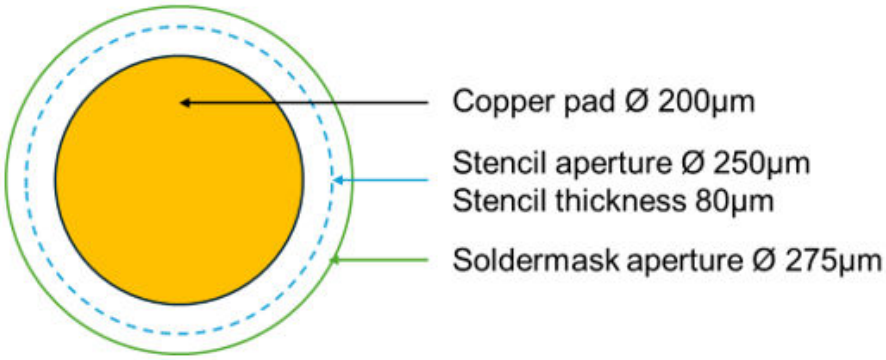
Table 10. PCB design recommendations for multi-bump Flip Chips

Name	Parameters
PCB pad design	Non solder mask defined micro via under bump allowed
PCB pad size	Ø = 200 µm (circular)
Solder mask opening	Ø = 275 µm
PCB pad finishing	Cu - Ni (2-6 µm) - Au (0.2 µm max) or Cu OSP (organic solderability preservative).

Note: A too thick gold layer finishing on the PCB pad is not recommended (low joint reliability)

To optimize the natural self-centering effect of Flip Chips on PCB, PCB pad positioning and size have to be properly designed (see Figure 17).

Figure 17. Flip-Chip bump footprint



4.2 PCB assembly guidelines

For WLCSP mounting on the PCB, STMicroelectronics recommends SAC alloys type 4 or 5 usage with No Clean flux type.

Recommended soldering reflow profile is shown in Figure 18.

Figure 18. ST ECOPACK recommended soldering reflow profile for Flip Chip mounting on PCB (definitions)

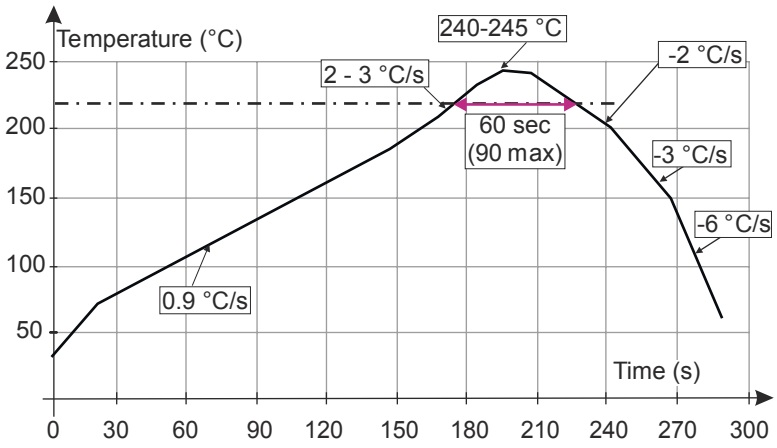


Table 11. ST ECOPACK recommended soldering reflow profile for Flip Chip mounting on PCB (value)

Profile	Value	
	Typ.	Max.
Temp. gradient in preheat (T = 70 – 180 °C)	0.9 °C/s	3 °C/s
Temp. Gradient (T = 200 – 225 °C)	2 °C/s	3 °C/s
Peak temp. in reflow	240 – 245 °C	260 °C
Time above 220 °C	60 s	90 s
Temp. gradient in cooling	-2 to -3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

4.3 Layout recommendations

Low impedance trace are recommended for IN_A, IN_B, OUT_5V GND_ESD, GND_DATA, and GND_BRIDGE to ensure layout optimization for ESD.

We recommend also to place C_{OUT} (see Table 2) as close as possible of OCVPB22-14F6.

To maximize current limit accuracy, we recommend also to place R_{LIM} (see Table 2) as close as possible of OCVPB22-14F6 (with Z < 500 mΩ).

Traces for USB data lines should be designed with 90 Ω differential impedances (USB_INC, USB_IND, USB_DP and USB_DM tracks).

5 Ordering information

Figure 19. **Ordering information scheme**

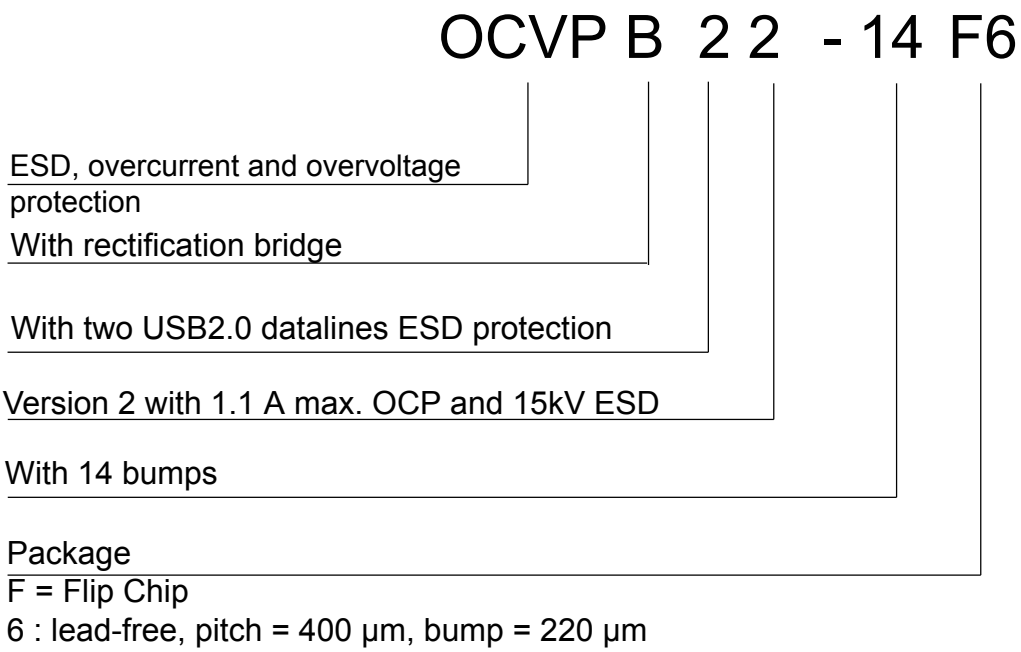


Table 12. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
OCVPB22-14F6	MMW0 OCV XXYY V2	WLCSP	3.7 mg	5000	Tape and reel

1. *XX YY: position of the die in the wafer, XX: column coordinate, YY: Row coordinate. Date code information available in trace code on labelling (see Figure 15).*

Note: More information is available in AN2348 application note :

- *STMicroelectronics 400 micro-meter Flip Chip: package description and recommendation for use.*

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
20-Jan-2026	1	Initial release.
22-Jun-2026	2	Updated confidentiality level to public.

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