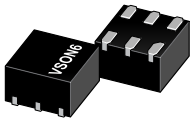
NMH1000

Datasheet

Magnetic switch



Features

- Threshold selection 3-state hardware pin
- Threshold selection data bit(s) in an I²C accessible register
- Sample rate selection 3-state hardware pin
- Sample rate selection data bit(s) in an I²C accessible register
- Mode selection hardware pin to select between standalone or I²C serial interface
- Mode selection data bit(s) in an I²C accessible register
- Two types of output indicate the absence of a magnetic field as compared to an internally set threshold:
  - Binary state hardware pin
  - Binary state data bit(s), configurable as assert-high or assert-low, in an I²C accessible register

Applications

- **Electronic system wake-up:** Detecting the proximity vs. lack of proximity to an included magnet when the electronics are removed from its delivery packaging, to wake up the electronics.
- **Laptop lid open / closed:** Detecting the proximity vs. lack of proximity to a magnet mounted to laptop lid, to trigger a status change, for example turn on / off the display.
- **Door or window open / closed:** Detecting the proximity vs. lack of proximity to a magnet mounted to a door, lid, or window, to trigger a status change, for example an alarm.

Description

The NMH1000 is a hall effect magnetic field switch. The switch is most sensitive to a vertical field passing through the top-to-bottom surfaces, orthogonal to the plane of the application printed circuit board. The switch operates at low voltage, low current, low output data rate, and is a small physical size.

Processing of input consists of functional blocks such as a configurable state machine, analog-to-voltage conversion of the input, and comparison to generate the bi-state output, arranged in linear succession.

1 Ordering information

Table 1. Ordering information

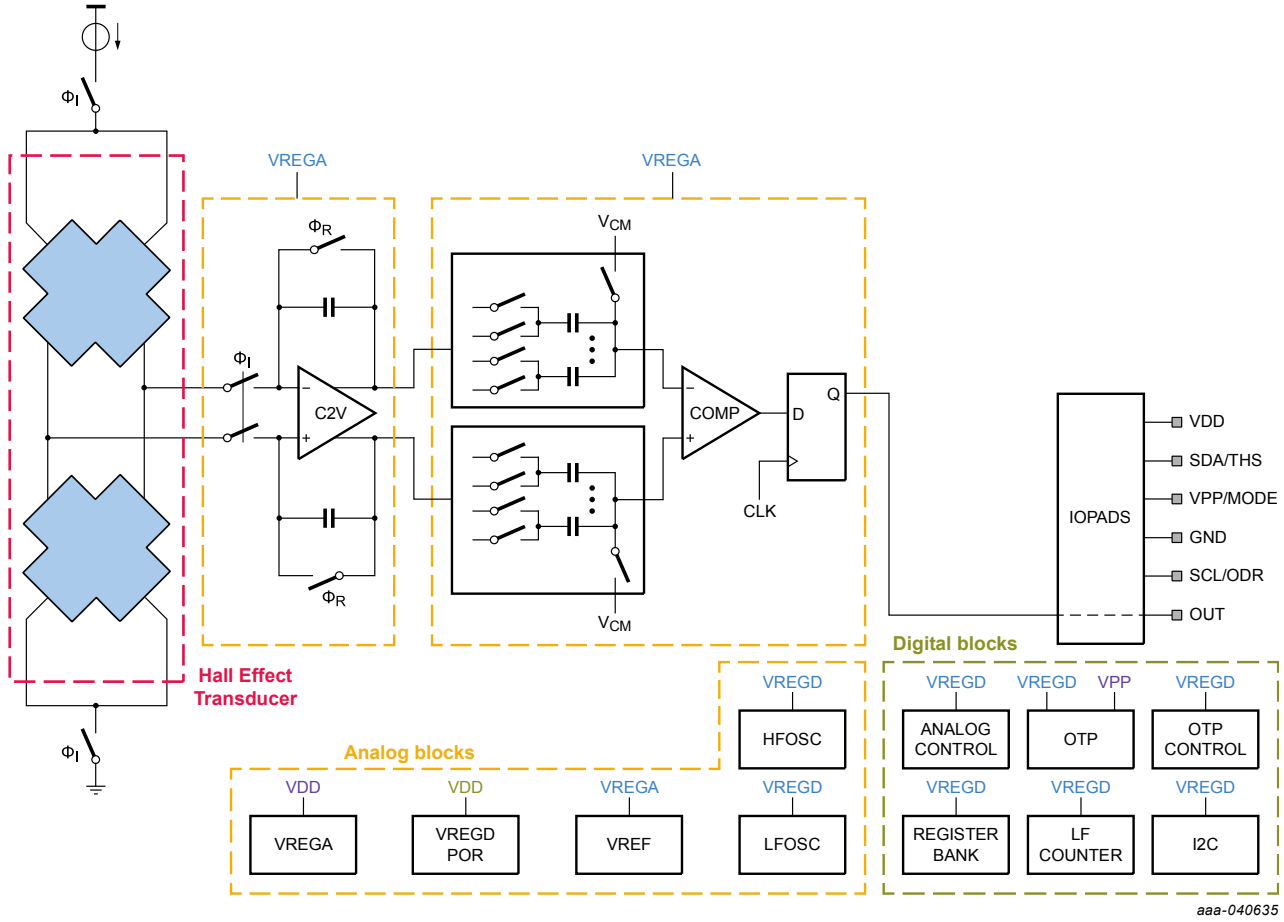
Type number	Package		
	Name	Description	Version
NMH1000	VSON	Very thin small outline package, no leads, 6 terminals, 0.5 mm pitch, 1.4 mm x 1.4 mm x 0.85 mm body	SOT2078-1

Refer to AN1902 [1] for additional information regarding use-case design and manufacturing recommendations.

2 Block diagram

The device consists of a monolithic die holding a Hall effect transducer, conversion, and comparison chain. Supporting blocks are described in Section 2.1: Block descriptions.

Figure 1. Block diagram



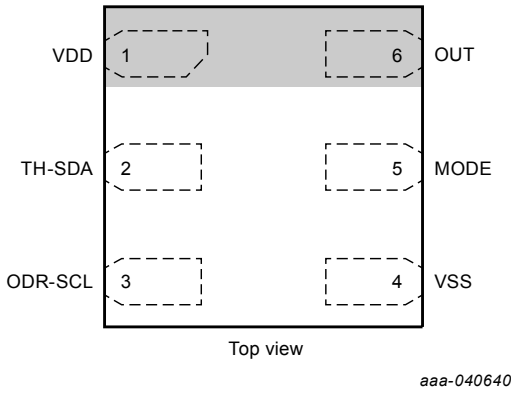
2.1 Block descriptions

- **Hall effect:** A transducer which generates a small charge which is proportional to the proximal magnetic flux density.
- **VREGA block:**
  - **C2V:** Converts the Hall effect charge to a voltage, which is stored onto the capacitor across the amplifier.
  - **Comparator:** Compares the voltage generated by the C2V with the pre-defined threshold voltage, then determines the state of the output Q, either Asserted or Cleared.
- **Analog blocks:**
  - **HF and LF Oscillator:** Configurable frequency (f_{HFO} and f_{LFO}) RC-Relaxation oscillators with independent trim bits for trimming.
  - **Regulators and references:** Regulators to step down the external supply for analog and digital circuits. Bandgap reference and current reference for biasing all analog module.
- **Digital blocks:**
  - **Analog control block:** Control signal generation for regulators and references, C2V, oscillators, comparator, for example, based on different operational modes.
  - **OTP:** A 16 x 8 bit array, it requires external V_{PPTM} for programming.
  - **OTP controller block:** Provides read and write control for OTP. All control signals needed by OTP are generated by this module.
  - **Register bank:** Provides the registers where users can write configurations or read status values.
  - **LF counter:** Counts the specific time depending on the sample rate (ODR) set by the user.
  - **I²C and test register block:** Includes the address decode logic and interrupt functions.

3 Pinning information

3.1 Pinning

Figure 2. Pin configuration



Note: Gray area denotes the end of the device where pin 1 is located.

3.2 Pin description

Package and pin assignments support the options of magnetic field threshold and sample rate selections, based on the voltage applied to the MODE pin, upon appropriate voltage applied to the V_{DD} pin, relative to the V_{SS} pin.

Table 2. Pin description

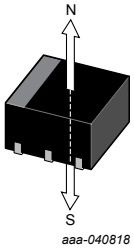
Symbol	Pin	Type	Description
V_{DD}	1	Supply	Main supply voltage
TH-SDA (1)	2	I/O	Standalone mode: Threshold I²C user mode: I²C serial data
ODR-SCL (2)	3	I	Standalone mode: Sample rate I²C user mode: I²C serial clock
V_{SS}	4	Ground	Main ground
MODE (3)	5	I	Selects between Standalone or I²C modes.
OUT (4)	6	O	Standalone mode: Output indicating absence of field

1. *Three states: low state for medium threshold B_O-M, open circuit for low threshold B_O-L, or high state for high threshold B_O-H, relative to V_{SS}*
2. *Three states: low state for medium sample rate f_{ODR}-M, open circuit for low sample rate f_{ODR}-L, or high state for high sample rate f_{ODR}-H, relative to V_{SS}*
3. *Two states: low state for standalone, high state for I²C User Mode, relative to V_{SS}*
4. *Two states: default assert for magnet not present, clear for magnet present, relative to V_{SS}*

3.3 Orientation

The device adheres to the convention of north magnetic field represented by positive/North polarity, orthogonal to the plane of the package body top surface and the arrows depict increasing strengths.

Figure 3. Magnetic field vs. package orientation



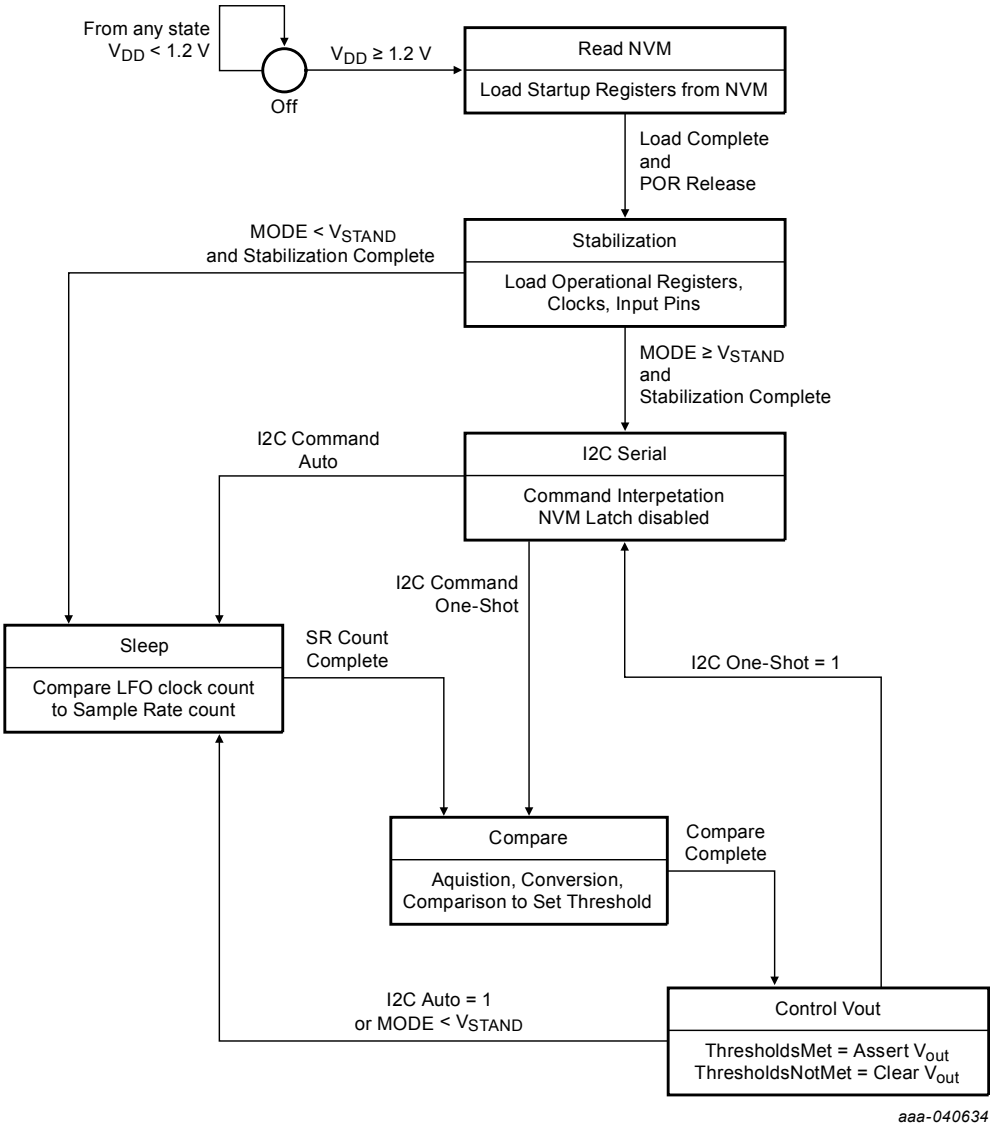
4 Functional description

4.1 Operating modes

4.1.1 Functional states

Figure 4 illustrates the functional states that the device transitions between.

Figure 4. NMH1000 functional state flow diagram



4.1.2 Interface Operational Modes

The NMH1000 operates under one of two modes when appropriately configured as described in the following sections:

- I²C user mode.
- Standalone mode.

Entry into each of the two user modes is initiated by the voltage existing at the MODE pin at the time of the V_{DD} pin rising above V_{DDMIN}, and followed by a read of NVM Start-up register(s), both relative to the V_{SS} pin:

- MODE < V_{STAND} results in the device entering standalone mode and forcing OPMODE to 0.
- MODE ≥ V_{STAND} results in the device entering I²C user mode and forcing OPMODE to 1.

Transition from I²C user mode to standalone mode is initiated by the host writing I2C_DIS to 1, which results in OPMODE being forced to 0.

Note: The device reloads the NVM into operating registers after t_{RLDS} seconds from final power application, needing a duration of t_{RLDC}.

4.2 Threshold configurations

4.2.1 Fixed thresholds

In standalone mode, fixed thresholds with fixed hysteresis are selected by voltage applied to V_{TH} pin relative to V_{SS} pin.

4.2.1.1 Fixed threshold selection via V_{TH} pin voltage

Table 3. Fixed threshold selection

V_{TH}	Threshold (1)
$V_{TH} < V_{BO}$-L	Medium magnetic field
V_{BO}-L ≤ V_{TH} ≤ V_{BO}-H	Low magnetic field
$V_{TH} > V_{BO}$-H	High magnetic field

1. See Table 27. Operating conditions.

4.2.2 User-defined threshold

In I²C mode, user-defined output assert threshold without hysteresis is selected by write to register bits, in units of BΔ in G/LSB:

Table 4. User-defined assert thresholds

USER_ASSERT_THRESH[7:3]	Assert Threshold (1) - B_{OA}
0 0 0 0 0	0 G
0 0 0 0 1	Lowest in-range magnetic field to assert the output
1 1 1 1 1	Highest in-range magnetic field to assert the output

1. See Section 7.6: I²C user mode, output assertion

In I²C mode, user-defined output clear threshold without hysteresis is selected by write to register bits, in units of BΔ in G/LSB:

Table 5. User-defined output clear thresholds

USER_CLEAR_THRESH[7:3]	Clear Threshold (1) - B_{OC}
0 0 0 0 0	0 G
0 0 0 0 1	Lowest in-range magnetic field to clear the output
1 1 1 1 1	Highest in-range magnetic field to clear the output

1. See Section 7.7: I²C user mode, output clear

Note: If the USER_ASSERT_THRESH and USER_CLEAR_THRESH are set too close in value to each other, the intended hysteresis may cause the output to change states at unintended magnetic field strengths, or may cause the output to not change states at intended magnetic field strengths.

Be aware of the minimum hysteresis noted in Table 32. Magnetic field characteristics.

4.3 Sample rate configurations

4.3.1 Fixed sample rates

In standalone mode, the sample rate is the selected voltage applied to V_{ODR} pin relative to V_{SS} pin.

4.3.1.1 Sample rate selection via V_{ODR} pin voltage

Table 6. Sample rate selection

V_{ODR}	Sample Rate (1)
$V_{ODR} < V_{fODR-L}$	f_{ODR}-M
$V_{fODR-L} \leq V_{ODR} \leq V_{fODR-H}$	f_{ODR}-L
$V_{ODR} > V_{fODR-H}$	f_{ODR}-H

1. See Section 7.2: Clocks and rates.

4.3.2 User-defined sample rate

In I²C mode, the user-defined sample rate is selected by a write to register bits:

Table 7. I²C mode user-defined sample rate

USER_ODR[2:0]	Sample Rate
0 0 0	f_{ODR}-L
0 0 1	5 x f_{ODR}-L
0 1 0	f_{ODR}-M
0 1 1	5 x f_{ODR}-M
1 0 0	f_{ODR}-H
1 0 1	5 x f_{ODR}-H
1 1 0	10 x f_{ODR}-H
1 1 1	config. error

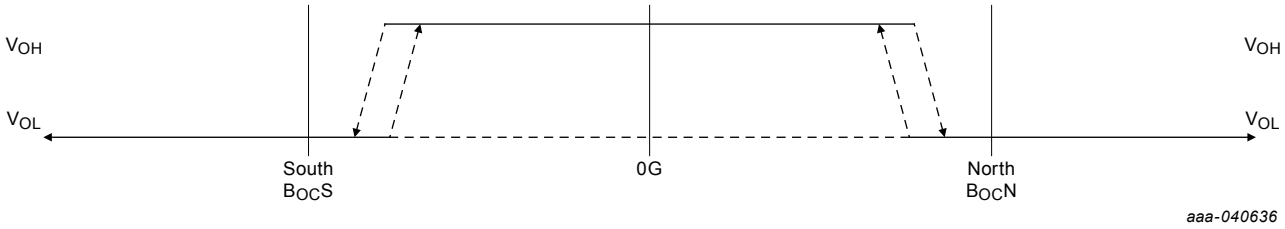
4.4 Output control function description

4.4.1 Output hysteresis

Hysteresis is implemented as the magnetic field difference between the output being cleared versus the output being asserted.

- In Standalone mode, the hysteresis is a fixed difference.
- In I²C mode with the selection of one of the three fixed thresholds, the hysteresis is a fixed difference, equal to the Standalone mode hysteresis.
- In I²C mode with customer selected thresholds, the hysteresis is the result of the customer choices of output Clear threshold versus output Assert threshold.

Figure 5. Output operation



4.4.2 Control Output State

4.4.2.1 Standalone mode output assert / clear states

In Standalone mode, the OUT pin asserts to high state upon the completion of the comparison stage, and the magnetic field is lower than the selected threshold Low, Medium, or High, minus the hysteresis.

In Standalone mode, the OUT pin is cleared to low state upon completion of the comparison stage, and the magnetic field is higher than the selected threshold Low, Medium, or High.

4.4.2.2 User-defined output assert / clear states

In I²C mode, the OUT pin and OUT-B register bit asserted and cleared states are selectable via the V_POL register bit.

Table 8. User-defined output assert and clear states

V_POL	OUT pin assert / clear state
0	OUT pin Assert = high / OUT pin Clear = low
1	OUT pin Assert = low / OUT pin Clear = high

4.5 I²C serial data function description

4.5.1 I²C pin functions

Two signals support the I²C-bus:

- Serial Clock Line - SCL.
- Serial Data line - SDA.

SCL is input and used for clocking the data into or out from the SDA data line.

SDA is bidirectional and used for sending and receiving the data.

When the bus is free, both the lines idle high.

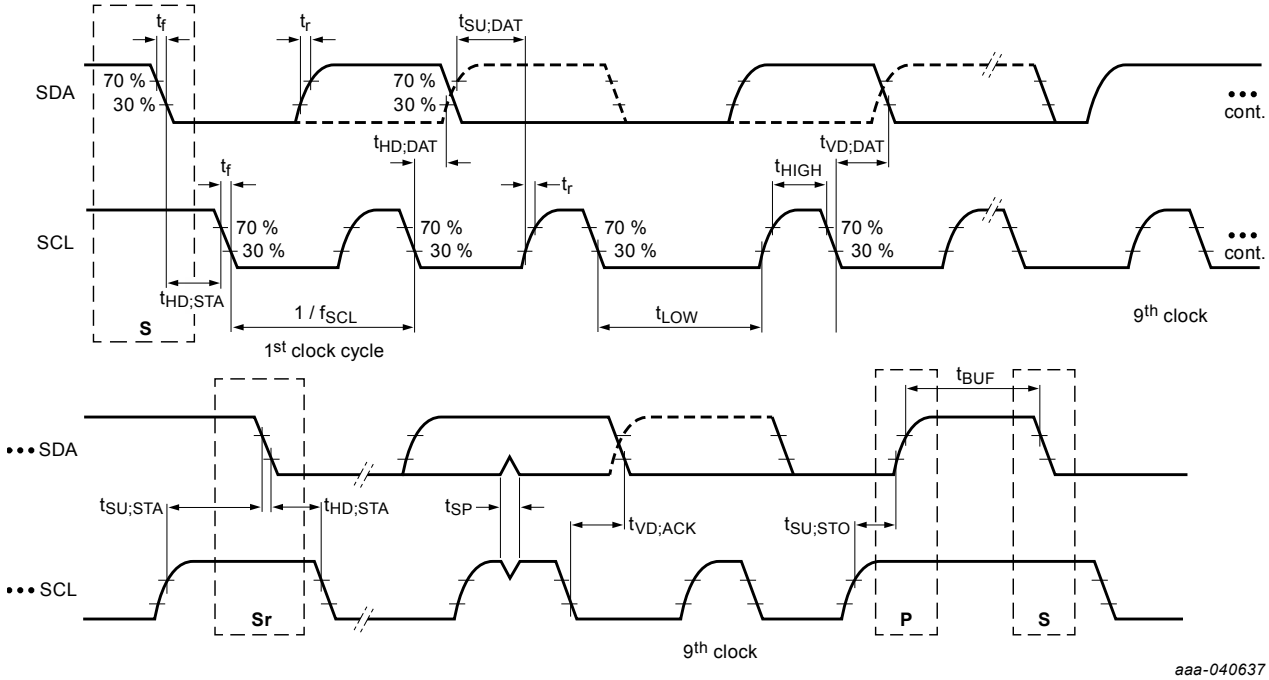
The I²C interface is compliant to the standard mode (100 kHz).

SDA and SCL both expect external pull-up resistors connected to V_{DD}.

- 1 kΩ minimum, board capacitance 20 pF maximum.

4.5.2 I²C timing diagram

Figure 6. I²C timing diagram



4.5.3 I²C operation

The I²C transaction on the bus is initiated through a start condition (START) signal. START signal is defined as a HIGH to LOW transition on the SDA line while the SCL line is held HIGH. After START is transmitted by the host, the bus is considered busy. The next byte of data transmitted after START contains the device address in the first seven bits, and the eighth bit indicates whether the host is receiving data from the device or transmitting data to the device. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the host. The ninth clock pulse, following the device address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low for it to remain stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited because the internal addressing wraps after $6D to $00, continuing to $6D again, then to $00, and so forth. The wrapping applies to both write transfers and read transfers. Note that usable addresses stop at $09, therefore a host may expect random values between $0A to $6D. If the host is unable to receive another complete byte of data until it has performed some other function, the host can hold the SCL line low, forcing the transmitter into a wait state. Data transfer continues only when the host is ready for another byte and releases the clock line.

A stop condition (STOP) is defined as a low to high transition on the SDA line while the SCL line is high. Data transfer is terminated by a STOP.

A host may also issue a RESTART during a data transfer. The device expects RESTARTs to randomly read from specific registers.

The bus logic of the device resets on receipt of a START, or RESTART condition. The device anticipates the sending of a device address, even if these START conditions are not positioned or follow proper format.

The device accepts the first bit of an address after each START, or RESTART condition.

The device detects when the SDA line is held low, and in such cases, releases the SDA line when the host issue no more than nine cycles of the SCL line.

The device determines the value in the NVM I²C address register. If the value is not $00, the device uses this address during I²C transactions. If the address register is $00, the address defaults to $60. The reset value of the I²C address register is also $60.

4.5.4 I²C protocol diagram

Figure 7. I²C write operation

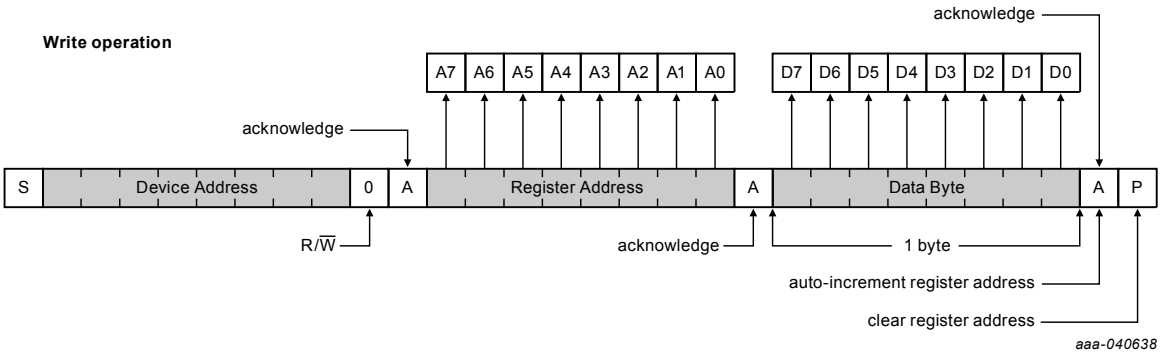
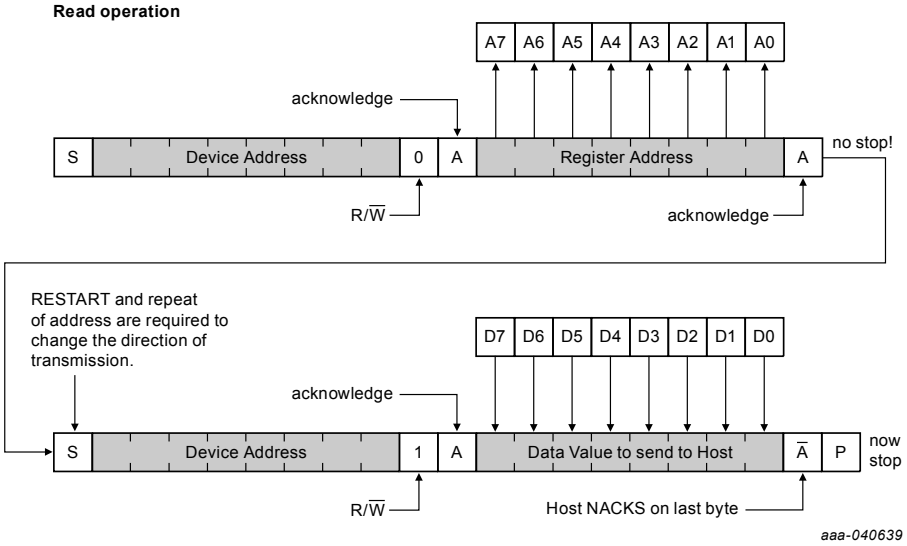


Figure 8. I²C read operation



4.6 Register map

4.6.1 Register overview

Table 9. Register map overview

Address	Name	Description	AO or S [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00	STATUS	Status reporting of modes and selections	S	OUTPUT	MDO	MDR	—	OPMODE	—	RST_STAT	OUT_B
$01	CONTROL_REG1	Control of Operations	S	—	—	V_POL	I2C_DIS	AUTO	ONE_SHOT	—	RST
$02	—	Reserved	—	—	—	—	—	—	—	—	—
$03	OUT_M_REG	Report of Magnetic Strength	S	MAG_DATA [7:2]						—	—
$04	USER_ASSERT_THRESH	User selectable output Assert threshold, N or S	AO	USER_ASSERT_THRESH [7:3]					Reserved		
$05	USER_CLEAR_ THRESH	User selectable output Clear threshold, N or S	AO	USER_CLEAR_THRESH [7:3]					Reserved		
$06	USER_ODR	User selectable sleep sample output data rates	AO	—	—	—	—	—	USER_ODR[2:0]		
$07	—	Reserved	—	—	—	—	—	—	—	—	—
$08	WHO_AM_I	I²C Configured Identifier	S	WHO_AM_I [7:0]							
$09	I2C_ADDR	I²C Configured Address - default after reset = $60	S	—	ADDR [6:0]						

1. *AO - Always On, S - Switched*

4.6.2 Register details

4.6.2.1 Status reporting of modes and selections (STATUS) ($00h)

Table 10. STATUS – Status reporting of modes and selections (address $00h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUTPUT	MDO	MDR	—	OPMODE	—	RST_STAT	OUT_B
Reset	0	1	1	—	1	—	1	x
Access	R/W	R/W	R/W	—	R/W	—	R/W	R/W

Table 11. STATUS – Status reporting of modes and selections (address $00h) bit descriptions

Bit	Symbol	Access	Value	Description
7	OUTPUT	R/W		V_{out} control block state. This bit follows the state of the OUT pin in either case of V_POL = 0 or 1.
			0	The state of VOUT is driven to low; Result of Reset.
			1	The state of VOUT is driven to high.
6	MDO	R/W		Magnetic data overwrite indicates the validity of the value in register $03. After asserting to 1, the MDO bit retains this value after the register $03 returns to the range of $00 to $1F, until a read operation is performed on register $00. The MDO reasserts if the register $03 is again > $1F.
			0	Register $03 value is within the range $00 to $1F.
			1	Register $03 value is >$1F indicates out-of-range or fault; Result of reset.
5	MDR	R/W		Magnetic data ready indicates the value in register $03 is available for read operation. After asserting to 1, the MDR bit retains this value after the register $03 becomes available, until a read operation is performed on register $00. The MDR reasserts if the register $03 is again not available.
			0	$03 data available.

Bit	Symbol	Access	Value	Description
5	MDR	R/W	1	$03 data not available; Result of reset.
3	OPMODE	R/W		The read-only OPMODE indicates the mode of the internal state-machine.
			0	Indicates VPP < VSTAND and the device in standalone mode indicating a state machine fault, since the registers are only accessible in the I²C mode.
			1	Indicates VPP ≥ VSTAND and the device in I²C user mode.
1	RST_STAT	R/W		Reset status indicates the state-machine reset sequence. RST_STAT set to 1 as the device enters POR or soft reset. This bit is cleared to 0 upon reading the register $00. After asserting to 1, the RST_STAT bit retains this value after the exit of POR or soft rest, until a read operation is performed on register $00. The RST_STAT reasserts if POR or soft reset is entered.
			0	Reset sequence complete and read operation performed on register $00.
			1	Reset sequence not complete; Result of reset.
0	OUT_B	R/W		Output buffer indicates a latched state of the OUT pin after a transition from either Asserted to Clear or Clear to Asserted. After asserting to 1, or clearing to 0, the OUT_B bit retains this value until a read operation is performed on register $00. This bit is intended to allow the user or tester to check for a transition while the actual OUT pin or OUTPUT bit may have changed state again between checks.
			0	OUT cleared on previous cycle.
			1	OUT asserted on previous cycle.

4.6.2.2 *Control of operations (CONTROL_Reg1) ($01h)*

Table 12. CONTROL_Reg1 – Control of operations(address $01h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	V_POL	I2C_DIS	AUTO	ONE_SHOT	—	RST
Reset	—	—	0	0	0	0	—	0
Access	—	—	R/W	R/W	R/W	R/W	—	R/W

Table 13. CONTROL_Reg1 – Control of operations (address $01h) bit description

Bit	Symbol	Access	Value	Description
5	V_POL	R/W		V_POL provides control of the user-defined OUT pin and resultant OUT_B register bit assert / clear polarity.
			0	Assert = out pin high, Clear = out pin low; Result of reset.
			1	Assert = out pin low, Clear = out pn high.
4	I2C_DIS	R/W		I2C_DIS provides control of the operating mode "on-the-fly" after the device exits POR or Soft Reset. I2C_DIS allows the user to force the device into standalone mode from the I²C mode. *Note: Writing 1 to I2C_DIS is a one-time-only operation. Bringing the device into I²C mode from standalone requires a full power cycle and release of POR.* *Note: MAG_DATA retains its last value, and is updated upon next write to ONE_SHOT.*
			0	Write to 0 has no effect; Read of 0 indicates I²C mode; Result of reset.
			1	Write to 1 forces the device from I²C mode to standalone mode; Read of 1 indicates a state machine fault, since the registers are only accessible in the I²C mode.
3	AUTO	R/W		AUTO provides control of the state machine to enter a sequential autonomous mode cycling from sleep to compare to Vout control, then back to sleep, for example. The sequence is halted when the AUTO is written to 0.
			0	Write to 0 halts or prevents autonomous mode; Read of 0 indicates that autonomous mode is not active; Result of reset.

Bit	Symbol	Access	Value	Description
3	AUTO	R/W	1	Write to 1 starts the autonomous mode; Read of 1 indicates that autonomous mode is active.
2	ONE_SHOT	R/W		ONE_SHOT provides control of the state machine to trigger a single sequence of compare to Vout control, then halt. The bit clears upon the sequence being completed.
			0	Write to 0 has no effect; Read of 0 indicates One-Shot is not active; Result of reset.
			1	Write to 1 triggers a one-shot sequence; Read of 1 has no effect.
				Note: The BUSY bit indicates that the sequence is underway or not completed. *Note: MAG_DATA retains its last value, and is updated upon next write to ONE_SHOT.*
0	RST	R/W		RST provides I²C access to force an internal device soft reset:
			0	No reset is forced.
			1	Internal device reset is forced.

4.6.2.3 *Magnetic strength report (OUT_M_REG) ($03h)*

Table 14. OUT_M_REG – Magnetic strength report (address $03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MAG_DATA [7:2]						reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Table 15. OUT_M_REG – Magnetic strength report (address $03h) bit description

Bit	Symbol	Access	Value	Description
7 to 2	MAG_DATA	R/W		MAG_DATA[7:2] indicates a relative magnetic field strength in units of BΔ in G/LSB.
			$00	0 G; Result of reset.
			$01	Lowest in-range magnetic field strength.
			$1F	Highest in-range magnetic field strength.

4.6.2.4 *User selectable output, assert threshold, N or S (USER_ASSERT_THRESH) ($04h)*

Table 16. USER_ASSERT_THRESH – User selectable output, assert threshold, N or S (address $04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USER_ASSERT_THRESH [7:3]					Reserved		
Reset	0	0	0	0	0	—	—	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 17. USER_ASSERT_THRESH – User selectable output, assert threshold, N or S (address $04h) bit description

Bit	Symbol	Access	Value	Description
7 to 3	USER_ASSERT_THRESH	R/W		In I²C mode, USER_ASSERT_THRESH[7:3] provides the capability for the user to override the fixed threshold controlling the output assert condition, in units of BΔ in G/LSB. *Note: Hysteresis is controlled by appropriate user settings for both USER_ASSERT_THRESH and USER_CLEAR_THRESH registers.*
			$00	0 G; Result of reset.

Bit	Symbol	Access	Value	Description
7 to 3	USER_ ASSERT_ THRESH	R/W	$01	Lowest in-range magnetic field to assert the output.
			$1F	Highest in-range magnetic field to assert the output.

4.6.2.5 *User selectable output, clear threshold, N or S (USER_CLEAR_THRESH) ($05h)*

Table 18. USER_CLEAR_THRESH – User selectable output, clear threshold, N or S (address $05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USER_CLEAR_THRESH [7:3]					Reserved		
Reset	0	0	0	0	0	—	—	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 19. USER_CLEAR_THRESH – User selectable output, clear threshold, N or S (address $05h) bit description

Bit	Symbol	Access	Value	Description
7 to 3	USER_ CLEAR_ THRESH	R/W		In I²C mode, USER_CLEAR_THRESH[7:3] provides the capability for the user to override the fixed threshold controlling the output clear condition, in units of BΔ in G/LSB. *Note: Hysteresis is controlled by appropriate user settings for both USER_ASSERT_THRESH and USER_CLEAR_THRESH registers.*
			$00	0 G; Result of reset.
			$01	Lowest in-range magnetic field to clear the output.
			$1F	Highest in-range magnetic field to clear the output.

4.6.2.6 *User selectable sleep sample output data rates (USER_ODR) ($06h)*

Table 20. USER_ODR – User selectable sleep sample output data rates (address $06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	—	—	—	USER_ODR[2:0]		
Reset	—	—	—	—	—	0	0	0
Access	—	—	—	—	—	R/W	R/W	R/W

Table 21. USER_ODR – User selectable sleep sample output data rates (address $06h) bit description

Bit	Symbol	Access	Value	Description
2 to 0	USER_ODR	R/W		In I²C mode, USER_ODR[2:0] provides the capability for the user to override the fixed sample rate controlling the sleep-compare-Vout cycle time.
			0 0 0	Low sample rate selected.
			0 0 1	5 x Low sample rate selected.
			0 1 0	Medium sample rate selected.
			0 1 1	5 x Medium sample rate selected.
			1 0 0	High sample rate selected.
			1 0 1	5 x High sample rate selected.
			1 1 0	10 x High sample rate selected.
			1 1 1	Configuration error.

4.6.2.7 I²C configured identifier (WHO_AM_I) ($08h)

Table 22. WHO_AM_I - I²C configured identifier (address $08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WHO_AM_I [7:0]							
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 23. WHO_AM_I - I²C configured identifier (address $08h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	WHO_AM_I	R/W		WHO_AM_I[7:0] provides the device identification register. The value is programmed in the NVM at final test. Each variation has its own unique device ID.
			$00	WHO_AM_I error condition.
			$01	Generic open market default value.
			$02 to $FE	Customer defined unique values.
			$FF	WHO_AM_I not programmed.

4.6.2.8 I²C configured identifier (I2C_ADDR) ($09h)

Table 24. I2C_ADDR - I²C configured identifier (address $09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	I2C_ADDR [6:0]						
Reset	—	1	1	0	0	0	0	0
Access	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25. I2C_ADDR - I²C configured identifier (address $09h) bit description

Bit	Symbol	Access	Value	Description
6 to 0	I2C_ADDR	R/W		I2C_ADDR[6:0] is register mapped and loaded by default value $60 at boot time. After that, users may write any non-zero value to it. This non-zero value is used until the device is reset. If the device is reset, the same default value of $60 is reloaded and used again.
				$60 = default loaded at exit of reset.
				$00 = lowest address value.
				$7F = highest address value.

5 Limiting values

Table 26. Limiting values

Symbol	Description	Condition	Min	Typ	Max	Unit
B_G	Magnetic field	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	—	Not limited	G (Gauss)
V_{SUP}	V_{DD} to V_{SS} range	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	–0.3	—	3.6	V
V_{IO}	IO pin voltage, each pin vs V_{DD} / V_{SS}	T_A Min ≤ T_A ≤ T_A Max	V_{SS} – 0.3	—	V_{SUP} + 0.3	V
I_{IO}	IO pin current, each pin vs V_{DD} / V_{SS}	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	–10	—	10	mA
I_{SUBIO}	Substrate current injection, all IO pins, current from pin to V_{SS} – 0.3 V	T_A Min ≤ T_A ≤ T_A Max, VDD Min ≤ VDD ≤ VDD Max	—	100	—	mA
I_{LATCH}	Latch-up current, current to/from pin to V_{DD}/V_{DDA} + 0.3 V	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	–100	—	100	mA
ESD_{HBM}	Electrostatic discharge, Human Body Model (HBM) all pins	T_A = 25 °C, V_{DD} = 1.5 V	–2000	—	2000	V
ESD_{CDM}	Electrostatic discharge, Charged Device Model (CDM) all pins	T_A = 25 °C, V_{DD} = 1.5 V	–500	—	500	V
EOS_{EMIR}	Conducted immunity DPI, until OUT unintentionally changes state or I²C corruption	T_A = 25 °C, V_{DD} = 1.5 V	—	30	—	dBm
T_{STG}	Unpowered storage temperature range	—	–40	—	150	°C

6 Recommended operating conditions

Table 27. Operating conditions

Symbol	Description	Condition	Min	Typ	Max	Unit
Transitions						
t_{OP}	Power-on initialization	From V_{DD} > 1.2 V to Operation Ready; 25 °C and 1.5 V.	—	4.8	5.1	ms
t_{BOC-A}	Cleared state to Asserted state phase delay	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	100	—	µs
Voltages						
V_{DD}	Operating voltage range where Min = V_{DD} Min, Typ = 1.5 V, Max = V_{DD} Max	T_A Min ≤ T_A ≤ T_A Max	1.2	1.5	V_{SUP}	V
V_{STAND}	MODE pin voltage - Standalone mode	T_A = 25 °C, V_{DD} = 1.5 V	V_{SS} – 0.3	—	0.3 x V_{DD}	V
V_{STAND}	Mode pin voltage - I²C mode	T_A = 25 °C, V_{DD} = 1.5 V	0.7 x V_{DD}	—	V_{DD} + 0.3	V
V_{TH}	TH-SDA pin - Standalone mode, Low threshold	TA Min ≤ TA ≤ TA Max, VDD Min ≤ VDD ≤ VDD Max	0.4 x V_{DD}	0.5 x V_{DD}	0.6 x V_{DD}	V
V_{TH}	TH-SDA pin - Standalone mode, Medium threshold	TA Min ≤ TA ≤ TA Max, VDD Min ≤ VDD ≤ VDD Max	—	—	0.3 x V_{DD}	V
V_{TH}	TH-SDA pin - Standalone mode, High threshold	TA Min ≤ TA ≤ TA Max, VDD Min ≤ VDD ≤ VDD Max	0.7 x V_{DD}	—	—	V
V_{ODR}	ODR-SCL pin - Standalone mode, Low sample rate	TA Min ≤ TA ≤ TA Max, VDD Min ≤ VDD ≤ VDD Max	0.4 x V_{DD}	0.5 x V_{DD}	0.6 x V_{DD}	V
V_{ODR}	ODR-SCL pin - Standalone mode, Medium sample rate	TA Min ≤ TA ≤ TA Max, VDD Min ≤ VDD ≤ VDD Max	—	—	0.3 x V_{DD}	V
V_{ODR}	ODR-SCL pin - Standalone mode, High sample rate	TA Min ≤ TA ≤ TA Max, VDD Min ≤ VDD ≤ VDD Max	0.7 x V_{DD}	—	—	V
Temperatures						
T_A	Operating temperature range where Min = T_A Min, Typ = 25 °C, Max = T_A Max	V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	–40 °C	25	+85	°C

7 Characteristics

7.1 Supply currents

Table 28. Supply currents

Symbol	Description	Condition	Min	Typ	Max	Unit
$I_{DDS-LODR}$	Supply current, Low ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the Low ODR stand-alone mode.	—	47.5	187	nA
$I_{DDS-MODR}$	Supply current, Medium ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the Medium ODR stand-alone mode	—	72.2	234	nA
$I_{DDS-HODR}$	Supply current, High ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the High ODR stand-alone mode.	—	319.6	760	nA
I_{DDS-S}	Supply current, Sleep mode	Typ = 25 °C, V_{DD} = 1.5 V Max = T_A Min to T_A Max and V_{DD} Min to V_{DD} Max	—	42	300	nA
I_{DDS-M}	Supply current, measurement	Typ = 25 °C, V_{DD} = 1.5 V Max = T_A Min to T_A Max and V_{DD} Min to V_{DD} Max	—	580	650	µA
I_{DDS-2}	Supply current, I²C command/ response	Typ = 25 °C, 1.5 V, Max = T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	35	45	µA

7.2 Clocks and rates

Table 29. Clocks and rates

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{LFO}	Low frequency oscillator	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	2.8	3.2	3.5	kHz
f_{HFO}	High frequency oscillator	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	1.7	2	2.3	MHz
f_{SCL}	I²C input clock	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	—	1	MHz
f_{ODR-H}	Sample rate - High	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	10	—	Hz
f_{ODR-M}	Sample rate - Medium	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	1	—	Hz
f_{ODR-L}	Sample rate - Low	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	0.1	—	Hz

7.3 I²C pin thresholds

Table 30. I²C pin thresholds

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{IH}	Digital high-level input voltage	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max at I_{IH} max	0.7 x V_{DD}	—	V_{DD} + 0.3	V
V_{IL}	Digital low-level input voltage	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max at I_{IL} Max	V_{SS} – 0.3	—	0.3 x V_{DD}	V
V_{OH}	Digital high-level output voltage	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max at I_{OH} Max	V_{DD} – 0.3	—	—	V
V_{OL}	Digital low-level output voltage	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max at I_{OL} Max	—	—	V_{SS} + 0.3	V
I_{pin}	Digital pin current	T_A = 25 °C, V_{DD} = 1.5 V		—	±10	mA

7.4 Serial data timing characteristics

Table 31. Serial data timing characteristics

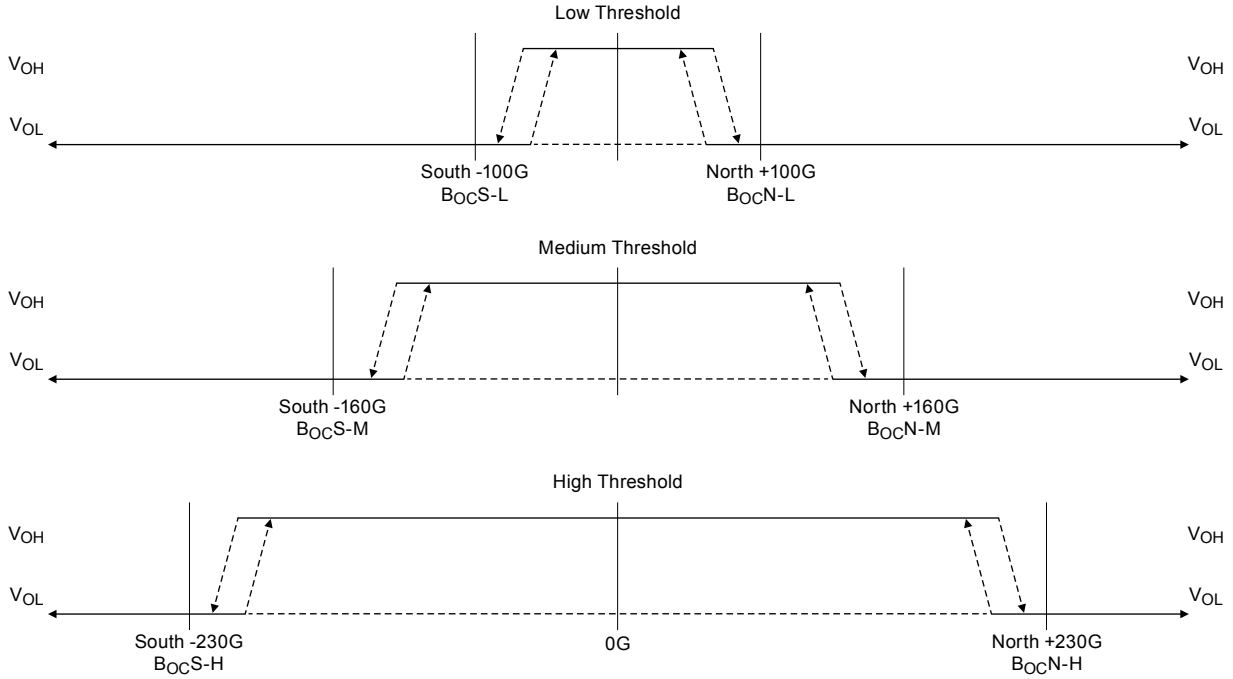
Symbol	Description	Condition	Min	Typ	Max	Unit
C_B	Board capacitive load SDA, SCL	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	—	1	µF
t_{BUF}	Bus free time, between stop and start	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	4.7	—	—	µs
t_{HD} to t_{STA}	Restart hold, after this period the first clock may be generated	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	4.0	—	—	µs
t_{SU} to t_{STA}	Restart setup	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	4.7	—	—	µs
t_{SU} to t_{STO}	Stop setup	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	4.0	—	—	µs
t_{HD} to t_{DAT}	SDA hold	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	300	—	—	ns
t_{SU} to t_{DAT}	SDA setup	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	250	—	—	ns
t_{LOW}	SCL low	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	4.7	—	—	µs
t_{HIGH}	SCL high	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	4.0	—	—	µs
t_r	SDA and SCL rise	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	—	1000	ns
t_f	SDA and SCL fall	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	—	300	ns

7.5 Magnetic field characteristics

Table 32. Magnetic field characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
Transfer Function						
BΔ	Sensitivity	T_A = 25 °C, V_{DD} = 1.5 V	—	1.75	—	G/LSB
B_{off}	Offset	T_A = 25 °C, V_{DD} = 1.5 V	—	0	—	G
Bhyst	Assert - Clear hysteresisa	T_A = 25 °C, V_{DD} = 1.5 V	20	—	—	G
BOC_{x-L}	OUT pin transition, Low threshold	T_A - 25 °C, V_{DD} = 1.5 v	—	—	±100	G
BOC_{x-M}	OUT pin transition, Medium threshold	T_A - 25 °C, V_{DD} = 1.5 v	—	—	±160	G
BOC_{x-H}	OUT pin transition, High threshold	T_A - 25 °C, V_{DD} = 1.5 v	—	—	±230	G

Figure 9. Output operation at each of the three standalone threshold settings



aaa-050608

7.6 I²C user mode, output assertion

Table 33. I²C user mode, recommended lowest USER_ASSERT_THRESH [7:3] output assertion

Symbol	Description	Condition	Min	Typ	Max	Unit
B_{OA}-I2C	Output assertion, magnetic field collapsing	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	< 0x10	—	hex

7.7 I²C user mode, output clear

Table 34. **I²C user mode, recommended highest USER_CLEAR_THRESH [7:3] output clear**

Symbol	Description	Condition	Min	Typ	Max	Unit
B_{OC}-I2C	Output clear, magnetic field increasing	T_A Min ≤ T_A ≤ T_A Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	> 0xF0	—	hex

8 Application information

Figure 10. **Standalone mode, Low threshold, High sample rate**

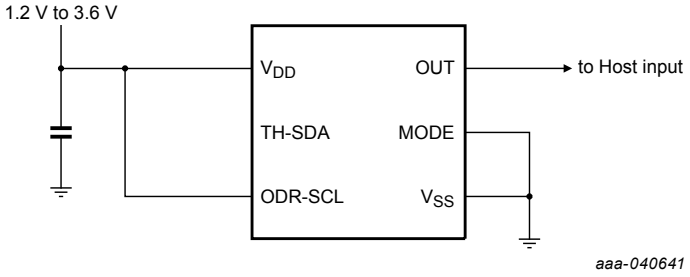


Figure 11. **Standalone mode, Medium threshold, High sample rate**

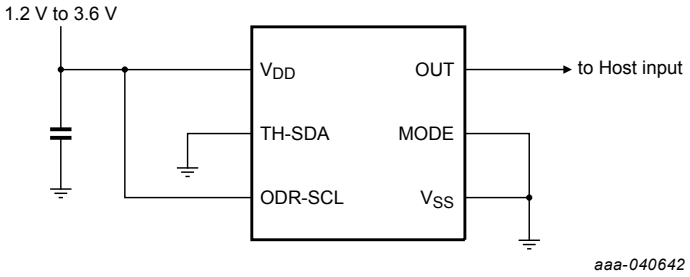


Figure 12. **Standalone mode, High threshold, High sample rate**

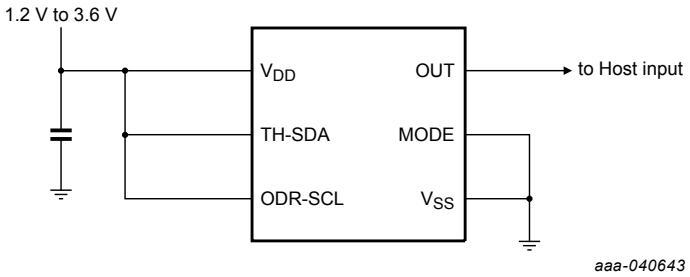


Figure 13. **Standalone mode, Low threshold, Medium sample rate**

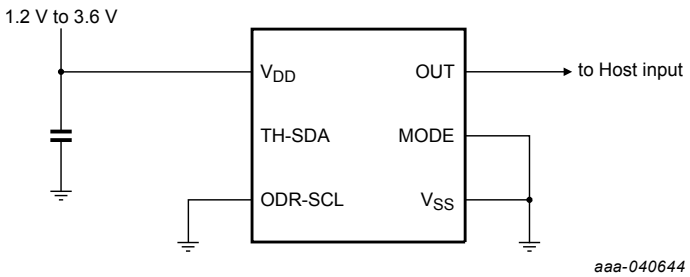


Figure 14. **Standalone mode, Medium threshold, Medium sample rate**

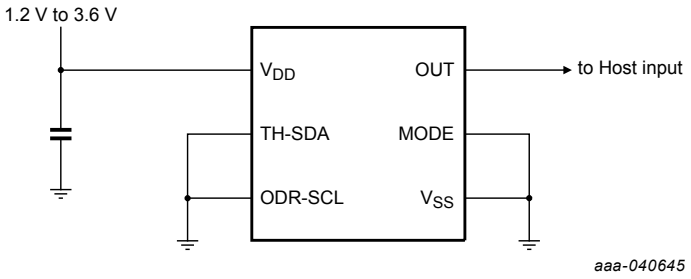


Figure 15. **Standalone mode, High threshold, Medium sample rate**

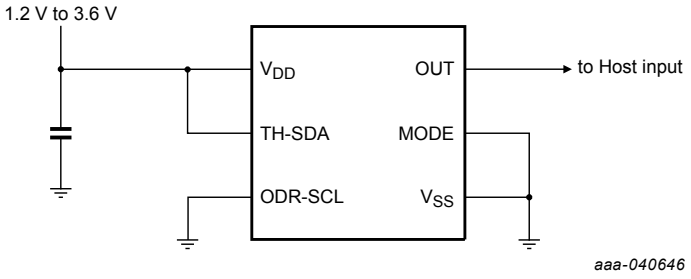


Figure 16. **Standalone mode, Low threshold, Low sample rate**

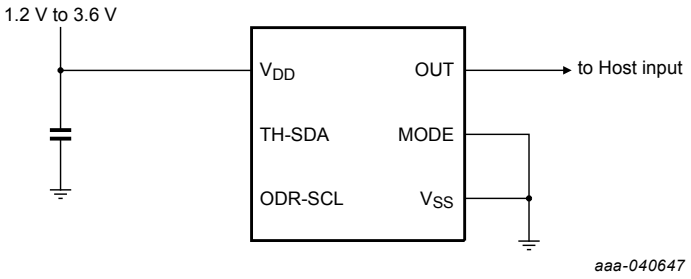


Figure 17. **Standalone mode, Medium threshold, Low sample rate**

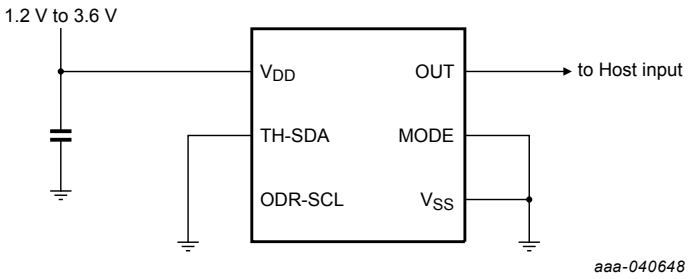


Figure 18. **Standalone mode, High threshold, Low sample rate**

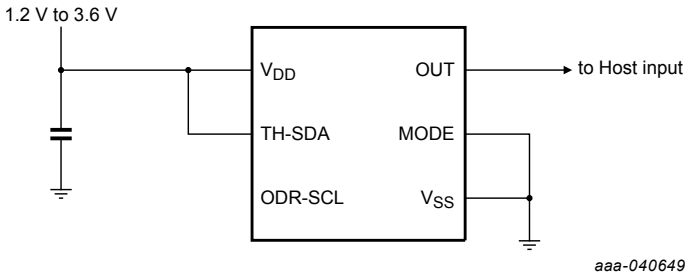
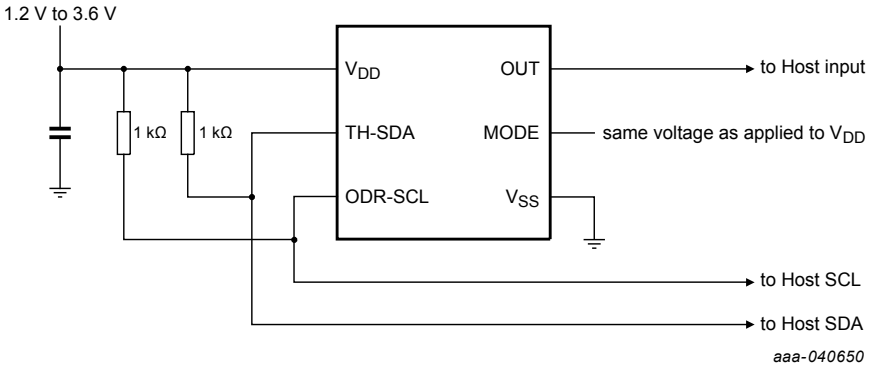


Figure 19. **I²C mode**



9 Package outline

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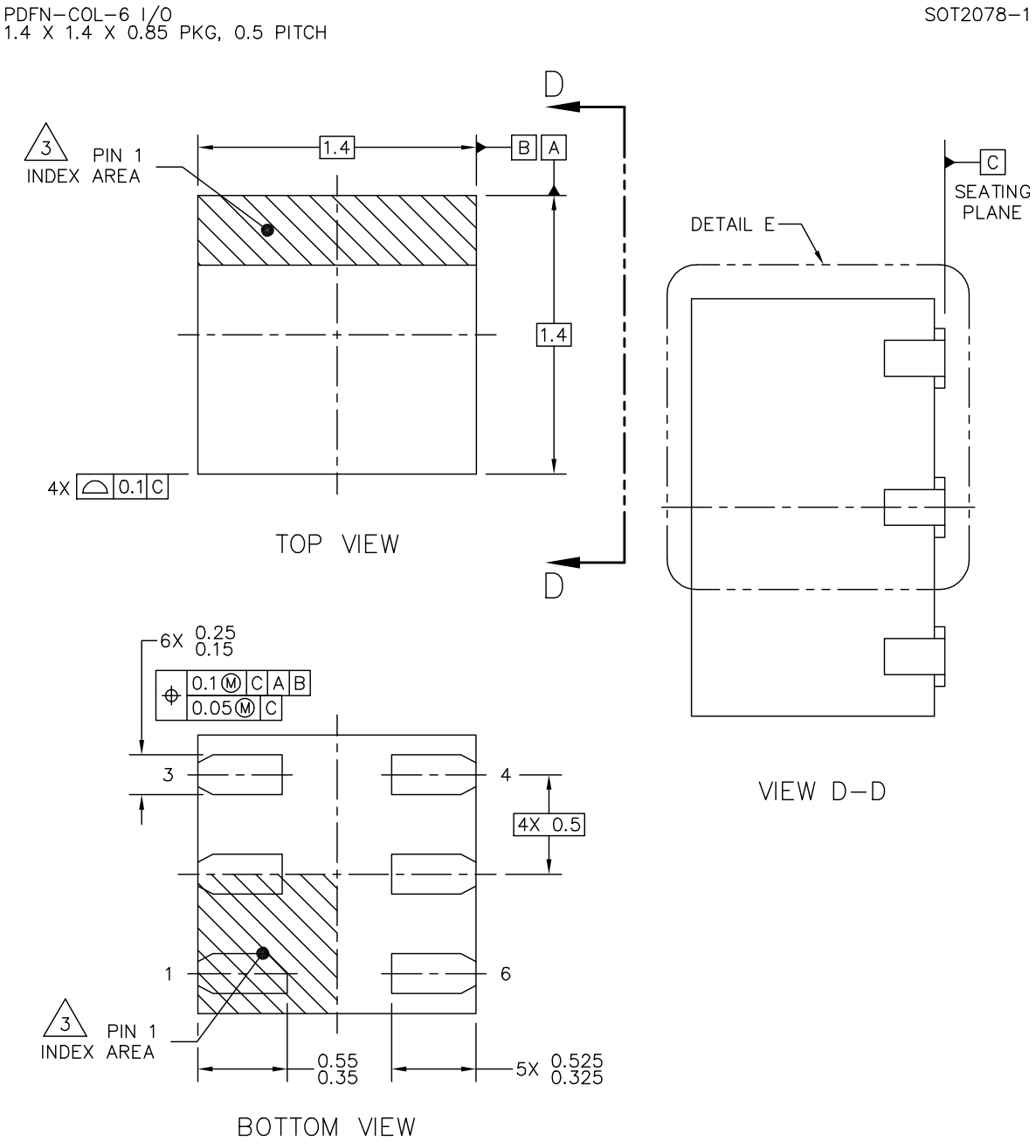
Figure 20. Package outline VSON6 (SOT2078-1)



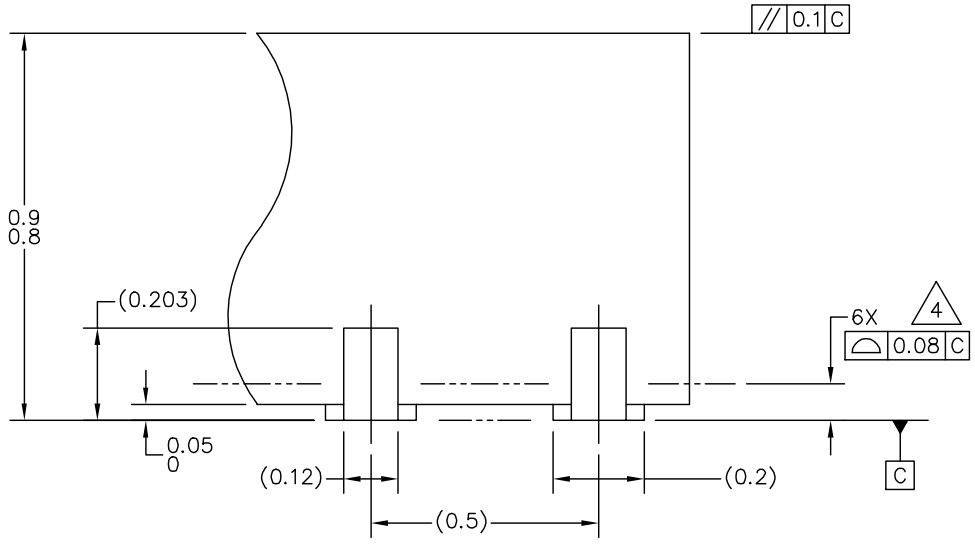
DATE: 26 AUG 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01688D	REVISION: O	PAGE:

Figure 21. Package outline detail of VSON6 (SOT2078-1)

PDFN−COL−6 I/O
1.4 X 1.4 X 0.85 PKG, 0.5 PITCH

SOT2078−1



DETAIL E
VIEW ROTATED 90°CW

DATE: 26 AUG 2020

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Figure 22. Package outline note VSON6 (SOT2078-1)

PDFN−COL−6 I/O
1.4 X 1.4 X 0.85 PKG, 0.5 PITCH

SOT2078−1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS.
5. MIN. METAL GAP SHOULD BE 0.15 MM.

DATE: 26 AUG 2020

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10 Soldering information

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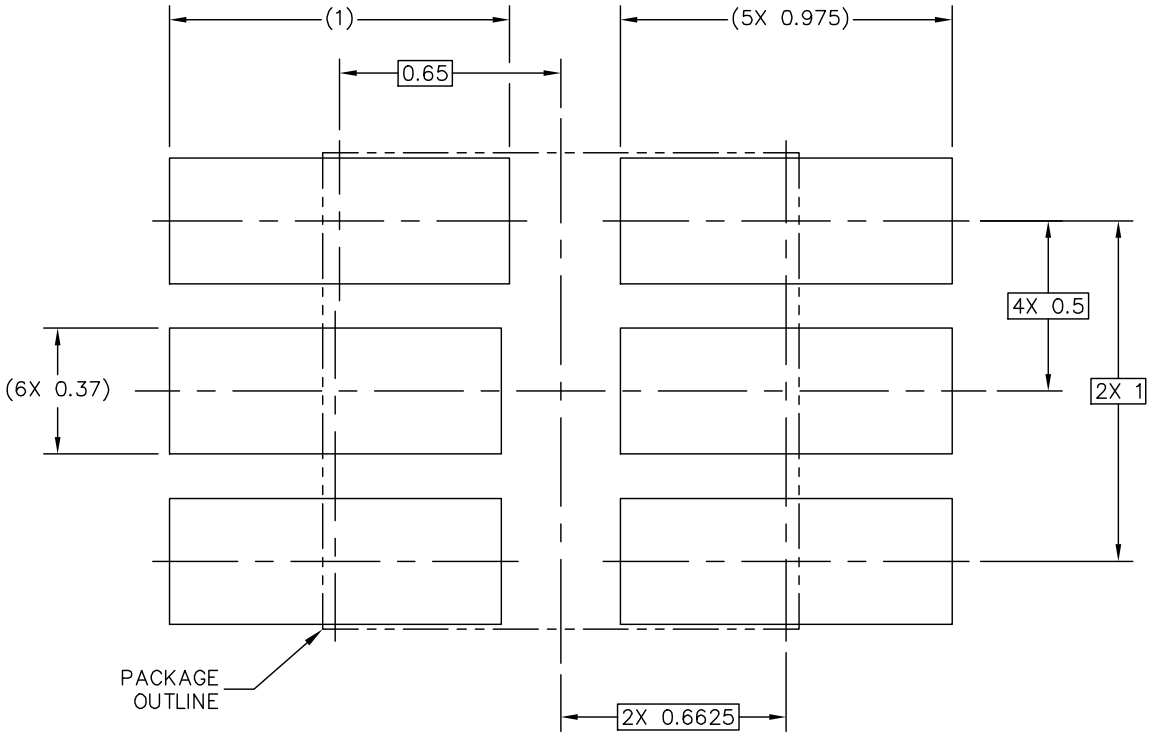
Figure 23. Reflow soldering footprint part 1 for VSON6 (SOT2078-1)

PDFN−COL−6 I/O
1.4 X 1.4 X 0.85 PKG, 0.5 PITCH

SOT2078−1



PCB DESIGN GUIDELINES − SOLDER MASK OPENING PATTERN

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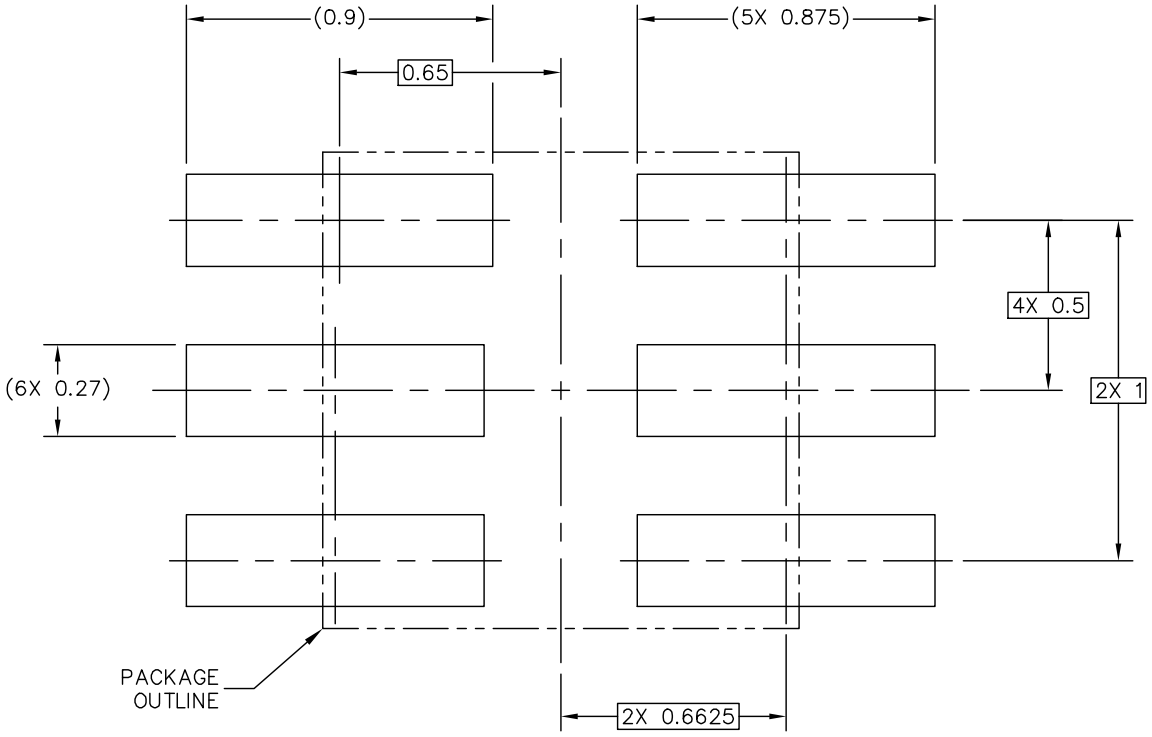
Figure 24. Reflow soldering footprint part 2 for VSON6 (SOT2078-1)

PDFN−COL−6 I/O
1.4 X 1.4 X 0.85 PKG, 0.5 PITCH

SOT2078−1



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DATE: 26 AUG 2020

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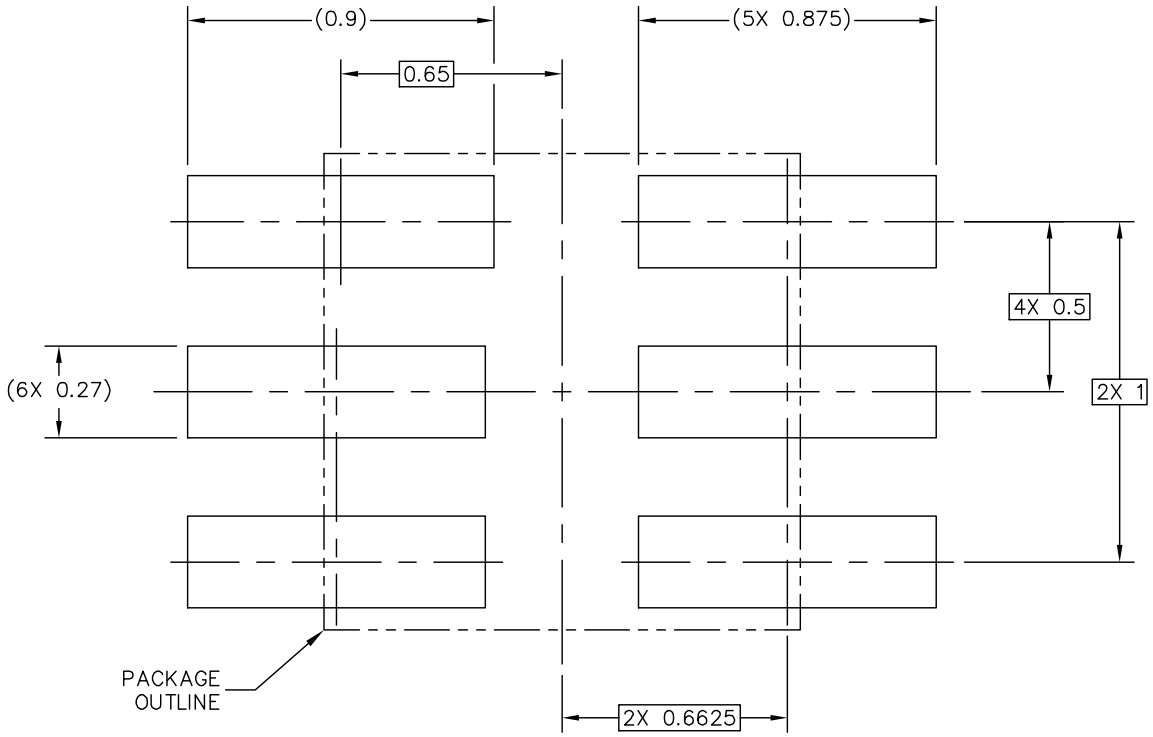
Figure 25. Reflow soldering footprint part 3 for VSON6 (SOT2078-1)

PDFN−COL−6 I/O
1.4 X 1.4 X 0.85 PKG, 0.5 PITCH

SOT2078−1



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES − SOLDER PASTE STENCIL

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DATE: 26 AUG 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01688D	REVISION: O	PAGE:

11 References

[1] AN1902 — Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages
https://www.nxp.com/docs/en/application-note/AN1902.pdf

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Revision history

Table 35. **Document revision history**

Date	Version	Changes
01-Feb-2026	1	Initial release from ST, rebranded NXP document

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List of figures

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