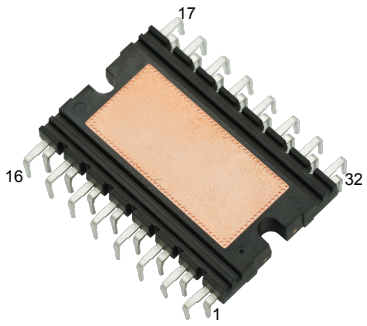
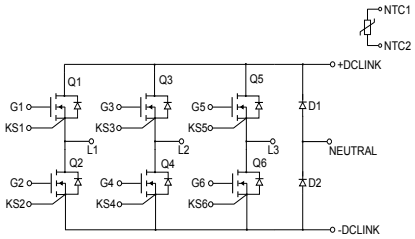
M2TP80M12W2-2LA

Datasheet

Automotive-grade ACEPACK DMT-32 power module, 3-phase four wire PFC topology, 1200 V, 84 mΩ typ. SiC Power MOSFET with rectifier diode and NTC



ACEPACK DMT-32
zig-zag



Features

- AQG 324 qualified
- 3-phase four wire PFC
  - 1200 V, 84 mΩ typ. SiC MOSFET (Q1, Q2, Q3, Q4, Q5, Q6)
  - 1200 V, 20 A rectifier diode (D1, D2)
  - Integrated NTC temperature sensor
- Maximum operating junction temperature T_J = 175 °C
- DBC Cu-AlN-Cu based substrate to improve thermal performance
- Isolation voltage 3.5 kV
- Zig-zag pin out

Applications

- On board charger (OBC)

Description

This ACEPACK DMT-32 power module realizes a 3-phase four wire PFC topology with integrated NTC, tailored for the PFC stage of the OBC in hybrid and electric vehicles. The power module features six silicon carbide Power MOSFETs of 2nd generation from STMicroelectronics. Thanks to the well-recognized chip technology, the ACEPACK DMT-32 ensures the best compromise between energy losses and high switching frequency operation mode. This module allows you to create complex topologies with very high power densities as well as high efficiency requirements. The AlN insulated substrate enables optimal thermal performance. Moreover, thanks to the specific design featuring grooves on the molding ensure a high creepage distance.

The zig-zag pin option improves the flexibility at PCB level.

Product status link
M2TP80M12W2-2LA

Product summary	
Order code	M2TP80M12W2-2LA
Marking	M2TP80M12W2-2LA
Package	ACEPACK DMT-32 zig-zag
Packing	Tube

1 SiC Power MOSFET (Q1, Q2, Q3, Q4, Q5, Q6)

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating values)	-5 to 18	
I_D	Drain current (continuous) at T_C = 50 °C	30	A
I_{DM}(1)	Drain current (pulsed, t_p = 1 ms)	58	A
T_J	Operating junction temperature range	-40 to 175	°C

1. *Pulse width is limited by safe operating area.*

Table 2. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 18 V, I_D = 20 A		84	114	mΩ
		V_{GS} = 18 V, I_D = 20 A T_J = 175 °C		178		
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	1.9	3.2	5	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1200 V			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±100	nA
C_{iss}	Input capacitance	V_{DS} = 800 V, f = 1 MHz, V_{GS} = 0 V		1230		pF
C_{oss}	Output capacitance			56		pF
C_{rss}	Reverse transfer capacitance			15		pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain		1		Ω
Q_g	Total gate charge	V_{DD} = 800 V, I_D = 20 A, V_{GS} = -5 to 18 V		63		nC
Q_{gs}	Gate-source charge			15		nC
Q_{gd}	Gate-drain charge			20		nC
E_{on}	Turn-on switching energy	V_{DS} = 800 V, I_D = 20 A, $R_{G(on)}$ = 12 Ω, $R_{G(off)}$ = 5.6 Ω, V_{GS} = -5 to 18 V		374		µJ
E_{off}	Turn-off switching energy			64		µJ
R_{thJC}	Thermal resistance, junction-to-case			0.54		°C/W

Table 3. Reverse intrinsic SiC diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	V_{GS} = 0 V, I_{SD} = 20 A	-	3.4	-	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, V_{DD} = 800 V, $R_{G(on)}$ = 12 Ω, $R_{G(off)}$ = 5.6 Ω	-	14.1	-	ns
Q_{rr}	Reverse recovery charge		-	163	-	nC
I_{IRRM}	Reverse recovery current		-	19	-	A

1.1 Electrical characteristics diagrams (Q1, Q2, Q3, Q4, Q5, Q6)

Figure 1. Typical output characteristics (T_J = 25 °C)

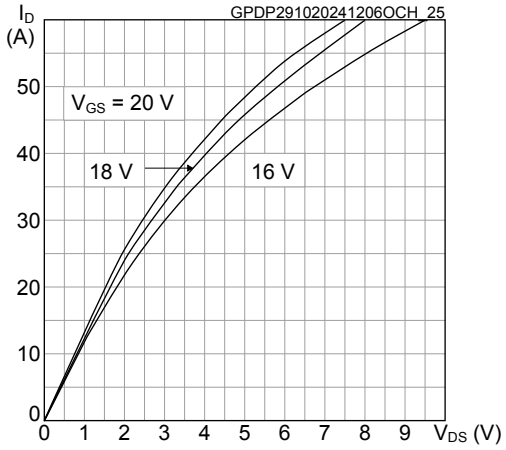


Figure 2. Typical output characteristics (T_J = -40 °C)

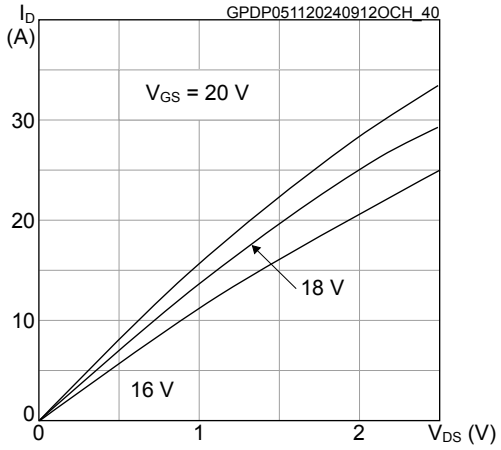


Figure 3. Typical output characteristics (T_J = 175 °C)

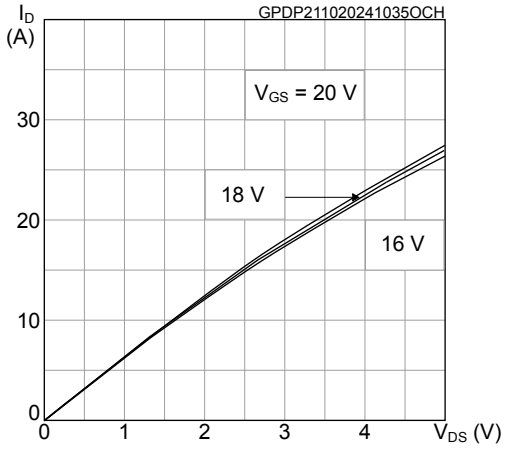


Figure 4. Typical transfer characteristics

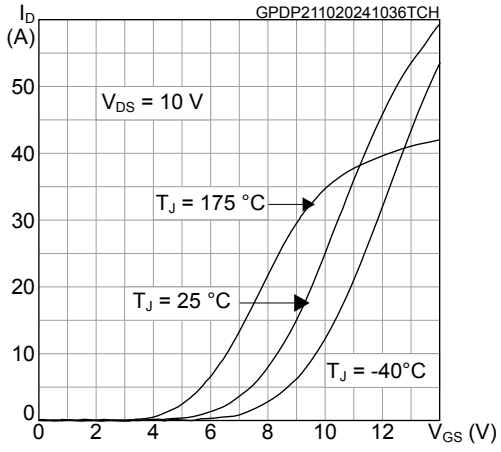


Figure 5. Typical reverse conduction characteristics (T_J = 25 °C)

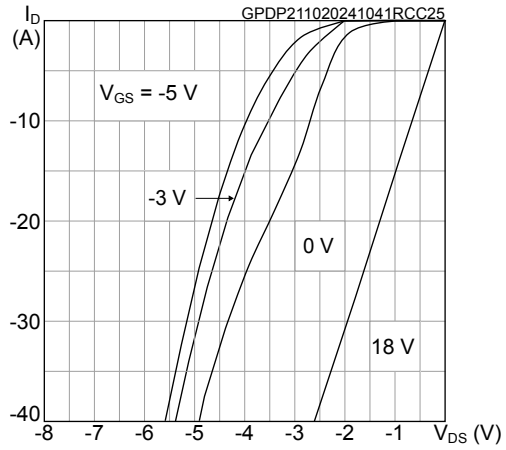


Figure 6. Typical reverse conduction characteristics (T_J = -40 °C)

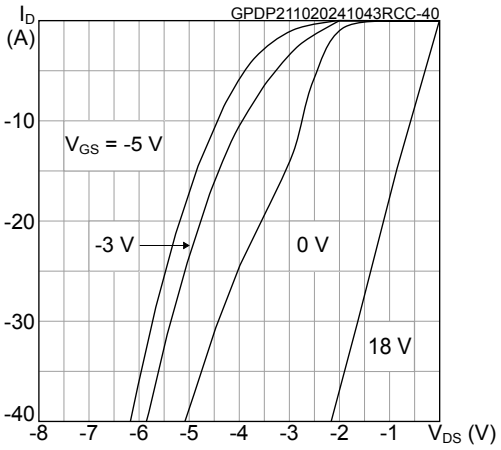


Figure 7. Typical reverse conduction characteristics (T_J = 175 °C)

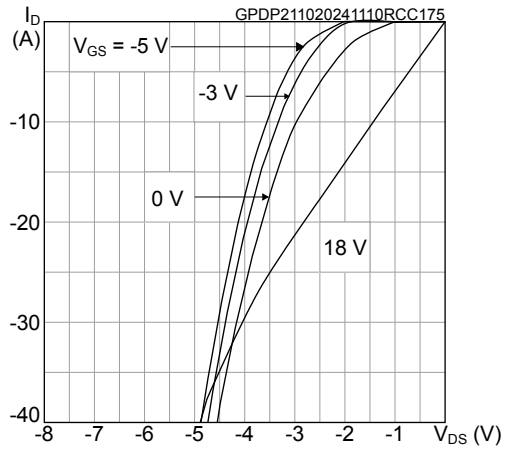


Figure 8. Typical switching energy vs drain current (T_J = 175 °C)

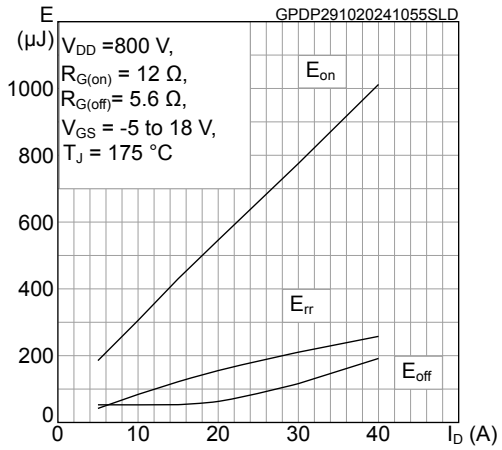


Figure 9. Typical switching energy vs drain current (T_J = 25 °C)

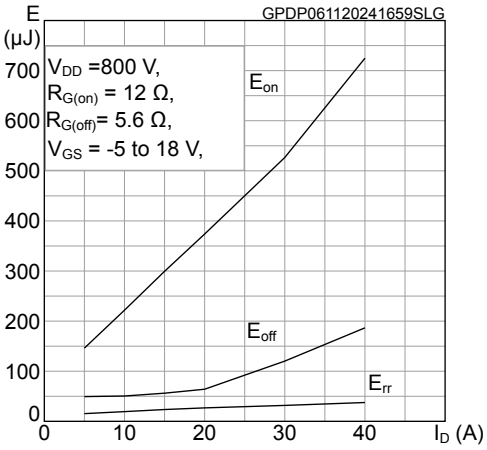


Figure 10. Typical switching energy vs gate resistance (T_J = 175 °C)

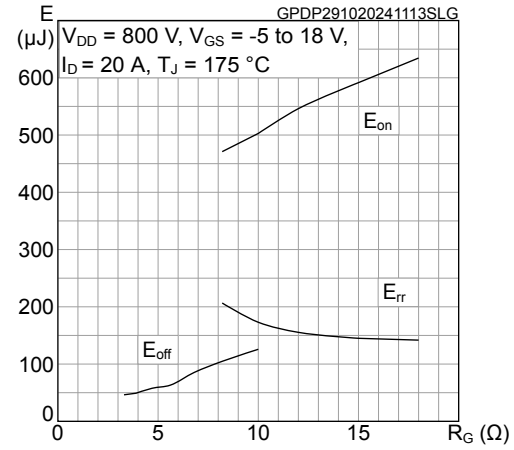


Figure 11. Typical switching energy vs gate resistance (T_J = 25 °C)

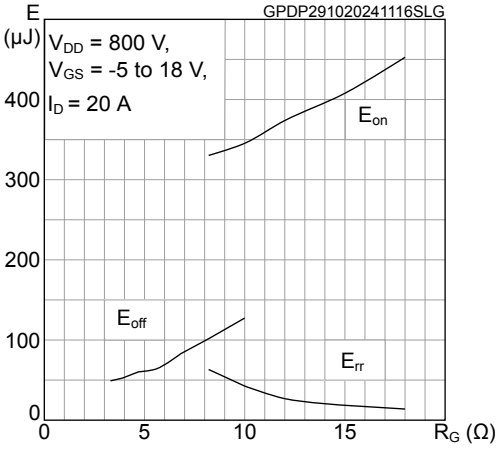


Figure 12. Typical switching energy vs temperature

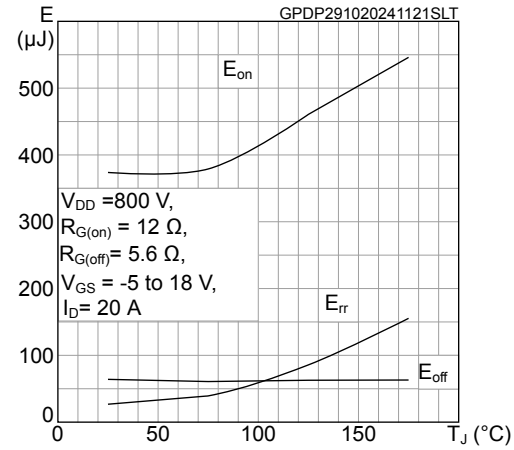


Figure 13. Typical switching energy vs supply voltage (T_J = 175 °C)

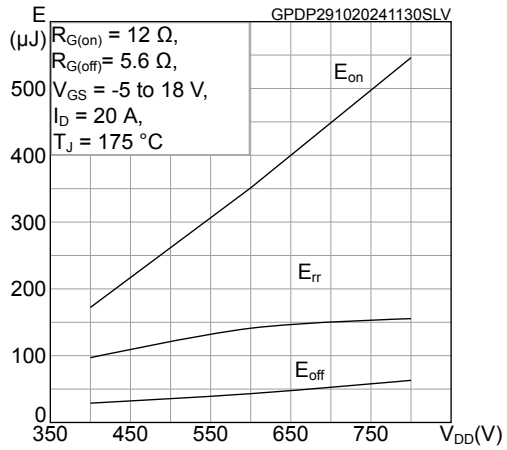


Figure 14. Typical switching energy vs supply voltage (T_J = 25 °C)

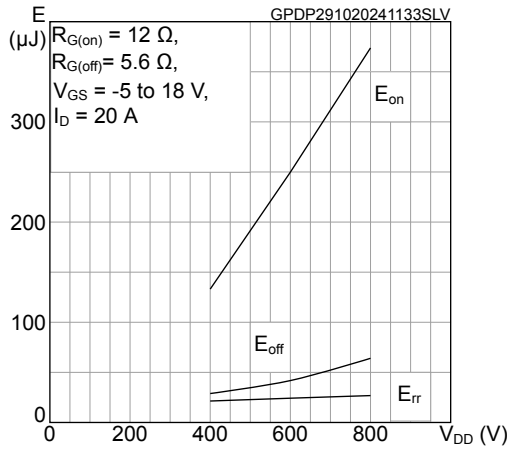


Figure 15. Typical gate charge characteristics

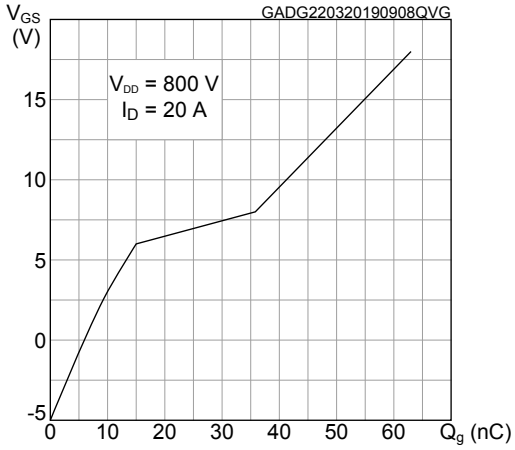


Figure 16. Typical capacitance characteristics

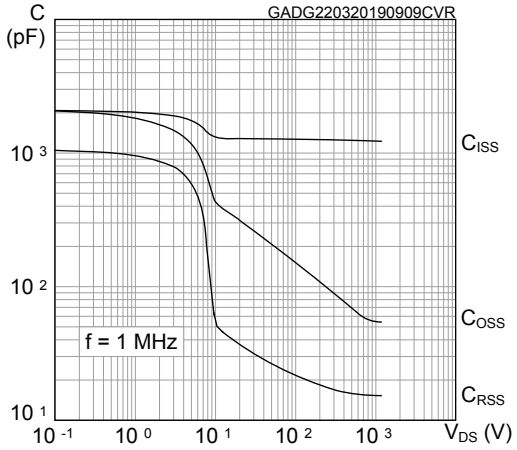
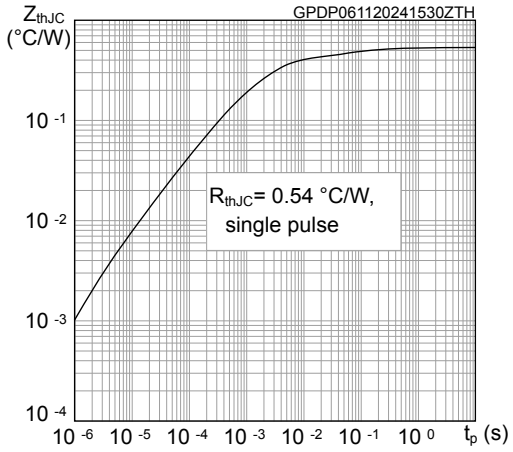


Figure 17. SiC typical transient thermal impedance



2 Rectifier diode (D1, D2)

All characteristics listed here are from datasheet of discrete component STBR3012-Y.

Table 4. Absolute maximum ratings (limiting values at 25 °C, unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{RSM}	Non-repetitive surge reverse voltage		1600	V
V_{RRM}	Repetitive peak reverse voltage	T_j = -40 °C to +175 °C	1200	V
$I_{F(RMS)}$	Forward rms current		30	A
T_j	Operating junction temperature		-40 to +175	°C

Table 5. Static electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_R (1)	Reverse leakage current	$V_R = V_{RRM}$	-		2	µA
		$V_R = V_{RRM}$, T_j = 150 °C	-	10	100	
V_F (2)	Forward voltage drop	I_F = 20 A	-	1.10	-	V
		I_F = 20 A, T_j = 150 °C	-	0.97	-	
$R_{th(j-c)}$	Thermal resistance junction to case		-	0.45		°C/W

1. *Pulse test: t_p = 5 ms, δ < 2%.*
2. *Pulse test: t_p = 380 µs, δ < 2%.*

To evaluate the conduction losses, use the following equation:

$P = 0.96 \times I_{F(AV)} + 0.008 \times I_F{}^2{}_{(RMS)}$

2.1 Electrical characteristics diagrams (D1, D2)

Figure 18. Diode typical forward voltage drop vs forward current

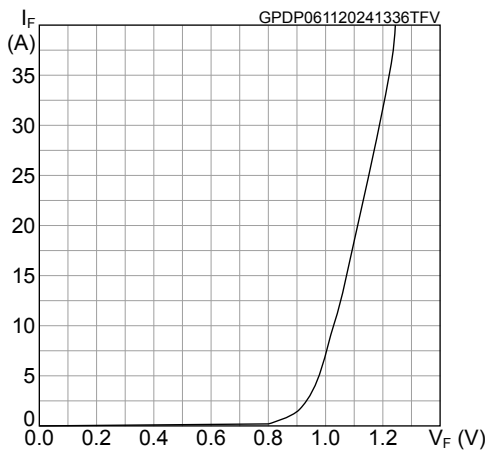
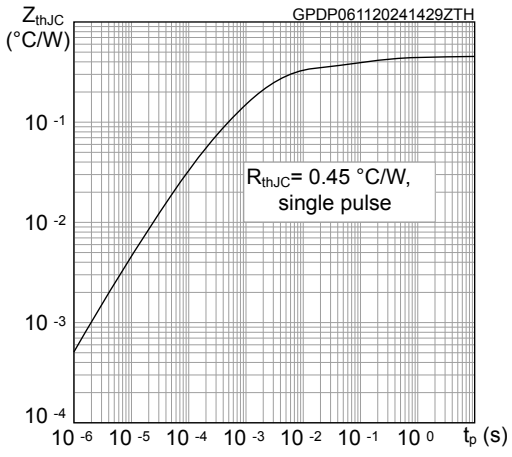


Figure 19. Diode typical transient thermal impedance



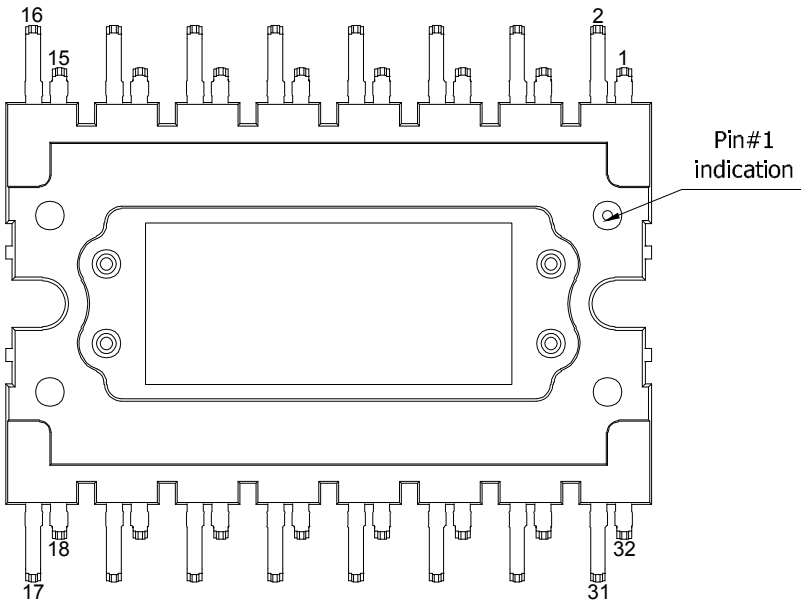
3 NTC

Table 6. Absolute maximum ratings for NTC temperature sensor, considered as stand-alone

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{25}	Resistance rating	T = 25 °C		10		kΩ
$\Delta R_{25}/R$	Resistance tolerance		-2		+2	%
R_{100}	Resistance rating	T = 100 °C		674.8		Ω
$\Delta R_{100}/R$	Resistance tolerance		-4.75		4.75	%
$R_{25/50}$	B-value	T = 25 °C to 50 °C		3940		K
$R_{25/85}$		T = 25 °C to 85 °C		3980		
$R_{25/100}$		T = 25 °C to 100 °C (±1%)		4000		
T	Operating temperature range		-40		150	°C

4 Electrical topology and pin description

Figure 20. **ACEPACK DMT-32 zig-zag pin layout (bottom view)**

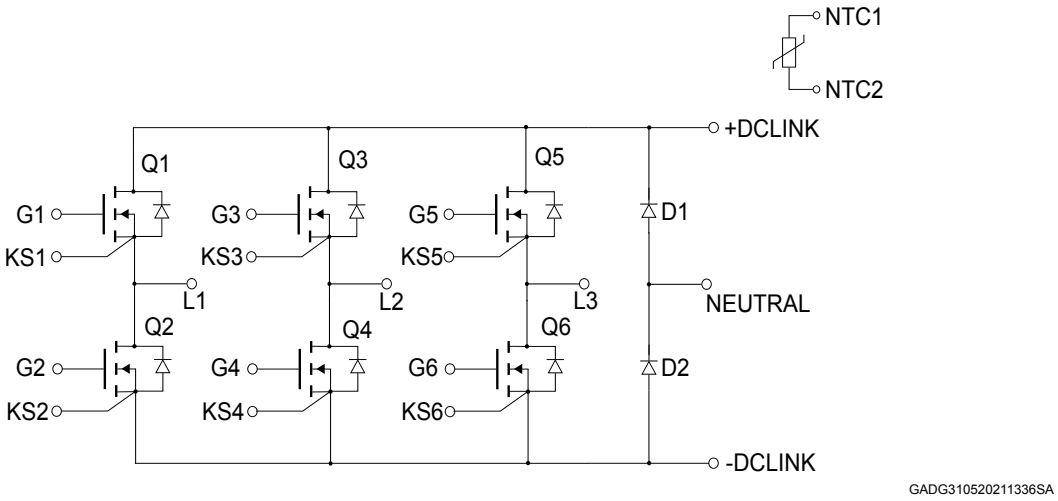


DM00692330_ZigZag_rev_6_pin _layout

Table 7. **Pin description**

Pin	Description	Pin	Description
1	-DCLINK	17	+DCLINK
2	-DCLINK	18	+DCLINK
3	NC	19	G6
4	NC	20	KS6
5	L1	21	G5
6	L1	22	KS5
7	L2	23	G3
8	L2	24	KS3
9	NEUTRAL	25	KS4
10	NEUTRAL	26	G4
11	L3	27	KS1
12	L3	28	G1
13	NC	29	KS2
14	NC	30	G2
15	NTC1	31	NC
16	NTC2	32	NC

Figure 21. Electrical topology and pin description

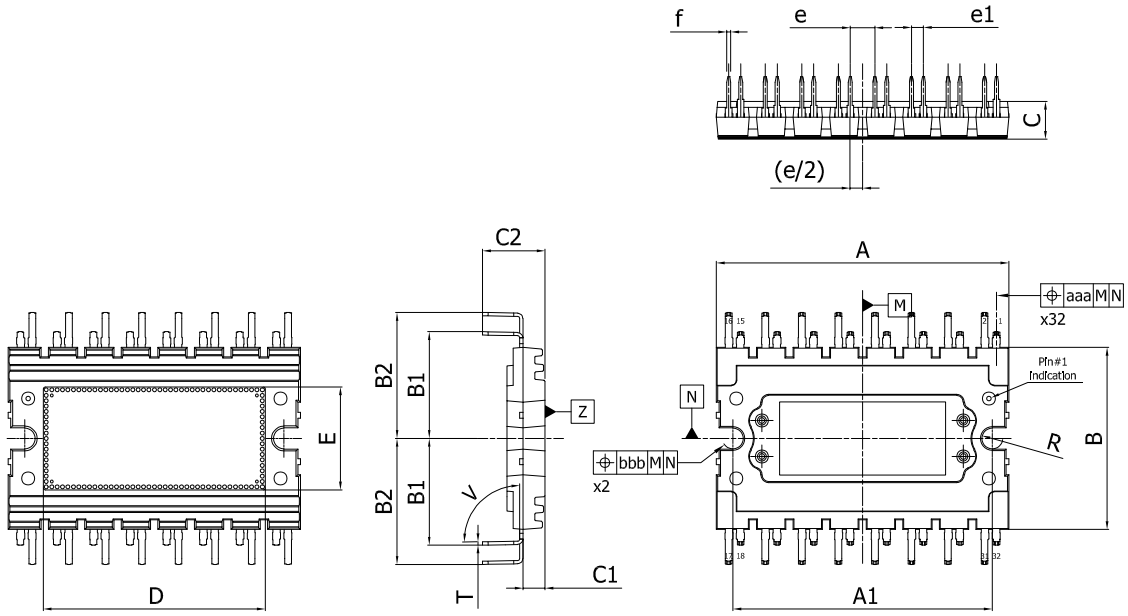


5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 ACEPACK DMT-32 zig-zag package information

Figure 22. ACEPACK DMT-32 zig-zag package outline



DM00692330_ZigZag_6

Table 8. **ACEPACK DMT-32 zig-zag package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	43.50	44.00	44.50
A1	38.80	39.00	39.20
B	26.90	27.40	27.90
B1	15.90	16.05	16.20
B2	18.80	18.95	19.10
C	5.50	5.70	5.90
C1	3.15	3.30	3.45
C2	8.90	9.40	9.90
e	3.50	3.70	3.90
e1	1.60	1.80	2.00
D	33.00	33.40	33.80
E	15.10	15.50	15.90
f	0.60	0.65	0.70
R	1.60		1.70
T	0.48	0.53	0.58
V	90°		93°
aaa		0.30	
bbb		0.15	

Table 9. **Ratings for module**

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation voltage (f = 50 Hz, t = 60 s)	3.5	kV
CTI	Comparative tracking index	600	V
T_{stg}	Storage temperature range	-40 to 150	°C

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
09-Oct-2023	1	First release.
11-Nov-2024	2	Updated title, *Description* and *Features* on cover page. Updated *Table 1. Absolute maximum ratings*. Updated *Table 2. Electrical characteristics*. Updated *Table 3. Reverse intrinsic SiC diode characteristics*. Inserted *Section 1.1: Electrical characteristics diagrams (Q1, Q2, Q3, Q4, Q5, Q6)*. Updated *Table 4. Absolute maximum ratings (limiting values at 25 °C, unless otherwise specified)*. Updated *Table 5. Static electrical characteristics*. Inserted *Section 2.1: Electrical characteristics diagrams (D1, D2)*. Minor text changes.
09-Apr-2025	3	Updated *Section 5.1: ACEPACK DMT-32 zig-zag package information*.
29-Jul-2025	4	Updated Features and Table 9. Ratings for module. Minor text changes.

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