M24C64X-DRE

Datasheet

64-Kbit serial I²C bus EEPROM operating up to 105°C with configurable device address and software write protection

WLCSP (CU)

Product status
Prerelease

Product label
LONGEVITY 10 YEARS COMMITMENT

Features

I²C interface

- Compatible with the following I²C bus modes:
  - 1 MHz (High speed transfert rate)
  - 400 kHz (Fast-mode)
  - 100 kHz (Standard-mode)

Memory

- 64-Kbit (8-Kbyte) of EEPROM
- Page size: 32 bytes

Supply voltage

- Single supply voltage from 1.7 V to 5.5 V

Temperature

- Extended operating temperature range: -40°C to +105°C

Fast write cycle time

- Byte and page write within 5 ms (3.5 ms typical)

Advanced features

- Chip enable register
- Software write protection
- Random and sequential read modes

Performance

- Enhanced 4kV ESD/latch-up protection
- More than 4 million write cycles
- More than 200-year data retention

Ultra-low power current consumption

- 300 nA (typical) in Standby supply current
- 170 µA (typical) in Supply current Read
- 250 µA (typical) in Supply current Write

Package

- WLCSP 4b (ECOPACK2-compliant)

1 Description

The M24C64X-DRE is a 64-Kbit I²C-compatible EEPROM (electrically erasable programmable memory) organized as 8 K x 8 bits. It can operate with a supply voltage from 1.7 V to 5.5 V with a clock frequency up to 1 MHz, over an ambient temperature range from -40°C to +105°C.

The device offers an additional 8-bit chip enable register for the configurable device address (CDA) and the memory write protection feature.

Thanks to these two features, the device offers the configurable device address, authorizing, through software, to configure up to eight possibilities of chip enable address, and the write protection of the whole memory array, by setting, always through software, the software write protection bit.

Figure 1. Logic diagram

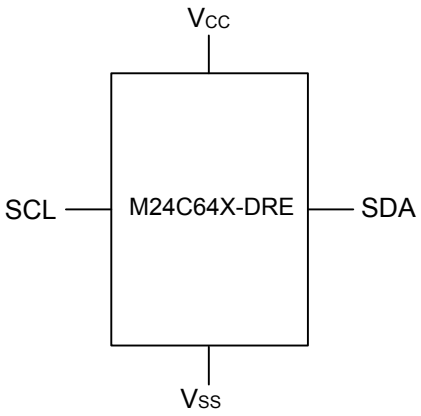
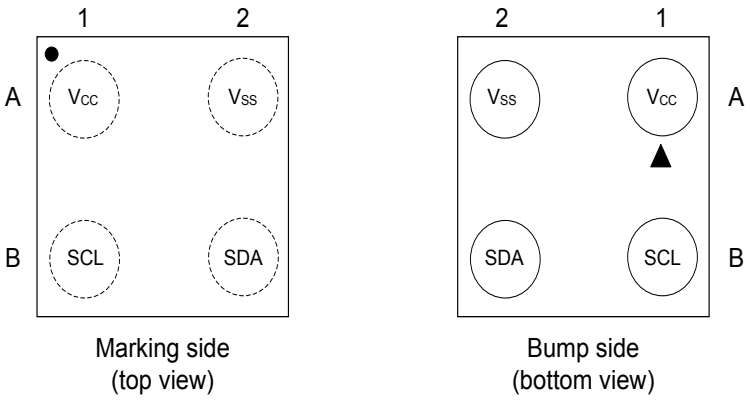


Table 1. Signal names

Signal name	Function	Direction
SDA	Serial data	I/O
SCL	Serial clock	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 4-bump WLCSP connections



Note: *1. Drawing is not to scale.*

2. Refer to Section 10.1 for mechanical data and outline details.

Table 2. **Signals vs. bump position**

Position	A	B
1	V_{CC}	SCL
2	V_{SS}	SDA

2 Signal description

2.1 Serial clock (SCL)

SCL is an input. The signal applied on it is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wired-AND with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC} (Figure 12 and Figure 13 indicate how to calculate the value of the pull-up resistor).

2.3 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.4 Supply voltage (V_{CC})

2.4.1 Operating supply voltage (V_{CC})

Before selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see operating conditions in Table 9). To secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually from 10 nF to 100 nF) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.4.2 Power-up conditions

The V_{CC} voltage increases from 0 V up to the minimum V_{CC} operating voltage (see operating conditions in Section 9).

2.4.3 Device reset

To prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see operating conditions in Table 9). When V_{CC} passes over the POR threshold, the device is reset and enters the standby power mode. The device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see operating conditions in Table 9).

Similarly, during power-down, when the V_{CC} decreases, the device must not be accessed once V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

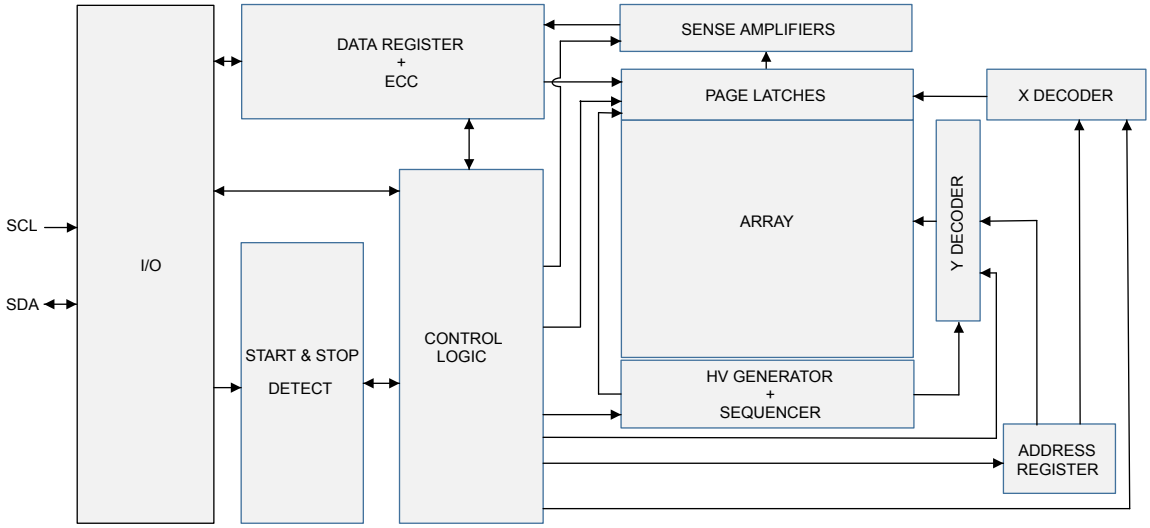
2.4.4 Power-down conditions

During power-down, when the V_{CC} decreases to 0 V, the device must be in the standby power mode. This mode is reached after decoding a stop condition, with no internal write cycle in progress.

3 Memory organization

The memory is organized as shown below.

Figure 3. Block diagram



4 Chip enable register

The chip enable register is an 8-bit register that allows the user to define a configurable device address (C2, C1, and C0) and includes a specific bit (SWP) named write protection activation bit, to freeze or unfreeze the memory protection. This register can be read and written by issuing the read or write chip enable register instruction. These instructions use the same protocol and format as the random address read or byte write (from/into memory array) except for the following differences (refer to Table 5. Device select code, Table 6. First byte address, and Table 7. Second byte address):

- Device type identifier = 1010
- MSB address bits A15 must be equal to 1
- MSB address bits from A14 to A8 are "don't care" bits
- LSB address bits from A7 to A0 are "don't care" bits

At power-up, the device loads the last configuration of the chip enable register.

Sending more than one byte during a write chip enable register command aborts the write cycle (content does not change).

The description of the chip enable register is given in Table 3.

Table 3. Chip enable register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Unused	Unused	Unused	Unused	C2	C1	C0	SWP
X (1)	X	X	X	Configurable device address bit	Configurable device address bit	Configurable device address bit	Write protection activation bit

1. *X = "don't care" bit*

Note: The factory default value is 00000000.

4.1 Configurable device address bits

C2, C1, and C0 define the chip enable address bits in the device select code, which makes it possible, through the chip enable register, to configure up to eight possibilities of chip enable address. At power-up or after reprogramming, the device loads the last configuration of C2, C1, and C0 values. These bits can be written and reconfigured with a byte write command.

The description of the configurable device address bits is given in Table 4.

Table 4. Configurable device address description

Bit	Function
7 to 4	Unused bits - Read as '0'. (b7, b6, b5, b4) = (0, 0, 0, 0)
3 to 1	**C2**, **C1**, **C0**: Configurable device address bits. b3, b2, b1 are used to configure up to eight possibilities of chip enable address: • (b3, b2, b1) = (0, 0, 0): the chip enable address is 000 (factory default value) • (b3, b2, b1) = (0, 0, 1): the chip enable address is 001 • (b3, b2, b1) = (0, 1, 0): the chip enable address is 010 • (b3, b2, b1) = (0, 1, 1): the chip enable address is 011 • (b3, b2, b1) = (1, 0, 0): the chip enable address is 100 • (b3, b2, b1) = (1, 0, 1): the chip enable address is 101 • (b3, b2, b1) = (1, 1, 0): the chip enable address is 110 • (b3, b2, b1) = (1, 1, 1): the chip enable address is 111
0	**SWP**: write protection activation bit b0 enables or disables the write protection of the memory array: • b0 = 0: the whole memory array can be written and read (factory default value) • b0 = 1: the whole memory array is write protected and is in read-only mode

4.2 Write protection activation bit

The SWP bit defines the write protection activation bit, which makes it possible, through the chip enable register, to enable or disable the write operation.

At power-up, the device loads the last configuration of the SWP value. This bit can be written and reconfigured with a byte write command.

Write operations are disabled (read-only memory) when the SWP is set to 1 (SWP=1). In the same way, the write operations are enabled when the SWP is set to 0 (SWP=0). Updating the SWP bit to a new value is a reversible action: the SWP bit can be updated from 0 to 1 and from 1 to 0.

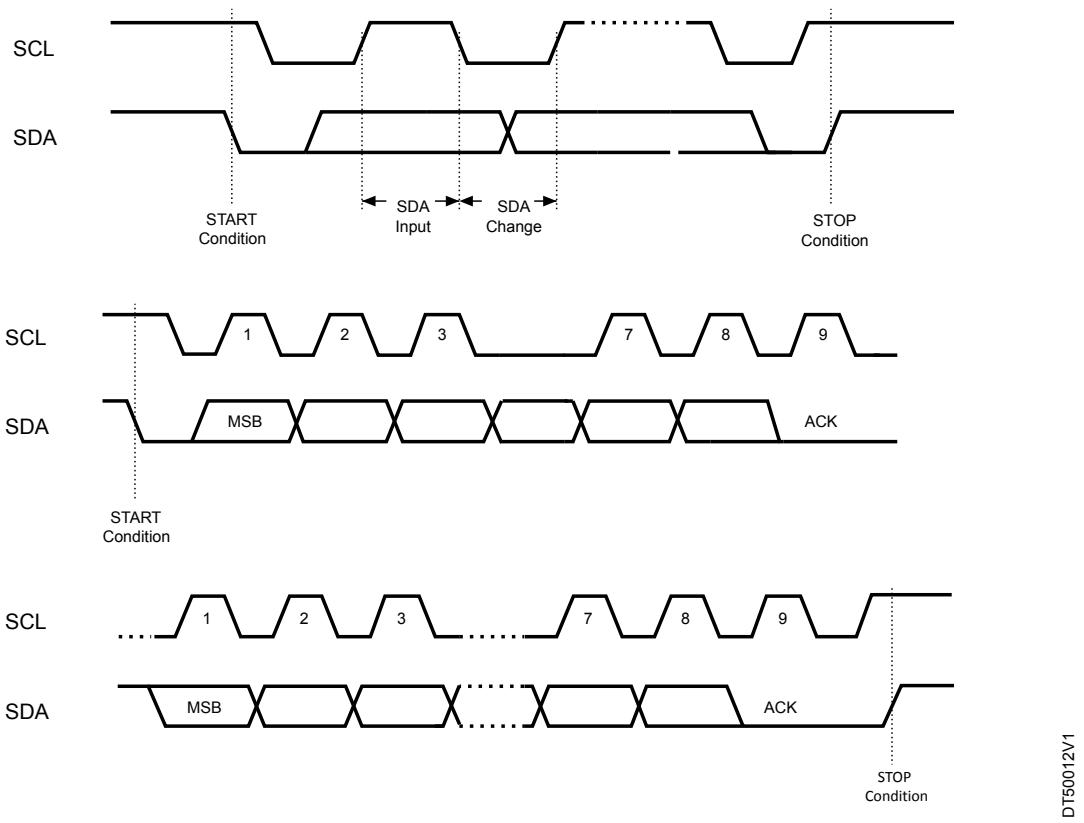
When SWP is set to 1, and in the case of writing to the memory, the device select and address bytes are acknowledged, but the data byte is not acknowledged, and the write cycle does not start.

The description of the software protection activation bit is given in Table 4.

5 Device operation

The device supports the I²C protocol summarized in Figure 4. Any device that sends data onto the bus is defined as a transmitter, and any device that reads the data is defined as a receiver. The device that controls the data transfer is known as the bus controller, and the other as the target. A data transfer can only be initiated by the bus controller, which also provides the serial clock for synchronization. The device is always a target in all communications.

Figure 4. I²C bus protocol



5.1 Start condition

The start condition is identified by a falling edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. This condition must precede any data transfer instruction. The device continuously monitors the SDA and SCL for a start signal, except during a write cycle.

5.2 Stop condition

The stop condition is identified by a rising edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. This condition terminates the communication between the device and the bus controller. A read instruction followed by NO ACK can be followed by a stop condition to force the device into the standby mode. A stop condition at the end of a write instruction triggers the internal write cycle.

5.3 Data input

During data input, the device samples the serial data (SDA) on the rising edge of the serial clock (SCL). For proper device operation, the SDA must be stable during the rising edge of the SCL, and the SDA signal must change only when the SCL is driven low.

5.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether a bus controller or target device, releases serial data (SDA) after sending eight bits of data. During the ninth clock pulse period, the receiver pulls SDA low to acknowledge the receipt of the eight data bits.

5.5 Device addressing

To start communication between the bus controller and the target device, the bus controller must initiate a start condition. Following this, the bus controller sends the device select code and byte address as specified in Table 5. Device select code, Table 6. First byte address, and Table 7. Second byte address. When the device select code is received, the device responds only if the bits b3, b2, and b1 values match the value of the C2, C1, and C0 bits programmed in the chip enable register.

If a match occurs, the corresponding device gives an acknowledgment on serial data (SDA) during the ninth bit time. If the device does not acknowledge the device select code, the device deselects itself from the bus and goes into standby mode (therefore it does not acknowledge the device select code).

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

Table 5. Device select code

Features	Device type identifier				Chip enable address(1)			R/W
-	Bit 7(MSB)(2)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	1	0	1	0	C2	C1	C0	R/W
Chip enable register	1	0	1	0	C2	C1	C0	R/W

1. *C0, C1 and C2 are compared with the value read on bits b1, b2, and b3 of the chip enable register.*
2. *The most significant bit, b7, is sent first.*

Table 6. First byte address

Features	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	A15(2)	A14(2)	A13(2)	A12	A11	A10	A9	A8
Chip enable register	1	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)

1. *The most significant bit, b7, is sent first.*
2. *"don't care".*
3. *X = "don't care" bit*

Table 7. Second byte address

Features	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	A7	A6	A5	A4	A3	A2	A1	A0
Chip enable register	X(2)	X(2)	X(2)	X(2)	X(2)	X(2)	X(2)	X(2)

1. *The most significant bit, b7, is sent first.*
2. *X = "don't care" bit.*

6 Instructions

6.1 Write operations on a memory array

Following a start condition the bus controller sends a device select code with the R/W bit (RW) reset to 0. The device acknowledges this, as shown in Figure 5, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Table 5. Device select code, Table 6. First byte address, and Table 7. Second byte address how to address the memory.

When the bus controller generates a stop condition immediately after a data byte ACK bit (in the “10^{th} bit” time slot), either at the end of a byte write or a page write, the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

After the stop condition and the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

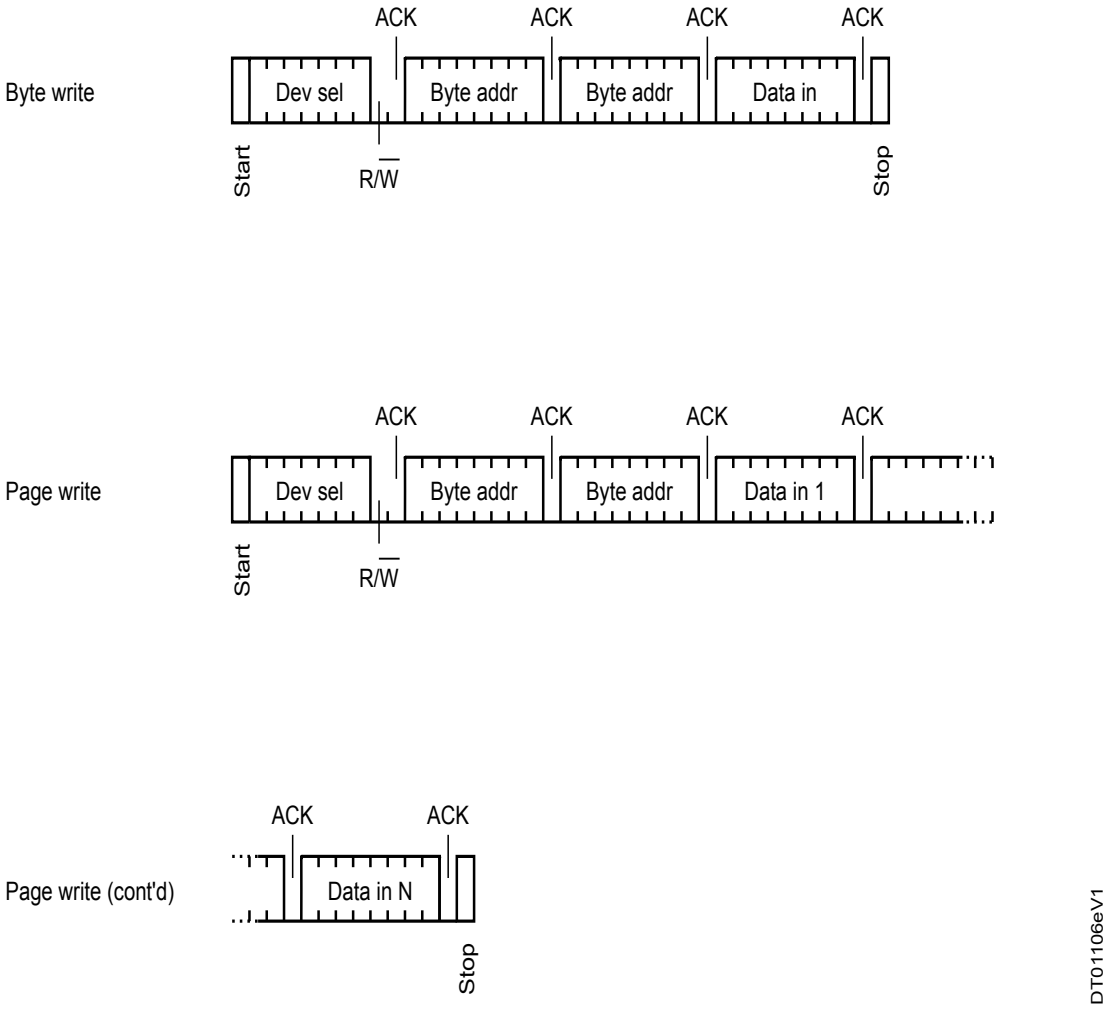
During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

If the write protection is enabled with the SWP bit set to '1', the write instruction is not executed and the accompanying data bytes are not acknowledged, as shown in Figure 6.

6.1.1 Byte write

After the device select code and the address bytes, the bus controller sends one data byte. If the addressed location is write-protected, with the SWP bit set to '1', the device replies with NoACK, and the location is not modified, as shown in Figure 6. If, instead, the addressed location is not Write-protected, the device replies with ACK. The bus controller terminates the transfer by generating a stop condition, as shown in Figure 5.

Figure 5. Write mode sequence SWP bit = 0 (data write enabled)



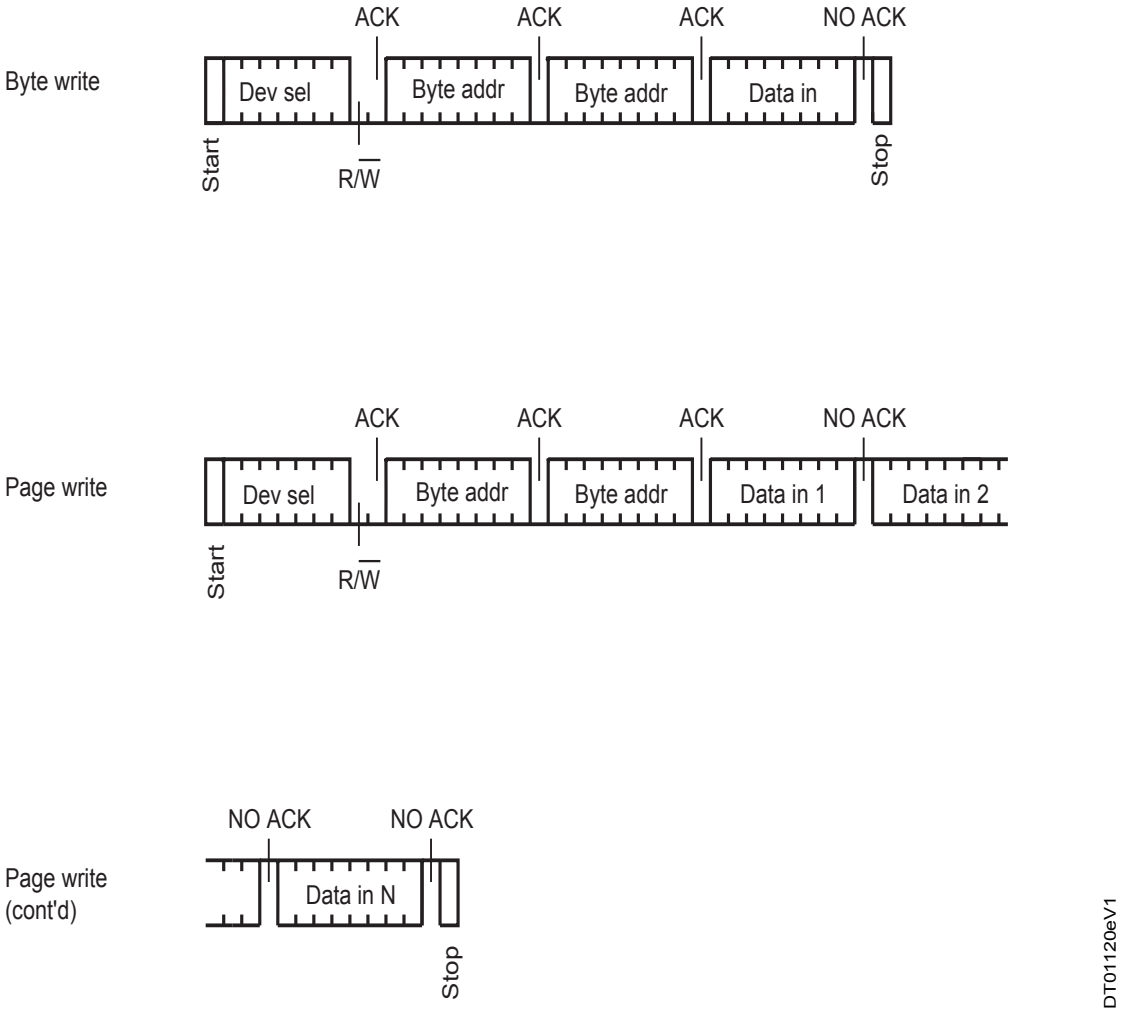
6.1.2 Page write

The page write mode allows up to 32 bytes to be written in a single write cycle, provided they are all located in the same page in the memory: that is, the most significant memory address bits, A15/A5, are the same. If more bytes than those that fit up to the end of the page are sent, a “roll-over” occurs, that is, the bytes exceeding the page end are written on the same page, from location 0.

The bus controller sends from 1 to 32 bytes of data. Each one is acknowledged by the device if the software write protection is disabled with the SWP bit set to '0'. If the software write protection is enabled with the SWP bit set to '1', the contents of the addressed memory location are not modified, and each data byte is followed by a NoACK, as shown in Figure 6. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus controller generating a stop condition.

Figure 6. Write mode sequence with SWP bit = 1 (data write inhibited)



6.1.3 Minimizing write delays by polling on ACK

During the internal write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in Table 15 and Table 16, but the typical time is shorter. The bus controller can implement a polling sequence to utilize this feature.

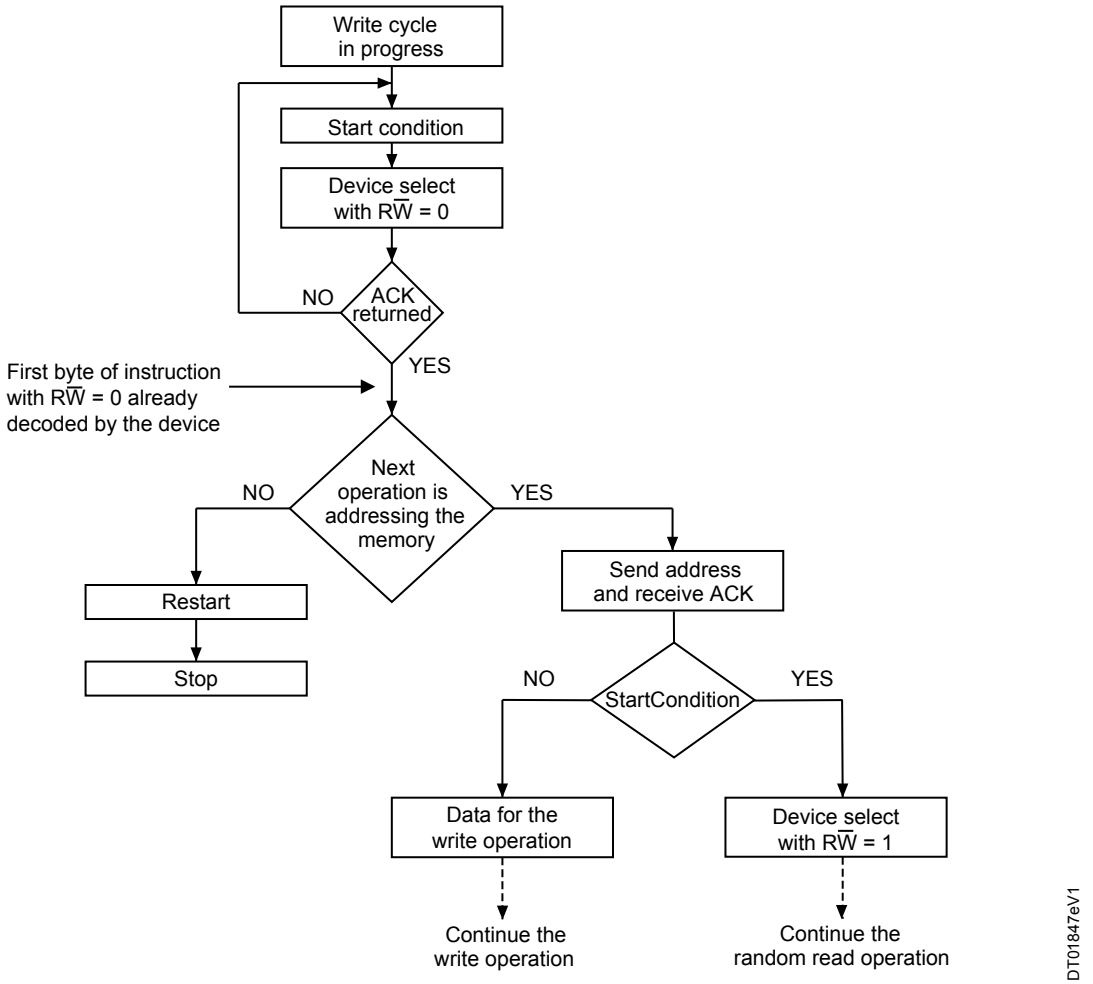
The sequence, as shown in Figure 7, is:

- Initial condition: A write cycle is in progress.
- Step 1: The bus controller issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: If the device is busy with the internal write cycle, NO ACK is returned and the bus controller goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during step 1).

Note: When writing a command to the configurable device address register with C2, C1, and C0 are reconfigured, the device returns ACK only if:

- *The chip enable address of the device select code is equal to the new C2, C1, and C0 values.*
- *An internal write cycle is completed (a new C2, C1, and C0 values have been programmed in the chip enable register).*

Figure 7. Write cycle polling flowchart using ACK



Note: The seven most significant bits of the device select code in a random read (bottom right box in the figure above) must match those of the device select code in the write operation (polling instruction).

6.2 Write operations on the chip enable register

Write operations on the chip enable register are performed independently of the SWP state.

Following a start condition the bus controller sends a device select code with the R/W bit (RW) set to 0. The device acknowledges this, as shown in Figure 8, and waits for the address bytes where the register is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Table 5. Device select code, Table 6. First byte address, and Table 7. Second byte address how to address the chip enable register.

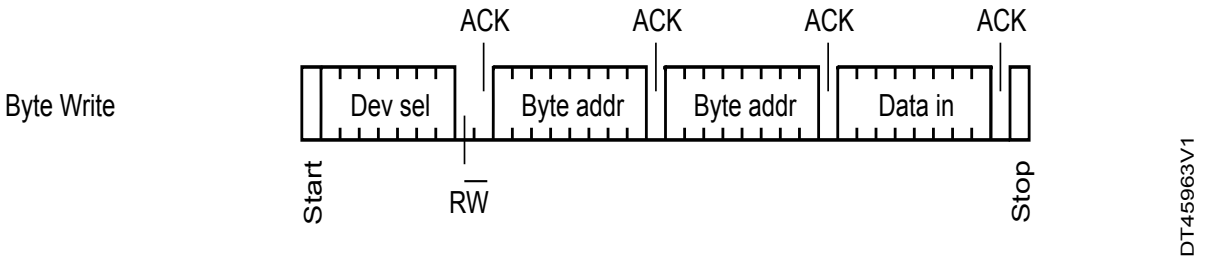
When the bus controller generates a stop condition immediately after the data byte ACK bit (in the "10th bit" time slot), the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests (NoACK).

If the 3-bits C2, C1 and C0 have been reconfigured with a correct write command, the device acknowledges if the chip enable address of the device select code is equal to the new values of C2, C1, and C0, otherwise NoACK.

Sending more than one byte aborts the write cycle (chip enable register content is not changed).

Figure 8. Write on chip enable register



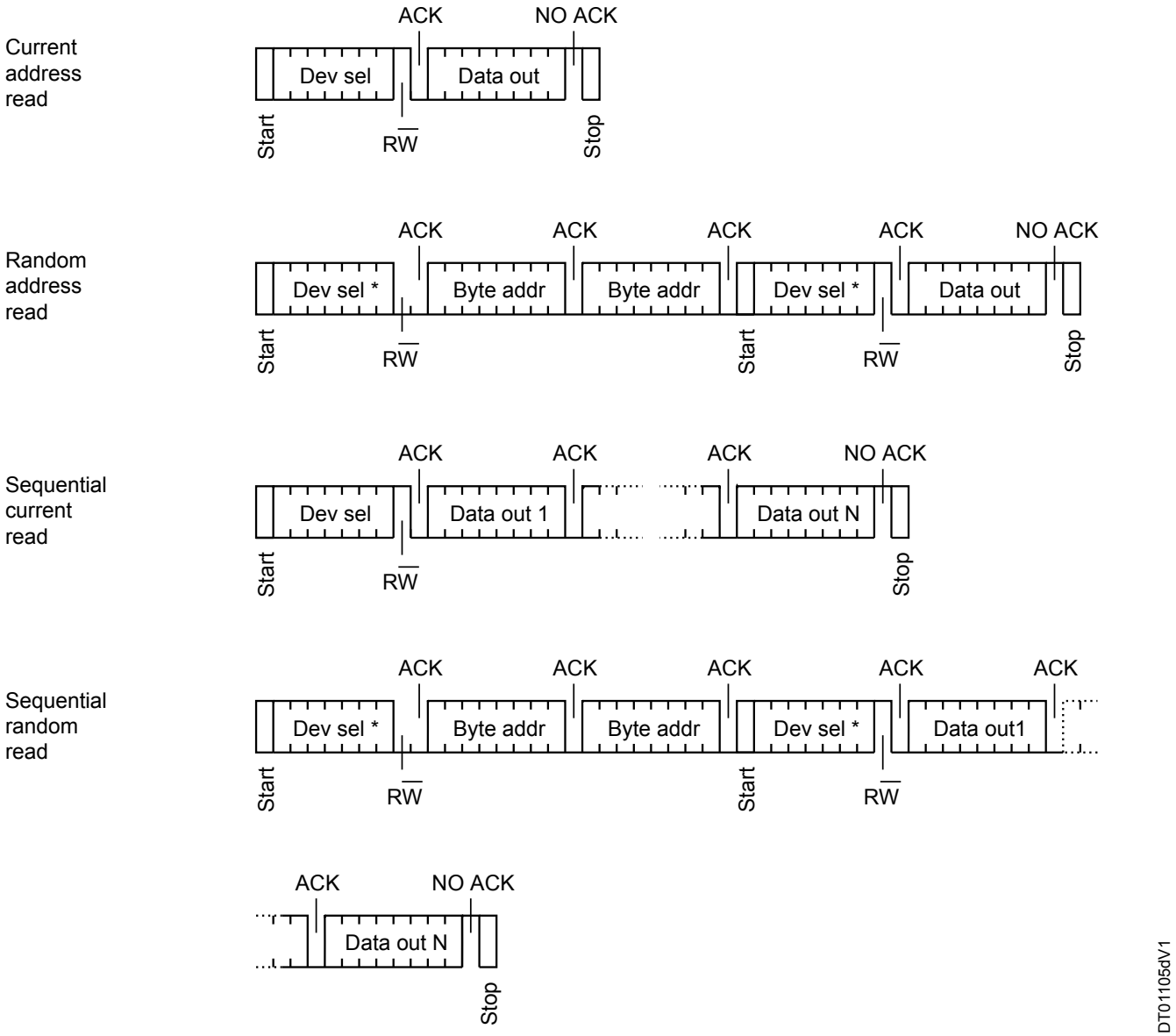
6.3 Read operations on memory array

Following a start condition the bus controller sends a device select code with the R/W bit (RW) set to 0. The device acknowledges this and waits for the two-byte address. The device responds to each address byte with an acknowledge bit. Then, the bus controller sends another start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the data. See in Table 5. Device select code, Table 6. First byte address, and Table 7. Second byte address how to address the memory.

After each byte read (data out), the device waits for an acknowledgment (data in) during the ninth bit time. If the bus controller does not acknowledge during this interval, the device terminates the data transfer and switches to its standby mode after a stop condition.

After the successful completion of a read operation, the internal address counter is incremented by one, to point to the next byte address.

Figure 9. Read mode sequences



Note: The seven most significant bits of the first device select code of a random read must be identical to the seven most significant bits of the device select code of the write.

6.3.1 Random address read

A dummy write is first performed to load the address into this address counter (as shown in Figure 9) but without sending a stop condition. Then, the bus controller sends another start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus controller must not acknowledge the byte, and terminates the transfer with a stop condition.

6.3.2 Current address read

For the current address read operation, following a start condition, the bus controller only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus controller terminates the transfer with a stop condition, as shown in Figure 9, without acknowledging the byte.

When accessing the memory, it is safer to use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the current address read instruction.

6.3.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus controller does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus controller must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 9.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

6.4 Read operations on chip enable register

Read operations are performed independently of the SWP state.

Following a start condition the bus controller sends a device select code with the R/W bit (RW) set to 0. The device acknowledges this and waits for the address bytes where the register is located. The device responds to each address byte with an acknowledge. Then, the bus controller sends another start condition, and repeats the device select code with the RW bit set to 1. The device acknowledges this, and outputs the contents of the chip enable register. See in Table 5. Device select code, Table 6. First byte address, and Table 7. Second byte address how to address the chip enable register.

After the successful completion of a read operation on the chip enable register, the device internal address counter is not incremented by one to point to the next byte address. Reading more than one byte loops on reading the chip enable register value.

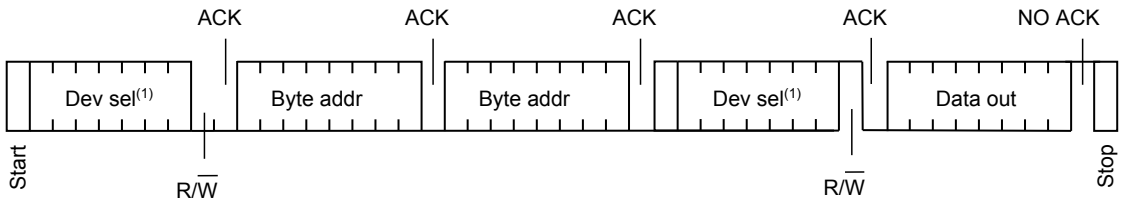
To terminate the stream of data bytes, the bus controller must not acknowledge the byte and must generate a stop condition, as shown in Figure 10.

The chip enable register cannot be read while a write cycle (t_W) is ongoing.

The configurable device address inside the chip enable register can be checked by sending the device select code.

- If the chip enable address b3, b2, and b1 sent in the device select code match the C2, C1, and C0 values, the device sends an ACK.
- Otherwise, the device answers no ACK.

Figure 10. Read on chip enable register



1. *The seven most significant bits of the first device select code of a random read must be identical to the seven most significant bits of the device select code of the write.*

7 Initial delivery state

At factory delivery, the device is delivered with:

- All the memory array bits set to 1 (each byte contains FFh)
- The chip enable register set to 00000000 (00h)

8 Maximum ratings

Stressing the device outside the ratings listed in Table 8 may permanently damage it. These are stress ratings only, and operation of the device at these or any other conditions outside those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	-40	130	°C
T_{STG}	Storage temperature	-65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	-0.50	6.5	V
V_{CC}	Supply voltage	-0.50	6.5	V
V_{ESD}	Electrostatic pulse (human body model)(2)	-	4000	V

1. *Compliant with JEDEC standard J-STD-020 (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK 7191395 specification, and the European directive on restrictions of hazardous substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to ANSI/ESDA/JEDEC JS-001 (C1=100 pF, R1=1500 Ω, R2=500 Ω).*

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics.

Table 9. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	-40	105	°C
f_C	Operating clock frequency	-	1	MHz

Table 10. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 11. AC measurement I/O waveform

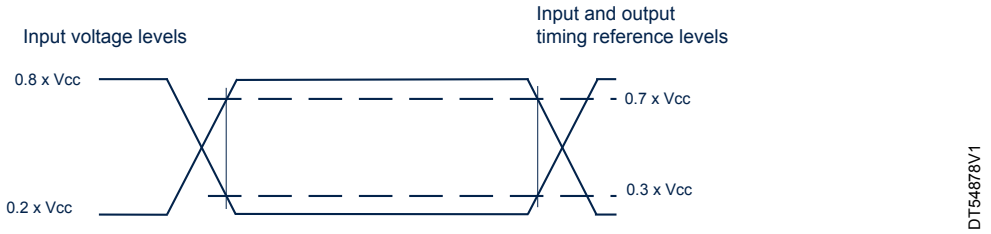


Table 11. Input parameters

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{IN} (1)	Input capacitance (SDA)	-	-	8	pF
C_{IN} (1)	Input capacitance (other pins)	-	-	6	pF

1. *Specified by design - Not tested in production.*

Table 12. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition	Max.	Unit
Ncycle	Write cycle endurance (1)	$T_A \leq 25°C$, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4.000.000	Write cycle (2)
		$T_A = 85°C$, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1.200.000	
		$T_A = 105°C$, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	100.000	

1. *The write cycle endurance is defined by characterization and qualification.*
2. *A write cycle is executed when either a page write, or a byte write, or a write chip enable register instruction is decoded.*

Table 13. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention (1)	T_A = 55 °C	200	Year

1. *The data retention behaviour is checked in production, while the data retention limit is extracted from the characterization and qualification results.*

Table 14. DC characteristics

Symbol	Parameter	Test conditions (in addition to those in Table 9)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC} device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} < 1.8 V, f_C = 400 kHz	-	0.8(1)	mA
		V_{CC} ≥ 1.8 V, f_C = 400 kHz	-	2(2)	
		V_{CC} ≥ 1.8 V, f_C = 1 MHz	-	2.5(3)	
I_{CC0}	Supply current (Write)(4)	During t_W	-	2 (5)	mA
I_{CC1}	Standby supply current	Device not selected, (6) V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8 V	-	1.5(7)	µA
		Device not selected, (6)V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5 V	-	2	
		Device not selected, (6)V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5 V	-	3	
V_{IL}	Input low voltage (SCL, SDA)	-	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.75 V_{CC}	6.5	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} < 1.8 V	-	0.2	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V	-	0.4	V
		I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. *150 µA typical value at 1.8 V. This value is evaluated by characterization - Not tested in production*
2. *130 µA typical value at 3.3 V. This value is evaluated by characterization - Not tested in production*
3. *170 µA typical value at 3.3 V. This value is evaluated by characterization - Not tested in production*
4. *Evaluated by characterization - Not tested in production.*
5. *250 µA typical value at 3.3 V. This value is evaluated by characterization - Not tested in production*
6. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*
7. *300 nA typical value at 1.8 V. This value is evaluated by characterization - Not tested in production*

Table 15. 400 kHz AC characteristics (Fast-mode)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2} (1)	t_F	SDA (out) fall time	20 (2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	50	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS} (1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	50	ns

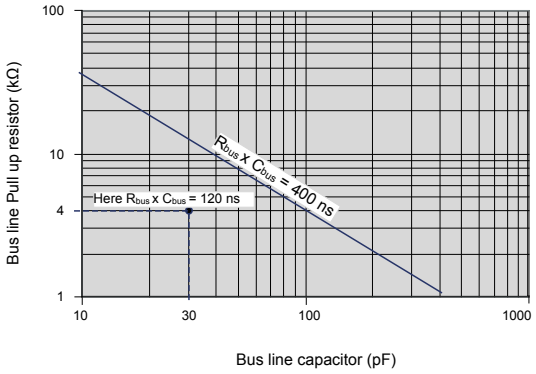
1. *Evaluated by characterization - Not tested in production.*
2. *With C_L = 10 pF.*
3. *There is no min. or max. value for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.*
4. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3V_{CC} or 0.7V_{CC}, assuming that R_{bus} × C_{bus} time constant is within the values specified in .*

Table 16. 1 MHz AC characteristics

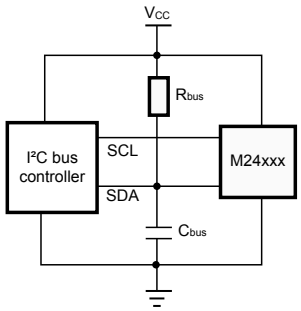
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	700	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(1)	(1)	ns
t_{XL1XL2}	t_F	Input signal fall time	(1)	(1)	ns
t_{QL1QL2} (2)	t_F	SDA (out) fall time	20 (3)	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	50	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	650	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS} (2)	-	Pulse width ignored (input filter on SCL and SDA)	-	50	ns

1. *There is no min. or max. values for the input signal rise and fall times. However, it is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns when f_C < 1 MHz.*
2. *Evaluated by characterization - Not tested in production.*
3. *With CL = 10 pF.*
4. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in .*

Figure 12. R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C_{bus} (f_C = 400 kHz)

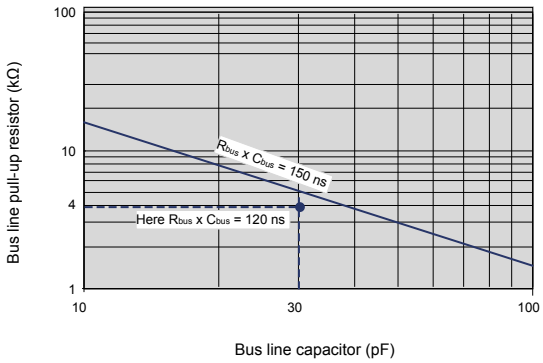


The R_{bus} x C_{bus} time constant must be below the 400 ns time constant line displayed on the left

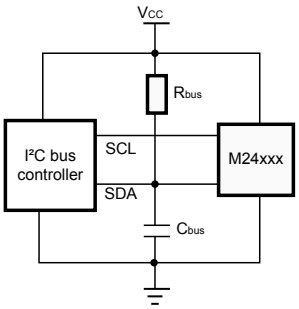


DT37916V5

Figure 13. R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus (f_C = 1 MHz)

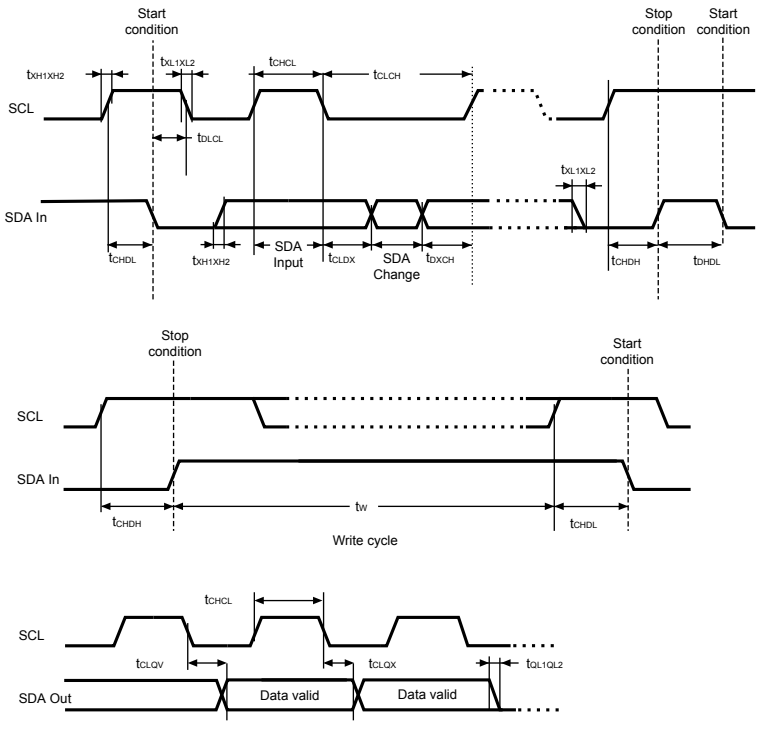


The R_{bus} x C_{bus} time constant must be below the 150 ns time constant line displayed on the left



DT19745V8

Figure 14. AC waveforms



DT00795J_V1

10 Package information

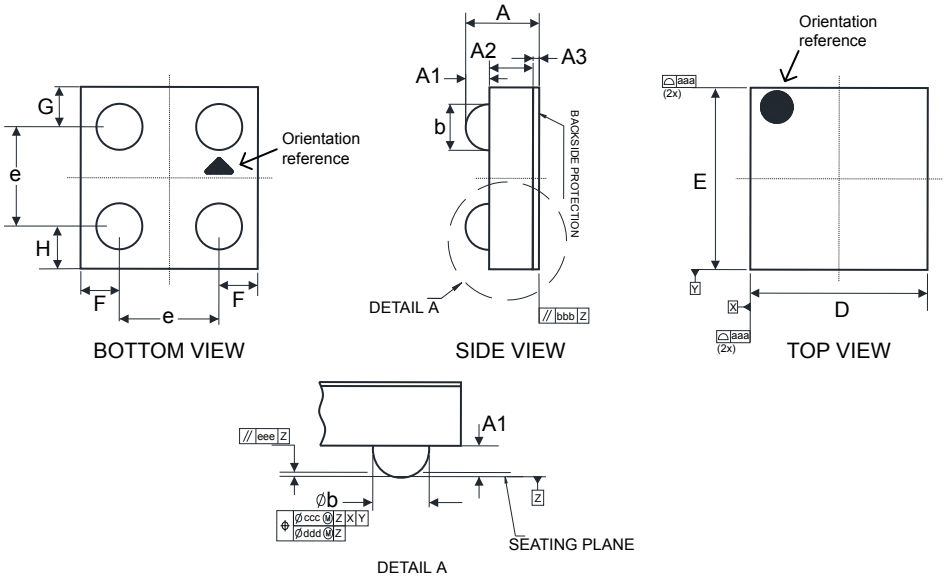
To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com.

ECOPACK is an ST trademark.

10.1 WLCSP4 (CU) ultra thin package information

This WLCSP is a 4 bumps, 0.711 x 0.731 mm, ultra thin wafer level chip scale package.

Figure 15. WLCSP4 (CU) - Outline



A0Z7_PTh_WLCSP4_XIAO_ME_V3

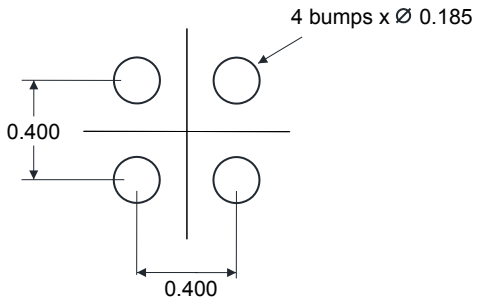
1. *Drawing is not to scale.*
2. *Primary datum Z and seating plane are defined by the spherical crowns of the bump.*
3. *Bump position designation per JESD 95-1, SPP-010.*

Table 17. WLCSP4 (CU) - Mechanical data

Symbol	millimeters			inches [1]		
	Min	Typ	Max	Min	Typ	Max
A	0.262	0.295	0.328	0.0103	0.0116	0.0129
A1	-	0.095	-	-	0.0037	-
A2	-	0.175	-	-	0.0069	-
A3	-	0.025	-	-	0.0010	-
b[2] [3]	-	0.185	-	-	0.0073	-
D	-	0.711	0.731	-	0.0280	0.0288
E	-	0.731	0.751	-	0.0288	0.0296
e	-	0.400	-	-	0.0157	-
F	-	0.156	-	-	0.0061	-
G	-	0.161	-	-	0.0063	-
H	-	0.171	-	-	0.0067	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.060	-	-	0.0024	-
eee	-	0.060	-	-	0.0024	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *Primary datum Z and seating plane are defined by the spherical crowns of the bump.*
3. *Dimension is measured at the maximum bump diameter parallel to primary datum Z.*

Figure 16. WLCSP4 (CU) - Footprint example



A0Z7_PTh_WLCSP4_XIAO_FP_V1

1. *Dimensions are expressed in millimeters.*

11 Ordering information

Table 18. Ordering information scheme

Example: M24 C64X - F CU 8 T / T F

Device type

M24 = I^2C serial access EEPROM

Device function

C64X = 64 Kbit (8192 x 8 bit)

Operating voltage

F = V_{CC} = 1.7 V to 5.5 V

Package (1)

CU = 4-bump WLCSP ultra-thin

Device grade

8 = Industrial: device tested with standard test flow over -40 to 105°C

Option

T = Tape and reel packing

Blank = tube packing

Process technology(2)

/ T = Process letter

Option

Blank = No back side coating

F = Back side coating

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).*
2. *The process letter appears on the device package (marking) and on the shipment box. Contact your nearest ST Sales Office for further information.*

Note: For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact your nearest ST sales office.

Note: Parts marked as "ES" or "E" are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 19. **Document revision history**

Date	Revision	Changes
21-May-2025	1	Initial release.

Contents

List of tables

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