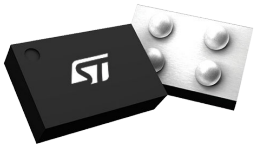
M24C08-G

Datasheet

8-Kbit serial I²C bus EEPROM with 1.8 V core and I/Os 1.2 V compatible



WLCSP (CT)

(0.703 x 0.713 mm)

Product status link
M24C08-G

Product label
LONGEVITY 10 YEARS COMMITMENT

Features

I²C interface

- Compatible with the following I²C bus modes:
  - 400 kHz (fast mode)
  - 100 kHz (standard mode)

Memory

- 8 Kbit (1-Kbyte) of EEPROM
- Page size: 16-byte

Supply voltage

- Voltage range: 1.8 V ± 5%

Input-output

- I/Os 1.2 V compatible

Temperature

- Operating temperature range: -40 °C up to +85 °C

Fast write cycle time

- Byte and page write within 5 ms (3.5 ms typical)

Performance

- Enhanced ESD/latch-up protection 3 kV (HBM)
- More than 4 million write cycles
- More than 200-year data retention

Ultra-low power current consumption

- 240 nA (typical) in Standby mode
- 130 µA (typical) for read current
- 100 µA (typical) for write current

Advanced features

- Hardware write protection of the whole memory array
- Random and sequential read modes

Package

- WLCSP4 4-ball

1 Description

The M24C08-G is an 8-Kbit I²C-compatible EEPROM (electrically erasable programmable read-only memory) organized as 1 K × 8 bits.

It can operate with a supply voltage of 1.8 V ± 5% over an ambient temperature range of -40 °C/+85 °C, with a maximum clock frequency of 400 kHz.

The product offers the I/Os compatible with 1.2 V, and is delivered in wafer level chip scale packaging 4-ball.

1.1 Logic diagram

Figure 1. Logic diagram

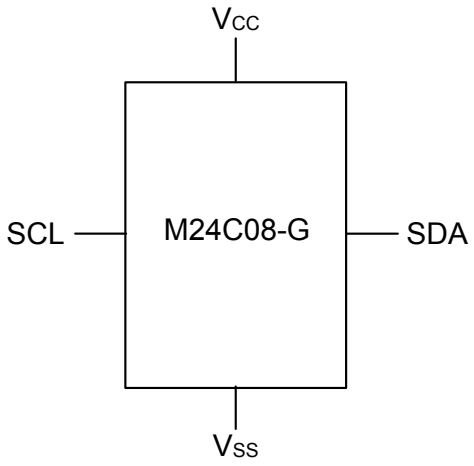


Table 1. Signal names

Signal name	Function	Direction
SDA	Serial data	I/O
SCL	Serial clock	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

1.2 Device packaging

Figure 2. **4-bump WLCSP connections**

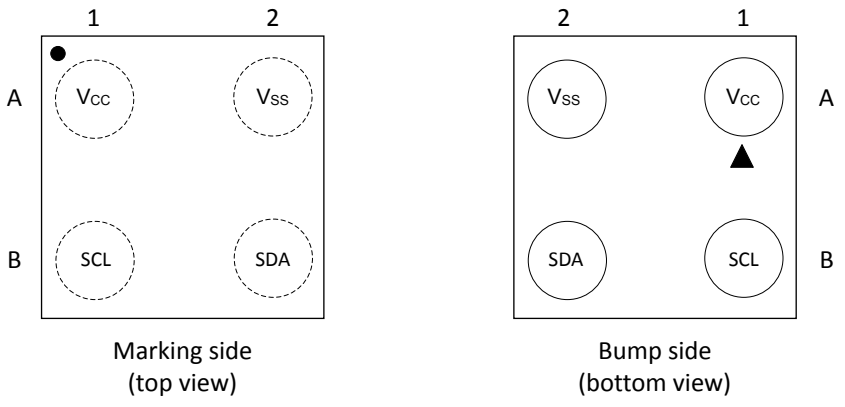


Table 2. **Signal names**

Signal name	Position
V_{CC}	A1
V_{SS}	A2
SCL	B1
SDA	B2

2 Signal description

2.1 Serial clock (SCL)

SCL is an input. The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or out of the device. SDA(out) is an open drain output that may be wired-AND with other open drain or open collector signals on the bus. A pull-up resistor must be connected from serial data (SDA) to V_{CC} (Figure 10 indicates how to calculate the value of the pull-up resistor).

2.3 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.4 Supply voltage (V_{CC})

2.4.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see operating conditions in Section 8: DC and AC parameters). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.4.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see operating conditions in Section 8: DC and AC parameters).

2.4.3 Device reset

To prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see operating conditions in Section 8: DC and AC parameters). When V_{CC} exceeds the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see operating conditions in Section 8: DC and AC parameters).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the internal reset threshold voltage, the device stops responding to any instruction sent to it.

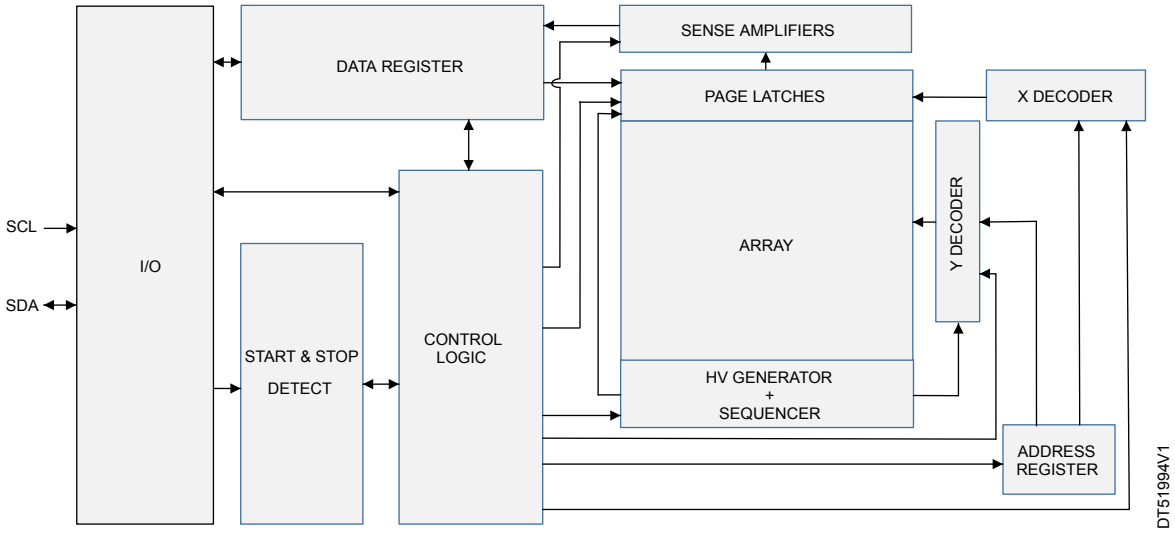
2.4.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the standby power mode (mode reached after decoding a stop condition, with no internal write cycle in progress).

3 Block diagram

The block diagram of the device is shown below.

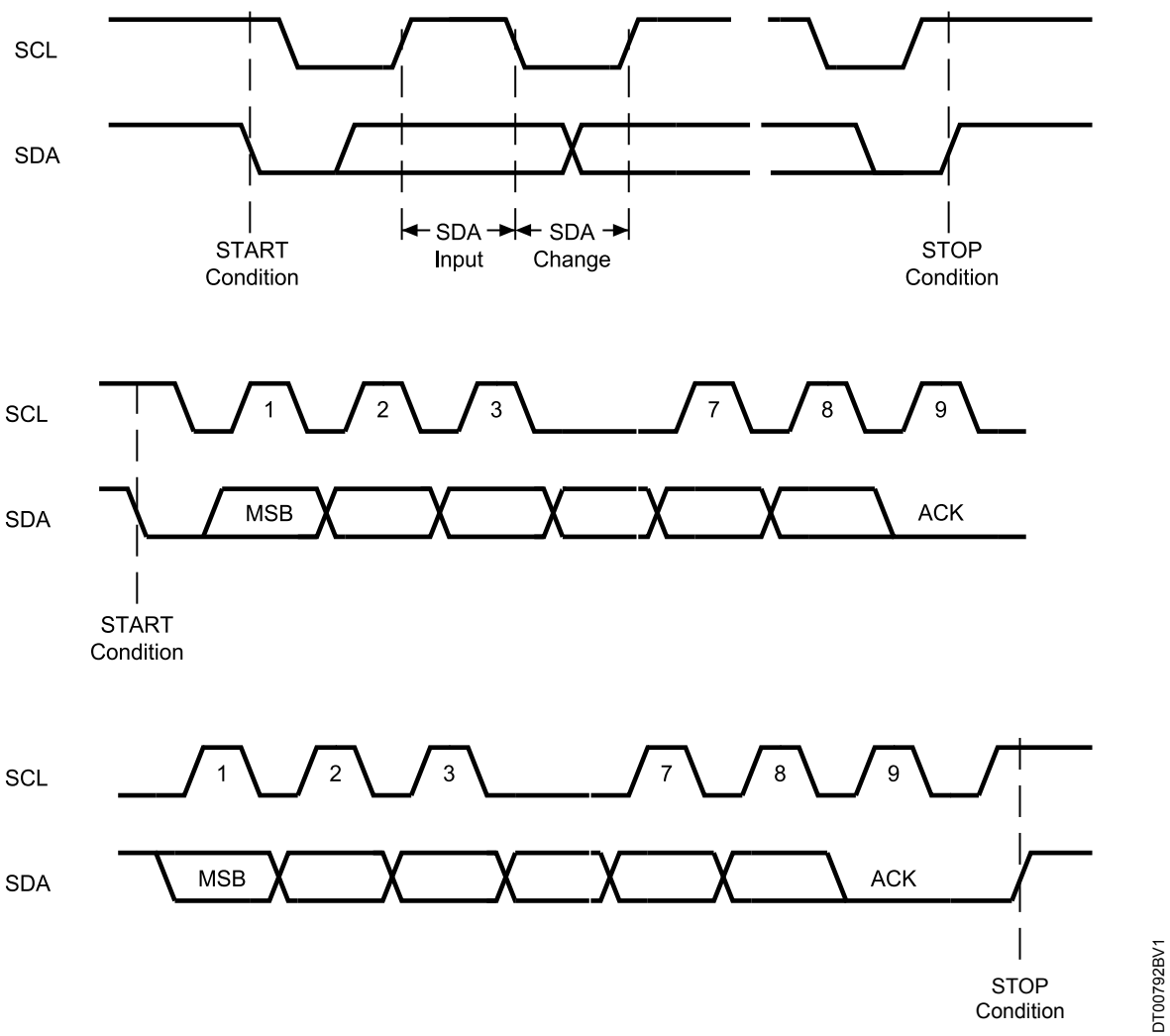
Figure 3. Block diagram



4 Device operation

The device supports the I²C protocol. This is summarized in Figure 4. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus controller, and the other as the target device. A data transfer can only be initiated by the bus controller, which also provides the serial clock for synchronization. The device is always a target in all communications.

Figure 4. I²C bus protocol



4.1 Start condition

Start is identified by a falling edge of serial data (SDA) while serial clock (SCL) is stable in the high state. A start condition must precede any data transfer instruction. The device continuously monitors (except during a write cycle) serial data (SDA) and serial clock (SCL) for a start condition.

4.2 Stop condition

Stop is identified by a rising edge of serial data (SDA) while serial clock (SCL) is stable in the high state. A stop condition terminates communication between the device and the bus controller. A read instruction that is followed by NoACK can be followed by a stop condition to force the device into the standby mode.

A stop condition at the end of a write instruction triggers the internal write cycle.

4.3 Data input

During data input, the device samples serial data (SDA) on the rising edge of serial clock (SCL). For correct device operation, serial data (SDA) must be stable during the rising edge of serial clock (SCL), and the serial data (SDA) signal must change only when serial clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus controller or target device, releases serial data (SDA) after sending eight bits of data. During the ninth clock pulse period, the receiver pulls serial data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus controller and the target device, the bus controller must initiate a Start condition. Following this, the bus controller sends the device select code and byte address as specified in Table 3, and Table 4.

When the device select code is received, the device responds only if the device select code value matches with the values specified in Table 3.

If a match occurs, the corresponding device gives an acknowledgment on serial data (SDA) during the ninth bit time. If the device does not acknowledge the device select code, the device deselects itself from the bus, and goes into standby mode (therefore it does not acknowledge the device select code) after a stop condition.

The eighth bit is the R/W bit ($R\overline{W}$). This bit is set to '1' for read and '0' for write operations.

The 1 Kbytes (8 Kbit) are addressed with 10 address bits, the eight lower address bits being defined by the address byte and the most significant address bits (A9 and A8) being included in the device select code (see Table 3).

Table 3. Device select code

	Device type identifier				Chip enable address	MSB address		$R\overline{W}$
Features	**Bit 7(1)**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0(2)**
Memory	1	0	1	0	0	A9	A8	$R\overline{W}$

1. *MSB is sent first*
2. *LSB*

Note: The most significant bit, b7, is sent first.

Table 4. Byte address

Features	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Memory	A7	A6	A5	A4	A3	A2	A1	A0

Note: The most significant bit, b7, is sent first.

5 Instructions

5.1 Write operations on memory array

Following a start condition, the bus controller sends a device select code with the R/W bit ($R\overline{W}$) reset to 0. The device acknowledges this, as shown in Figure 5. Byte write mode sequences, and waits for one address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus controller generates a stop condition immediately after a data byte ack bit (in the “tenth bit” time slot), either at the end of a byte write or a page write, the internal write cycle (t_W) is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

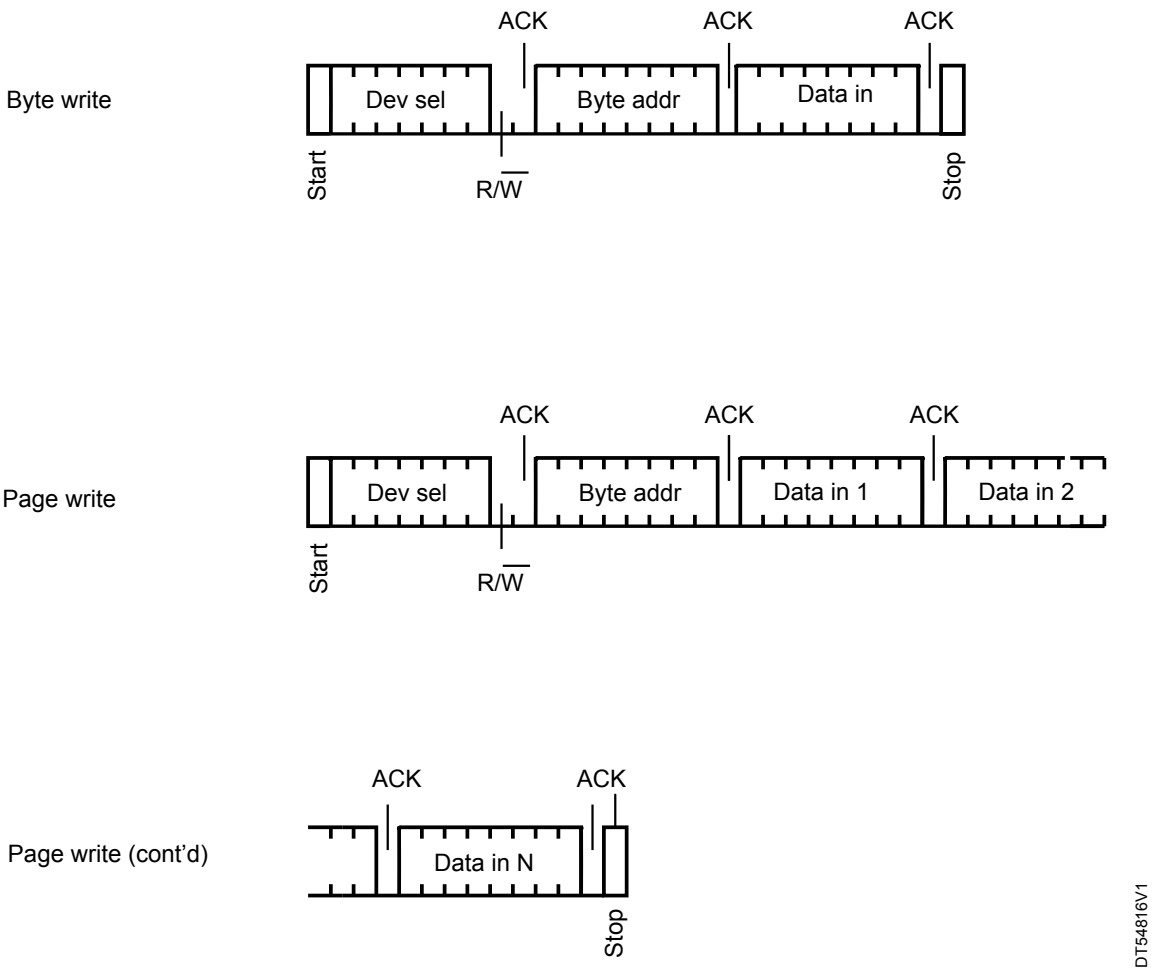
After the stop condition and the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

5.1.1 Byte write

After the device select code and the address byte, the bus controller sends one data byte and the device replies with ACK. The bus controller terminates the transfer by generating a stop condition, as shown in Figure 5 :

Figure 5. Byte write mode sequences



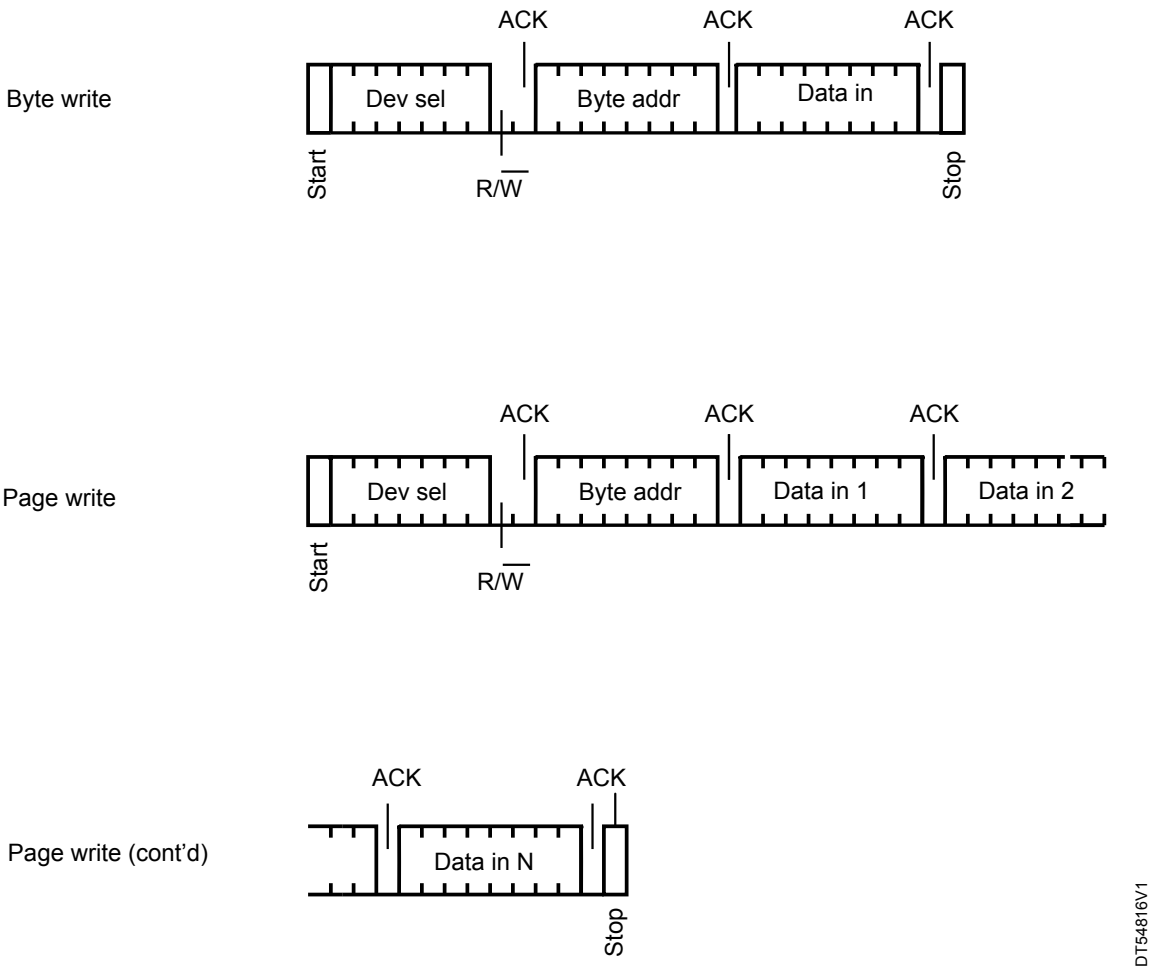
5.1.2 Page write

The page write mode allows up to 16 byte to be written in a single write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A9/A4, are the same. If more bytes are sent (a number higher than the page size), a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus controller sends from 1 to 16 byte of data, each one is acknowledged by the device. The contents of the addressed memory location are then modified, and each data byte is followed by an ACK, as shown in Figure 6. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus controller generating a stop condition.

Figure 6. Page write mode sequences



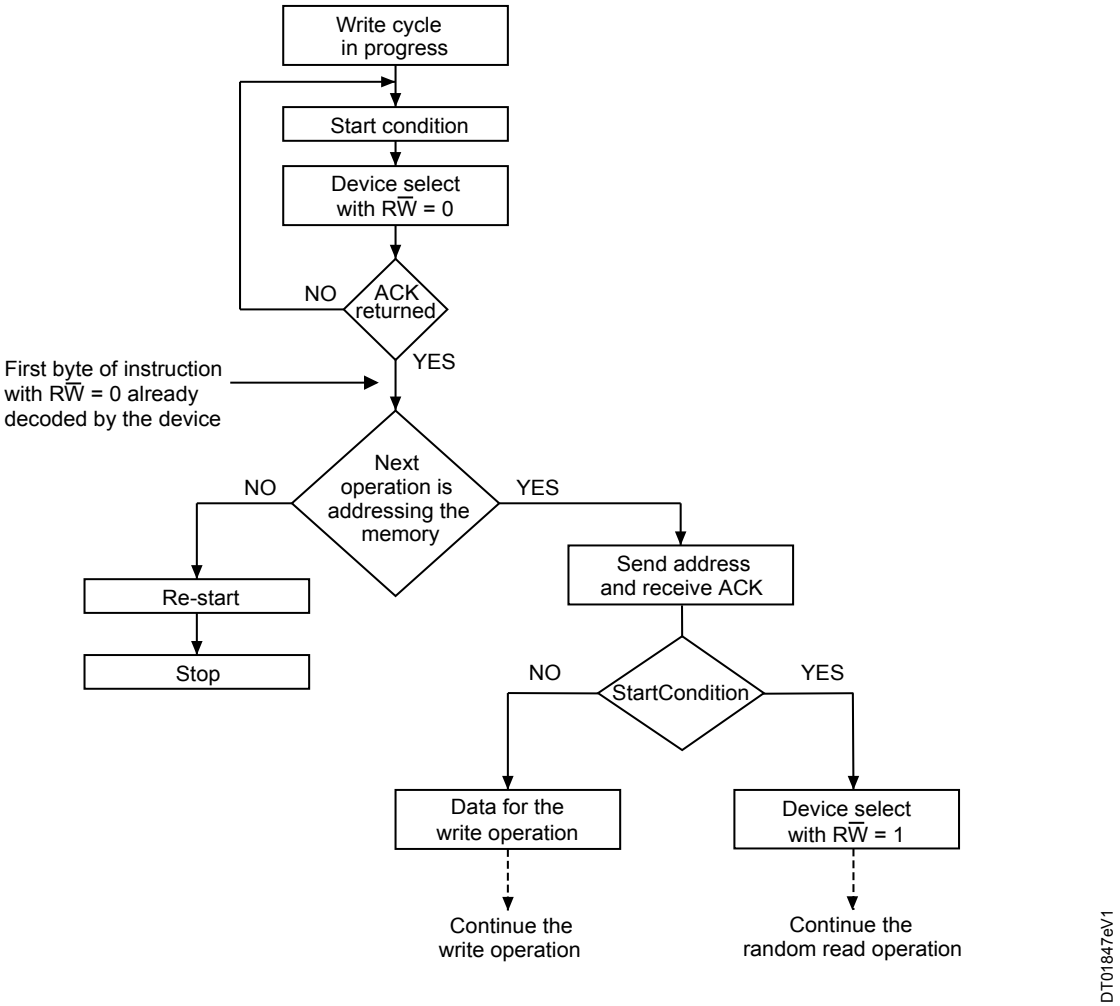
5.1.3 Minimizing write delays by polling on ACK

The maximum write time (t_w) is shown in AC characteristics table in Section 8: DC and AC parameters, but the typical time is shorter. To use this, a polling sequence can be used by the bus controller.

The polling sequence, as shown in Figure 7, is:

- Initial condition: a write cycle is in progress.
- Step 1: the bus controller issues a start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal write cycle, no ACK is returned and the bus controller goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during step 1).

Figure 7. Write cycle polling flow using ACK



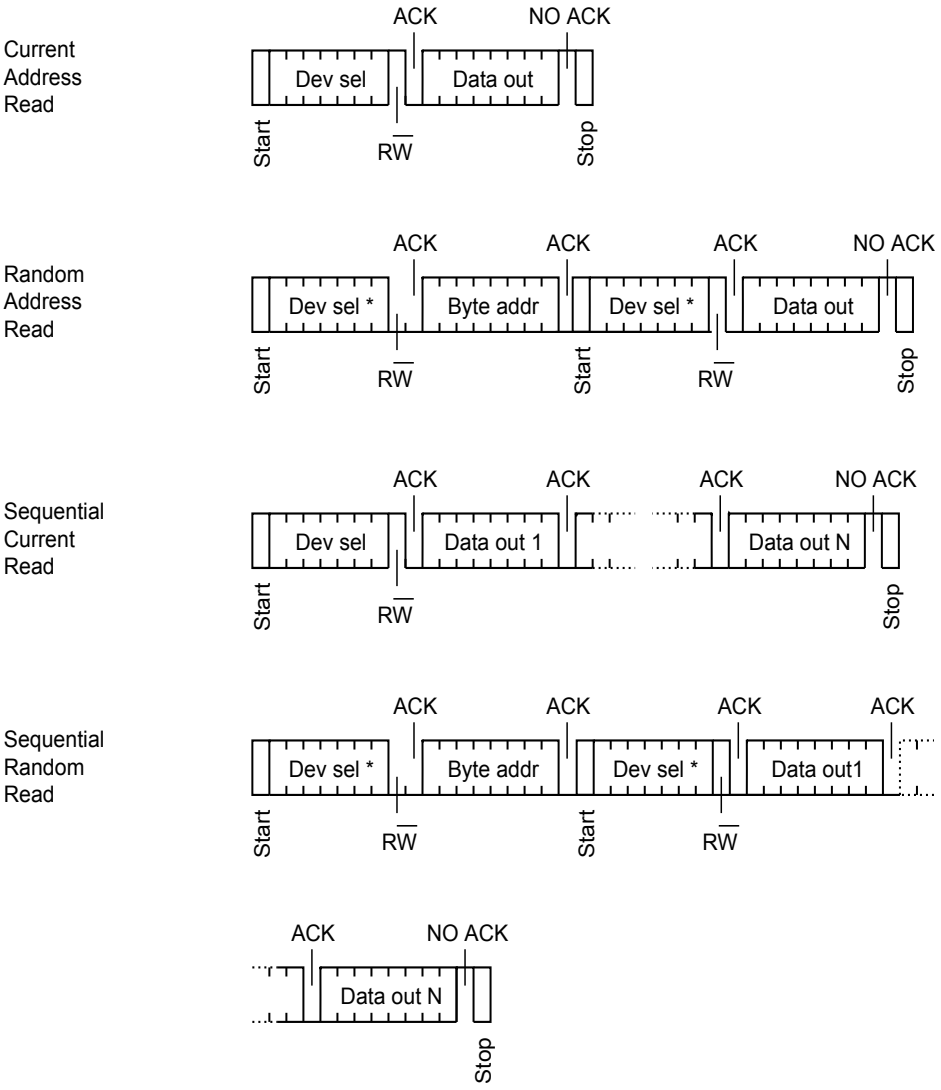
1. *The seven most significant bits of the device select code of a random read (bottom right box in the figure) must be identical to the seven most significant bits of the device select code of the write (polling instruction in the figure).*

5.2 Read operations on memory array

After the successful completion of a read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the read instructions, after each byte read (data out), the device waits for an acknowledgement (data in) during the ninth bit time. If the bus controller does not acknowledge during this ninth time, the device terminates the data transfer and switches to its standby mode.

Figure 8. Read mode sequences



The seven most significant bits of the first device select code of a random read must be identical to the seven most significant bits of the second device select code.

5.2.1 Random address read

A dummy write is first performed to load the address into address counter (as shown in Figure 8) but without sending a stop condition. Then, the bus controller sends another start condition, and repeats the device select code, with the R/W bit ($\overline{RW}$) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. To terminate the transfer, the bus controller must not acknowledge the byte and send a stop condition.

5.2.2 Current address read

For the current address read operation, following a start condition, the bus controller only sends a device select code with the R/W bit ($R\overline{W}$) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus controller terminates the transfer with a stop condition, as shown in Figure 8, without acknowledging the byte.

When accessing the memory, it is safer to always use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory, see Section 5.2.1: Random address read) instead of the current address read instruction.

5.2.3 Sequential read

This operation can be used after a current address read or a random address read. The bus controller does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus controller must not acknowledge the last byte, and must generate a stop condition, as shown in Figure 8.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

6 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh).

7 Maximum rating

Stressing the device outside the ratings listed in Table 5. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at conditions, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	-40	130	°C
T_{STG}	Storage temperature	-65	150	°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	-0.50	6.5	V
V_{CC}	Supply voltage	-0.50	6.5	V
V_{ESD}	Electrostatic pulse (human body model)(1)	-	3000	V

1. *Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001 standard, C1 = 100 pF, R1 = 1500 Ω).*

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 6. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.71	1.89	V
T_A	Ambient operating temperature	-40	85	°C
f_C	Operating clock frequency	-	400	kHz

Table 7. Input parameters

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{IN}(1)	Input capacitance (SDA)	-	-	8	pF
C_{IN}(1)	Input capacitance (other pins)	-	-	6	pF

1. *Specified by design – Not tested in production*

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels(1)	0.315 to 0.855		V
-	Output levels(2)	0.342 to 0.882		V

1. *Timing reference level: 0.25 V_{CC} controller - 0.75 V_{CC} controller*
2. *Timing reference level: 0.3 V_{CC} controller - 0.7 V_{CC} controller*

Figure 9. AC measurement I/O waveform

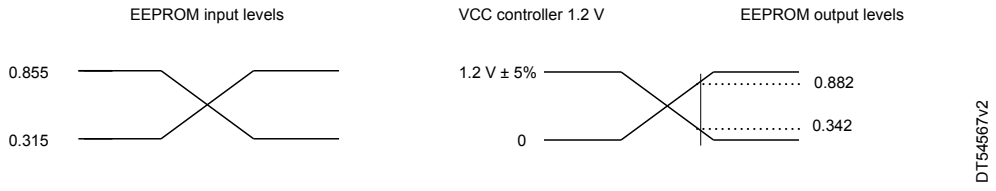


Table 9. Cycling performance

Symbol	Parameter	Test condition	Max	Unit
Ncycle	Write cycle endurance (1)	$T_A \leq$ 25 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)	4,000,000	Write cycle (2)
		T_A = 85 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)	1,200,000	

1. *Evaluated by characterization and qualification- Not tested in production.*
2. *A write cycle is executed when either a page write, or a byte write instruction is decoded.*

Table 10. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention (1)	T_A = 55 °C	200	Year

1. *The data retention behavior is checked in production, while the data retention limit defined in this table is extracted from characterization and qualification results.*

Table 11. DC characteristics

Symbol	Parameter	Test conditions (in addition to those in Table 6)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC} device in standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in high-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V ± 5%	-	0.8(1)	mA
I_{CC0} (2)	Supply current (Write)	During t_W	-	1(3)	mA
I_{CC1}	Standby supply current	Device not selected, (4) V_{IN} = 0 V or 1.14 V	-	1(5)	µA
V_{IL}	Input low voltage (SCL, SDA)	V_{CC} = 1.8 V ± 5%	-0.45	0.315	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.855	1.32	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V	-	0.2	V

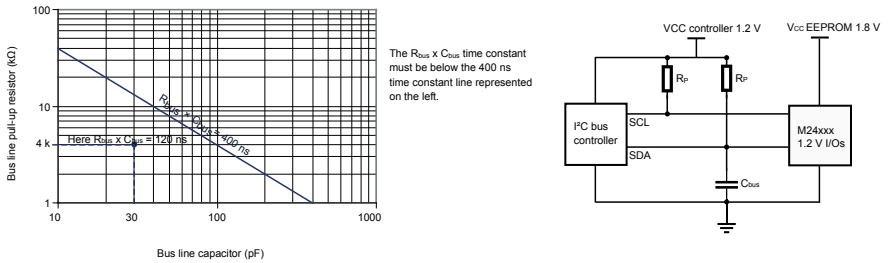
1. *130 µA typical value at 25 °C . Evaluated by characterization - Not tested in production.*
2. *Evaluated by characterization – Not tested in production*
3. *100 µA typical value at 25 °C Evaluated by characterization - Not tested in production*
4. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*
5. *240 nA typical value at 25 °C Evaluated by characterization - Not tested in production*

Table 12. 400 kHz AC characteristics (fast mode)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	400(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	400(3)	ns
t_{DVCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	t_{WR}	Write cycle time	-	5	ms
t_{NS}(1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	100	ns

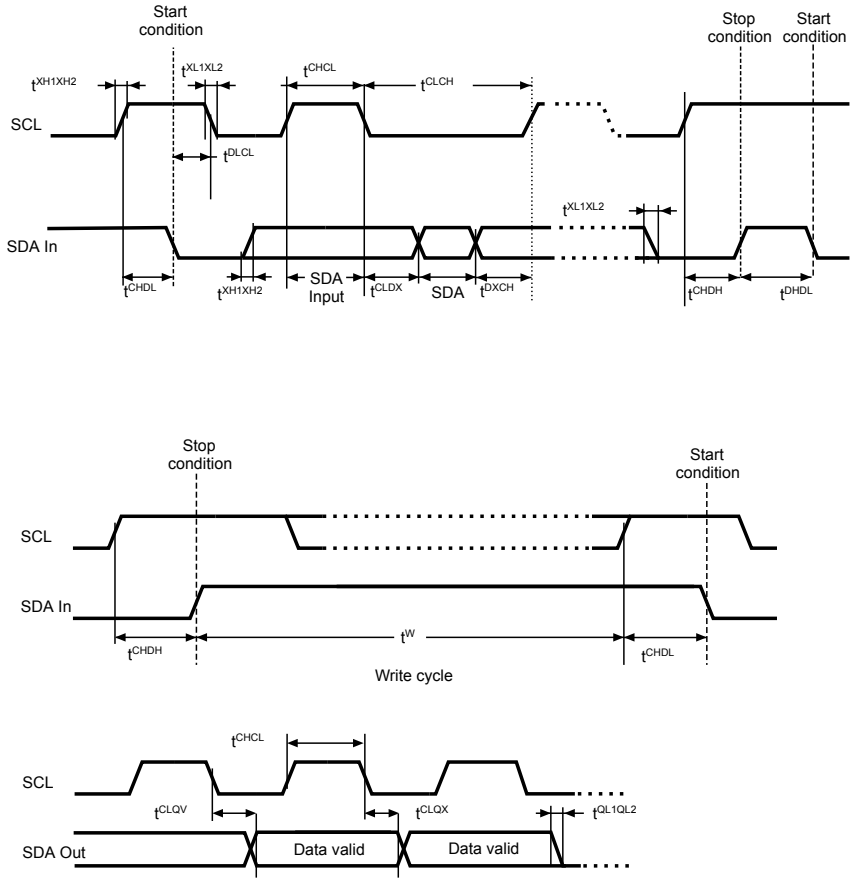
1. *Evaluated by characterization – Not tested in production.*
2. *With C_L = 10 pF.*
3. *It is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.*
4. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.342 V or 0.882 V, assuming that R_{bus} × C_{bus} time constant is within the values specified in Figure 10 .*

Figure 10. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I²C bus at maximum frequency f_C = 400 kHz



DT54568v2

Figure 11. AC waveforms



DT74678v1

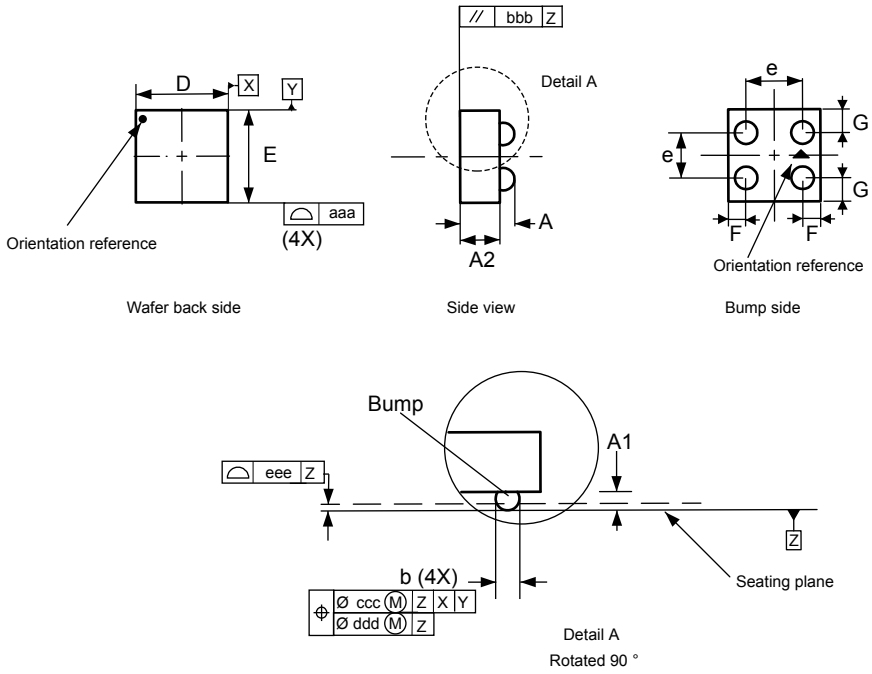
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 WLCSP4 (CT) package information

This WLCSP4 is a 4 ball, 0.703 x 0.713 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 12. WLCSP4 - Outline



(Vc_WLCSP4_ME_V1)

1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

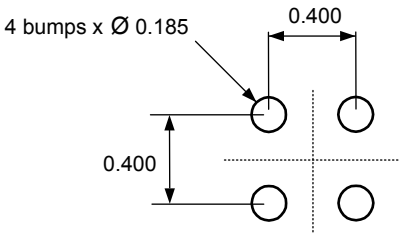
Table 13. **WLCSP4 - Mechanical data**

Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.270	0.295	0.330	0.0106	0.0116	0.0130
A1	-	0.095	-	-	0.0037	-
A2	-	0.200	-	-	0.0079	-
b	-	0.185	-	-	0.0073	-
D	-	0.703	0.723	-	0.0277	0.0285
E	-	0.713	0.733	-	0.0281	0.0288
e	-	0.400	-	-	0.0157	-
F	-	0.152	-	-	0.0060	-
G	-	0.156	-	-	0.0061	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.060	-	-	0.0024	-
eee	-	0.060	-	-	0.0024	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

9.1.1 WLCSP4 package footprint

Figure 13. **WLCSP4 - Footprint example**



(Vc_WLCSP4_FP_V1)

1. Dimensions are expressed in millimeters.

10 Ordering information

Table 14. Ordering information scheme

Example: M24 C08- G CT 6 T P /T

Device type

M24 = I^2C serial access EEPROM

Device function

C08 = 08 Kbit (1 K x 8 bit)

Operating voltage

G = V_{CC} = 1.8 V ± 5% and 1.2 V on I/Os

Package (1)

CT = Thin 4 bump WLCSP

Device grade

6 = Industrial device tested with standard test flow over -40 to 85 °C

Option

T = Tape and reel packing

blank = tube packing

Plating technology

P or G = ECOPACK2

Process(2)

/T = Manufacturing technology code

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).*
2. *The process letter appears on the device package (marking) and on the shipment box. Contact your nearest ST Sales Office for further information.*

Note: Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 15. **Document revision history**

Date	Version	Changes
20-Nov-2024	1	Initial release.

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