LSM6DSV80X

Datasheet

6-axis IMU (inertial measurement unit) with high-*g* accelerometer, embedded AI, and sensor fusion for wearables and sport trackers

LGA-14L
(2.5 x 3.0 x 0.83 mm) typ.

Product status link
LSM6DSV80X

Product summary	
Order code	LSM6DSV80XTR
Temp. range [°C]	-40 to +85
Package	LGA-14L (2.5 x 3.0 x 0.83 mm)
Packing	Tape and reel

Product resources
AN6281 (device application note)
AN6287 (finite state machine)
AN6288 (machine learning core)
TN0018 (design and soldering)

Features

- Dedicated and independent gyroscope, low-*g* and high-*g* accelerometer channels, and data processing
- Smart FIFO up to 4.5 KB
- Dual accelerometer channels
  - Low-*g* channel ±2/±4/±8/±16 *g* full scale
  - High-*g* channel ±32/±64/±80 *g* full scale
- ±250/±500/±1000/±2000/±4000 dps full scale
- SPI / I²C & MIPI I3C® v1.1 serial interface with main processor data synchronization
- Programmable finite state machine for high-*g* and low-*g* accelerometer, gyroscope, and external sensor data processing with high rate @ 960 Hz
- Machine learning core with exportable features and filters for AI applications
- Embedded adaptive self-configuration (ASC)
- Embedded sensor fusion low-power (SFLP) algorithm
- Embedded temperature sensor
- Independent I/O supply
  - I²C voltage range: 1.62 V to 3.6 V
  - SPI / MIPI I3C® extended voltage range: 1.08 V to 3.6 V
- Supply current
  - 6-axis configuration @ 0.67 mA in combo high-performance mode
  - 9-axis configuration @ 0.80 mA in combo high-performance mode
- Compact footprint: 2.5 mm x 3 mm x 0.83 mm
- ECOPACK and RoHS compliant

Applications

- Wearables
- Sport trackers
- High-shock detection
- IoT and connected devices
- Augmented reality (AR) / virtual reality (VR) / mixed reality (MR) applications

Description

The LSM6DSV80X is a breakthrough in the world of wearable technology. Its ability to handle both high and low acceleration values, combined with its energy efficiency and advanced processing capabilities, makes it a sensor for anyone looking to acquire data for in-depth analysis and achieve better performance in high-intensity impact and tracking activities in sports such as volleyball, soccer, tennis, boxing, or explosive jumps, and so forth. This IMU is a comprehensive solution for wearables, high-intensity impact and activity tracking, offering a blend of accuracy, integration, and efficiency.

The LSM6DSV80X is the world's first IMU to combine high-*g* (80 *g*) and low-*g* capabilities in a single package, integrating advanced features (edge processing and sensor fusion) and delivering consistent performance and valuable data for tracking and high-intensity impact detection in sports wearables.

The device enables edge AI, leveraging on a finite state machine (FSM) for configurable motion tracking and a machine learning core (MLC) for context awareness with exportable AI features for wearable applications.

The LSM6DSV80X supports the adaptive self-configuration (ASC) feature, which allows automatically reconfiguring the device in real time based on the detection of a specific motion pattern or based on the output of a specific decision tree configured in the MLC, without any intervention from the host processor.

1 Overview

The LSM6DSV80X is a 6-axis system-in-package featuring a high-performance 3-axis digital low-*g* accelerometer (16 *g*), a 3-axis digital high-*g* accelerometer (80 *g*), and a 3-axis digital gyroscope.

The LSM6DSV80X delivers best-in-class motion sensing that can detect high-intensity impacts in order to empower developers to improve tracking in sports activities by accurately measuring both high and low accelerations efficiently. Whether it is the high-intensity forces in sports or the movements in everyday tracking, the LSM6DSV80X delivers consistent performance and valuable data for analysis.

The event-detection interrupts enable efficient and reliable motion tracking and context awareness, implementing hardware recognition of free-fall events, 6D orientation, click and double-click sensing, activity or inactivity, stationary/motion detection and wake-up events. Machine learning and finite state machine processing allow moving some algorithms from the application processor to the LSM6DSV80X sensor, enabling consistent reduction of power consumption.

The device supports the main OS requirements, offering real, virtual, and batch mode sensors. In particular, the LSM6DSV80X is designed to detect significant motion tracking, stationary/motion states, tilt, pedometer functions, timestamping and to support the data acquisition of external sensors.

The LSM6DSV80X offers hardware flexibility to connect the pins with different mode connections to external sensors to expand functionalities such as adding a sensor hub.

Channel 1 is designed to track motion detection. Data are available on the output of the I²C / SPI / I3C for the accelerometer and gyroscope with independent ODR and FS.

Channel 2 is designed for high-*g* applications with accelerometer processing and independent FS from ±32 *g* to ±80 *g*.

Up to 4.5 KB of FIFO with compression and dynamic allocation of significant data (that is, external sensors, timestamp, and so forth) allows overall power saving of the system.

The LSM6DSV80X embeds a sensor fusion low-power (SFLP) algorithm able to provide a 6-axis (accelerometer + gyroscope) game rotation vector represented as a quaternion. The X, Y, Z quaternion components are stored in FIFO.

Like the entire portfolio of MEMS sensor modules, the LSM6DSV80X leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The device embeds advanced dedicated features like a finite state machine and data filtering for motion processing.

The LSM6DSV80X is available in a small plastic, land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultracompact solutions.

2 Embedded low-power features

The LSM6DSV80X features the following on-chip functions:

- 4.5 KB FIFO data buffering, data can be compressed two or three times
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable)
  - Free-fall
  - Wake-up
  - 6D orientation
  - Click and double-click sensing
  - Activity/inactivity recognition
  - Stationary/motion detection
  - High-*g* wake-up and high-*g* shock
- Specific IP blocks (called "embedded functions") with negligible power consumption and high performance
  - Pedometer functions: step detector and step counters
  - Tilt
  - Significant motion detection
  - Finite state machine (FSM)
  - Machine learning core (MLC) with exportable features and filters for AI applications
  - Adaptive self-configuration (ASC)
  - Embedded sensor fusion low-power (SFLP) algorithm
- Sensor hub
  - Up to six total sensors: two internal (accelerometer and gyroscope) and four external sensors

2.1 Pedometer functions: step detector and step counters

The LSM6DSV80X embeds an advanced pedometer with an algorithm running in an ultralow-power domain in order to ensure extensive battery life in battery-constrained applications.

Leveraging enhanced configurability, the advanced embedded pedometer is suitable for a large range of applications from mobile to wearable devices.

The algorithm processes and analyzes the accelerometer waveform in order to count the user's steps during walking and running activities.

The pedometer works at 30 Hz and it is not affected by the selected device power mode (ultralow-power, low-power, high-performance), thus guaranteeing an ultralow-power experience and extreme flexibility in conjunction with other device functionalities.

The pedometer output can be batched in the device's FIFO buffer, in order to decrease overall system supply current.

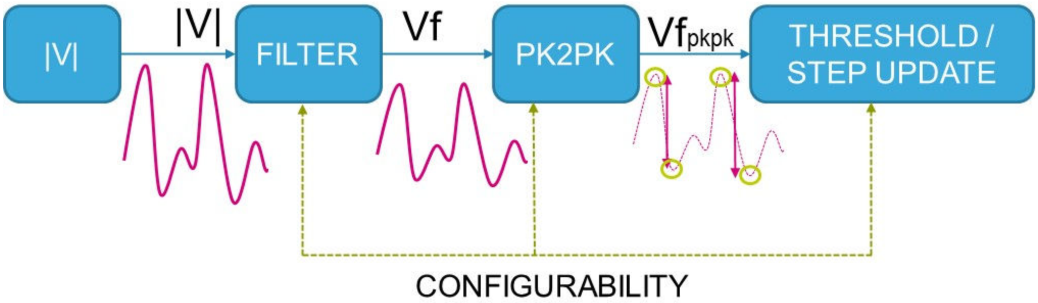
ST freely provides the support and the tools for easily configuring the device and tuning the algorithm configuration for a best-in-class user experience.

2.2 Pedometer algorithm

The pedometer algorithm is composed of a cascade of four stages:

1. Computation of the acceleration magnitude signal in order to detect the signal independently from device orientation;
2. FIR filter to extract relevant frequency components and to smooth the signal by cutting off high frequencies;
3. Peak detector to find the maximum and minimum of the waveform and compute the peak-to-peak value;
4. Step count: if the peak-to-peak value is greater than the settled threshold, a step is counted.

Figure 1. Four-stage pedometer algorithm



The LSM6DSV80X embeds a dynamic internal threshold for step detection that is updated after each peak-to-peak evaluation: the internal threshold is increased with a configurable speed if a step is detected or decreased with a configurable speed if a step is not detected.

This approach ensures high accuracy when the user starts to walk and a false peak rejection when the user is walking or running.

An internal configurable debounce algorithm can be also set to filter false walks: indeed, an accelerometer pattern is recognized as a walk or run only if a minimum number of steps are counted.

The LSM6DSV80X has been designed to reject a false-positive signal inside the algorithm core.

On top of the mechanisms detailed above, the LSM6DSV80X allows enabling and configuring a dedicated false-positive rejection block to further boost pedometer accuracy.

2.3 Tilt detection

The tilt function helps to detect activity change and has been implemented in hardware using only the accelerometer to achieve targets of both ultralow power consumption and robustness during the short duration of dynamic accelerations.

The tilt function is based on a trigger of an event each time the device's tilt changes and can be used with different scenarios, for example:

- Triggers when a phone is in a front pants pocket and the user goes from sitting to standing or standing to sitting;
- Does not trigger when a phone is in a front pants pocket and the user is walking, running, or going upstairs.

2.4 Significant motion detection

The significant motion detection (SMD) function generates an interrupt when a ‘significant motion’, that could be due to a change in user location, is detected. In the LSM6DSV80X device this function has been implemented in hardware using only the accelerometer.

SMD functionality can be used in location-based applications in order to receive a notification indicating when the user is changing location.

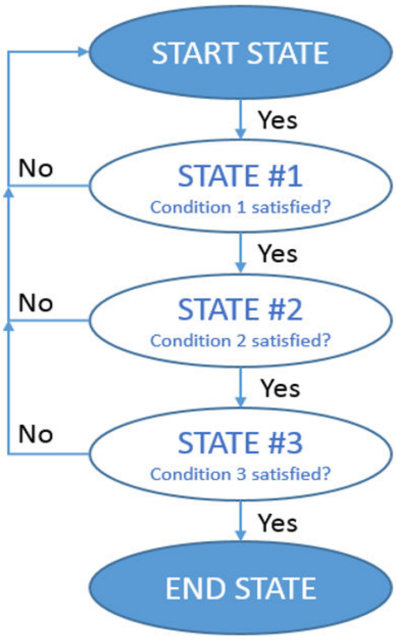
2.5 Finite state machine

The LSM6DSV80X can be configured to generate interrupt signals activated by user-defined motion patterns. To do this, up to 8 embedded finite state machines can be programmed independently for motion detection such as glance gestures, absolute wrist tilt, shake and double-shake detection.

Definition of finite state machine

A state machine is a mathematical abstraction used to design logic connections. It is a behavioral model composed of a finite number of states and transitions between states, similar to a flow chart in which one can inspect the way logic runs when certain conditions are met. The state machine begins with a start state, goes to different states through transitions dependent on the inputs, and can finally end in a specific state (called stop state). The current state is determined by the past states of the system. The following figure shows a generic state machine.

Figure 2. Generic state machine

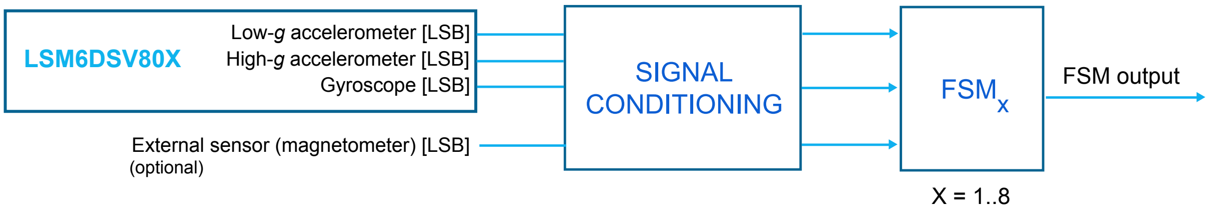


Finite state machine in the LSM6DSV80X

The LSM6DSV80X works as a combo accelerometer-gyroscope sensor, generating acceleration and angular rate output data. It is also possible to connect an external sensor like a magnetometer or pressure sensor by using the sensor hub feature (mode 2). These data can be used as input of up to 8 programs in the embedded finite state machine (Figure 3. State machine in the LSM6DSV80X).

All 8 finite state machines are independent: each one has its dedicated memory area and it is independently executed. An interrupt is generated when the end state is reached or when some specific command is performed.

Figure 3. State machine in the LSM6DSV80X



High-*g* peak tracking feature

The high-*g* accelerometer peak tracking feature allows monitoring the magnitude of the high-*g* accelerometer within a time window that can be defined by issuing dedicated commands from the finite state machine. When issuing the command related to the end of the monitoring window, this feature stores the high-*g* accelerometer three-axis components of the detected peak in the FIFO with a dedicated TAG.

2.6 Machine learning core

The LSM6DSV80X embeds a dedicated core for machine learning processing that provides system flexibility, allowing some algorithms run in the application processor to be moved to the MEMS sensor with the advantage of consistent reduction in power consumption.

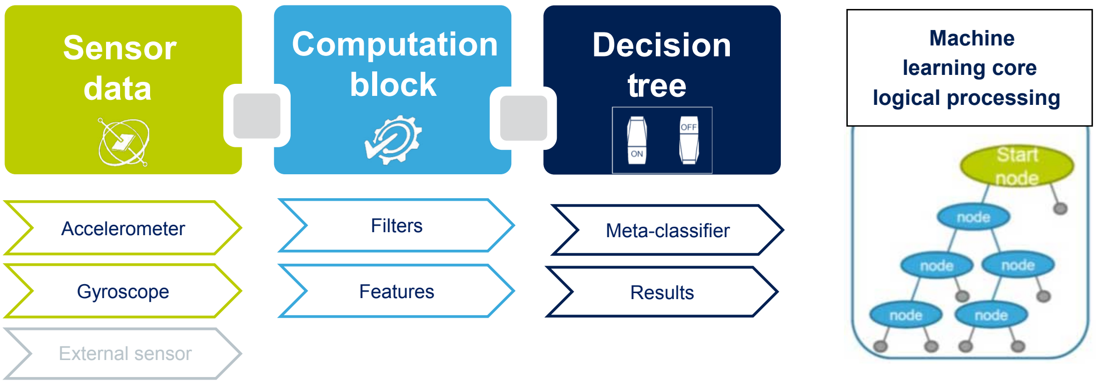
Machine learning core logic allows identifying if a data pattern (for example motion, pressure, temperature, magnetic data, and so forth) matches a user-defined set of classes. Typical examples of applications could be activity detection like running, walking, driving, and so forth.

The LSM6DSV80X machine learning core works on data patterns coming from the low-*g*, high-*g* accelerometer and gyroscope sensors, but it is also possible to connect and process external sensor data (like magnetometer or pressure sensor) by using the sensor hub feature (mode 2).

The input data can be filtered using a dedicated configurable computation block containing filters and features computed in a fixed time window defined by the user. Computed feature values and filtered data values can also be read through the FIFO buffer.

Machine learning processing is based on logical processing composed of a series of configurable nodes characterized by "if-then-else" conditions where the "feature" values are evaluated against defined thresholds.

Figure 4. Machine learning core in the LSM6DSV80X



The LSM6DSV80X can be configured to run up to 8 decision trees simultaneously and independently and every decision tree can generate up to 16 results. The total number of nodes can be up to 256.

The results of the machine learning processing are available in dedicated output registers readable from the application processor at any time.

The LSM6DSV80X machine learning core can be configured to generate an interrupt when a change in the result occurs.

2.7 Adaptive self-configuration (ASC)

The LSM6DSV80X supports the adaptive self-configuration (ASC) feature, which allows the FSM to automatically reconfigure the device in real time based on the detection of a specific motion pattern or based on the output of a specific decision tree configured in the MLC, without any intervention from the host processor. The FSM can write a subset of the device registers using the SETR command, which allows indicating the register address and the new value to be written in such a register. The access to these device registers is mutually exclusive to the host.

2.8 Sensor fusion low power

A sensor fusion low-power (SFLP) block is available in the LSM6DSV80X for generating the following data based on the (low-*g*) accelerometer and gyroscope data processing:

- Game rotation vector, which provides a quaternion representing the attitude of the device
- Gravity vector, which provides a three-dimensional vector representing the direction of gravity
- Gyroscope bias, which provides a three-dimensional vector representing the gyroscope bias

The SFLP block is enabled by setting the SFLP_GAME_EN bit to 1 of the EMB_FUNC_EN_A (04h) embedded functions register.

The SFLP block can be reinitialized by setting the SFLP_GAME_INIT bit to 1 of the EMB_FUNC_INIT_A (66h) embedded functions register.

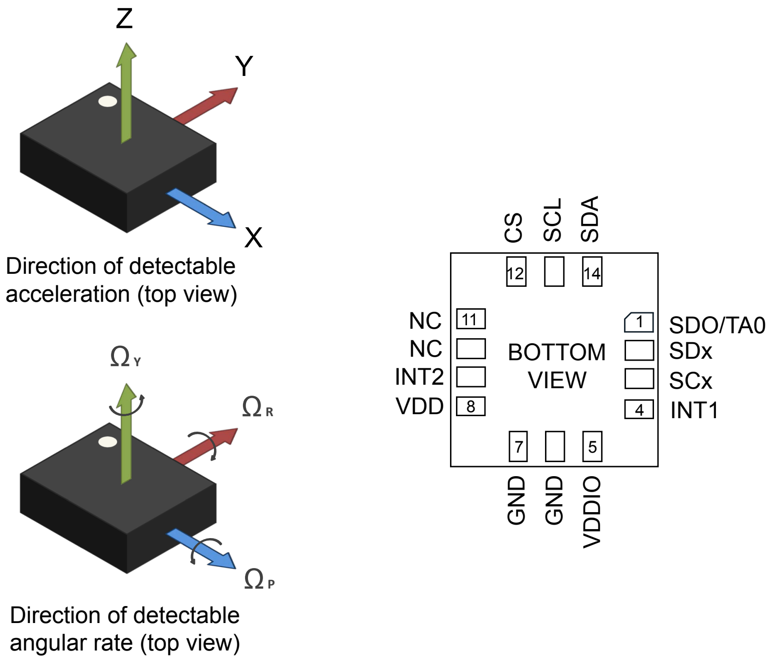
Table 1. Sensor fusion performance

Parameter		Value
Static accuracy	heading / yaw	0.5 deg. / 5 minutes
	pitch	1.5 deg.
	roll	1.5 deg.
Low dynamic accuracy	heading / yaw	0.7 deg. / 5 minutes
	pitch	0.5 deg.
	roll	0.5 deg.
High dynamic accuracy	heading / yaw	5.9 deg. / 5 minutes
	pitch	1.6 deg.
	roll	1.2 deg.
Calibration time		0.8 seconds[1]
Orientation stabilization time		0.7 seconds

1. *Time required to reach steady state*

3 Pin description

Figure 5. Pin connections

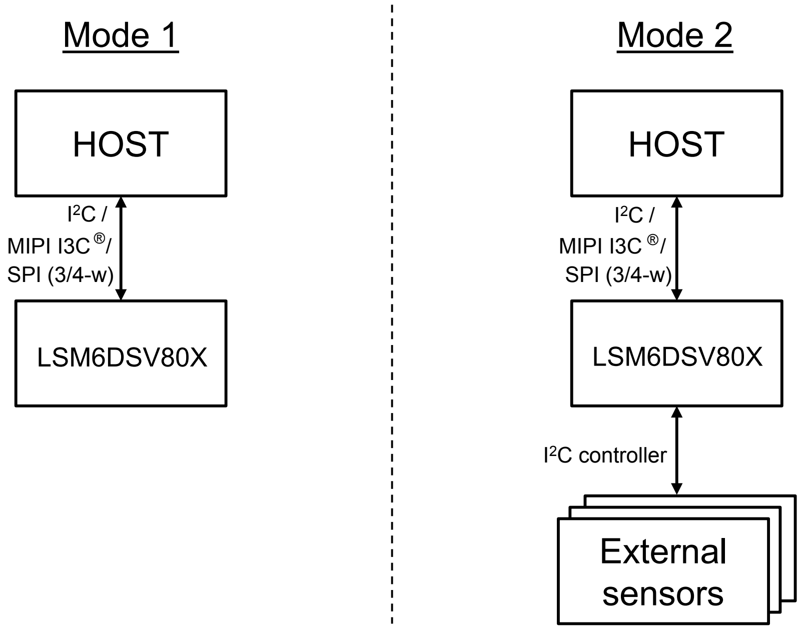


3.1 Pin connections

The LSM6DSV80X offers flexibility to connect the pins in order to have three different mode connections and functionalities. In detail:

- **Mode 1**: I²C / MIPI I3C® target interface or SPI (3- and 4-wire) serial interface is available.
- **Mode 2**: I²C / MIPI I3C® target interface or SPI (3- and 4-wire) serial interface and I²C controller interface for external sensor connections are available.

Figure 6. **LSM6DSV80X connection modes**



In the following table, each mode is described for the pin connections and function.

Table 2. Pin description

Pin#	Name	Mode 1 function	Mode 2 function
1	SDO TA0	SPI 4-wire interface serial data output (SDO) I²C least significant bit of the device address (TA0)	SPI 4-wire interface serial data output (SDO) I²C least significant bit of the device address (TA0)
2	SDx	Connect to VDDIO or GND	I²C controller serial data (CSDA)
3	SCx	Connect to VDDIO or GND	I²C controller serial clock (CSCL)
4	INT1	Programmable interrupt in I²C and SPI	
5	VDDIO(1)	Power supply for I/O pins	
6	GND	0 V supply	
7	GND	0 V supply	
8	VDD(1)	Power supply	
9	INT2	Programmable interrupt 2 (INT2)	Programmable interrupt 2 (INT2) I²C controller external synchronization signal (CDRDY)
10	NC	Leave unconnected(2)	Leave unconnected(2)
11	NC	Leave unconnected(2)	Leave unconnected(2)
12	CS	I²C / MIPI I3C® / SPI mode selection (1: SPI idle mode / I²C / MIPI I3C® communication enabled; 0: SPI communication mode / I²C / MIPI I3C® disabled)	I²C / MIPI I3C® / SPI mode selection (1: SPI idle mode / I²C / MIPI I3C® communication enabled; 0: SPI communication mode / I²C / MIPI I3C® disabled)
13	SCL	I²C / MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)	I²C / MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)
14	SDA	I²C / MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	I²C / MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

1. *Recommended 100 nF filter capacitor.*
2. *Leave pin electrically unconnected and soldered to PCB.*

4 Module specifications

4.1 Mechanical characteristics

@ VDD = 1.8 V, T = 25°C, unless otherwise noted.

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range (low-*g*)			±2		*g*
				±4		
				±8		
				±16		
	Linear acceleration measurement range (high-*g*)			±32		
				±64		
				±80		
G_FS	Angular rate measurement range			±250		dps
				±500		
				±1000		
				±2000		
				±4000		
LA_So	Linear acceleration sensitivity (low-*g*)	FS = ±2 *g*		0.061		m*g*/LSB
		FS = ±4 *g*		0.122		
		FS = ±8 *g*		0.244		
		FS = ±16 *g*		0.488		
	Linear acceleration sensitivity (high-*g*)	FS = ±32 *g*		0.976		m*g*/LSB
		FS = ±64 *g*		1.952		
		FS = ±80 *g*		3.904		
G_So	Angular rate sensitivity[2]	FS = ±250 dps		8.75		mdps/LSB
		FS = ±500 dps		17.50		
		FS = ±1000 dps		35		
		FS = ±2000 dps		70		
		FS = ±4000 dps		140		
G_So%	Sensitivity tolerance[2]	at component level		±0.3		%
LA_SoDr	Linear acceleration sensitivity change vs. temperature (low-*g*)[3]	from -40°C to +85°C		±0.01		%/°C
	Linear acceleration sensitivity change vs. temperature (high-*g*)[3]	from -40°C to +85°C		±0.01		%/°C
G_SoDr	Angular rate sensitivity change vs. temperature[3]	from -40°C to +85°C		±0.007		%/°C
LA_TyOff	Linear acceleration zero-*g* level offset accuracy (low-*g*)[4]			±12		m*g*
	Linear acceleration zero-*g* level offset accuracy (high-*g*)[4]			±1.5		*g*
G_TyOff	Angular rate zero-rate level[4]			±1		dps
LA_OffDr	Linear acceleration zero-*g* level change vs. temperature (low-*g*)[3]			±0.07		m*g*/°C
	Linear acceleration zero-*g* level change vs. temperature (high-*g*)[3]			±2		m*g*/°C
G_OffDr	Angular rate typical zero-rate level change vs. temperature[3]			±0.006		dps/°C

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
Rn	Rate noise density in high-performance mode[5]	FS = ±250 dps - ±4000 dps		3.8		mdps/√Hz
An	Acceleration noise density (low-*g*) in high-performance mode[6]	FS = ±2 *g* - ±16 *g*		60		μg/√Hz
	Acceleration noise density (high-*g*) in high-performance mode	FS = ±32 *g* - ±80 *g*		1000		μg/√Hz
	Acceleration noise density in normal mode (low-*g*)[7][8]	FS = ±2 *g* - ±16 *g*		100		μg/√Hz
RMS	Accelerometer RMS noise in low-power mode (low-*g*)	LPM1		2.7		*mg* RMS
		LPM2		2.1		
		LPM3		1.5		
LA_ODR	Linear acceleration output data rate (low-*g*)			1.875[9] 7.5 15 30 60 120 240 480 960 1.92 k 3.84 k 7.68 k		Hz
G_ODR	Angular rate output data rate			7.5 15 30 60 120 240 480 960 1.92 k 3.84 k 7.68 k		
HAODR	ODR variation over temperature and supply range in high-accuracy mode[10]	Gyro on			±1	%
		Gyro off			±3	
Vst	Linear acceleration self-test output change (low-*g*)[11][12][13]		50		1700	*mg*
	Linear acceleration self-test output change (high-*g*)[11][12][13]		150		2500	*mg*
	Angular rate self-test output change[14][15]	FS = ±250 dps	20		80	dps
		FS = ±4000 dps	150		700	dps
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed.*
2. *Preliminary sensitivity tolerance for FS at ±250 dps on first eng. samples*
3. *Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured during final test for production.*
4. *Value after calibration.*
5. *Gyroscope rate noise density in high-performance mode is independent of the ODR and FS setting*
6. *Accelerometer noise density in high-performance mode is independent of the selected ODR and FS.*

7. *Accelerometer noise density in normal mode is independent of the ODR and FS setting.*
8. *Noise RMS related to BW = ODR/2.*
9. *This ODR is available when the accelerometer is in low-power mode.*
10. *Values specified by design.*
11. *The sign of the linear acceleration self-test output change is defined by the ST_XL_[1:0] bits in a dedicated register for all axes.*
12. *The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 0.061 mg at ±2 g full scale.*
13. *Accelerometer self-test limits are full-scale independent.*
14. *The sign of the angular rate self-test output change is defined by the ST_G_[1:0] bits in a dedicated register for all axes.*
15. *The angular rate self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 70 mdps at ±4000 dps full scale.*

4.2 Electrical characteristics

@ VDD = 1.8 V, T = 25°C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
VDD	Supply voltage		1.71	1.8	3.6	V
VDDIO	Power supply for I/O		1.08		3.6	V
IddHP	Gyroscope and low-*g* accelerometer supply current in high-performance mode			0.670		mA
IddHPC9	Gyroscope and accelerometer supply current in high-performance mode			0.8		mA
LA_IddHP	Accelerometer supply current in high-performance mode (low-*g*)			200		µA
	Accelerometer supply current in high-performance mode (high-*g*)			225		
LA_IddNM	Accelerometer supply current in normal mode (low-*g*)			115		µA
LA_IddLPM2	Accelerometer supply current in low-power mode (LPM2) (low-*g*)	ODR = 60 Hz		21		µA
		ODR = 1.875 Hz		4.6		
LA_IddLPM1	Accelerometer supply current in low-power mode (LPM1) (low-*g*)	ODR = 60 Hz		18		µA
		ODR = 1.875 Hz		4.5		
IddPD	Supply current during power-down			2.9		µA
Ton	Turn-on time - gyroscope			40		ms
V_{IH}	Digital high-level input voltage	VDDIO = 1.8 V (typ)	0.7 * VDDIO			V
		VDDIO = 1.2 V (typ)	0.8 * VDDIO			
V_{IL}	Digital low-level input voltage	VDDIO = 1.8 V (typ)			0.3 * VDDIO	V
		VDDIO = 1.2 V (typ)			0.2 * VDDIO	
V_{OH}	High-level output voltage	VDDIO = 1.8 V I_{OH} = 4 mA[2]	VDDIO - 0.2			V
		VDDIO = 1.2 V I_{OH} = 2 mA[2]	VDDIO - 0.2			
V_{OL}	Low-level output voltage	Vdd_IO = 1.8 V I_{OL} = 4 mA[2]			0.2	V
		VDDIO = 1.2 V I_{OH} = 2 mA[2]	VDDIO - 0.2			
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed.*
2. *I_{OL}/I_{OH} are the driving capabilities, that is, the DC currents that can be sourced/sunk by the digital pin to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.*

4.3 Temperature sensor characteristics

@ VDD = 1.8 V, T = 25°C unless otherwise noted.

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ. (1)	Max.	Unit
TODR(2)	Temperature refresh rate			60		Hz
Toff	Temperature offset(3)		-15		+15	°C
TSen	Temperature sensitivity			256		LSB/°C
TST	Temperature stabilization time(4)				500	µs
T_ADC_res	Temperature ADC resolution			16		bit
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed*
2. *When the accelerometer is in low-power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.*
3. *The output of the temperature sensor is 0 LSB (typ.) at 25°C.*
4. *Time from power ON to valid data based on characterization data.*

4.4 Communication interface characteristics

4.4.1 SPI - serial peripheral interface

Subject to general operating conditions for VDD and Top. @VDDIO = 1.8 V, T = 25°C unless otherwise noted.

Table 6. SPI target timing values (VDDIO at 1.8 V)

Symbol	Parameter	Value[1]			Unit
		Min	Typ	Max	
$f_{c(SPC)}$	SPI clock frequency			10	MHz
$t_{c(SPC)}$	SPI clock period	100			ns
$t_{high(SPC)}$	SPI clock high period	45			
$t_{low(SPC)}$	SPI clock low period	45			
$t_{su(CS)}$	CS setup time (mode 3)	5			
	CS setup time (mode 0)	20			
$t_{h(CS)}$	CS hold time (mode 3)	20			
	CS hold time (mode 0)	20			
$t_{su(SI)}$	SDI input setup time	5			
$t_{h(SI)}$	SDI input hold time	15			
$t_{v(SO)}$	SDO valid output time		15	25	
$t_{dis(SO)}$	SDO output disable time			50	
C_{load}	Bus capacitance			100	pF

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*

Subject to general operating conditions for VDD and Top. @VDDIO = 1.2 V, T = 25°C unless otherwise noted.

Table 7. SPI target timing values (VDDIO at 1.2 V)

Symbol	Parameter	Value[1]			Unit
		Min	Typ	Max	
$f_{c(SPC)}$	SPI clock frequency			10	MHz
$t_{c(SPC)}$	SPI clock period	100			ns
$t_{high(SPC)}$	SPI clock high period	45			
$t_{low(SPC)}$	SPI clock low period	45			
$t_{su(CS)}$	CS setup time (mode 3)	25			
	CS setup time (mode 0)	50			
$t_{h(CS)}$	CS hold time (mode 3)	50			
	CS hold time (mode 0)	50			
$t_{su(SI)}$	SDI input setup time	15			
$t_{h(SI)}$	SDI input hold time	30			
$t_{v(SO)}$	SDO valid output time			30	
$t_{dis(SO)}$	SDO output disable time			50	
C_{load}	Bus capacitance			50	pF

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*

Figure 7. **SPI target timing in mode 0**

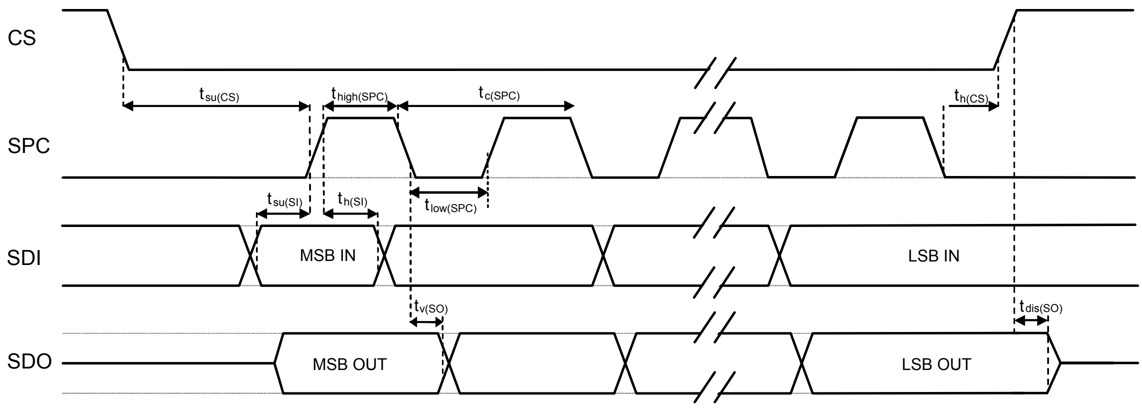
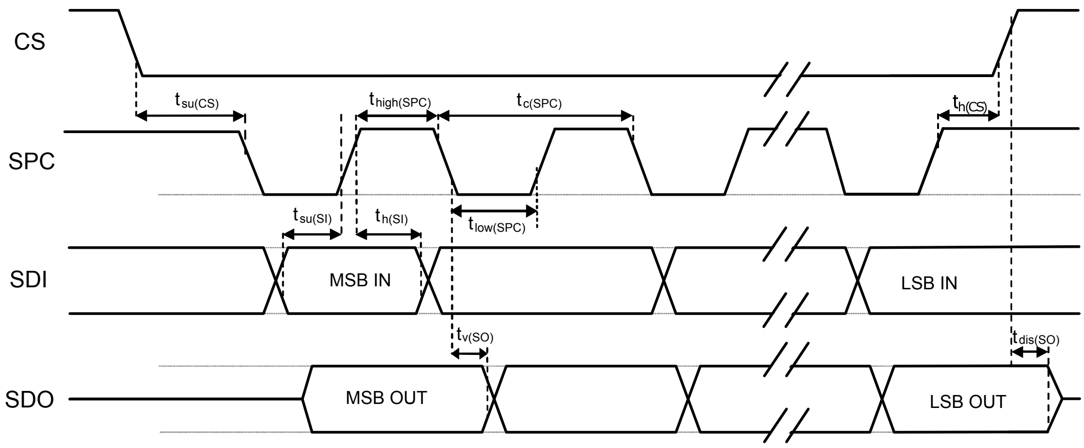


Figure 8. **SPI target timing in mode 3**



Note: Measurement points are done at 0.3·VDDIO and 0.7·VDDIO for both input and output ports.

4.4.2 I²C - inter-IC control interface

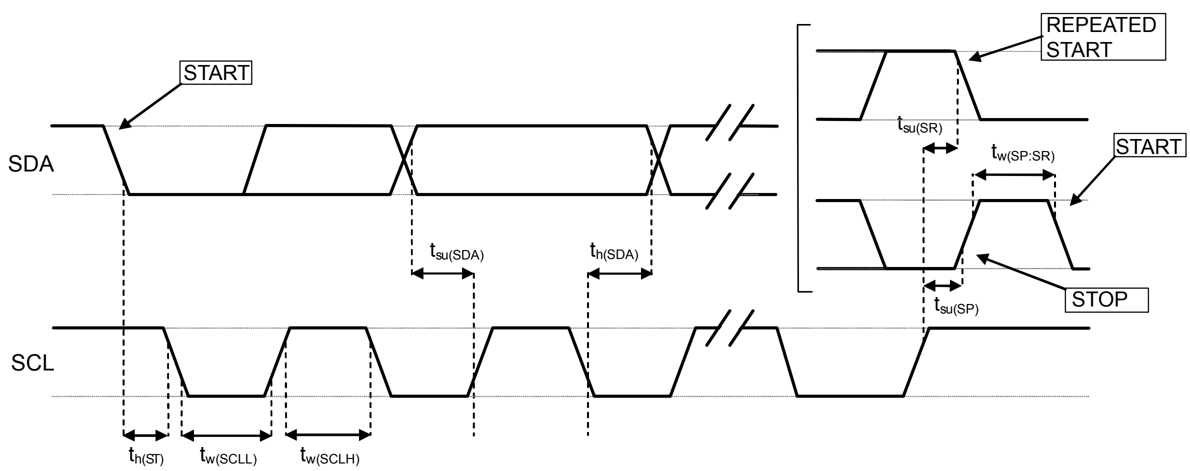
Subject to general operating conditions for VDD and Top.

Table 8. I²C target timing values

Symbol	Parameter	I²C fast mode(1)(2)		I²C fast mode plus(1)(2)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	400	0	1000	kHz
$t_{w(SCLL)}$	SCL clock low period	1.3		0.5		μs
$t_{w(SCLH)}$	SCL clock high period	0.6		0.26		
$t_{su(SDA)}$	SDA setup time	100		50		ns
$t_{h(SDA)}$	SDA data hold time	0	0.9	0		μs
$t_{h(ST)}$	START/REPEATED START condition hold time	0.6		0.26		
$t_{su(SR)}$	REPEATED START condition setup time	0.6		0.26		
$t_{su(SP)}$	STOP condition setup time	0.6		0.26		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	1.3		0.5		
	Data valid time		0.9		0.45	
	Data valid acknowledge time		0.9		0.45	
C_B	Capacitive load for each bus line		400		550(3)	pF

1. *Data based on standard I²C protocol requirement, not tested in production.*
2. *Data for I²C fast mode and I²C fast mode plus have been validated by characterization, not tested in production.*
3. *Maximum capacitive load if VDDIO ≥ 1.62 V. If VDDIO < 1.62 V, the maximum load must be reduced to 400 pF.*

Figure 9. I²C target timing diagram



Note: Measurement points are done at 0.3·VDDIO and 0.7·VDDIO for both ports.

4.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
VDD	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.2 ms	20,000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/TA0)	-0.3 to VDDIO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.


This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.


This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4.6 Terminology

4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see Table 3).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see Table 3).

4.6.2 Zero-*g* and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 *g* on both the X-axis and Y-axis, whereas the Z-axis measures 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in Table 3. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see Table 3).

5 Digital interfaces

5.1 I²C/SPI interface

The registers embedded inside the LSM6DSV80X may be accessed through both the I²C and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped to the same pins. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to VDDIO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	Enables SPI I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO/TA0	SPI serial data output (SDO) I²C less significant bit of the device address

5.1.1 I²C serial interface

The LSM6DSV80X I²C is a bus target. The I²C is employed to write the data to the registers, whose content can also be read back.

The relevant I²C terminology is provided in the table below.

Table 11. I²C terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Controller	The device that initiates a transfer, generates clock signals, and terminates a transfer
Target	The device addressed by the controller

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to VDDIO through external pull-up resistors. When the bus is free, both the lines are high.

The I²C interface is implemented with fast mode (400 kHz) I²C standards as well as with fast mode plus (1000 kHz).

In order to disable the I²C block, I2C_I3C_disable = 1 must be written in IF_CFG (03h).

5.1.2 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the controller, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the target in the first 7 bits and the eighth bit tells whether the controller is receiving data from the target or transmitting data to the target. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the controller.

The target address (TAD) associated to the LSM6DSV80X is 110101xb. The SDO/TA0 pin can be used to modify the less significant bit of the device address. If the SDO/TA0 pin is connected to the supply voltage, LSb is 1 (address 1101011b); else if the SDO/TA0 pin is connected to ground, the LSb value is 0 (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver that has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM6DSV80X behaves like a target device and the following protocol must be adhered to. After the start condition (ST) a target address is sent, once a target acknowledge (TAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The increment of the address is configured by the CTRL3 (12h) (IF_INC).

The target address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the controller transmits to the target with direction unchanged. Table 12 explains how the TAD+read/write bit pattern is composed, listing all the possible configurations.

Table 12. TAD+read/write patterns

Command	TAD[6:1]	TAD[0] = TA0	R/W	TAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 13. Transfer when controller is writing one byte to target

Controller	ST	SAD + W		SUB		DATA		SP
Target			TAK		TAK		TAK	

Table 14. Transfer when controller is writing multiple bytes to target

Controller	ST	TAD + W		SUB		DATA		DATA		SP
Target			TAK		TAK		TAK		TAK	

Table 15. Transfer when controller is receiving (reading) one byte of data from target

Controller	ST	TAD + W		SUB		SR	TAD + R			NCAK	SP
Target			TAK		TAK			TAK	DATA		

Table 16. Transfer when controller is receiving (reading) multiple bytes of data from target

Controller	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Target			TAK		TAK			TAK	DATA		DATA		DATA		

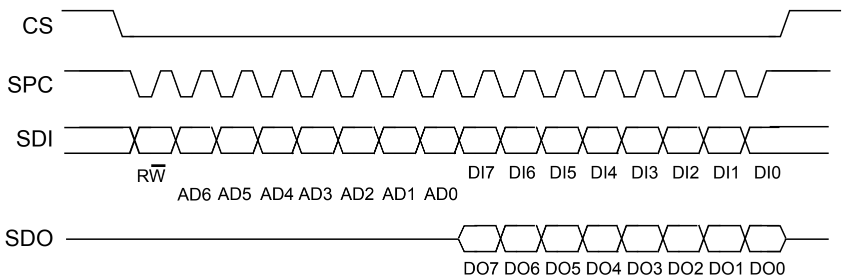
Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a target receiver does not acknowledge the target address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the target. The controller can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

In the presented communication format, CAK is controller acknowledge and NCAK is no controller acknowledge.

5.1.3 SPI bus interface

The SPI on the LSM6DSV80X is a bus target that allows writing and reading the registers of the device.

Figure 10. Read and write protocol (in mode 3)



CS enables the serial port and it is controlled by the SPI controller. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI controller. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

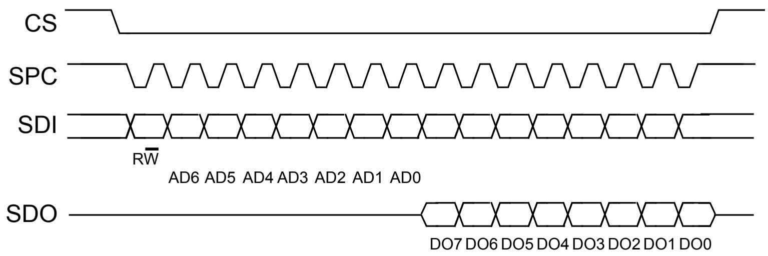
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the CTRL3 (12h) (IF_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3 (12h) (IF_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.1.3.1 SPI read

Figure 11. **SPI read protocol (in mode 3)**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

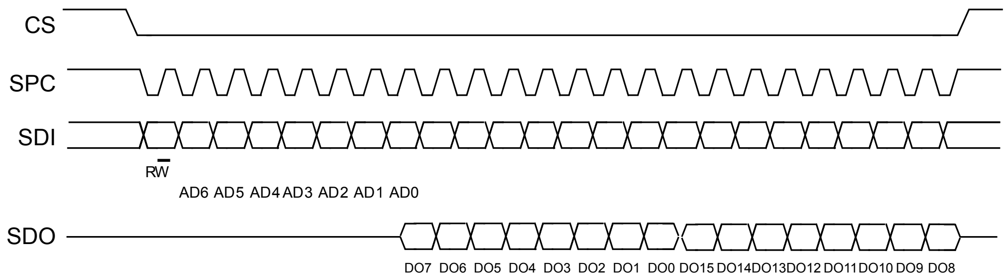
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

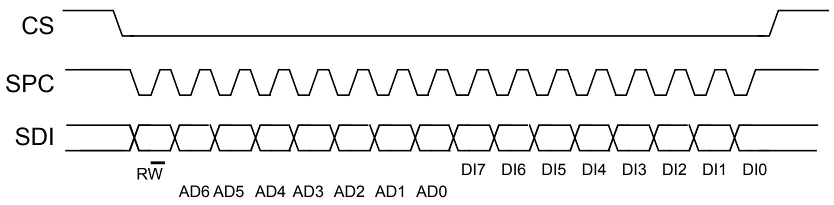
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 12. **Multiple byte SPI read protocol (2-byte example) (in mode 3)**



5.1.3.2 *SPI write*

Figure 13. SPI write protocol (in mode 3)



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

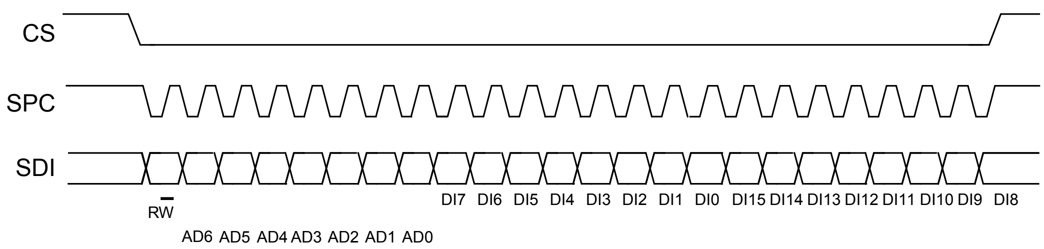
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

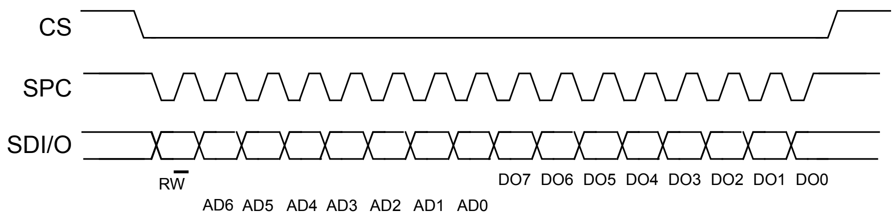
Figure 14. Multiple byte SPI write protocol (2-byte example) (in mode 3)



5.1.3.3 *SPI read in 3-wire mode*

3-wire mode is entered by setting the IF_CFG (03h) (SIM) bit equal to 1 (SPI serial interface mode selection).

Figure 15. SPI read protocol in 3-wire mode (in mode 3)



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

5.2 MIPI I3C® interface

5.2.1 MIPI I3C® target interface

The LSM6DSV80X interface includes a MIPI I3C® SDR-only target interface (compliant with release 1.1 of the specification) with MIPI I3C® SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-band interrupt request
- Target reset pattern
- Group address
- Full range Vdd_IO support
- Asynchronous modes 0 and 1
- Synchronous mode
- Error detection and recovery methods (S0-S6)

In order to disable the MIPI I3C® block, I2C_I3C_disable = 1 must be written in IF_CFG (03h).

5.2.2 MIPI I3C® CCC supported commands

The list of MIPI I3C® CCC commands supported by the device is detailed in the following table.

Table 17. **MIPI I3C® CCC commands**

Command	Command code	Default	Description
ENTDAA	0x07		DAA procedure
SETDASA	0x87		Assign dynamic address using static address 0x6B/0x6A depending on SDO pin
ENEC	0x80 / 0x00		Target activity control (direct and broadcast)
DISEC	0x81/ 0x01		Target activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
SETXTIME	0x98 / 0x28		Timing information exchange
GETXTIME	0x99	0x07 0x00 0x06 0x92	Timing information exchange
RSTDAA	0x06		Reset the assigned dynamic address (broadcast only)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B	0x00 0x08 (2 byte)	Get maximum write length during private write
GETMRL	0x8C	0x00 0x10 0x0A (3 byte)	Get maximum read length during private read
GETPID	0x8D	0x02 0x08 0x00 0x73 0x92 0x0B	SDO = 1
		0x02 0x08 0x00 0x73 0x12 0x0B	SDO = 0
GETBCR	0x8E	0x27 (1 byte)	Bus characteristics register
GETDCR	0x8F	0x44 default	MIPI I3C® device characteristics register
GETSTATUS	0x90	0x00 0x00 (2 byte)	Status register

Command	Command code	Default	Description
GETMXDS	0x94	0x08 0x60	Return max write and read speed
GETCAPS	0x95	0x00 0x11 0x18 0x00	Provide information about device capabilities and supported extended features
SETGRPA	0x9B		Group address assignment command
RSTGRPA	0x2C / 0x9C		Reset the group address
RSTACT	0x9A / 0x2A		Configure target reset action

5.2.3 Overview of antispike filter management

The device acts as a standard I²C target as long as it has an I²C static address. The device is capable of detecting and disabling the I²C antispike filter after detecting the broadcast address (7'h7E/W). In order to guarantee proper behavior of the device, the I3C controller must emit the first START, 7'h7E/W at open-drain speed using I²C fast mode plus reference timing.

After detecting the broadcast address, the device can receive the I3C dynamic address following the I3C push-pull timing. If the device is not assigned a dynamic address, then the device continues to operate as an I²C device with no antispike filter. For the case in which the host decides to keep the device as I²C with an antispike filter, there is a configuration required to keep the antispike filter active. This configuration is done by writing the ASF_CTRL bit to 1 in the IF_CFG (03h) register. This configuration forces the antispike filter to always be turned on instead of being managed by the communication on the bus.

5.3 I²C controller interface

If the LSM6DSV80X is configured in mode 2, an I²C controller line is available. The controller serial interface is mapped to the following dedicated pins.

Table 18. I²C controller pin details

Pin name	Pin description
CSCL	I²C controller serial clock
CSDA	I²C controller serial data
CDRDY	I²C controller external synchronization signal

6 Functionality

This section describes all the operating modes and power modes of the LSM6DSV80X.

Note: Refer to the product application note for the details regarding operating/power mode configurations, settings, turn-on/off time and on-the-fly changes.

6.1 Operating modes

In the LSM6DSV80X, the low-*g*, high-*g* accelerometers and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

6.1.1 Low-*g* accelerometer

In the LSM6DSV80X, the accelerometer can be configured in six different operating modes: power-down mode, low-power mode (1, 2, 3), normal mode, high-performance mode, high-accuracy ODR mode, and ODR-triggered mode.

The operating mode selected depends on the value of the OP_MODE_XL_[2:0] bits in CTRL1 (10h).

If the value of the OP_MODE_XL_[2:0] bits is 000 (default), high-performance mode is valid for all ODRs (from 7.5 Hz up to 7.68 kHz).

Normal mode is available for ODR values from 7.5 Hz to 1.92 kHz and it is enabled by setting the OP_MODE_XL_[2:0] bits to 111.

In high-performance mode and in normal mode, the analog antialiasing filter is active.

Low-power mode is available for lower ODRs (1.875 Hz, 15 Hz, 30 Hz, 60 Hz, 120 Hz, 240 Hz). The three low-power modes are enabled by setting OP_MODE_XL_[2:0] to 100 (LPM1), 101 (LPM2), 110 (LPM3).

High-accuracy ODR mode is available for ODR values from 15 Hz up to 7.68 kHz and it is enabled by setting the OP_MODE_XL_[2:0] bits to 001. Refer to Section 6.1.4: High-accuracy ODR mode for more details.

ODR-triggered mode is available for ODR values from 15 Hz up to 7.68 kHz and it is enabled by setting the OP_MODE_XL_[2:0] bits to 011. Refer to Section 6.1.5: ODR-triggered mode for more details.

The embedded functions based on accelerometer data (free-fall, 6D/4D, tap/double-tap, wake-up, activity/inactivity, stationary/motion, step counter, step detection, significant motion, tilt) and the FIFO batching functionality are supported in all modes.

6.1.2 High-*g* accelerometer

In the LSM6DSV80X, the high-*g* accelerometer can be configured with different ODRs from 480 Hz up to 7.68 kHz.

When the high-*g* accelerometer is used, the low-*g* accelerometer must be configured in high-performance mode or in high-accuracy ODR mode. In these configurations, antialiasing is enabled. The ODRs are independent between the low-*g* and high-*g* accelerometers.

There are no limitations on the selectable operating mode of the gyroscope when the high-*g* channel is enabled.

Table 19. High-*g* accelerometer compatibility with low-*g* accelerometer operating modes and ODRs

Low-*g* accelerometer modes	Low-*g* accelerometer ODR_XL	High-*g* compatibility
High-performance	All	Y
High-accuracy ODR	All	Y
Low-power	All	N
Normal mode	All	N
ODR-triggered	All	N

6.1.3 Gyroscope

In the LSM6DSV80X, the gyroscope can be configured in six different operating modes: power-down mode, sleep mode, low-power mode, high-performance mode, high-accuracy ODR mode, and ODR-triggered mode.

The operating mode selected depends on the value of the OP_MODE_G_[2:0] bits in CTRL2 (11h).

If the value of the OP_MODE_G_[2:0] bits is 000 (default), high-performance mode is valid for all ODRs (from 7.5 Hz up to 7.68 kHz).

Low-power mode is available for lower ODRs (7.5 Hz, 15 Hz, 30 Hz, 60 Hz, 120 Hz, 240 Hz) and it is enabled by setting the OP_MODE_G_[2:0] bits to 101.

High-accuracy ODR mode is available for ODR values from 15 Hz up to 7.68 kHz and it is enabled by setting the OP_MODE_G_[2:0] bits to 001. Refer to Section 6.1.4: High-accuracy ODR mode for more details.

ODR-triggered mode is available for ODR values from 15 Hz up to 7.68 kHz and it is enabled by setting the OP_MODE_XL_[2:0] bits to 011. Refer to Section 6.1.5: ODR-triggered mode for more details.

6.1.4 High-accuracy ODR mode

High-accuracy ODR (HAODR) mode can be enabled to reduce the part-to-part output data rate variation. It supports both the low-*g*, high-*g* accelerometers and the gyroscope. When this mode is used for one sensor (accelerometers or gyroscope), the other sensor also has to be configured in high-accuracy ODR (HAODR) mode.

The main high-accuracy ODR features are:

- Noise level is aligned with high-performance mode
- The power consumption in HAODR mode depends on the selected ODR and on the enabled sensors. As an example, at ODR = 960 Hz in combo mode (low-*g* accelerometer + gyroscope) it increases 20 μA (typical) compared to high-performance mode. Refer to the application note for more details.
- The UI channel bandwidth can be selected through the gyroscope LPF1 and accelerometer HPF/LPF2 filters.
- When HAODR mode is enabled, it is applied to the low-*g*, high-*g* accelerometers, gyroscope, and temperature.

Note: HAODR mode has to be enabled / disabled when the device is in power-down mode.

When HAODR mode is enabled, four different sets of ODRs are supported based on the configuration of the HAODR_SEL_[1:0] bitfield in the HAODR_CFG (62h) register, as shown in the table below.

Note: High-accuracy ODR mode is not compatible with the activity/inactivity functionality (motion/stationary can be used).

Table 20. Accelerometer and gyroscope ODR selection in high-accuracy ODR mode

ODR_XL_[3:0] ODR_G_[3:0]	ODR [Hz] HAODR_SEL_[1:0] = 00	ODR [Hz] HAODR_SEL_[1:0] = 01	ODR [Hz] HAODR_SEL_[1:0] = 10	ODR [Hz] HAODR_SEL_[1:0] = 11
0000	Power-down	Power-down	Power-down	Power-down
0001	Reserved	Reserved	Reserved	Reserved
0010	Reserved	Reserved	Reserved	Reserved
0011	15	15.625	12.5	13
0100	30	31.25	25	26
0101	60	62.5	50	52
0110	120	125	100	104
0111	240	250	200	208
1000	480	500	400	417
1001	960	1000	800	833
1010	1920	2000	1600	1667
1011	3840	4000	3200	3333
1100	7680	8000	6400	6667
Others	Reserved	Reserved	Reserved	Reserved

6.1.5 ODR-triggered mode

When ODR-triggered mode is enabled, a reference signal must be provided to the INT2 pin, and the device then automatically aligns (in frequency and phase) the data generation to the edges of the reference signal.

It supports the low-*g* accelerometer only, gyroscope only, and the combo of low-*g* accelerometer and gyroscope. When both the accelerometer and gyroscope are enabled, the user must configure the same ODR on both the accelerometer and gyroscope. It is not possible to select different ODRs for the accelerometer and gyroscope; if different output data rate values are set, the ODR configured for the gyroscope data is also applied to the accelerometer data.

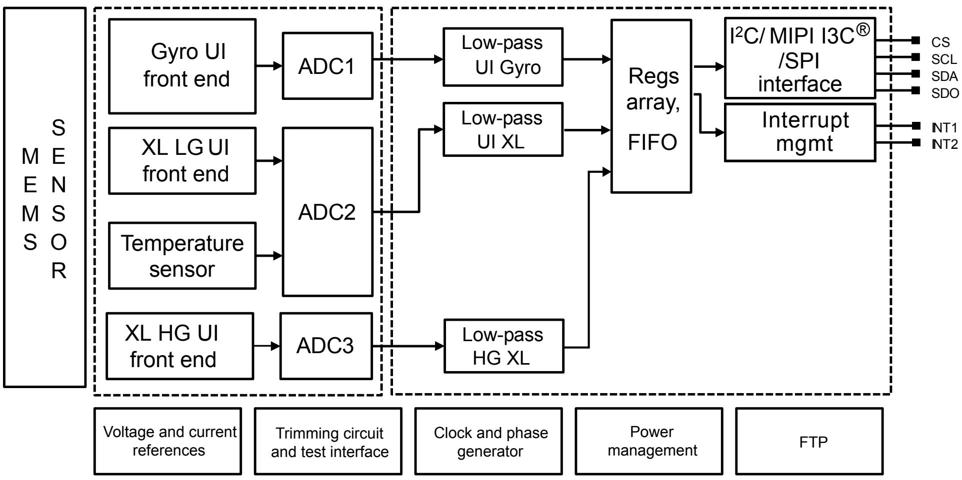
The full-scale configurations are totally independent between the accelerometer and gyroscope and they can be set in any combination.

Note: ODR-triggered mode has to be enabled / disabled when the device is in power-down mode.

Note: When ODR-triggered mode is enabled, the 1100 configuration of the ODR_XL_[3:0] bits in register CTRL1 (10h) and the 1100 configuration of the ODR_G_[3:0] bits in register CTRL2 (11h) cannot be used.

6.2 Block diagram of filters

Figure 16. **Block diagram of filters**



6.2.1 Block diagrams of the low-*g* accelerometer filters

In the LSM6DSV80X, the filtering chain for the low-*g* accelerometer is composed of the following:

- Digital filter (LPF1)
- Composite filter

Details of the block diagrams appear in the following figures.

Figure 17. Low-*g* accelerometer UI chain

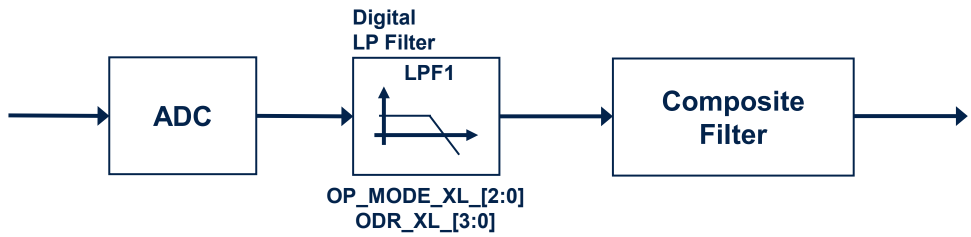
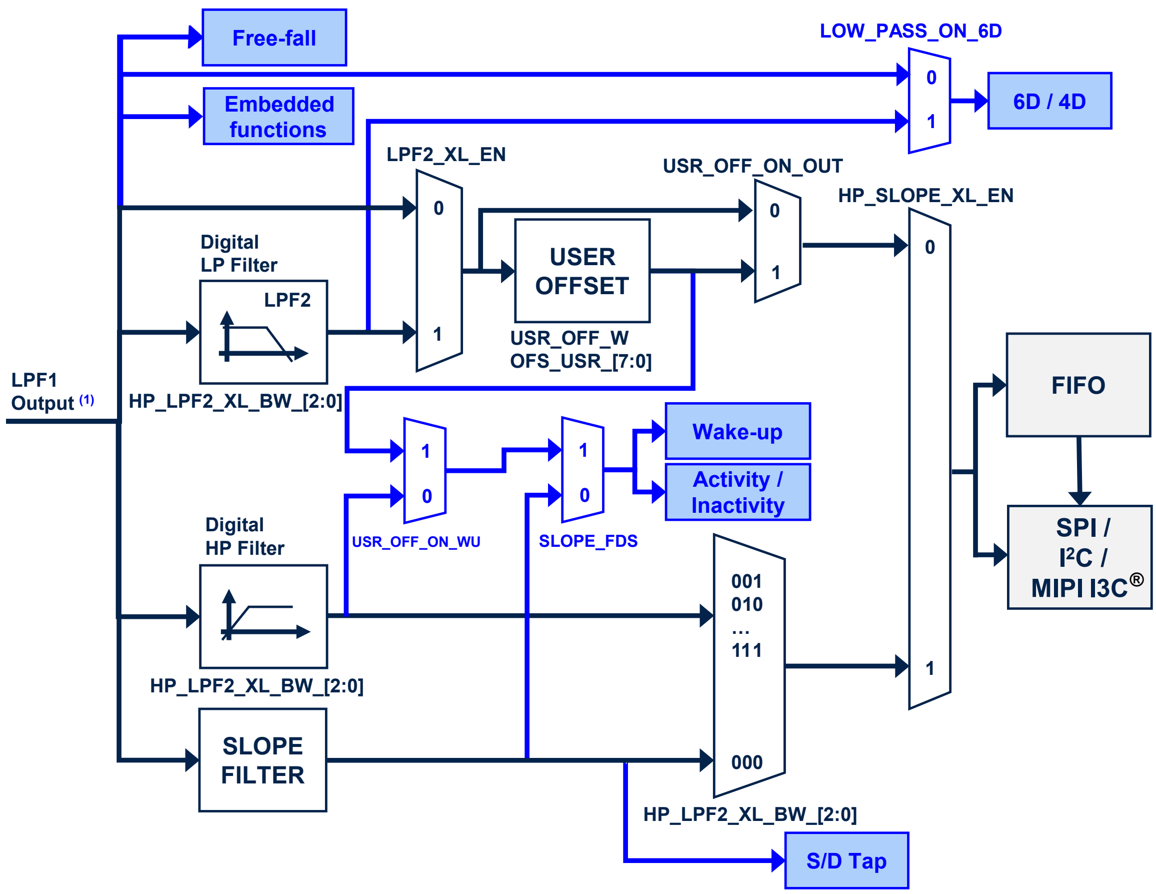


Figure 18. Low-*g* accelerometer composite filter



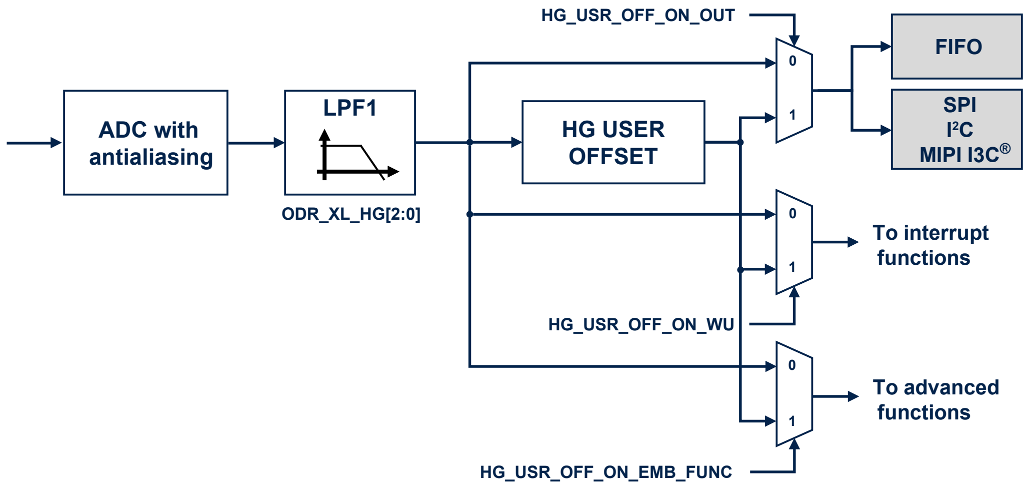
1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode, high-accuracy ODR mode, or normal mode. This value is equal to 2300 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) or 431 Hz in low-power mode 3 (8 mean).*

Note: Embedded functions include finite state machine, machine learning core, pedometer, step detector and step counter, significant motion detection, and tilt functions.

6.2.2 Block diagram of the high-*g* accelerometer filter

The LSM6DSV80X high-*g* accelerometer filtering chain is shown in the following figure.

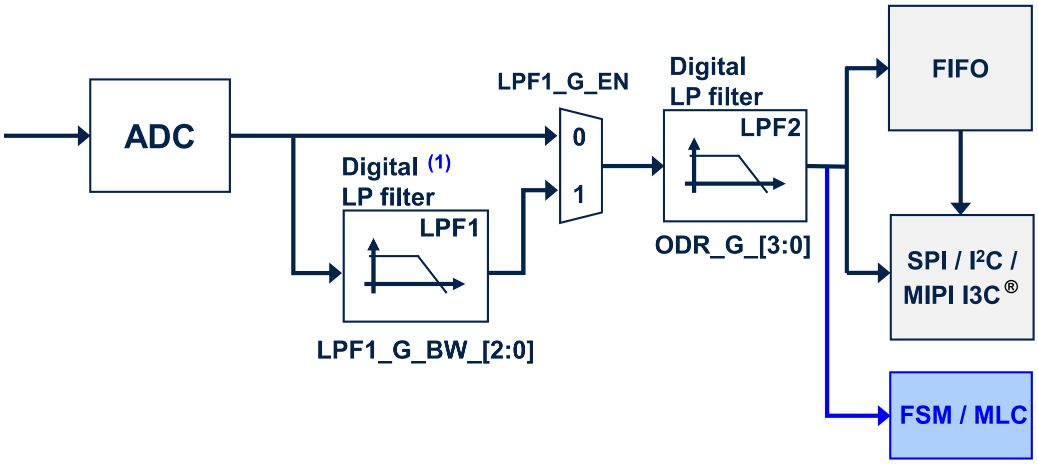
Figure 19. High-*g* accelerometer filtering chain



6.2.3 Block diagram of the gyroscope filters

The LSM6DSV80X gyroscope filtering chain is shown in the following figure.

Figure 20. Gyroscope digital chain



1. *The LPF1 filter is available in high-performance mode only. If the gyroscope is configured in low-power mode, the LPF1 filter is bypassed.*

In this configuration, the gyroscope ODR is selectable from 7.5 Hz up to 7.68 kHz. A low-pass filter (LPF1) is available, for more details about the filter characteristics see Table 63. Gyroscope LPF1 + LPF2 bandwidth selection.

The digital LPF2 filter's cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

Table 21. Gyroscope LPF2 bandwidth selection

Gyroscope ODR [Hz]	LPF2 cutoff [Hz]
7.5	3.4
15	6.6
30	13.0
60	24.6
120	49.4
240	96
480	187
960	342
1.92 kHz	491
3.84 kHz	528
7.68 kHz	537

Note: Data can be acquired from the output registers and FIFO over the I²C/MIPI I3C®/SPI interface.

6.3 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The LSM6DSV80X embeds 1.5 KB of data in FIFO (up to 4.5 KB with the compression feature enabled) to store the following data:

- Gyroscope
- Low-*g* accelerometer
- High-*g* accelerometer
- External sensors (up to four)
- Step counter
- Timestamp
- Temperature
- FSM events
- High-*g* accelerometer peak value
- MLC features, filters, and results
- SFLP output data (quaternion, gyroscope bias, gravity vector)

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: low-*g* accelerometer, gyroscope, and temperature sensor batch rates can be selected by the user. Writing external sensors in the FIFO can be triggered depending on the sensor hub rate chosen or by an external sensor interrupt. The step counter can be stored in the FIFO with an associated timestamp each time a step is detected. The status of the FSMs when they are generating an interrupt event can be stored in the FIFO, as well as the long counter overrun event or the long counter value when a specific command is executed from one FSM, all associated with the timestamp value. The high-*g* accelerometer peak value detected from the high-*g* peak tracking feature is stored in FIFO. Results from SFLP (quaternion, gyroscope bias, gravity vector) can be stored in the FIFO at the rate selected for the algorithm. Moreover, MLC features, filters, and results can be enabled to be stored in the FIFO. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO_DATA_OUT_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (batch data rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

Finally, FIFO embeds a compression algorithm that the user can enable in order to have up to 4.5 KB data stored in FIFO and take advantage of interface communication length for FIFO flushing and communication power consumption.

The programmable FIFO watermark threshold can be set using the WTM[7:0] bits in the FIFO_CTRL1 (07h) register. To monitor the FIFO status, dedicated registers (FIFO_STATUS1 (1Bh), FIFO_STATUS2 (1Ch)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status, and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1_CTRL (0Dh) and INT2_CTRL (0Eh).

The FIFO buffer can be configured according to seven different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- ContinuousWTM-to-full mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO_MODE_[2:0] bits in the FIFO_CTRL4 (0Ah) register.

6.3.1 Bypass mode

In bypass mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

6.3.2 FIFO mode

In FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, bypass mode should be selected by writing FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0]) to 000. After this reset command, it is possible to restart FIFO mode by writing FIFO_CTRL4 (0Ah) (FIFO_MODE_[2:0]) to 001.

The FIFO buffer memorizes up to 4.5 KB of data (with compression enabled) but the depth of the FIFO can be resized by setting the WTM[7:0] bits in FIFO_CTRL1 (07h). If the STOP_ON_WTM bit in FIFO_CTRL2 (08h) is set to 1, FIFO depth is limited up to the WTM[7:0] bits in the FIFO_CTRL1 (07h) register.

6.3.3 Continuous mode

Continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag FIFO_STATUS2 (1Ch)(FIFO_WTM_IA) is asserted when the number of unread samples in FIFO is greater than or equal to FIFO_CTRL1 (07h) (WTM[7:0]).

It is possible to route the FIFO_WTM_IA flag to the INT1 pin by writing in register INT1_CTRL (0Dh) (INT1_FIFO_TH) = 1 or to the INT2 pin by writing in register INT2_CTRL (0Eh)(INT2_FIFO_TH) = 1.

A full-flag interrupt can be enabled, INT1_CTRL (0Dh)(INT1_FIFO_FULL) = 1 or INT2_CTRL (0Eh) (INT2_FIFO_FULL) = 1, in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the FIFO_OVR_IA flag in FIFO_STATUS2 (1Ch) is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in FIFO_STATUS1 (1Bh) and FIFO_STATUS2 (1Ch)(DIFF_FIFO_[8:0]).

6.3.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- High-*g* wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 1, FIFO operates in FIFO mode.

When the selected trigger bit is equal to 0, FIFO operates in continuous mode.

6.3.5 ContinuousWTM-to-full mode

In continuousWTM-to-full mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 010), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- High-*g* wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 0, FIFO operates in continuous mode with the FIFO size limited to the FIFO watermark level (defined by the WTM[7:0] bits in the FIFO_CTRL1 (07h) register).

When the selected trigger bit is equal to 1, FIFO continues to store data until it is full.

6.3.6 Bypass-to-continuous mode

In bypass-to-continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 100), data measurement storage inside FIFO operates in continuous mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- High-*g* wake-up
- Free-fall
- D6D

6.3.7 Bypass-to-FIFO mode

In bypass-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 111), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- High-*g* wake-up
- Free-fall
- D6D

6.3.8 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (FIFO_DATA_OUT_TAG (78h), in order to identify the sensor, and 6 bytes of fixed data (FIFO_DATA_OUT registers from (79h) to (7Eh)).

The DIFF_FIFO_[8:0] field in the FIFO_STATUS1 (1Bh) and FIFO_STATUS2 (1Ch) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

In addition, it is possible to configure a counter of the batch events of accelerometer or gyroscope sensors. The flag COUNTER_BDR_IA in FIFO_STATUS2 (1Ch) alerts that the counter reaches a selectable threshold (CNT_BDR_TH_[9:0] field in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch)). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the TRIG_COUNTER_BDR_[1:0] bits in COUNTER_BDR_REG1 (0Bh). As for the other FIFO status events, the flag COUNTER_BDR_IA can be routed on the INT1 or INT2 pins by asserting the corresponding bits (INT1_CNT_BDR of INT1_CTRL (0Dh) and INT2_CNT_BDR of INT2_CTRL (0Eh)).

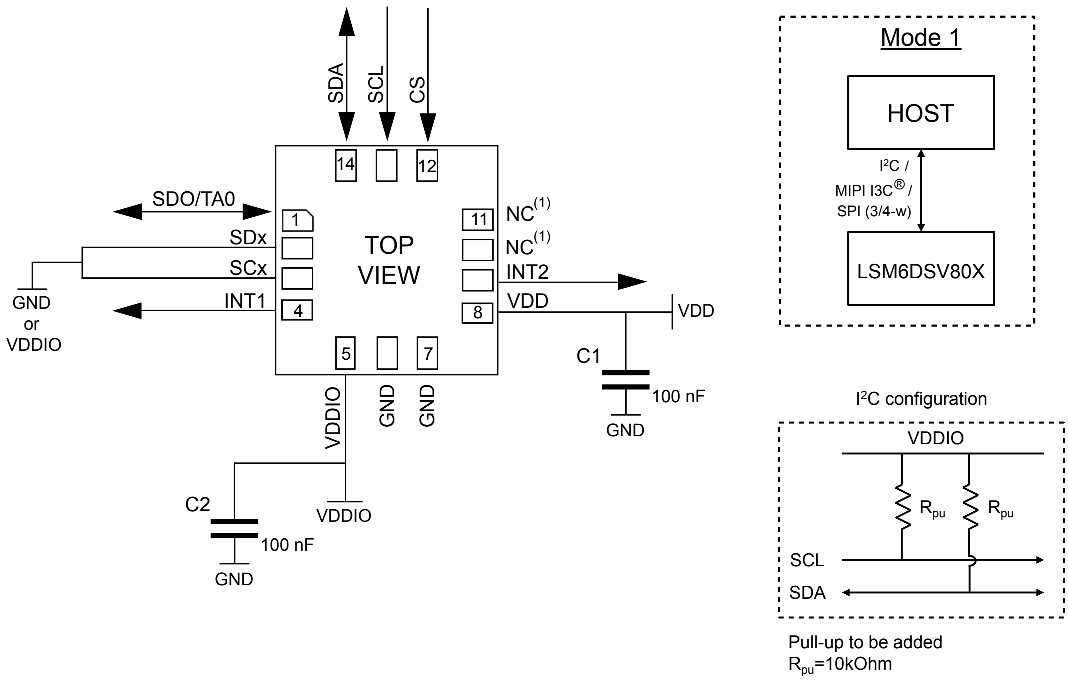
In order to maximize the amount of accelerometer and gyroscope data in FIFO, the user can enable the compression algorithm by setting to 1 both the FIFO_COMPR_EN bit in EMB_FUNC_EN_B (05h) (embedded functions registers bank) and the FIFO_COMPR_RT_EN bit in FIFO_CTRL2 (08h). When compression is enabled, it is also possible to force writing noncompressed data at a selectable rate using the UNCOMPR_RATE_[1:0] field in FIFO_CTRL2 (08h).

Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the ODR_CHG_EN bit in FIFO_CTRL2 (08h).

7 Application hints

7.1 LSM6DSV80X electrical connections in mode 1

Figure 21. **LSM6DSV80X electrical connections in mode 1**



1. *Leave pin electrically unconnected and soldered to PCB.*

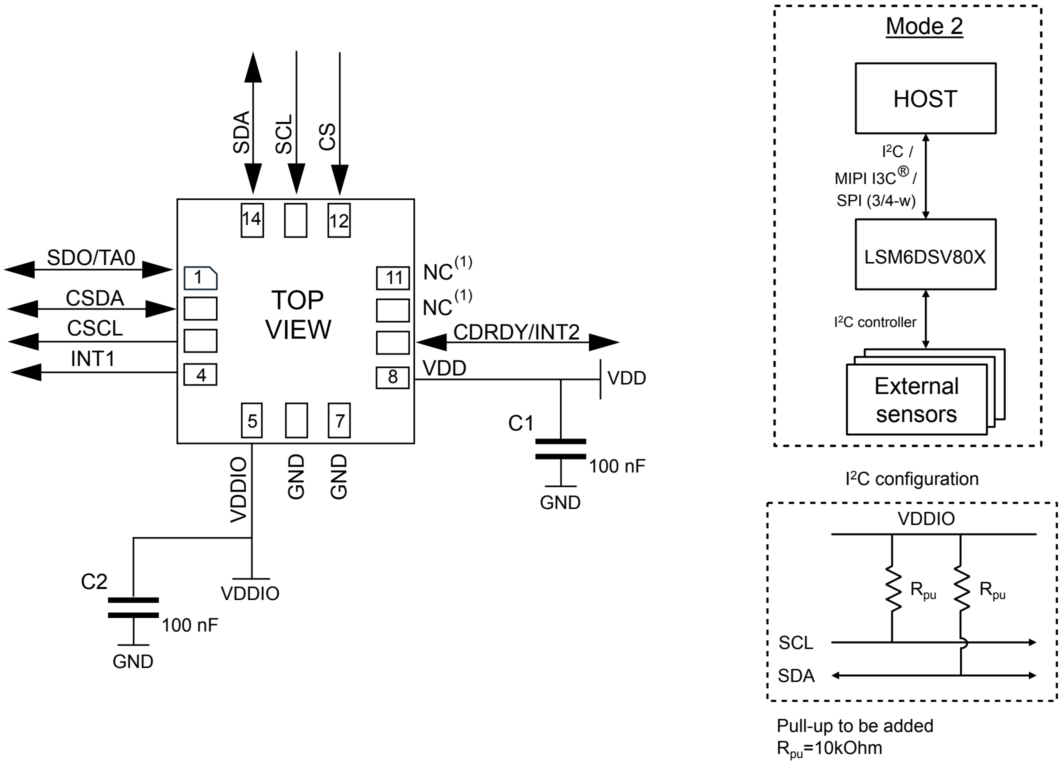
The device core is supplied through the VDD line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® interface.

The functions, the threshold, and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® interface.

7.2 LSM6DSV80X electrical connections in mode 2

Figure 22. **LSM6DSV80X electrical connections in mode 2**



1. *Leave pin electrically unconnected and soldered to PCB.*

The device core is supplied through the VDD line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® interface.

The functions, the threshold, and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® interface.

Table 22. **Internal pin status**

pin#	Name	Mode 1 function	Mode 2 function	Pin status mode 1	Pin status mode 2
1	SDO	SPI 4-wire interface serial data output (SDO)	SPI 4-wire interface serial data output (SDO)	Default: input without pull-up Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h).	Default: input without pull-up Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h).
	TA0	I²C least significant bit of the device address (TA0) MIPI I3C® least significant bit of the static address (TA0)	I²C least significant bit of the device address (TA0) MIPI I3C® least significant bit of the static address (TA0)		
2	SDx	Connect to VDDIO or GND	I²C controller serial data (CSDA)	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h).	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h).
3	SCx	Connect to VDDIO or GND	I²C controller serial clock (CSCL)	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h).	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h).
4	INT1	Programmable interrupt 1	Programmable interrupt 1	Default: output forced to ground	Default: output forced to ground
5	VDDIO	Power supply for I/O pins	Power supply for I/O pins		
6	GND	0 V supply	0 V supply		
7	GND	0 V supply	0 V supply		
8	VDD	Power supply	Power supply		
9	INT2	Programmable interrupt 2 (INT2)	Programmable interrupt 2 (INT2) / I²C controller external synchronization signal (CDRDY)	Default: output forced to ground	Default: output forced to ground
10	NC	Leave unconnected	Leave unconnected	Default: input with pull-up	Default: input with pull-up
11	NC	Leave unconnected	Leave unconnected	Default: input with pull-up	Default: input with pull-up
12	CS	I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	Default: input with pull-up Pull-up is disabled if bit I2C_I3C_disable = 1 in register IF_CFG (03h).	Default: input with pull-up Pull-up is disabled if bit I2C_I3C_disable = 1 in register IF_CFG (03h).
13	SCL	I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC)	I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC)	Default: input without pull-up	Default: input without pull-up
14	SDA	I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	Default: input without pull-up Pull-up is enabled if bit SDA_PU_EN = 1 in register IF_CFG (03h).	Default: input without pull-up Pull-up is enabled if bit SDA_PU_EN = 1 in register IF_CFG (03h).

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on VDDIO.

8 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

All these registers are accessible from the SPI/I²C/MIPI I3C® interface only.

Table 23. **Registers address map**

Name	Type	Register address		Default	Comment
		Hex	Binary		
FUNC_CFG_ACCESS	R/W	01	00000001	00000000	
PIN_CTRL	R/W	02	00000010	00100011	
IF_CFG	R/W	03	00000011	00000000	
RESERVED	-	04-05			
ODR_TRIG_CFG	R/W	06	00000110	00000000	
FIFO_CTRL1	R/W	07	00000111	00000000	
FIFO_CTRL2	R/W	08	00001000	00000000	
FIFO_CTRL3	R/W	09	00001001	00000000	
FIFO_CTRL4	R/W	0A	00001010	00000000	
COUNTER_BDR_REG1	R/W	0B	00001011	00000000	
COUNTER_BDR_REG2	R/W	0C	00001100	00000000	
INT1_CTRL	R/W	0D	00001101	00000000	
INT2_CTRL	R/W	0E	00001110	00000000	
WHO_AM_I	R	0F	00001111	01110011	
CTRL1	R/W	10	00010000	00000000	
CTRL2	R/W	11	00010001	00000000	
CTRL3	R/W	12	00010010	01000100	
CTRL4	R/W	13	00010011	00000000	
CTRL5	R/W	14	00010100	00000000	
CTRL6	R/W	15	00010101	00001000	
CTRL7	R/W	16	00010110	00000000	
CTRL8	R/W	17	0001 0111	00000000	
CTRL9	R/W	18	00011000	00000000	
CTRL10	R/W	19	00011001	00000000	
CTRL_STATUS	R	1A	00011010	output	
FIFO_STATUS1	R	1B	00011011	output	
FIFO_STATUS2	R	1C	00011100	output	
ALL_INT_SRC	R	1D	00011101	output	
STATUS_REG	R	1E	00011110	output	
RESERVED	-	1F			
OUT_TEMP_L	R	20	00100000	output	
OUT_TEMP_H	R	21	00100001	output	
OUTX_L_G	R	22	00100010	output	
OUTX_H_G	R	23	00100011	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
OUTY_L_G	R	24	00100100	output	
OUTY_H_G	R	25	00100101	output	
OUTZ_L_G	R	26	00100110	output	
OUTZ_H_G	R	27	00100111	output	
OUTX_L_A	R	28	00101000	output	
OUTX_H_A	R	29	00101001	output	
OUTY_L_A	R	2A	00101010	output	
OUTY_H_A	R	2B	00101011	output	
OUTZ_L_A	R	2C	00101100	output	
OUTZ_H_A	R	2D	00101101	output	
RESERVED	-	2E-33			
UI_OUTX_L_A_HG	R	34	00110100	output	
UI_OUTX_H_A_HG	R	35	00110101	output	
UI_OUTY_L_A_HG	R	36	00110110	output	
UI_OUTY_H_A_HG	R	37	00110111	output	
UI_OUTZ_L_A_HG	R	38	00111000	output	
UI_OUTZ_H_A_HG	R	39	00111001	output	
RESERVED	-	3A-3F			
TIMESTAMP0	R	40	01000000	output	
TIMESTAMP1	R	41	01000001	output	
TIMESTAMP2	R	42	01000010	output	
TIMESTAMP3	R	43	01000011	output	
UI_STATUS_REG	R	44	01000100	output	
WAKE_UP_SRC	R	45	01000101	output	
TAP_SRC	R	46	01000110	output	
D6D_SRC	R	47	01000111	output	
STATUS_CONTROLLER_ MAINPAGE	R	48	01001000	output	
EMB_FUNC_STATUS_ MAINPAGE	R	49	01001001	output	
FSM_STATUS_MAINPAGE	R	4A	01001010	output	
MLC_STATUS_MAINPAGE	R	4B	01001011	output	
HG_WAKE_UP_SRC	R/W	4C	01001100	00000000	
CTRL2_XL_HG	R/W	4D	01001101	00000000	
CTRL1_XL_HG	R/W	4E	01001110	00000000	
INTERNAL_FREQ_FINE	R	4F	01001111	output	
FUNCTIONS_ENABLE	RW	50	01010000	00000000	
RESERVED	-	51			
HG_FUNCTIONS_ENABLE	R	52	01010010	output	
HG_WAKE_UP_THS	R	53	01010011	output	
INACTIVITY_DUR	R/W	54	01010100	00000100	

Name	Type	Register address		Default	Comment
		Hex	Binary		
INACTIVITY_THS	R/W	55	01010101	00000000	
TAP_CFG0	R/W	56	01010110	00000000	
TAP_CFG1	R/W	57	01010111	00000000	
TAP_CFG2	R/W	58	01011000	00000000	
TAP_THS_6D	R/W	59	01011001	00000000	
TAP_DUR	R/W	5A	01011010	00000000	
WAKE_UP_THS	R/W	5B	01011011	00000000	
WAKE_UP_DUR	R/W	5C	01011100	00000000	
FREE_FALL	R/W	5D	01011101	00000000	
MD1_CFG	R/W	5E	01011110	00000000	
MD2_CFG	R/W	5F	01011111	00000000	
RESERVED	-	60-61			
HAODR_CFG	R/W	62	01100010	00000000	
EMB_FUNC_CFG	R/W	63	01100011	00000000	
RESERVED	-	64-6B			
XL_HG_X_OFS_USR	R/W	6C	01101100	00000000	
XL_HG_Y_OFS_USR	R/W	6D	01101101	00000000	
XL_HG_Z_OFS_USR	R/W	6E	01101110	00000000	
RESERVED	-	6F-73			
X_OFS_USR	R/W	73	01110011	00000000	
Y_OFS_USR	R/W	74	01110100	00000000	
Z_OFS_USR	R/W	75	01110101	00000000	
RESERVED	-	76-77			
FIFO_DATA_OUT_TAG	R	78	01111000	output	
FIFO_DATA_OUT_X_L	R	79	01111001	output	
FIFO_DATA_OUT_X_H	R	7A	01111010	output	
FIFO_DATA_OUT_Y_L	R	7B	01111011	output	
FIFO_DATA_OUT_Y_H	R	7C	01111100	output	
FIFO_DATA_OUT_Z_L	R	7D	01111101	output	
FIFO_DATA_OUT_Z_H	R	7E	01111110	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate, and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

9.1 FUNC_CFG_ACCESS (01h)

Enable embedded functions register (R/W)

Table 24. FUNC_CFG_ACCESS register

EMB_FUNC_ REG_ACCESS	SHUB_REG _ACCESS	0[(1)]	0[(1)]	FSM_WR_ CTRL_EN	SW_POR	0[(1)]	0[(1)]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 25. FUNC_CFG_ACCESS register description

EMB_FUNC_REG_ACCESS	Enables access to the embedded functions configuration registers.[(1)] Default value: 0
SHUB_REG_ACCESS	Enables access to the sensor hub (I²C controller) configuration registers.[(2)] Default value: 0
FSM_WR_CTRL_EN	Enables the control of the CTRL registers to FSM (FSM can change some configurations of the device autonomously). Default value: 0 (0: disabled; 1: enabled)
SW_POR	Global reset of the device. Default value: 0

1. *Details concerning the embedded functions configuration registers are available in Section 10: Embedded functions register mapping and Section 11: Embedded functions register description.*
2. *Details concerning the sensor hub registers are available in Section 14: Sensor hub register mapping and Section 15: Sensor hub register description.*

9.2 PIN_CTRL (02h)

SDO pin pull-up register (R/W). This register is not reset during the software reset procedure (see bit 0 of the CTRL3 (12h) register).

Table 26. PIN_CTRL register

0[(1)]	SDO_ PU_EN	IBHR_ POR_EN	0[(1)]	0[(1)]	0[(1)]	IO_PAD_ STRENGTH_1	IO_PAD_ STRENGTH_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 27. PIN_CTRL register description

SDO_PU_EN	Enables pull-up on SDO pin. For details, refer to Table 22. Default value: 0 (0: SDO pin pull-up disconnected; 1: SDO pin with pull-up)
IBHR_POR_EN	Selects the action that the device performs after "reset whole chip" I3C pattern. Default value: 1 (0: configuration reset (software reset + dynamic address reset); (1: global reset (POR reset))
IO_PAD_STRENGTH[1:0]	Defines the drive strength for the interrupt pads. Default value: 11 (00: lowest strength (recommended for VDDIO ≥ 3.0 V); 01: intermediate strength (recommended for VDDIO ≥ 2.0 V and VDDIO < 3 V); 10: reserved (do not use); 11: highest strength (recommended for VDDIO < 2 V))

9.3 IF_CFG (03h)

Interface configuration register (R/W). This register is not reset during the software reset procedure (see bit 0 of the CTRL3 (12h) register).

Table 28. IF_CFG register

SDA_PU_EN	SHUB_PU_EN	ASF_CTRL	H_LACTIVE	PP_OD	SIM	0[(1)]	I2C_I3C_disable

1. *This bit must be set to 0 for the correct operation of the device.*

Table 29. IF_CFG register description

SDA_PU_EN	Enables pull-up on SDA pin. Default value: 0 (0: SDA pin pull-up disconnected; 1: SDA pin with pull-up)
SHUB_PU_EN	Enables I²C controller pull-up. Default value: 0 (0: internal pull-up on auxiliary I²C line disabled; 1: internal pull-up on auxiliary I²C line enabled)
ASF_CTRL	Enables antispike filters. Default value: 0 (0: antispike filters are managed by the protocol and turned off after the broadcast address; 1: antispike filters on SCL and SDA lines are always enabled)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pins. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
I2C_I3C_disable	Disables I²C and MIPI I3C® interfaces. Default value: 0 (0: SPI, I²C and MIPI I3C® interfaces enabled; 1: I²C and MIPI I3C® interfaces disabled)

9.4 ODR_TRIG_CFG (06h)

ODR-triggered mode configuration register (R/W)

Table 30. ODR_TRIG_CFG register

ODR_TRIG_NODR_7	ODR_TRIG_NODR_6	ODR_TRIG_NODR_5	ODR_TRIG_NODR_4	ODR_TRIG_NODR_3	ODR_TRIG_NODR_2	ODR_TRIG_NODR_1	ODR_TRIG_NODR_0

Table 31. ODR_TRIG_CFG register description

ODR_TRIG_NODR_[7:0]	When ODR-triggered mode is set, these bits are used to define the number of data generated in the reference period. Allowed values for ODR_TRIG_NODR_[7:0] are 0 (default) and values in the range from 4 to 255.

9.5 FIFO_CTRL1 (07h)

FIFO control register 1 (R/W)

Table 32. FIFO_CTRL1 register

WTM_7	WTM_6	WTM_5	WTM_4	WTM_3	WTM_2	WTM_1	WTM_0

Table 33. FIFO_CTRL1 register description

WTM_[7:0]	FIFO watermark threshold: 1 LSB = TAG (1 byte) + 1 sensor (6 bytes) written in FIFO. Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.

9.6 FIFO_CTRL2 (08h)

FIFO control register 2 (R/W)

Table 34. FIFO_CTRL2 register

STOP_ON_WTM	FIFO_COMPR_RT_EN	0[(1)]	ODR_CHG_EN	0[(1)]	UNCOMPR_RATE_1	UNCOMPR_RATE_0	0[(1)]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 35. FIFO_CTRL2 register description

STOP_ON_WTM	Sensing chain FIFO stop values memorization at threshold level. Default value: 0 (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level, defined in FIFO_CTRL1 (07h))
FIFO_COMPR_RT_EN[(1)]	Enables/disables compression algorithm runtime. Default value: 0 (0: FIFO compression algorithm disabled; 1: FIFO compression algorithm enabled)
ODR_CHG_EN	Enables ODR CHANGE virtual sensor to be batched in FIFO. Default value: 0 (0: ODR CHANGE virtual sensor not batched in FIFO; 1: ODR CHANGE virtual sensor batched in FIFO) *Note: Refer to the product application note for the details regarding operating/power mode configurations, settings, turn-on/off time and on-the-fly changes.*
UNCOMPR_RATE_[1:0]	This field configures the compression algorithm to write uncompressed data at each rate. (0: uncompressed data writing is not forced (default); 1: uncompressed data every 8 batch data rate; 2: uncompressed data every 16 batch data rate; 3: uncompressed data every 32 batch data rate)

1. *This bit is activated if the FIFO_COMPR_EN bit of EMB_FUNC_EN_B (05h) is set to 1.*

9.7 FIFO_CTRL3 (09h)

FIFO control register 3 (R/W)

Table 36. **FIFO_CTRL3 register**

BDR_GY_3	BDR_GY_2	BDR_GY_1	BDR_GY_0	BDR_XL_3	BDR_XL_2	BDR_XL_1	BDR_XL_0

Table 37. **FIFO_CTRL3 register description**

BDR_GY_[3:0]	Selects batch data rate (write frequency in FIFO) for gyroscope data. (0000: gyroscope not batched in FIFO (default); 0001: 1.875 Hz; 0010: 7.5 Hz; 0011: 15 Hz; 0100: 30 Hz; 0101: 60 Hz; 0110: 120 Hz; 0111: 240 Hz; 1000: 480 Hz; 1001: 960 Hz; 1010: 1.92 kHz; 1011: 3.84 kHz; 1100: 7.68 kHz 1101-1111: reserved)
BDR_XL_[3:0]	Selects batch data rate (write frequency in FIFO) for accelerometer data. (0000: accelerometer not batched in FIFO (default); 0001: 1.875 Hz; 0010: 7.5 Hz; 0011: 15 Hz; 0100: 30 Hz; 0101: 60 Hz; 0110: 120 Hz; 0111: 240 Hz; 1000: 480 Hz; 1001: 960 Hz; 1010: 1.92 kHz; 1011: 3.84 kHz; 1100: 7.68 kHz 1101-1111: reserved)

9.8 FIFO_CTRL4 (0Ah)

FIFO control register 4 (R/W)

Table 38. FIFO_CTRL4 register

DEC_TS_ BATCH_1	DEC_TS_ BATCH_0	ODR_T_ BATCH_1	ODR_T_ BATCH_0	0[(1)]	FIFO_ MODE_2	FIFO_ MODE_1	FIFO_ MODE_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 39. FIFO_CTRL4 register description

DEC_TS_BATCH_[1:0]	Selects decimation for timestamp batching in FIFO. Write rate is the maximum rate between the accelerometer and gyroscope BDR divided by decimation decoder. (00: timestamp not batched in FIFO (default); 01: decimation 1: max(BDR_XL[Hz],BDR_GY[Hz]) [Hz]; 10: decimation 8: max(BDR_XL[Hz],BDR_GY[Hz])/8 [Hz]; 11: decimation 32: max(BDR_XL[Hz],BDR_GY[Hz])/32 [Hz])
ODR_T_BATCH_[1:0]	Selects batch data rate (write frequency in FIFO) for temperature data (00: temperature not batched in FIFO (default); 01: 1.875 Hz; 10: 15 Hz; 11: 60 Hz)
FIFO_MODE_[2:0]	FIFO mode selection (000: bypass mode: FIFO disabled (default); 001: FIFO mode: stops collecting data when FIFO is full; 010: continuousWTM-to-full mode: continuous mode with FIFO watermark size until trigger is deasserted, then data are stored in FIFO until the buffer is full; 011: continuous-to-FIFO mode: continuous mode until trigger is deasserted, then FIFO mode; 100: bypass-to-continuous mode: bypass mode until trigger is deasserted, then continuous mode; 101: reserved; 110: continuous mode: if the FIFO is full, the new sample overwrites the older one; 111: bypass-to-FIFO mode: bypass mode until trigger is deasserted, then FIFO mode.)

9.9 COUNTER_BDR_REG1 (0Bh)

Counter batch data rate register 1 (R/W)

Table 40. **COUNTER_BDR_REG1 register**

0[(1)]	TRIG_COUNTER_BDR_1	TRIG_COUNTER_BDR_0	0[(1)]	XL_HG_BATCH_EN	0[(1)]	CNT_BDR_TH_9	CNT_BDR_TH_8

1. *This bit must be set to 0 for the correct operation of the device.*

Table 41. **COUNTER_BDR_REG1 register description**

TRIG_COUNTER_BDR_[1:0]	Selects the trigger for the internal counter of batch events between the accelerometer and gyroscope. (00: low-*g* accelerometer batch event; 01: gyroscope batch event; 10: reserved; 11: high-*g* accelerometer batch event)
XL_HG_BATCH_EN	Enables batching accelerometer high-*g* data in FIFO. Default value: 0
CNT_BDR_TH_[9:8]	In conjunction with CNT_BDR_TH_[7:0] in COUNTER_BDR_REG2 (0Ch), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (1Ch) is set to 1.

9.10 COUNTER_BDR_REG2 (0Ch)

Counter batch data rate register 2 (R/W)

Table 42. **COUNTER_BDR_REG2 register**

CNT_BDR_TH_7	CNT_BDR_TH_6	CNT_BDR_TH_5	CNT_BDR_TH_4	CNT_BDR_TH_3	CNT_BDR_TH_2	CNT_BDR_TH_1	CNT_BDR_TH_0

Table 43. **COUNTER_BDR_REG2 register description**

CNT_BDR_TH_[7:0]	In conjunction with CNT_BDR_TH_[9:8] in COUNTER_BDR_REG1 (0Bh), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (1Ch) is set to 1.

9.11 INT1_CTRL (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1 when the MIPI I3C® dynamic address is not assigned (I²C or SPI is used). Some bits can be also used to trigger an IBI (in-band interrupt) when the MIPI I3C® interface is used. The output of the pin is the OR combination of the signals selected here and in MD1_CFG (5Eh).

Table 44. INT1_CTRL register

0[(1)]	INT1_ CNT_BDR	INT1_ FIFO_FULL	INT1_ FIFO_OVR	INT1_ FIFO_TH	0[(1)]	INT1_ DRDY_G	INT1_ DRDY_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 45. INT1_CTRL register description

INT1_CNT_BDR	Enables COUNTER_BDR_IA interrupt on INT1 pin. Default value: 0
INT1_FIFO_FULL	Enables FIFO full flag interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT1_FIFO_OVR	Enables FIFO overrun interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT1_FIFO_TH	Enables FIFO threshold interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT1_DRDY_G	Enables gyroscope data-ready interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT1_DRDY_XL	Enables accelerometer data-ready interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0

9.12 INT2_CTRL (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2 when the MIPI I3C® dynamic address is not assigned (I²C or SPI is used). Some bits can be also used to trigger an IBI when the MIPI I3C® interface is used. The output of the pin is the OR combination of the signals selected here and in MD2_CFG (5Fh).

Table 46. INT2_CTRL register

INT2_EMB_ FUNC_ENDOP	INT2_ CNT_BDR	INT2_ FIFO_FULL	INT2_ FIFO_OVR	INT2_ FIFO_TH	0[(1)]	INT2_ DRDY_G	INT2_ DRDY_XL

1. This bit must be set to 0 for the correct operation of the device.

Table 47. INT2_CTRL register description

INT2_EMB_FUNC_ENDOP	Enables routing the embedded functions end of operations signal to the INT2 pin. Default value: 0
INT2_CNT_BDR	Enables COUNTER_BDR_IA interrupt on INT2. Default value: 0
INT2_FIFO_FULL	Enables FIFO full flag interrupt on INT2 pin.Default value: 0
INT2_FIFO_OVR	Enables FIFO overrun interrupt on INT2 pin. Default value: 0
INT2_FIFO_TH	Enables FIFO threshold interrupt on INT2 pin. Default value: 0
INT2_DRDY_G	Gyroscope data-ready interrupt on INT2 pin. Default value: 0
INT2_DRDY_XL	Accelerometer data-ready interrupt on INT2 pin. Default value: 0

9.13 WHO_AM_I (0Fh)

WHO_AM_I register (R). This is a read-only register. Its value is fixed at 73h.

Table 48. WhoAmI register

0	1	1	1	0	0	1	1

9.14 CTRL1 (10h)

Accelerometer control register 1 (R/W)

Table 49. CTRL1 register

0[(1)]	OP_MODE_XL_2	OP_MODE_XL_1	OP_MODE_XL_0	ODR_XL_3	ODR_XL_2	ODR_XL_1	ODR_XL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 50. CTRL1 register description

OP_MODE_XL_[2:0]	Accelerometer operating mode selection. (000: high-performance mode (default); 001: high-accuracy ODR mode; 010: reserved; 011: ODR-triggered mode; 100: low-power mode 1 (2 mean); 101: low-power mode 2 (4 mean); 110: low-power mode 3 (8 mean); 111: normal mode)
ODR_XL_[3:0]	Accelerometer ODR selection (see Table 51)

Table 51. Accelerometer ODR selection

ODR_XL_3	ODR_XL_2	ODR_XL_1	ODR_XL_0	ODR selection [Hz]
0	0	0	0	Power-down (default)
0	0	0	1	1.875 Hz (low-power mode)
0	0	1	0	7.5 Hz (high-performance, normal mode)
0	0	1	1	15 Hz (low-power, high-performance, normal mode)
0	1	0	0	30 Hz (low-power, high-performance, normal mode)
0	1	0	1	60 Hz (low-power, high-performance, normal mode)
0	1	1	0	120 Hz (low-power, high-performance, normal mode)
0	1	1	1	240 Hz (low-power, high-performance, normal mode)
1	0	0	0	480 Hz (high-performance, normal mode)
1	0	0	1	960 Hz (high-performance, normal mode)
1	0	1	0	1.92 kHz (high-performance, normal mode)
1	0	1	1	3.84 kHz (high-performance mode)
1	1	0	0	7.68 kHz (high-performance mode)
Others				Reserved

9.15 CTRL2 (11h)

Gyroscope control register 2 (R/W)

Table 52. CTRL2 register

0[(1)]	OP_MODE_ G_2	OP_MODE_ G_1	OP_MODE_ G_0	ODR_G_3	ODR_G_2	ODR_G_1	ODR_G_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 53. CTRL2 register description

OP_MODE_G_[2:0]	Gyroscope operating mode selection. (000: high-performance mode (default); 001: high-accuracy ODR mode; 010: reserved; 011: ODR-triggered mode; 100: sleep mode; 101: low-power mode; 110-111: reserved)
ODR_G_[3:0]	Gyroscope output data rate selection. (See Table 54)

Table 54. Gyroscope ODR selection

ODR_G_3	ODR_G_2	ODR_G_1	ODR_G_0	ODR [Hz]
0	0	0	0	Power-down (default)
0	0	1	0	7.5 Hz (low-power, high-performance mode)
0	0	1	1	15 Hz (low-power, high-performance mode)
0	1	0	0	30 Hz (low-power, high-performance mode)
0	1	0	1	60 Hz (low-power, high-performance mode)
0	1	1	0	120 Hz (low-power, high-performance mode)
0	1	1	1	240 Hz (low-power, high-performance mode)
1	0	0	0	480 Hz (high-performance mode)
1	0	0	1	960 Hz (high-performance mode)
1	0	1	0	1.92 kHz (high-performance mode)
1	0	1	1	3.84 kHz (high-performance mode)
1	1	0	0	7.68 kHz (high-performance mode)
Others				Reserved

9.16 CTRL3 (12h)

Control register 3 (R/W)

Table 55. CTRL3 register

BOOT	BDU	0[1]	0[1]	0[1]	IF_INC	0[1]	SW_RESET

1. *This bit must be set to 0 for the correct operation of the device.*

Table 56. CTRL3 register description

BOOT	Reboots memory content. This bit is automatically cleared. Default value: 0 (0: normal mode; 1: reboot memory content)
BDU	Block data update. Default value: 1 (0: continuous update; 1: output registers are not updated until LSB and MSB have been read)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I²C, MIPI I3C, or SPI). Default value: 1 (0: disabled; 1: enabled)
SW_RESET	Software reset, resets all control registers to their default value. This bit is automatically cleared. Default value: 0 (0: normal mode; 1: reset device)

9.17 CTRL4 (13h)

Control register 4 (R/W)

Table 57. CTRL4 register

0[(1)]	0[(1)]	0[(1)]	INT2_on_INT1	DRDY_MASK	INT2_DRDY_TEMP	DRDY_PULSED	INT2_IN_LH

1. *This bit must be set to 0 for the correct operation of the device.*

Table 58. CTRL4 register description

INT2_on_INT1	Enables routing the embedded functions interrupt signals to the INT1 pin. Default value: 0 • The corresponding bits in the INT2 control registers need to be enabled. • These interrupts are in OR with those enabled on the INT1 pin. • They are not fed to the INT2 pin. • The movable interrupts are: – INT2_EMB_FUNC_ENDOP enabled through INT2_CTRL (0Eh) – INT2_TIMESTAMP enabled through MD2_CFG (5Fh) – INT2_DRDY_TEMP enabled through CTRL4 (13h)
DRDY_MASK	Enables / masks data-ready signal. Default value: 0 (0: disabled; 1: masks DRDY signals (both low-*g* accelerometer, high-*g* accelerometer and gyroscope) until filter settling ends (low-*g* accelerometer, high-*g* accelerometer and gyroscope independently masked)) *Note: Refer to the product application note for the details regarding operating/power mode configurations, settings, turn-on/off time, and on-the-fly changes.*
INT2_DRDY_TEMP	Enables temperature sensor data-ready interrupt on the INT2 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used and INT2_ON_INT1 = 1 in CTRL4_C (13h). Default value: 0 (0: disabled; 1: enabled)
DRDY_PULSED	Enables pulsed data-ready mode. Default value: 0 (0: data-ready latched mode (returns to 0 only after the higher part of the associated output register has been read); 1: data-ready pulsed mode (the data-ready pulses are 65 μs long))
INT2_IN_LH	Set to 1 in order to change the polarity of the INT2 pin input trigger for the embedded functions. Default value: 0 (0: trigger for the embedded functions pin is active low; 1: trigger for the embedded functions pin is active high)

9.18 CTRL5 (14h)

Control register 5 (R/W)

Table 59. CTRL5 register

0[(1)]	0[(1)]	0[(1)]	0[(1)]	0[(1)]	BUS_ACT_SEL_1	BUS_ACT_SEL_0	INT_EN_I3C

1. *This bit must be set to 0 for the correct operation of the device.*

Table 60. CTRL5 register description

BUS_ACT_SEL_[1:0]	Bus available time selection for IBI (in-band interrupt): 00: 50 μs (default); 01: 2 μs; 10: 1 ms; 11: 50 ms)
INT_EN_I3C	Enables the INT pin when I3C is enabled. Default value: 0 (0: disabled; 1: enabled)

9.19 CTRL6 (15h)

Control register 6 (R/W)

Table 61. CTRL6 register

0[(1)]	LPF1_G_BW_2	LPF1_G_BW_1	LPF1_G_BW_0	1[(2)]	FS_G_2	FS_G_1	FS_G_0

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 62. CTRL6 register description

LPF1_G_BW_[2:0]	Gyroscope low-pass filter (LPF1) bandwidth selection Table 63 shows the selectable bandwidth values.
FS_G_[2:0][(1)]	Gyroscope UI chain full-scale selection: (000: reserved (default); 001: ±250 dps; 010: ±500 dps; 011: ±1000 dps; 100: ±2000 dps; 101: ±4000 dps)

1. *The default configuration of FS_G_[2:0] is 000 (reserved). For the correct operation of the device, the user must set a configuration from 001 to 101 when the gyroscope is in power-down mode.*

Table 63. Gyroscope LPF1 + LPF2 bandwidth selection

LPF1_G_BW_[2:0]	60 Hz	120 Hz	240 Hz	480 Hz	960 Hz	1.92 kHz	3.84 kHz	7.68 kHz
000	24.6	49.4	96	175	241	273	280	281
001	24.6	49.4	96	157	195	210	213	213
010	24.6	49.4	96	131	149	155	156	156
011	24.6	49.4	96	188	310	387	403	407
100	24.6	49.4	78.4	94	100	101	102	102
101	24.6	42.6	53	56.7	57.9	58.2	58.3	58
110	18.0	24.2	27.3	28.4	28.7	28.8	28.8	28.8
111	12.1	13.6	14.2	14.3	14.4	14.4	14.4	14.4

9.20 CTRL7 (16h)

Control register 7 (R/W)

Table 64. CTRL7 register

INT1_DRDY_XL_HG	INT2_DRDY_XL_HG	0[(1)]	0[(1)]	0[(1)]	0[(1)]	0[(1)]	LPF1_G_EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 65. CTRL7 register description

INT1_DRDY_XL_HG	Enables a high-*g* accelerometer data-ready interrupt on the INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT2_DRDY_XL_HG	Enables a high-*g* accelerometer data-ready interrupt on the INT2 pin. Default value: 0
LPF1_G_EN	Enables the gyroscope digital LPF1 filter. The bandwidth can be selected through LPF1_G_BW_[2:0] in CTRL6 (15h)

9.21 CTRL8 (17h)

Control register 8 (R/W)

Table 66. CTRL8 register

HP_LPF2_ XL_BW_2	HP_LPF2_ XL_BW_1	HP_LPF2_ XL_BW_0	0[(1)]	0[(1)]	0[(1)]	FS_XL_1	FS_XL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 67. CTRL8 register description

HP_LPF2_XL_BW_[2:0]	Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to Table 68.
FS_XL_[1:0]	Accelerometer full-scale selection: (00: ±2 *g*; 01: ±4 *g*; 10: ±8 *g*; 11: ±16 *g*)

Table 68. Accelerometer bandwidth configurations

Filter type	HP_SLOPE_ XL_EN	LPF2_XL_EN	HP_LPF2_XL_BW_[2:0]	Bandwidth
Low pass	0	0	-	ODR/2[(1)]
		1	000	ODR/4
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800
High pass	1	-	000	SLOPE (ODR/4)
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800

1. *This value is ODR/2 when the accelerometer is in high-performance mode, high-accuracy ODR mode and normal mode. It is equal to 2300 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) and 431 Hz in low-power mode 3 (8 mean).*

9.22 CTRL9 (18h)

Control register 9 (R/W)

Table 69. CTRL9 register

0[(1)]	HP_REF_MODE_XL	XL_FASTSETTL_MODE	HP_SLOPE_XL_EN	LPF2_XL_EN	0[(1)]	USR_OFF_W	USR_OFF_ON_OUT

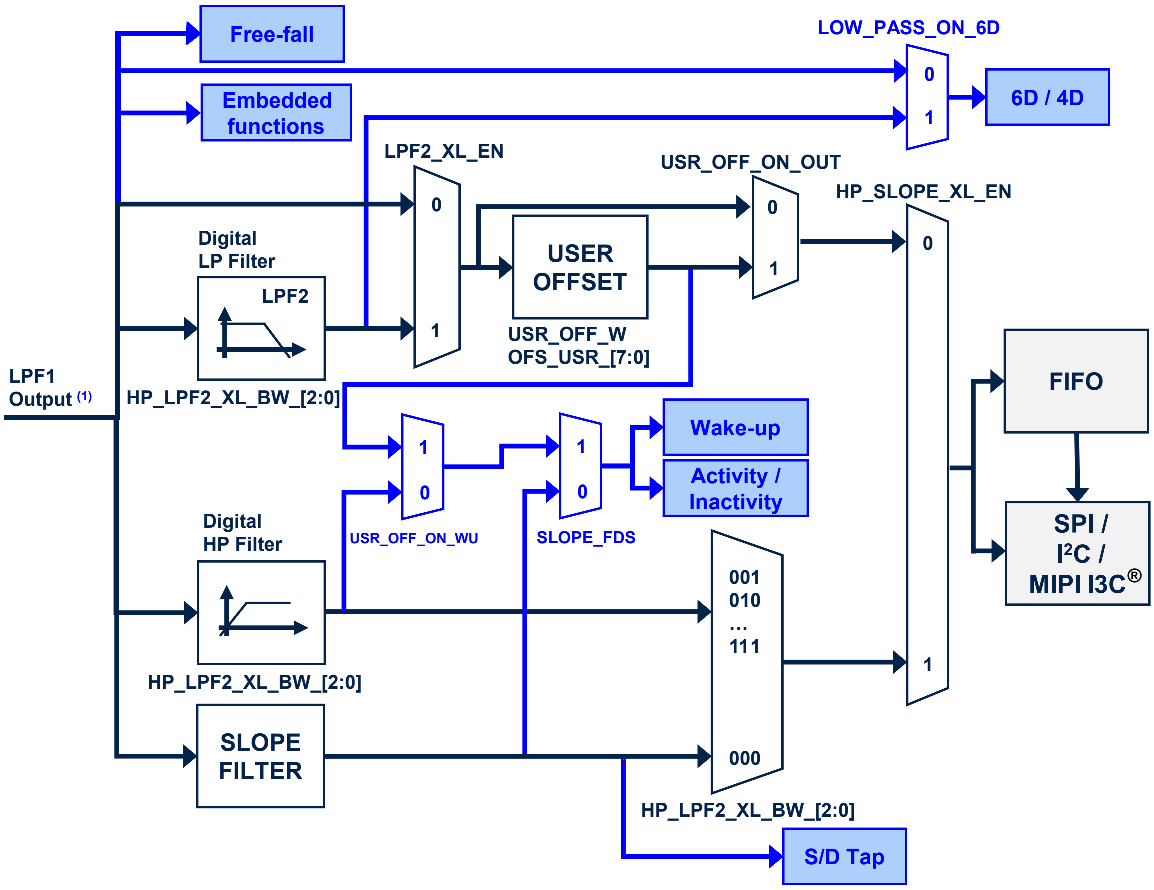
1. *This bit must be set to 0 for the correct operation of the device.*

Table 70. CTRL9 register description

HP_REF_MODE_XL	Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be 1). Default value: 0 (0: disabled, 1: enabled)[(1)]
XL_FASTSETTL_MODE	Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the first sample after writing this bit. Active only during device exit from power-down mode. Default value: 0 (0: disabled, 1: enabled)
HP_SLOPE_XL_EN	Accelerometer slope filter / high-pass filter selection. Refer to Figure 23. Default value: 0 (0: low-pass filter path selected; 1: high-pass filter path selected)
LPF2_XL_EN	Accelerometer high-resolution selection. Refer to Figure 23. Default value: 0 (0: output from first stage digital filtering selected; 1: output from LPF2 second filtering stage selected)
USR_OFF_W	Weight of XL user offset bits of registers XL_HG_X_OFS_USR (6Ch), XL_HG_Y_OFS_USR (6Dh), XL_HG_Z_OFS_USR (6Eh). Default value: 0 (0: 2^{-10} *g*/LSB; 1: 2^{-6} *g*/LSB)
USR_OFF_ON_OUT	Enables accelerometer user offset correction block; it is valid for the low-pass path. Refer to Figure 23. Default value: 0 (0: accelerometer user offset correction block bypassed; 1: accelerometer user offset correction block enabled)

1. *When enabled, the first output data has to be discarded.*

Figure 23. Low-*g* accelerometer composite filter



1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode, high-accuracy ODR mode or normal mode. This value is equal to 2300 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) or 431 Hz in low-power mode 3 (8 mean).*

9.23 CTRL10 (19h)

Control register 10 (R/W)

Table 71. CTRL10 register

0[(1)]	EMB_FUNC_DEBUG	0[(1)]	0[(1)]	ST_G_1	ST_G_0	ST_XL_1	ST_XL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 72. CTRL10 register description

EMB_FUNC_DEBUG	Enables debug mode for the embedded functions. (0: disabled; 1: enabled)
ST_G_[1:0]	Gyroscope self-test selection (00: normal mode (default); 01: positive sign self-test; 10: negative sign self-test; 11: reserved)
ST_XL_[1:0]	Accelerometer self-test selection (00: normal mode (default); 01: positive sign self-test; 10: negative sign self-test; 11: reserved)

9.24 CTRL_STATUS (1Ah)

(R)

Table 73. CTRL_STATUS register

0	0	0	0	0	FSM_WR_CTRL_STATUS	-	0

Table 74. CTRL_STATUS register description

FSM_WR_CTRL_STATUS	This flag indicates the current controller of the device configuration registers. This flag must be used as an acknowledge flag when the value of the FSM_WR_CTRL_EN bit in the FUNC_CFG_ACCESS (01h) register is changed. Default value: 0 (0: all registers and configurations are writable from the standard interface; 1: some registers and configurations are under FSM control and are in read-only mode from the standard interface).

9.25 FIFO_STATUS1 (1Bh)

FIFO status register 1 (R)

Table 75. **FIFO_STATUS1 register**

DIFF_ FIFO_7	DIFF_ FIFO_6	DIFF_ FIFO_5	DIFF_ FIFO_4	DIFF_ FIFO_3	DIFF_ FIFO_2	DIFF_ FIFO_1	DIFF_ FIFO_0

Table 76. **FIFO_STATUS1 register description**

DIFF_FIFO_[7:0]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO In conjunction with DIFF_FIFO_8 in FIFO_STATUS2 (1Ch).

9.26 FIFO_STATUS2 (1Ch)

FIFO status register 2 (R)

Table 77. **FIFO_STATUS2 register**

FIFO_ WTM_IA	FIFO_ OVR_IA	FIFO_ FULL_IA	COUNTER_ BDR_IA	FIFO_OVR_ LATCHED	0	0	DIFF_ FIFO_8

Table 78. **FIFO_STATUS2 register description**

FIFO_WTM_IA	FIFO watermark status. Default value: 0 (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or greater than WTM) Watermark is set through bits WTM[7:0] in FIFO_CTRL2 (08h) and FIFO_CTRL1 (07h).
FIFO_OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_FULL_IA	Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR)
COUNTER_BDR_IA	Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0 This bit is reset when these registers are read.
FIFO_OVR_LATCHED	Latched FIFO overrun status. Default value: 0 This bit is reset when this register is read.
DIFF_FIFO_8	Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00 In conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (1Bh)

9.27 ALL_INT_SRC (1Dh)

Source register for all interrupts (R)

Table 79. ALL_INT_SRC register

EMB_ FUNC_IA	SHUB_IA	SLEEP_ CHANGE_IA	D6D_IA	HG_IA	TAP_IA	WU_IA	FF_IA

Table 80. ALL_INT_SRC register description

EMB_FUNC_IA	Embedded functions interrupt status. Default value: 0 (0: embedded functions event not detected; 1: embedded functions event detected)
SHUB_IA	Sensor hub (I²C controller) interrupt status. Default value: 0 (0: sensor hub interrupt not generated; 1: sensor hub interrupt generated)
SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
D6D_IA	Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0 (0: change in position not detected; 1: change in position detected)
HG_IA	High-*g* interrupt status (logical OR between the high-*g* wake-up and high-*g* shock) (0: event on high-*g* not detected, 1: event on high-*g* detected)
TAP_IA	Single or double-tap event detection status depending on the SINGLE_DOUBLE_TAP_bit value (see WAKE_UP_THS (5Bh) register). Default value: 0 (0: tap event not detected; 1: tap event detected)
WU_IA	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)
FF_IA	Free-fall event status. Default value: 0 (0: event not detected, 1: event detected)

9.28 STATUS_REG (1Eh)

The STATUS_REG register is read by the SPI/I²C & MIPI I3C® interface (R).

Table 81. STATUS_REG register

TIMESTAMP_ ENDCOUNT	0	0	0	XLHGDA	TDA	GDA	XLDA

Table 82. STATUS_REG register description

TIMESTAMP_ENDCOUNT	Alerts timestamp overflow within 5.6 ms
XLHGDA	High-*g* accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)
TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

9.29 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two's complement.

Table 83. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 84. OUT_TEMP_H register

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8

Table 85. OUT_TEMP register description

Temp[15:0]	Temperature sensor output data The value is expressed in two's complement.

9.30 OUTX_L_G (22h) and OUTX_H_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

Table 86. OUTX_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 87. OUTX_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 88. OUTX_G register description

D[15:0]	Gyroscope UI chain pitch axis (X) angular rate output value

9.31 OUTY_L_G (24h) and OUTY_H_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

Table 89. **OUTY_L_G register**

D7	D6	D5	D4	D3	D2	D1	D0

Table 90. **OUTY_H_G register**

D15	D14	D13	D12	D11	D10	D9	D8

Table 91. **OUTY_G register description**

D[15:0]	Gyroscope UI chain roll axis (Y) angular rate output value

9.32 OUTZ_L_G (26h) and OUTZ_H_G (27h)

Angular rate sensor yaw axis (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

Table 92. **OUTZ_L_G register**

D7	D6	D5	D4	D3	D2	D1	D0

Table 93. **OUTZ_H_G register**

D15	D14	D13	D12	D11	D10	D9	D8

Table 94. **OUTZ_H_G register description**

D[15:0]	Gyroscope UI chain yaw axis (Z) angular rate output value

9.33 OUTX_L_A (28h) and OUTX_H_A (29h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

Table 95. OUTX_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 96. OUTX_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 97. OUTX_A register description

D[15:0]	Accelerometer UI chain X-axis linear acceleration output value

9.34 OUTY_L_A (2Ah) and OUTY_H_A (2Bh)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

Table 98. OUTY_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 99. OUTY_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 100. OUTY_A register description

D[15:0]	Accelerometer UI chain Y-axis linear acceleration output value

9.35 OUTZ_L_A (2Ch) and OUTZ_H_A (2Dh)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

Table 101. OUTZ_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 102. OUTZ_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 103. OUTZ_A register description

D[15:0]	Accelerometer UI chain Z-axis linear acceleration output value

9.36 UI_OUTX_L_A_HG (34h) and UI_OUTX_H_A_HG (35h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two’s complement.

Data are according to the accelerometer full-scale and ODR settings of the accelerometer high-*g* mode configuration.

Table 104. UI_OUTX_L_A_HG register

D7	D6	D5	D4	D3	D2	D1	D0

Table 105. UI_OUTX_H_A_HG register

D15	D14	D13	D12	D11	D10	D9	D8

Table 106. UI_OUTX_A_HG register description

D[15:0]	Accelerometer X-axis high-*g* output expressed in two's complement

9.37 UI_OUTY_L_A_HG (36h) and UI_OUTY_H_A_HG (37h)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two’s complement.

Data are according to the accelerometer full-scale and ODR settings of the accelerometer high-*g* mode configuration.

Table 107. UI_OUTY_L_A_HG register

D7	D6	D5	D4	D3	D2	D1	D0

Table 108. UI_OUTY_H_A_HG register

D15	D14	D13	D12	D11	D10	D9	D8

Table 109. UI_OUTY_A_HG register description

D[15:0]	Accelerometer Y-axis high-*g* output expressed in two's complement

9.38 UI_OUTZ_L_A_HG (38h) and UI_OUTZ_H_A_HG (39h)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two’s complement.

Data are according to the accelerometer full-scale and ODR settings of the accelerometer high-*g* mode configuration.

Table 110. UI_OUTZ_L_A_HG register

D7	D6	D5	D4	D3	D2	D1	D0

Table 111. UI_OUTZ_H_A_HG register

D15	D14	D13	D12	D11	D10	D9	D8

Table 112. UI_OUTZ_A_HG register description

D[15:0]	Accelerometer Z-axis high-*g* output expressed in two's complement

9.39 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 21.7 µs (typical).

Table 113. TIMESTAMP output registers

D31	D30	D29	D28	D27	D26	D25	D24

D23	D22	D21	D20	D19	D18	D17	D16

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 114. TIMESTAMP output register description

D[31:0]	Timestamp output registers: 1LSB = 21.7 µs (typical)

9.40 UI_STATUS_REG (44h)

Table 115. UI_STATUS_REG register

0	0	0	0	0	GYRO_ SETTLING	0	0

Table 116. UI_STATUS_REG register description

GYRO_SETTLING	High when the gyroscope output is in the settling phase

9.41 WAKE_UP_SRC (45h)

Wake-up interrupt source register (R)

Table 117. **WAKE_UP_SRC register**

0	SLEEP_ CHANGE_IA	FF_IA	SLEEP_ STATE	WU_IA	X_WU	Y_WU	Z_WU

Table 118. **WAKE_UP_SRC register description**

SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
FF_IA	Free-fall event detection status. Default: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE	Sleep status bit. Default value: 0 (0: Activity status; 1: Inactivity status)
WU_IA	Wake-up event detection status. Default value: 0 (0: wake-up event not detected; 1: wake-up event detected.)
X_WU	Wake-up event detection status on X-axis. Default value: 0 (0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected)
Y_WU	Wake-up event detection status on Y-axis. Default value: 0 (0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected)
Z_WU	Wake-up event detection status on Z-axis. Default value: 0 (0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected)

9.42 TAP_SRC (46h)

Tap source register (R)

Table 119. TAP_SRC register

0	TAP_IA	SINGLE_TAP	DOUBLE_TAP	TAP_SIGN	X_TAP	Y_TAP	Z_TAP

Table 120. TAP_SRC register description

TAP_IA	Tap event detection status. Default: 0 (0: tap event not detected; 1: tap event detected)
SINGLE_TAP	Single-tap event status. Default value: 0 (0: single tap event not detected; 1: single tap event detected)
DOUBLE_TAP	Double-tap event detection status. Default value: 0 (0: double-tap event not detected; 1: double-tap event detected.)
TAP_SIGN	Sign of acceleration detected by tap event. Default: 0 (0: positive sign of acceleration detected by tap event; 1: negative sign of acceleration detected by tap event)
X_TAP	Tap event detection status on X-axis. Default value: 0 (0: tap event on X-axis not detected; 1: tap event on X-axis detected)
Y_TAP	Tap event detection status on Y-axis. Default value: 0 (0: tap event on Y-axis not detected; 1: tap event on Y-axis detected)
Z_TAP	Tap event detection status on Z-axis. Default value: 0 (0: tap event on Z-axis not detected; 1: tap event on Z-axis detected)

9.43 D6D_SRC (47h)

Portrait, landscape, face-up and face-down source register (R)

Table 121. D6D_SRC register

0	D6D_IA	ZH	ZL	YH	YL	XH	XL

Table 122. D6D_SRC register description

D6D_IA	Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over-threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

9.44 STATUS_CONTROLLER_MAINPAGE (48h)

Sensor hub source register (R)

Table 123. STATUS_CONTROLLER_MAINPAGE register

WR_ONCE_ DONE	TARGET3_ NACK	TARGET2_ NACK	TARGET1_ NACK	TARGET0_ NACK	0	0	SENS_HUB _ENDOP

Table 124. STATUS_CONTROLLER_MAINPAGE register description

WR_ONCE_DONE	When the bit WRITE_ONCE in CONTROLLER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on target 0 has been performed and completed. Default value: 0
TARGET3_NACK	This bit is set to 1 if not acknowledge occurs on target 3 communication. Default value: 0
TARGET2_NACK	This bit is set to 1 if not acknowledge occurs on target 2 communication. Default value: 0
TARGET1_NACK	This bit is set to 1 if not acknowledge occurs on target 1 communication. Default value: 0
TARGET0_NACK	This bit is set to 1 if not acknowledge occurs on target 0 communication. Default value: 0
SENS_HUB_ENDOP	Sensor hub communication status. Default value: 0 (0: sensor hub communication not concluded; 1: sensor hub communication concluded)

9.45 EMB_FUNC_STATUS_MAINPAGE (49h)

Embedded function status register (R)

Table 125. **EMB_FUNC_STATUS_MAINPAGE register**

IS_FSM_LC	0	IS_SIGMOT	IS_TILT	IS_STEP_DET	0	0	0

Table 126. **EMB_FUNC_STATUS_MAINPAGE register description**

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)
IS_SIGMOT	Interrupt status bit for significant motion detection (1: interrupt detected; 0: no interrupt)
IS_TILT	Interrupt status bit for tilt detection (1: interrupt detected; 0: no interrupt)
IS_STEP_DET	Interrupt status bit for step detection (1: interrupt detected; 0: no interrupt)

9.46 FSM_STATUS_MAINPAGE (4Ah)

Finite state machine status register (R)

Table 127. **FSM_STATUS_MAINPAGE register**

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1

Table 128. **FSM_STATUS_MAINPAGE register description**

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

9.47 MLC_STATUS_MAINPAGE (4Bh)

Machine learning core status register (R)

Table 129. MLC_STATUS _MAINPAGE register

IS_MLC8	IS_MLC7	IS_MLC6	IS_MLC5	IS_MLC4	IS_MLC3	IS_MLC2	IS_MLC1

Table 130. MLC_STATUS_MAINPAGE register description

IS_MLC8	Interrupt status bit for MLC8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC7	Interrupt status bit for MLC7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC6	Interrupt status bit for MLC6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC5	Interrupt status bit for MLC5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC4	Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC3	Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC2	Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC1	Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt)

9.48 HG_WAKE_UP_SRC (4Ch)

High-*g* wake-up source register (R)

Table 131. HG_WAKE_UP_SRC register

-	HG_SHOCK_ CHANGE_IA	HG_SHOCK_ STATE	HG_WU_ CHANGE_IA	HG_WU_IA	HG_X_WU	HG_Y_WU	HG_Z_WU

Table 132. HG_WAKE_UP_SRC register description

HG_SHOCK_CHANGE_IA	High-*g* shock state change event detected. Default value: 0 (0: shock state change event not detected; 1: shock state change event detected)
HG_SHOCK_STATE	High-*g* shock function is in shock state. Default value: 0 (0: high-*g* shock function not in shock state; 1: high-*g* shock function in shock state)
HG_WU_CHANGE_IA	High-*g* wake-up change event detection status (high-*g* data passes from all axes under the threshold to at least one axis over the threshold, or vice versa). Default value: 0 (0: wake-up change event not detected; 1: wake-up change event detected)
HG_WU_IA	High-*g* wake-up event detection status (one axis exceeds threshold). Default value: 0 (0: wake-up event not detected; 1: wake-up event detected)
HG_X_WU	High-*g* wake-up event detection status on the X-axis. Default value: 0 (0: wake-up event on the X-axis not detected; 1: wake-up event on the X-axis detected)
HG_Y_WU	High-*g* wake-up event detection status on the Y-axis. Default value: 0 (0: wake-up event on the Y-axis not detected; 1: wake-up event on the Y-axis detected)
HG_Z_WU	High-*g* wake-up event detection status on the Z-axis. Default value: 0 (0: wake-up event on the Z-axis not detected; 1: wake-up event on the Z-axis detected)

9.49 CTRL2_XL_HG (4Dh)

Control register 2 high-*g* accelerometer (R/W)

Table 133. **CTRL2_XL_HG register**

0[(1)]	0[(1)]	0[(1)]	HG_USR_ OFF_ON_WU	0[(1)]	0[(1)]	XL_HG_ST1	XL_HG_ST0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 134. **CTRL2_XL_HG register description**

HG_USR_OFF_ON_WU	Drives the data with user offset correction to the high-*g* wake-up and high-*g* shock
XL_HG_ST[1:0]	High-*g* accelerometer self-test selection (00: normal mode (default); 01: positive sign self-test; 10: negative sign self-test; 11: reserved)

9.50 CTRL1_XL_HG (4Eh)

Control register 1 high-*g* accelerometer (R/W)

Table 135. **CTRL1_XL_HG register**

XL_HG_ REGOUT_EN	HG_USR_ OFF_ON_OUT	ODR_XL_ HG_2	ODR_XL_ HG_1	ODR_XL_ HG_0	FS_XL_ HG_2	FS_XL_ HG_1	FS_XL_ HG_0

Table 136. **CTRL1_XL_HG register description**

XL_HG_REGOUT_EN	Enables read of high-*g* accelerometer channel from output registers UI_OUTX_L_A_HG (34h) and UI_OUTX_H_A_HG (35h) through UI_OUTZ_L_A_HG (38h) and UI_OUTZ_H_A_HG (39h)
HG_USR_OFF_ON_OUT	Enables high-*g* accelerometer user offset functionality on output registers
ODR_XL_HG_[2:0]	High-*g* accelerometer ODR selection, see Table 137
FS_XL_HG_[2:0]	High-*g* accelerometer full-scale selection, see Table 138

Table 137. **High-*g* accelerometer ODR selection**

Code	ODR	Code	ODR
000	Power-down (default)	100	960 Hz
001	N/A	101	1.92 kHz
010	N/A	110	3.84 kHz
011	480 Hz	111	7.68 kHz

Table 138. **High-*g* accelerometer full-scale selection**

FS_XL_HG_[2:0]	Full scale [*g*]
000	32
001	64
010	80
011	Reserved
100	Reserved

9.51 INTERNAL_FREQ_FINE (4Fh)

Internal frequency register (R)

Table 139. INTERNAL_FREQ_FINE register

FREQ_FINE_7	FREQ_FINE_6	FREQ_FINE_5	FREQ_FINE_4	FREQ_FINE_3	FREQ_FINE_2	FREQ_FINE_1	FREQ_FINE_0

Table 140. INTERNAL_FREQ_FINE register description

FREQ_FINE_[7:0]	Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.13%. 8-bit format, two's complement.

The actual timestamp resolution and the actual output data rate can be calculated using the following formulas:

$$t_{actual}[s] = \frac{1}{46080 \cdot (1 + 0.0013 \cdot FREQ\_FINE)}$$

$$ODR_{actual}[Hz] = \frac{7680 \cdot (1 + 0.0013 \cdot FREQ\_FINE)}{ODR_{coeff}}$$

Table 141. ODR_{coeff} values

Selected ODR [Hz]	ODRcoeff
7.5	1024
15	512
30	256
60	128
120	64
240	32
480	16
960	8
1.92 kHz	4
3.84 kHz	2
7.68 kHz	1

9.52 FUNCTIONS_ENABLE (50h)

Enable interrupt functions register (R/W)

Table 142. FUNCTIONS_ENABLE register

INTERRUPTS_ENABLE	TIMESTAMP_EN	0[(1)]	0[(1)]	DIS_RST_LIR_ALL_INT	0[(1)]	INACT_EN_1	INACT_EN_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 143. FUNCTIONS_ENABLE register description

INTERRUPTS_ENABLE	Enables basic interrupts (6D/4D, free-fall, wake-up, tap, activity/inactivity). Default value: 0 (0: interrupt disabled; 1: interrupt enabled)
TIMESTAMP_EN	Enables timestamp counter. The counter is readable in TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h). Default value: 0 (0: disabled; 1: enabled)
DIS_RST_LIR_ALL_INT	When this bit is set to 1, reading the ALL_INT_SRC (1Dh) register does not reset the latched interrupt signals. This can be useful in order to not reset some status flags before reading the corresponding status register. Default value: 0 (0: disabled; 1: enabled)
INACT_EN_[1:0]	Enables activity/inactivity (sleep) function. Default value: 00 (00: stationary/motion-only interrupts generated, accelerometer and gyroscope configuration do not change; 01: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope configuration does not change; 10: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope in sleep mode; 11: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope in power-down mode)

9.53 HG_FUNCTIONS_ENABLE (52h)

Enable high-*g* functions register (R/W)

Table 144. HG_FUNCTIONS_ENABLE register

HG_INTERRUPTS_ENABLE	HG_WU_CHANGE_INT_SEL	INT2_HG_WU	INT1_HG_WU	HG_SHOCK_DUR_3	HG_SHOCK_DUR_2	HG_SHOCK_DUR_1	HG_SHOCK_DUR_0

Table 145. HG_FUNCTIONS_ENABLE register description

HG_INTERRUPTS_ENABLE	Enables high-*g* interrupt generator (high-*g* wake-up and high-*g* shock). Default value: 0 (0: interrupt disabled; 1: interrupt enabled)
HG_WU_CHANGE_INT_SEL	Selects the type of wake-up interrupt to be sent to the INT1 pin, INT2 pin, and described by the HG_IA bit (ALL_INT_SRC (1Dh)). Default value: 0 (0: interrupt generated each time one of the three axes is higher than the threshold; 1: interrupt when high-*g* passes from all axes under the threshold to at least one axis over the threshold, or vice versa.)
INT2_HG_WU	Routes high-*g* wake-up event to INT2. Default value: 0 (0: routing high-*g* wake-up event to INT2 disabled; 1: routing high-*g* wake-up event to INT2 enabled)
INT1_HG_WU	Routes high-*g* wake-up event to INT1. Default value: 0 (0: routing high-*g* wake-up event to INT1 disabled; 1: routing high-*g* wake-up event to INT1 enabled)
HG_SHOCK_DUR_[3:0]	High-*g* duration to exit from shock state. Allowed values for HG_SHOCK_DUR_[3:0] are in the range of 0 (default) to 14. HG_SHOCK_DUR[s] = (HG_SHOCK_DUR_[3:0] +1)*512/ODR_XL_HG

9.54 HG_WAKE_UP_THS (53h)

High-*g* wake-up threshold register (R)

Table 146. HG_WAKE_UP_THS register

HG_WK_THS_7	HG_WK_THS_6	HG_WK_THS_5	HG_WK_THS_4	HG_WK_THS_3	HG_WK_THS_2	HG_WK_THS_1	HG_WK_THS_0

Table 147. HG_WAKE_UP_THS register description

HG_WK_THS_[7:0]	High-*g* wake-up threshold. The resolution of the threshold is 1 *g*/LSB. Default value: 00000000

9.55 INACTIVITY_DUR (54h)

Activity/inactivity configuration register (R/W)

Table 148. **INACTIVITY_DUR register**

SLEEP_STATUS _ON_INT	WU_INACT_ THS_W_2	WU_INACT_ THS_W_1	WU_INACT_ THS_W_0	XL_INACT _ODR_1	XL_INACT _ODR_0	INACT _DUR_1	INACT _DUR_0

Table 149. **INACTIVITY_DUR register description**

SLEEP_STATUS_ON_INT	Activity/inactivity interrupt mode configuration. If the INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bit is enabled, drives the sleep status or sleep change on the INT pin. Default value: 0 (0: sleep change notification on INT pin; 1: sleep status reported on INT pin)
WU_INACT_THS_W_[2:0]	Weight of 1 LSB of wake-up (WU_THS) and activity/inactivity (INACT_THS) threshold. (000: 7.8125 m*g*/LSB (default); 001: 15.625 m*g*/LSB; 010: 31.25 m*g*/LSB; 011: 62.5 m*g*/LSB; 100: 125 m*g*/LSB; 101 - 110 - 111: 250 m*g*/LSB)
XL_INACT_ODR_[1:0]	Selects the ODR_XL target during inactivity. (00: 1.875 Hz; 01: 15 Hz (default); 10: 30 Hz; 11: 60 Hz)
INACT_DUR_[1:0]	Duration in the transition from stationary to motion (from inactivity to activity). (00: transition to motion (activity) immediately at first overthreshold event (default); 01: transition to motion (activity) after two consecutive overthreshold events; 10: transition to motion (activity) after three consecutive overthreshold events; 11: transition to motion (activity) after four consecutive overthreshold events)

9.56 INACTIVITY_THS (55h)

Activity/inactivity threshold setting register (R/W)

Table 150. INACTIVITY_THS register

INT2_HG_ SHOCK_CHANGE	INT1_HG_ SHOCK_CHANGE	INACT_ THS_5	INACT_ THS_4	INACT_ THS_3	INACT_ THS_2	INACT_ THS_1	INACT_ THS_0

Table 151. INACTIVITY_THS register description

INT2_HG_SHOCK_CHANGE	Routes high-*g* shock event to INT2. Default value: 0 (0: routing high-*g* shock event to INT2 disabled; 1: routing high-*g* shock event to INT2 enabled)
INT1_HG_SHOCK_CHANGE	Routes high-*g* shock event to INT1. Default value: 0 (0: routing high-*g* shock event to INT1 disabled; 1: routing high-*g* shock event to INT1 enabled)
INACT_THS_[5:0]	Activity/inactivity threshold. The resolution of the threshold depends on the value of WU_INACT_THS_W_[2:0] in the INACTIVITY_DUR (54h) register. Default value: 000000

9.57 TAP_CFG0 (56h)

Tap configuration register 0 (R/W)

Table 152. TAP_CFG0 register

0[(1)]	LOW_PASS_ON_6D	HW_FUNC_MASK_XL_SETTL	SLOPE_FDS	TAP_X_EN	TAP_Y_EN	TAP_Z_EN	LIR

1. *This bit must be set to 0 for the correct operation of the device.*

Table 153. TAP_CFG0 register description

LOW_PASS_ON_6D	LPF2 filter on 6D function selection. Refer to Figure 23. Default value: 0 (0: ODR/2 low-pass filtered data sent to 6D interrupt function; 1: LPF2 output data sent to 6D interrupt function)
HW_FUNC_MASK_XL_SETTL	Enables masking the execution trigger of the basic interrupt functions (6D/4D, free-fall, wake-up, tap, activity/inactivity) when accelerometer data are settling. Default value: 0 (0: disabled; 1: enabled) *Note: Refer to the product application note for the details regarding operating/power mode configurations, settings, turn-on/off time and on-the-fly changes.*
SLOPE_FDS	HPF or slope filter selection on wake-up and activity/inactivity functions. Refer to Figure 23. Default value: 0 (0: slope filter applied; 1: HPF applied)
TAP_X_EN	Enables X direction in tap recognition. Default value: 0 (0: X direction disabled; 1: X direction enabled)
TAP_Y_EN	Enables Y direction in tap recognition. Default value: 0 (0: Y direction disabled; 1: Y direction enabled)
TAP_Z_EN	Enables Z direction in tap recognition. Default value: 0 (0: Z direction disabled; 1: Z direction enabled)
LIR	Latched interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)

9.58 TAP_CFG1 (57h)

Tap configuration register 1 (R/W)

Table 154. TAP_CFG1 register

TAP_ PRIORITY_2	TAP_ PRIORITY_1	TAP_ PRIORITY_0	TAP_ THS_X_4	TAP_ THS_X_3	TAP_ THS_X_2	TAP_ THS_X_1	TAP_ THS_X_0

Table 155. TAP_CFG1 register description

TAP_PRIORITY_[2:0]	Selection of axis priority for tap detection (see Table 156)
TAP_THS_X_[4:0]	X-axis tap recognition threshold. Default value: 0 1 LSB = FS_XL / (2^5)

Table 156. TAP priority decoding

TAP_PRIORITY_[2:0]	Max. priority	Mid. priority	Min. priority
000	X	Y	Z
001	Y	X	Z
010	X	Z	Y
011	Z	Y	X
100	X	Y	Z
101	Y	Z	X
110	Z	X	Y
111	Z	Y	X

9.59 TAP_CFG2 (58h)

Tap configuration register 2 (R/W)

Table 157. TAP_CFG2 register

0[(1)]	0[(1)]	0[(1)]	TAP_ THS_Y_4	TAP_ THS_Y_3	TAP_ THS_Y_2	TAP_ THS_Y_1	TAP_ THS_Y_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 158. TAP_CFG2 register description

TAP_THS_Y_[4:0]	Y-axis tap recognition threshold. Default value: 0 1 LSB = FS_XL / (2^5)

9.60 TAP_THS_6D (59h)

Portrait/landscape position and tap function threshold register (R/W)

Table 159. TAP_THS_6D register

D4D_EN	SIXD_THS_1	SIXD_THS_0	TAP_ THS_Z_4	TAP_ THS_Z_3	TAP_ THS_Z_2	TAP_ THS_Z_1	TAP_ THS_Z_0

Table 160. TAP_THS_6D register description

D4D_EN	Enables 4D orientation detection. Z-axis position detection is disabled. Default value: 0 (0: disabled; 1: enabled)
SIXD_THS_[1:0]	Threshold for 4D/6D function. Default value: 00 For details, refer to Table 161.
TAP_THS_Z_[4:0]	Z-axis recognition threshold. Default value: 0 1 LSB = FS_XL / (2^5)

Table 161. Threshold for D4D/D6D function

SIXD_THS_[1:0]	Threshold value
00	80 degrees
01	70 degrees
10	60 degrees
11	50 degrees

9.61 TAP_DUR (5Ah)

Tap recognition function setting register (R/W)

Table 162. **TAP_DUR register**

DUR_3	DUR_2	DUR_1	DUR_0	QUIET_1	QUIET_0	SHOCK_1	SHOCK_0

Table 163. **TAP_DUR register description**

DUR_[3:0]	Duration of maximum time gap for double-tap recognition. Default: 0000 When double-tap recognition is enabled, this register expresses the maximum time between two consecutive detected taps to determine a double-tap event. The default value of these bits is 0000b which corresponds to 16/ODR_XL time. If the DUR_[3:0] bits are set to a different value, 1LSB corresponds to 32/ODR_XL time.
QUIET_[1:0]	Expected quiet time after a tap detection. Default value: 00 Quiet time is the time after the first detected tap in which there must not be any overthreshold event. The default value of these bits is 00b which corresponds to 2/ODR_XL time. If the QUIET_[1:0] bits are set to a different value, 1LSB corresponds to 4/ODR_XL time.
SHOCK_[1:0]	Maximum duration of overthreshold event. Default value: 00 Maximum duration is the maximum time of an overthreshold signal detection to be recognized as a tap event. The default value of these bits is 00b which corresponds to 4/ODR_XL time. If the SHOCK_[1:0] bits are set to a different value, 1LSB corresponds to 8/ODR_XL time.

9.62 WAKE_UP_THS (5Bh)

Single/double-tap selection and wake-up configuration (R/W)

Table 164. **WAKE_UP_THS register**

SINGLE_ DOUBLE_TAP	USR_OFF _ON_WU	WK_THS_5	WK_THS_4	WK_THS_3	WK_THS_2	WK_THS_1	WK_THS_0

Table 165. **WAKE_UP_THS register description**

SINGLE_DOUBLE_TAP	Enables single/double-tap event. Default value: 0 (0: only single-tap event enabled; 1: both single and double-tap events enabled)
USR_OFF_ON_WU	Drives the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wake-up and the activity/inactivity functions. Refer to Figure 23. Default value: 0
WK_THS_[5:0]	Wake-up threshold. The resolution of the threshold depends on the value of WU_INACT_THS_W_[2:0] in the INACTIVITY_DUR (54h) register. Default value: 000000

9.63 WAKE_UP_DUR (5Ch)

Free-fall, wake-up, and sleep mode functions duration setting register (R/W)

Table 166. WAKE_UP_DUR register

FF_DUR_5	WAKE_DUR_1	WAKE_DUR_0	0(1)	SLEEP_DUR_3	SLEEP_DUR_2	SLEEP_DUR_1	SLEEP_DUR_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 167. WAKE_UP_DUR register description

FF_DUR_5	Free-fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR_[4:0] in the FREE_FALL (5Dh) configuration. 1 LSB = 1/ODR_XL time
WAKE_DUR_[1:0]	Wake-up duration event. Default: 00 1 LSB = 1/ODR_XL time
SLEEP_DUR_[3:0]	Duration to go in sleep mode. Default value: 0000 (this corresponds to 18 ODR) 1 LSB = 2 + 512/ODR_XL time

9.64 FREE_FALL (5Dh)

Free-fall function duration setting register (R/W)

Table 168. FREE_FALL register

FF_DUR_4	FF_DUR_3	FF_DUR_2	FF_DUR_1	FF_DUR_0	FF_THS_2	FF_THS_1	FF_THS_0

Table 169. FREE_FALL register description

FF_DUR_[4:0]	Free-fall duration event. Default: 00000 For the complete configuration of the free-fall duration, refer to FF_DUR_5 in the WAKE_UP_DUR (5Ch) configuration.
FF_THS_[2:0]	Free-fall threshold setting. Default: 000 For details refer to Table 170.

Table 170. Threshold for free-fall function

FF_THS_[2:0]	Threshold value
000	156 *mg*
001	219 *mg*
010	250 *mg*
011	312 *mg*
100	344 *mg*
101	406 *mg*
110	469 *mg*
111	500 *mg*

9.65 MD1_CFG (5Eh)

Functions routing to INT1 pin register (R/W). Each bit in this register enables a signal to be carried over the INT1 pin. The output of the pin is the OR combination of the signals selected here and in the INT1_CTRL (0Dh) register.

Table 171. **MD1_CFG register**

INT1_SLEEP_ CHANGE	INT1_ SINGLE_TAP	INT1_WU	INT1_FF	INT1_ DOUBLE_TAP	INT1_6D	INT1_ EMB_FUNC	INT1_SHUB

Table 172. **MD1_CFG register description**

INT1_SLEEP_CHANGE[1]	Routing activity/inactivity recognition event to INT1. Default: 0 (0: routing activity/inactivity event to INT1 disabled; 1: routing activity/inactivity event to INT1 enabled)
INT1_SINGLE_TAP	Routing single-tap recognition event to INT1. Default: 0 (0: routing single-tap event to INT1 disabled; 1: routing single-tap event to INT1 enabled)
INT1_WU	Routing wake-up event to INT1. Default value: 0 (0: routing wake-up event to INT1 disabled; 1: routing wake-up event to INT1 enabled)
INT1_FF	Routing free-fall event to INT1. Default value: 0 (0: routing free-fall event to INT1 disabled; 1: routing free-fall event to INT1 enabled)
INT1_DOUBLE_TAP	Routing tap event to INT1. Default value: 0 (0: routing double-tap event to INT1 disabled; 1: routing double-tap event to INT1 enabled)
INT1_6D	Routing 6D event to INT1. Default value: 0 (0: routing 6D event to INT1 disabled; 1: routing 6D event to INT1 enabled)
INT1_EMB_FUNC	Routing embedded functions event to INT1. Default value: 0 (0: routing embedded functions event to INT1 disabled; 1: routing embedded functions event to INT1 enabled)
INT1_SHUB	Routing sensor hub communication concluded event to INT1. Default value: 0 (0: routing sensor hub communication concluded event to INT1 disabled; 1: routing sensor hub communication concluded event to INT1 enabled)

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INACTIVITY_DUR (54h) register.*

9.66 MD2_CFG (5Fh)

Functions routing to INT2 pin register (R/W). Each bit in this register enables a signal to be carried over the INT2 pin. The output of the pin is the OR combination of the signals selected here and in the INT2_CTRL (0Eh) register.

Table 173. MD2_CFG register

INT2_SLEEP _CHANGE	INT2_ SINGLE_TAP	INT2_WU	INT2_FF	INT2_ DOUBLE_TAP	INT2_6D	INT2_ EMB_FUNC	INT2_ TIMESTAMP

Table 174. MD2_CFG register description

INT2_SLEEP_CHANGE[(1)]	Routing activity/inactivity recognition event to INT2. Default: 0 (0: routing activity/inactivity event to INT2 disabled; 1: routing activity/inactivity event to INT2 enabled)
INT2_SINGLE_TAP	Single-tap recognition routing to INT2. Default: 0 (0: routing single-tap event to INT2 disabled; 1: routing single-tap event to INT2 enabled)
INT2_WU	Routing wake-up event to INT2. Default value: 0 (0: routing wake-up event to INT2 disabled; 1: routing wake-up event to INT2 enabled)
INT2_FF	Routing free-fall event to INT2. Default value: 0 (0: routing free-fall event to INT2 disabled; 1: routing free-fall event to INT2 enabled)
INT2_DOUBLE_TAP	Routing tap event to INT2. Default value: 0 (0: routing double-tap event to INT2 disabled; 1: routing double-tap event to INT2 enabled)
INT2_6D	Routing 6D event to INT2. Default value: 0 (0: routing 6D event to INT2 disabled; 1: routing 6D event to INT2 enabled)
INT2_EMB_FUNC	Routing embedded functions event to INT2. Default value: 0 (0: routing embedded functions event to INT2 disabled; 1: routing embedded functions event to INT2 enabled)
INT2_TIMESTAMP	Enables routing the alert for timestamp overflow within 5.6 ms to the INT2 pin.

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INACTIVITY_DUR (54h) register.*

9.67 HAODR_CFG (62h)

HAODR data rate configuration register (R/W)

Table 175. HAODR_CFG register

0[(1)]	0[(1)]	0[(1)]	0[(1)]	0[(1)]	0[(1)]	HAODR_ SEL_1	HAODR_ SEL _0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 176. HAODR_CFG register description

HAODR_SEL_[1:0]	Selects the ODR set supported when high-accuracy ODR (HAODR) mode is enabled (see Table 20). Default: 00

9.68 EMB_FUNC_CFG (63h)

Embedded functions configuration register (R/W)

Table 177. **EMB_FUNC_CFG register**

HG_USR_OFF_ON_EMB_FUNC	EMB_FUNC_IRQ_MASK_XL_HG_SETTL	EMB_FUNC_IRQ_MASK_G_SETTL	EMB_FUNC_IRQ_MASK_XL_SETTL	EMB_FUNC_DISABLE	0[(1)]	0[(1)]	0[(1)]

1. This bit must be set to 0 for the correct operation of the device.

Table 178. **EMB_FUNC_CFG register description**

HG_USR_OFF_ON_EMB_FUNC	Drives the high-*g* accelerometer data with user offset correction to the embedded functions
EMB_FUNC_IRQ_MASK_XL_HG_SETTL	Enables / masks the execution trigger of the embedded functions when the high-*g* accelerometer data are settling. Default value: 0 (0: disabled; 1: masks the execution trigger of the embedded functions until the high-*g* accelerometer filter settling ends) *Note: Refer to the product application note for the details regarding operating/ power mode configurations, settings, turn-on/off time, and on-the-fly changes.*
EMB_FUNC_IRQ_MASK_G_SETTL	Enables / masks the execution trigger of the embedded functions when the gyroscope data are settling. Default value: 0 (0: disabled; 1: masks the execution trigger of the embedded functions until the gyroscope filter settling ends) *Note: Refer to the product application note for the details regarding operating/ power mode configurations, settings, turn-on/off time, and on-the-fly changes.*
EMB_FUNC_IRQ_MASK_XL_SETTL	Enables / masks the execution trigger of the embedded functions when the low-*g* accelerometer data are settling. Default value: 0 (0: disabled; 1: masks the execution trigger of the embedded functions until the low-*g* accelerometer filter settling ends) *Note: Refer to the product application note for the details regarding operating/ power mode configurations, settings, turn-on/off time, and on-the-fly changes.*
EMB_FUNC_DISABLE	Disables execution of the embedded functions. Default value: 0 (0: execution of the embedded functions is enabled; 1: execution trigger of the embedded functions is not generated anymore and all initialization procedures are forced when this bit is set back to 0).

9.69 XL_HG_X_OFS_USR (6Ch)

High-*g* accelerometer X-axis user offset correction (R/W). The offset value set in the XL_HG_X_OFS_USR offset register is internally added to the acceleration value measured on the X-axis.

Table 179. XL_HG_X_OFS_USR register

XL_HG_X_OFS_USR_7	XL_HG_X_OFS_USR_6	XL_HG_X_OFS_USR_5	XL_HG_X_OFS_USR_4	XL_HG_X_OFS_USR_3	XL_HG_X_OFS_USR_2	XL_HG_X_OFS_USR_1	XL_HG_X_OFS_USR_0

Table 180. XL_HG_X_OFS_USR register description

XL_HG_X_OFS_USR_[7:0]	High-*g* accelerometer X-axis user offset expressed in two's complement, weight is 0.25*g*/LSb. The value must be in the range [-127 127].

9.70 XL_HG_Y_OFS_USR (6Dh)

High-*g* accelerometer Y-axis user offset correction (R/W). The offset value set in the XL_HG_Y_OFS_USR offset register is internally added to the acceleration value measured on the Y-axis.

Table 181. XL_HG_Y_OFS_USR register

XL_HG_Y_OFS_USR_7	XL_HG_Y_OFS_USR_6	XL_HG_Y_OFS_USR_5	XL_HG_Y_OFS_USR_4	XL_HG_Y_OFS_USR_3	XL_HG_Y_OFS_USR_2	XL_HG_Y_OFS_USR_1	XL_HG_Y_OFS_USR_0

Table 182. XL_HG_Y_OFS_USR register description

XL_HG_OFS_Y_OFS_USR_[7:0]	High-*g* accelerometer Y-axis user offset expressed in two's complement, weight is 0.25*g*/LSb. The value must be in the range [-127 127].

9.71 XL_HG_Z_OFS_USR (6Eh)

High-*g* accelerometer Z-axis user offset correction (R/W). The offset value set in the XL_HG_Z_OFS_USR offset register is internally added to the acceleration value measured on the Z-axis.

Table 183. XL_HG_Z_OFS_USR register

XL_HG_Z_OFS_USR_7	XL_HG_Z_OFS_USR_6	XL_HG_Z_OFS_USR_5	XL_HG_Z_OFS_USR_4	XL_HG_Z_OFS_USR_3	XL_HG_Z_OFS_USR_2	XL_HG_Z_OFS_USR_1	XL_HG_Z_OFS_USR_0

Table 184. XL_HG_Z_OFS_USR register description

XL_HG_Z_OFS_USR_[7:0]	High-*g* accelerometer Z-axis user offset expressed in two's complement, weight is 0.25*g*/LSb. The value must be in the range [-127 127].

9.72 X_OFS_USR (73h)

Accelerometer X-axis user offset correction (R/W). The offset value set in the X_OFS_USR offset register is internally added to the acceleration value measured on the X-axis.

Table 185. X_OFS_USR register

X_OFS_USR_7	X_OFS_USR_6	X_OFS_USR_5	X_OFS_USR_4	X_OFS_USR_3	X_OFS_USR_2	X_OFS_USR_1	X_OFS_USR_0

Table 186. X_OFS_USR register description

X_OFS_USR_[7:0]	Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wake-up function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register). The value must be in the range [-127 127].

9.73 Y_OFS_USR (74h)

Accelerometer Y-axis user offset correction (R/W). The offset value set in the Y_OFS_USR offset register is internally added to the acceleration value measured on the Y-axis.

Table 187. Y_OFS_USR register

Y_OFS_USR_7	Y_OFS_USR_6	Y_OFS_USR_5	Y_OFS_USR_4	Y_OFS_USR_3	Y_OFS_USR_2	Y_OFS_USR_1	Y_OFS_USR_0

Table 188. Y_OFS_USR register description

Y_OFS_USR_[7:0]	Accelerometer Y-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wake-up function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register). The value must be in the range [-127 127].

9.74 Z_OFS_USR (75h)

Accelerometer Z-axis user offset correction (R/W). The offset value set in the Z_OFS_USR offset register is internally added to the acceleration value measured on the Z-axis.

Table 189. Z_OFS_USR register

Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0

Table 190. Z_OFS_USR register description

Z_OFS_USR_[7:0]	Accelerometer Z-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wake-up function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register). The value must be in the range [-127 127].

9.75 FIFO_DATA_OUT_TAG (78h)

FIFO tag register (R)

Table 191. FIFO_DATA_OUT_TAG register

TAG_ SENSOR_4	TAG_ SENSOR_3	TAG_ SENSOR_2	TAG_ SENSOR_1	TAG_ SENSOR_0	TAG_CNT_1	TAG_CNT_0	-

Table 192. FIFO_DATA_OUT_TAG register description

TAG_SENSOR_[4:0]	FIFO tag. Identifies the sensor in: FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah), FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch), and FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh) For details, refer to Table 193.
TAG_CNT_[1:0]	2-bit counter which identifies sensor time slot

Table 193. FIFO tag

TAG_SENSOR_[4:0]	Sensor name
0x00	FIFO empty
0x01	Gyroscope NC
0x02	Accelerometer NC
0x03	Temperature
0x04	Timestamp
0x05	CFG_Change
0x06	Accelerometer NC_T_2
0x07	Accelerometer NC_T_1
0x08	Accelerometer 2xC
0x09	Accelerometer 3xC
0x0A	Gyroscope NC_T_2
0x0B	Gyroscope NC_T_1
0x0C	Gyroscope 2xC
0x0D	Gyroscope 3xC
0x0E	Sensor hub target 0
0x0F	Sensor hub target 1
0x10	Sensor hub target 2
0x11	Sensor hub target 3
0x12	Step counter
0x13	SFLP game rotation vector
0x16	SFLP gyroscope bias
0x17	SFLP gravity vector
0x18	High-*g* accelerometer peak value
0x19	Sensor hub nack
0x1A	MLC result
0x1B	MLC filter
0x1C	MLC feature
0x1D	High-*g* accelerometer
0x1F	FSM results

9.76 FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah)

FIFO data output X (R)

Table 194. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 195. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L register description

D[15:0]	FIFO X-axis output

9.77 FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch)

FIFO data output Y (R)

Table 196. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 197. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L register description

D[15:0]	FIFO Y-axis output

9.78 FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh)

FIFO data output Z (R)

Table 198. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 199. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L register description

D[15:0]	FIFO Z-axis output

10 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when EMB_FUNC_REG_ACCESS is set to 1 in FUNC_CFG_ACCESS (01h).

Table 200. Register address map - embedded functions

Name	Type	Register address		Default	Comment
		Hex	Binary		
PAGE_SEL	R/W	02	00000010	00000001	
EMB_FUNC_EN_A	R/W	04	00000100	00000000	
EMB_FUNC_EN_B	R/W	05	00000101	00000000	
EMB_FUNC_EXEC_STATUS	R	07	00000111	output	
PAGE_ADDRESS	R/W	08	00001000	00000000	
PAGE_VALUE	R/W	09	00001001	00000000	
EMB_FUNC_INT1	R/W	0A	00001010	00000000	
FSM_INT1	R/W	0B	00001011	00000000	
RESERVED	-	0C			
MLC_INT1	R/W	0D	00001101	00000000	
EMB_FUNC_INT2	R/W	0E	00001110	00000000	
FSM_INT2	R/W	0F	00001111	00000000	
RESERVED	-	10			
MLC_INT2	R/W	11	00010001	00000000	
EMB_FUNC_STATUS	R	12	00010010	output	
FSM_STATUS	R	13	00010011	output	
RESERVED	-	14			
MLC_STATUS	R	15	00010101	output	
PAGE_RW	R/W	17	00010111	00000000	
SFLP_GBIASX_L	R	18	00011000	output	
SFLP_GBIASX_H	R	19	00011001	output	
SFLP_GBIASY_L	R	1A	00011010	output	
SFLP_GBIASY_H	R	1B	00011011	output	
SFLP_GBIASZ_L	R	1C	00011100	output	
SFLP_GBIASZ_H	R	1D	00011101	output	
SFLP_GRAVX_L	R	1E	00011110	output	
SFLP_GRAVX_H	R	1F	00011111	output	
SFLP_GRAVY_L	R	20	00100000	output	
SFLP_GRAVY_H	R	21	00100001	output	
SFLP_GRAVZ_L	R	22	00100010	output	
SFLP_GRAVZ_H	R	23	00100011	output	
SFLP_QUATW_L	R	2A	00101010	output	
SFLP_QUATW_H	R	2B	00101011	output	
SFLP_QUATX_L	R	2C	00101100	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
SFLP_QUATX_H	R	2D	00101101	output	
SFLP_QUATY_L	R	2E	00101110	output	
SFLP_QUATY_H	R	2F	00101111	output	
SFLP_QUATZ_L	R	30	00110000	output	
SFLP_QUATZ_H	R	31	00110001	output	
SFLP_GBIASX_INIT_L	R/W	32	00110010	00000000	
SFLP_GBIASX_INIT_H	R/W	33	00110011	00000000	
SFLP_GBIASY_INIT_L	R/W	34	00110100	00000000	
SFLP_GBIASY_INIT_H	R/W	35	00110101	00000000	
SFLP_GBIASZ_INIT_L	R/W	36	00110110	00000000	
SFLP_GBIASZ_INIT_H	R/W	37	00110111	00000000	
RESERVED	-	38-43			
EMB_FUNC_FIFO_EN_A	R/W	44	01000100	00000000	
EMB_FUNC_FIFO_EN_B	R/W	45	01000101		
FSM_ENABLE	R/W	46	01000110	00000000	
RESERVED	-	47			
FSM_LONG_COUNTER_L	R/W	48	01001000	00000000	
FSM_LONG_COUNTER_H	R/W	49	01001001	00000000	
RESERVED	-	4A			
INT_ACK_MASK	R/W	4B	01001011	00000000	
FSM_OUTS1	R	4C	01001100	output	
FSM_OUTS2	R	4D	01001101	output	
FSM_OUTS3	R	4E	01001110	output	
FSM_OUTS4	R	4F	01001111	output	
FSM_OUTS5	R	50	01010000	output	
FSM_OUTS6	R	51	01010001	output	
FSM_OUTS7	R	52	01010010	output	
FSM_OUTS8	R	53	01010011	output	
RESERVED	-	54- 5D			
SFLP_ODR	R/W	5E	01011110	01011011	
FSM_ODR	R/W	5F	01011111	01001011	
MLC_ODR	R/W	60	01100000	00010101	
STEP_COUNTER_L	R	62	01100010	output	
STEP_COUNTER_H	R	63	01100011	output	
EMB_FUNC_SRC	R/W	64	01100100	output	
EMB_FUNC_INIT_A	R/W	66	01100110	00000000	
EMB_FUNC_INIT_B	R/W	67	01100111	00000000	
EMB_FUNC_SENSOR_CONV_EN	R/W	6E	01101110	00001111	
MLC1_SRC	R	70	01110000	output	
MLC2_SRC	R	71	01110001	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
MLC3_SRC	R	72	01110010	output	
MLC4_SRC	R	73	01110011	output	
MLC5_SRC	R	74	01110100	output	
MLC6_SRC	R	75	01110101	output	
MLC7_SRC	R	76	01110110	output	
MLC8_SRC	R	77	01110111	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

11 Embedded functions register description

11.1 PAGE_SEL (02h)

Enable advanced features dedicated page (R/W)

Table 201. PAGE_SEL register

PAGE_SEL3	PAGE_SEL2	PAGE_SEL1	PAGE_SEL0	0[1]	0[1]	0[1]	1[2]

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 202. PAGE_SEL register description

PAGE_SEL[3:0]	Selects the advanced features dedicated page. Default value: 0000

11.2 EMB_FUNC_EN_A (04h)

Enable embedded functions register (R/W)

Table 203. EMB_FUNC_EN_A register

MLC_BEFORE_FSM_EN	0[1]	SIGN_MOTION_EN	TILT_EN	PEDO_EN	0[1]	SFLP_GAME_EN	0[1]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 204. EMB_FUNC_EN_A register description

MLC_BEFORE_FSM_EN[1]	Enables machine learning core function. When the machine learning core is enabled by setting this bit to 1, the MLC algorithms are executed before the FSM programs. Default value: 0 (0: machine learning core function disabled; 1: machine learning core function enabled and executed before FSM programs)
SIGN_MOTION_EN	Enables significant motion detection function. Default value: 0 (0: significant motion detection function disabled; 1: significant motion detection function enabled)
TILT_EN	Enables tilt calculation. Default value: 0 (0: tilt algorithm disabled; 1: tilt algorithm enabled)
PEDO_EN	Enables pedometer algorithm. Default value: 0 (0: pedometer algorithm disabled; 1: pedometer algorithm enabled)
SFLP_GAME_EN	Enables sensor fusion low-power algorithm for 6-axis (accelerometer + gyroscope) game rotation vector. Default value: 0 (0: sensor fusion algorithm for 6-axis accelerometer + gyroscope disabled; 1: sensor fusion algorithm for 6-axis accelerometer + gyroscope enabled)

1. *MLC_EN bit in the EMB_FUNC_EN_B (05h) register must be set to 0 when using this bit.*

11.3 EMB_FUNC_EN_B (05h)

Enable embedded functions register (R/W)

Table 205. EMB_FUNC_EN_B register

0[(1)]	0[(1)]	0[(1)]	MLC_EN	FIFO_ COMPR_EN	0[(1)]	0[(1)]	FSM_EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 206. EMB_FUNC_EN_B register description

MLC_EN[(1)]	Enables machine learning core function. When the machine learning core is enabled by setting this bit to 1, the MLC algorithms are executed after executing the FSM programs. Default value: 0 (0: machine learning core function disabled; 1: machine learning core function enabled and executed after FSM programs)
FIFO_COMPR_EN[(2)]	Enables FIFO compression function. Default value: 0 (0: FIFO compression function disabled; 1: FIFO compression function enabled)
FSM_EN	Enables finite state machine (FSM) function. Default value: 0 (0: FSM function disabled; 1: FSM function enabled)

1. *MLC_BEFORE_FSM_EN bit in the EMB_FUNC_EN_A (04h) register must be set to 0 when using this bit.*
2. *This bit is activated if the FIFO_COMPR_RT_EN bit of FIFO_CTRL2 (08h) is set to 1.*

11.4 EMB_FUNC_EXEC_STATUS (07h)

Embedded functions execution status register (R)

Table 207. EMB_FUNC_EXEC_STATUS register

0	0	0	0	0	0	EMB_FUNC_ EXEC_OVR	EMB_FUNC _ENDOP

Table 208. EMB_FUNC_EXEC_STATUS register description

EMB_FUNC_EXEC_OVR	This bit is set to 1 when the execution of the embedded functions program exceeds maximum time (new data are generated before the end of the algorithms). Default value: 0
EMB_FUNC_ENDOP	When this bit is set to 1, no embedded function is running. Default value: 0

11.5 PAGE_ADDRESS (08h)

Page address register (R/W)

Table 209. PAGE_ADDRESS register

PAGE_ ADDR7	PAGE_ ADDR6	PAGE_ ADDR5	PAGE_ ADDR4	PAGE_ ADDR3	PAGE_ ADDR2	PAGE_ ADDR1	PAGE_ ADDR0

Table 210. PAGE_ADDRESS register description

PAGE_ADDR[7:0]	After setting the bit PAGE_WRITE / PAGE_READ in register PAGE_RW (17h), this register is used to set the address of the register to be written/read in the advanced features page selected through the bits PAGE_SEL[3:0] in register PAGE_SEL (02h).

11.6 PAGE_VALUE (09h)

Page value register (R/W)

Table 211. PAGE_VALUE register

PAGE_ VALUE7	PAGE_ VALUE6	PAGE_ VALUE5	PAGE_ VALUE4	PAGE_ VALUE3	PAGE_ VALUE2	PAGE_ VALUE1	PAGE_ VALUE0

Table 212. PAGE_VALUE register description

PAGE_VALUE[7:0]	These bits are used to write (if the bit PAGE_WRITE = 1 in register PAGE_RW (17h)) or read (if the bit PAGE_READ = 1 in register PAGE_RW (17h)) the data at the address PAGE_ADDR[7:0] of the selected advanced features page.

11.7 EMB_FUNC_INT1 (0Ah)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

Table 213. EMB_FUNC_INT1 register

INT1_ FSM_LC	0[1]	INT1_ SIG_MOT	INT1_TILT	INT1_STEP _DETECTOR	0[1]	0[1]	0[1]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 214. EMB_FUNC_INT1 register description

INT1_FSM_LC[1]	Routing FSM long counter timeout interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_SIG_MOT[1]	Routing significant motion event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_TILT[1]	Routing tilt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_STEP_DETECTOR[1]	Routing pedometer step recognition event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

1. *This bit is activated if the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

11.8 FSM_INT1 (0Bh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

Table 215. FSM_INT1 register

INT1_FSM8	INT1_FSM7	INT1_FSM6	INT1_FSM5	INT1_FSM4	INT1_FSM3	INT1_FSM2	INT1_FSM1

Table 216. FSM_INT1 register description

INT1_FSM8[(1)]	Routing FSM8 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM7[(1)]	Routing FSM7 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM6[(1)]	Routing FSM6 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM5[(1)]	Routing FSM5 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM4[(1)]	Routing FSM4 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM3[(1)]	Routing FSM3 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM2[(1)]	Routing FSM2 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM1[(1)]	Routing FSM1 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

1. *This bit is activated if the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

11.9 MLC_INT1 (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

Table 217. MLC_INT1 register

INT1_MLC8	INT1_MLC7	INT1_MLC6	INT1_MLC5	INT1_MLC4	INT1_MLC3	INT1_MLC2	INT1_MLC1

Table 218. MLC_INT1 register description

INT1_MLC8	Routing MLC8 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC7	Routing MLC7 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC6	Routing MLC6 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC5	Routing MLC5 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC4	Routing MLC4 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC3	Routing MLC3 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC2	Routing MLC2 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC1	Routing MLC1 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

11.10 EMB_FUNC_INT2 (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

Table 219. EMB_FUNC_INT2 register

INT2_ FSM_LC	0[(1)]	INT2_ SIG_MOT	INT2_TILT	INT2_STEP _DETECTOR	0[(1)]	0[(1)]	0[(1)]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 220. EMB_FUNC_INT2 register description

INT2_FSM_LC[(1)]	Routing FSM long counter timeout interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_SIG_MOT[(1)]	Routing significant motion event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_TILT[(1)]	Routing tilt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_STEP_DETECTOR[(1)]	Routing pedometer step recognition event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

1. *This bit is activated if the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

11.11 FSM_INT2 (0Fh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

Table 221. FSM_INT2 register

INT2_FSM8	INT2_FSM7	INT2_FSM6	INT2_FSM5	INT2_FSM4	INT2_FSM3	INT2_FSM2	INT2_FSM1

Table 222. FSM_INT2 register description

INT2_FSM8[1]	Routing FSM8 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM7[1]	Routing FSM7 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM6[1]	Routing FSM6 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM5[1]	Routing FSM5 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM4[1]	Routing FSM4 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM3[1]	Routing FSM3 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM2[1]	Routing FSM2 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM1[1]	Routing FSM1 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

1. *This bit is activated if the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

11.12 MLC_INT2 (11h)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

Table 223. MLC_INT2 register

INT2_MLC8	INT2_MLC7	INT2_MLC6	INT2_MLC5	INT2_MLC4	INT2_MLC3	INT2_MLC2	INT2_MLC1

Table 224. MLC_INT2 register description

INT2_MLC8	Routing MLC8 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC7	Routing MLC7 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC6	Routing MLC6 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC5	Routing MLC5 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC4	Routing MLC4 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC3	Routing MLC3 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC2	Routing MLC2 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC1	Routing MLC1 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

11.13 EMB_FUNC_STATUS (12h)

Embedded function status register (R)

Table 225. EMB_FUNC_STATUS register

IS_FSM_LC	0	IS_SIGMOT	IS_TILT	IS_STEP_DET	0	0	0

Table 226. EMB_FUNC_STATUS register description

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)
IS_SIGMOT	Interrupt status bit for significant motion detection (1: interrupt detected; 0: no interrupt)
IS_TILT	Interrupt status bit for tilt detection (1: interrupt detected; 0: no interrupt)
IS_STEP_DET	Interrupt status bit for step detection (1: interrupt detected; 0: no interrupt)

11.14 FSM_STATUS (13h)

Finite state machine status register (R)

Table 227. FSM_STATUS register

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1

Table 228. FSM_STATUS register description

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

11.15 MLC_STATUS (15h)

Machine learning core status register (R)

Table 229. MLC_STATUS register

IS_MLC8	IS_MLC7	IS_MLC6	IS_MLC5	IS_MLC4	IS_MLC3	IS_MLC2	IS_MLC1

Table 230. MLC_STATUS register description

IS_MLC8	Interrupt status bit for MLC8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC7	Interrupt status bit for MLC7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC6	Interrupt status bit for MLC6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC5	Interrupt status bit for MLC5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC4	Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC3	Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC2	Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC1	Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt)

11.16 PAGE_RW (17h)

Enable read and write mode of advanced features dedicated page (R/W)

Table 231. **PAGE_RW register**

EMB_ FUNC_LIR	PAGE_ WRITE	PAGE_ READ	0[1]	0[1]	0[1]	0[1]	0[1]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 232. **PAGE_RW register description**

EMB_FUNC_LIR	Latched interrupt mode for embedded functions. Default value: 0 (0: embedded functions interrupt request not latched; 1: embedded functions interrupt request latched)
PAGE_WRITE	Enables writes to the selected advanced features dedicated page.[1] Default value: 0 (1: enable; 0: disable)
PAGE_READ	Enables reads from the selected advanced features dedicated page.[1] Default value: 0 (1: enable; 0: disable)

1. *Page selected by PAGE_SEL[3:0] in PAGE_SEL (02h) register.*

11.17 SFLP_GBIASX_L (18h) and SFLP_GBIASX_H (19h)

SFLP gyroscope bias X-axis output register (R). The value is expressed as a 16-bit word in two's complement with 4.375 mdps/LSB sensitivity.

Table 233. SFLP_GBIASX_H and SFLP_GBIASX_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 234. SFLP_GBIASX_H and SFLP_GBIASX_L register description

D[15:0]	SFLP gyroscope bias X-axis output value

11.18 SFLP_GBIASY_L (1Ah) and SFLP_GBIASY_H (1Bh)

SFLP gyroscope bias Y-axis output register (R). The value is expressed as a 16-bit word in two's complement with 4.375 mdps/LSB sensitivity.

Table 235. SFLP_GBIASY_H and SFLP_GBIASY_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 236. SFLP_GBIASY_H and SFLP_GBIASY_L register description

D[15:0]	SFLP gyroscope bias Y-axis output value

11.19 SFLP_GBIASZ_L (1Ch) and SFLP_GBIASZ_H (1Dh)

SFLP gyroscope bias Z-axis output register (R). The value is expressed as a 16-bit word in two's complement with 4.375 mdps/LSB sensitivity.

Table 237. SFLP_GBIASZ_H and SFLP_GBIASZ_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 238. SFLP_GBIASZ_H and SFLP_GBIASZ_L register description

D[15:0]	SFLP gyroscope bias Z-axis output value

11.20 SFLP_GRAVX_L (1Eh) and SFLP_GRAVX_H (1Fh)

SFLP gravity X-axis output register (R). The value is expressed as a 16-bit word in two's complement with 0.061 mg/LSB sensitivity.

Table 239. SFLP_GRAVX_H and SFLP_GRAVX_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 240. SFLP_GRAVX_H and SFLP_GRAVX_L register description

D[15:0]	SFLP gravity X-axis output value

11.21 SFLP_GRAVY_L (20h) and SFLP_GRAVY_H (21h)

SFLP gravity Y-axis output register (R). The value is expressed as a 16-bit word in two's complement with 0.061 mg/LSB sensitivity.

Table 241. SFLP_GRAVY_H and SFLP_GRAVY_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 242. SFLP_GRAVY_H and SFLP_GRAVY_L register description

D[15:0]	SFLP gravity Y-axis output value

11.22 SFLP_GRAVZ_L (22h) and SFLP_GRAVY_H (23h)

SFLP gravity Z-axis output register (R). The value is expressed as a 16-bit word in two's complement with 0.061 mg/LSB sensitivity.

Table 243. SFLP_GRAVZ_H and SFLP_GRAVZ_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 244. SFLP_GRAVZ_H and SFLP_GRAVZ_L register description

D[15:0]	SFLP gravity Z-axis output value

11.23 SFLP_QUATW_L (2Ah) and SFLP_QUATW_H (2Bh)

SFLP game rotation vector W value output register (R). The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 245. SFLP_QUATW_H and SFLP_QUATW_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 246. SFLP_QUATW_H and SFLP_QUATW_L register description

D[15:0]	SFLP game rotation vector W value output value

11.24 SFLP_QUATX_L (2Ch) and SFLP_QUATX_H (2Dh)

SFLP game rotation vector X value output register (R). The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 247. SFLP_QUATX_H and SFLP_QUATX_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 248. SFLP_QUATX_H and SFLP_QUATX_L register description

D[15:0]	SFLP game rotation vector X value output value

11.25 SFLP_QUATY_L (2Eh) and SFLP_QUATY_H (2Fh)

SFLP game rotation vector Y value output register (R). The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 249. SFLP_QUATY_H and SFLP_QUATY_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 250. SFLP_QUATY_H and SFLP_QUATY_L register description

D[15:0]	SFLP game rotation vector Y value output value

11.26 SFLP_QUATZ_L (30h) and SFLP_QUATZ_H (31h)

SFLP game rotation vector Z value output register (R). The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 251. SFLP_QUATZ_H and SFLP_QUATZ_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 252. SFLP_QUATZ_H and SFLP_QUATZ_L register description

D[15:0]	SFLP game rotation vector Z value output value

11.27 SFLP_GBIASX_INIT_L (32h) and SFLP_GBIASX_INIT_H (33h)

SFLP gyroscope bias X-axis initialization register (R/W). The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 253. SFLP_GBIASX_INIT_H and SFLP_GBIASX_INIT_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 254. SFLP_GBIASX_INIT_H and SFLP_GBIASX_INIT_L register description

D[15:0]	SFLP gyroscope bias X-axis initial value

11.28 SFLP_GBIASY_INIT_L (34h) and SFLP_GBIASY_INIT_H (35h)

SFLP gyroscope bias Y-axis initialization register (R/W). The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 255. SFLP_GBIASY_INIT_H and SFLP_GBIASY_INIT_L registers

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0

Table 256. SFLP_GBIASY_INIT_H and SFLP_GBIASY_INIT_L register description

D[15:0]	SFLP gyroscope bias Y-axis initial value

11.29 SFLP_GBIASZ_INIT_L (36h) and SFLP_GBIASZ_INIT_H (37h)

SFLP gyroscope bias Z-axis initialization register (R/W). The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 257. SFLP_GBIASZ_INIT_H and SFLP_GBIASZ_INIT_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 258. SFLP_GBIASZ_INIT_H and SFLP_GBIASZ_INIT_L register description

D[15:0]	SFLP gyroscope bias Z-axis initial value

11.30 EMB_FUNC_FIFO_EN_A (44h)

Embedded functions FIFO configuration register A (R/W)

Table 259. EMB_FUNC_FIFO_EN_A register

MLC_ FIFO_EN	STEP_COUNTER _FIFO_EN	SFLP_GBIAS _FIFO_EN	SFLP_GRAVITY _FIFO_EN	0[(1)]	0[(1)]	SFLP_GAME _FIFO_EN	0[(1)]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 260. EMB_FUNC_FIFO_EN_A register description

MLC_FIFO_EN	Enables batching the machine learning core results in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
STEP_COUNTER_FIFO_EN	Enables batching the step counter values in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
SFLP_GBIAS_FIFO_EN	Enables batching the gyroscope bias values computed by the SFLP algorithm in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
SFLP_GRAVITY_FIFO_EN	Enables batching the gravity values computed by the SFLP algorithm in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
SFLP_GAME_FIFO_EN	Enables batching the game rotation vector (quaternion) values computed by the SFLP algorithm in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)

11.31 EMB_FUNC_FIFO_EN_B (45h)

Embedded functions FIFO configuration register B (R/W)

Table 261. EMB_FUNC_FIFO_EN_B register

0[1]	0[1]	0[1]	0[1]	0[1]	FSM_FIFO_EN	MLC_FILTER_ FEATURE_FIFO_ EN	0[1]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 262. EMB_FUNC_FIFO_EN_B register description

FSM_FIFO_EN	Enables batching the status of the FSMs when they are generating an interrupt event, the long counter overrun event, or the long counter value when a specific command is executed from one FSM. Default value: 0 (0: disabled; 1: enabled)
MLC_FILTER_FEATURE_FIFO_EN	Enables batching the machine learning core filters and features in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)

11.32 FSM_ENABLE (46h)

Enable FSM register (R/W)

Table 263. FSM_ENABLE register

FSM8_EN	FSM7_EN	FSM6_EN	FSM5_EN	FSM4_EN	FSM3_EN	FSM2_EN	FSM1_EN

Table 264. FSM_ENABLE register description

FSM8_EN	Enables FSM8. Default value: 0 (0: FSM8 disabled; 1: FSM8 enabled)
FSM7_EN	Enables FSM7. Default value: 0 (0: FSM7 disabled; 1: FSM7 enabled)
FSM6_EN	Enables FSM6. Default value: 0 (0: FSM6 disabled; 1: FSM6 enabled)
FSM5_EN	Enables FSM5. Default value: 0 (0: FSM5 disabled; 1: FSM5 enabled)
FSM4_EN	Enables FSM4. Default value: 0 (0: FSM4 disabled; 1: FSM4 enabled)
FSM3_EN	Enables FSM3. Default value: 0 (0: FSM3 disabled; 1: FSM3 enabled)
FSM2_EN	Enables FSM2. Default value: 0 (0: FSM2 disabled; 1: FSM2 enabled)
FSM1_EN	Enables FSM1. Default value: 0 (0: FSM1 disabled; 1: FSM1 enabled)

11.33 FSM_LONG_COUNTER_L (48h) and FSM_LONG_COUNTER_H (49h)

FSM long counter status register (R/W)

The long counter value is an unsigned integer value (16-bit format).

Table 265. FSM_LONG_COUNTER_L register

FSM_LC_7	FSM_LC_6	FSM_LC_5	FSM_LC_4	FSM_LC_3	FSM_LC_2	FSM_LC_1	FSM_LC_0

Table 266. FSM_LONG_COUNTER_L register description

FSM_LC_[7:0]	Long counter current value (LSbyte). Default value: 00000000

Table 267. FSM_LONG_COUNTER_H register

FSM_LC_15	FSM_LC_14	FSM_LC_13	FSM_LC_12	FSM_LC_11	FSM_LC_10	FSM_LC_9	FSM_LC_8

Table 268. FSM_LONG_COUNTER_H register description

FSM_LC_[15:8]	Long counter current value (MSbyte). Default value: 00000000

11.34 INT_ACK_MASK (4Bh)

Reset status register (R/W)

Table 269. INT_ACK_MASK register

IACK_ MASK7	IACK_ MASK6	IACK_ MASK5	IACK_ MASK4	IACK_ MASK3	IACK_ MASK2	IACK_ MASK1	IACK_ MASK0

Table 270. INT_ACK_MASK register description

IACK_MASK7	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 7 of the status register is not reset. When this bit is set to 0, bit 7 of the status register is reset. Default value: 0
IACK_MASK6	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 6 of the status register is not reset. When this bit is set to 0, bit 6 of the status register is reset. Default value: 0
IACK_MASK5	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 5 of the status register is not reset. When this bit is set to 0, bit 5 of the status register is reset. Default value: 0
IACK_MASK4	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 4 of the status register is not reset. When this bit is set to 0, bit 4 of the status register is reset. Default value: 0
IACK_MASK3	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 3 of the status register is not reset. When this bit is set to 0, bit 3 of the status register is reset. Default value: 0
IACK_MASK2	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 2 of the status register is not reset. When this bit is set to 0, bit 2 of the status register is reset. Default value: 0
IACK_MASK1	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 1 of the status register is not reset. When this bit is set to 0, bit 1 of the status register is reset. Default value: 0
IACK_MASK0	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 0 of the status register is not reset. When this bit is set to 0, bit 0 of the status register is reset. Default value: 0

11.35 FSM_OUTS1 (4Ch)

FSM1 output register (R)

Table 271. **FSM_OUTS1 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 272. **FSM_OUTS1 register description**

P_X	FSM1 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM1 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM1 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM1 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM1 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM1 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM1 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM1 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.36 FSM_OUTS2 (4Dh)

FSM2 output register (R)

Table 273. **FSM_OUTS2 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 274. **FSM_OUTS2 register description**

P_X	FSM2 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM2 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM2 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM2 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM2 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM2 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM2 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM2 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.37 FSM_OUTS3 (4Eh)

FSM3 output register (R)

Table 275. **FSM_OUTS3 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 276. **FSM_OUTS3 register description**

P_X	FSM3 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM3 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM3 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM3 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM3 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM3 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM3 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM3 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.38 FSM_OUTS4 (4Fh)

FSM4 output register (R)

Table 277. **FSM_OUTS4 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 278. **FSM_OUTS4 register description**

P_X	FSM4 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM4 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM4 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM4 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM4 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM4 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM4 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM4 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.39 FSM_OUTS5 (50h)

FSM5 output register (R)

Table 279. **FSM_OUTS5 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 280. **FSM_OUTS5 register description**

P_X	FSM5 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM5 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM5 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM5 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM5 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM5 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM5 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM5 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.40 FSM_OUTS6 (51h)

FSM6 output register (R)

Table 281. **FSM_OUTS6 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 282. **FSM_OUTS6 register description**

P_X	FSM6 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM6 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM6 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM6 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM6 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM6 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM6 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM6 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.41 FSM_OUTS7 (52h)

FSM7 output register (R)

Table 283. **FSM_OUTS7 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 284. **FSM_OUTS7 register description**

P_X	FSM7 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM7 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM7 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM7 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM7 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM7 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM7 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM7 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.42 FSM_OUTS8 (53h)

FSM8 output register (R)

Table 285. **FSM_OUTS8 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 286. **FSM_OUTS8 register description**

P_X	FSM8 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM8 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM8 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM8 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM8 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM8 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM8 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM8 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.43 SFLP_ODR (5Eh)

Sensor fusion low-power output data rate configuration register (R/W)

Table 287. SFLP_ODR register

0(1)	1(2)	SFLP_GAME _ODR_2	SFLP_GAME _ODR_1	SFLP_GAME _ODR_0	0(1)	1(2)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 288. SFLP_ODR register description

SFLP_GAME_ODR_[2:0]	ODR configuration of the SFLP game algorithm: (000: 15 Hz; 001: 30 Hz; 010: 60 Hz; 011: 120 Hz (default); 100: 240 Hz; 101: 480 Hz)

11.44 FSM_ODR (5Fh)

Finite state machine output data rate configuration register (R/W)

Table 289. FSM_ODR register

0(1)	1(2)	FSM_ODR_2	FSM_ODR_1	FSM_ODR_0	0(1)	1(2)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 290. FSM_ODR register description

FSM_ODR_[2:0]	Finite state machine ODR configuration: (000: 15 Hz; 001: 30 Hz (default); 010: 60 Hz; 011: 120 Hz; 100: 240 Hz; 101: 480 Hz; 110: 960 Hz)

11.45 MLC_ODR (60h)

Machine learning core output data rate configuration register (R/W)

Table 291. MLC_ODR register

0[(1)]	MLC_ODR_2	MLC_ODR_1	MLC_ODR_0	0[(1)]	1[(2)]	0[(1)]	1[(2)]

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 292. MLC_ODR register description

MLC_ODR_[2:0]	Machine learning core ODR configuration: (000: 15 Hz; 001: 30 Hz (default); 010: 60 Hz; 011: 120 Hz; 100: 240 Hz; 101: 480 Hz; 110: 960 Hz)

11.46 STEP_COUNTER_L (62h) and STEP_COUNTER_H (63h)

Step counter output register (R)

Table 293. STEP_COUNTER_L register

STEP_7	STEP_6	STEP_5	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0

Table 294. STEP_COUNTER_L register description

STEP_[7:0]	Step counter output (LSbyte)

Table 295. STEP_COUNTER_H register

STEP_15	STEP_14	STEP_13	STEP_12	STEP_11	STEP_10	STEP_9	STEP_8

Table 296. STEP_COUNTER_H register description

STEP_[15:8]	Step counter output (MSbyte)

11.47 EMB_FUNC_SRC (64h)

Embedded function source register (R/W)

Table 297. **EMB_FUNC_SRC register**

PEDO_ RST_STEP	0[(1)]	STEP_ DETECTED	STEP_COUNT _DELTA_IA	STEP_ OVERFLOW	STEPCOUNTER _BIT_SET	0[(1)]	0[(1)]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 298. **EMB_FUNC_SRC register description**

PEDO_RST_STEP	Reset pedometer step counter. Read/write bit. (0: disabled; 1: enabled)
STEP_DETECTED	Step detector event detection status. Read-only bit. (0: step detection event not detected; 1: step detection event detected)
STEP_COUNT_DELTA_IA	Pedometer step recognition on delta time status. Read-only bit. (0: no step recognized during delta time; 1: at least one step recognized during delta time)
STEP_OVERFLOW	Step counter overflow status. Read-only bit. (0: step counter value < 2^{16}; 1: step counter value reached 2^{16})
STEPCOUNTER_BIT_SET	This bit is equal to 1 when the step count is increased. If a timer period is programmed in PEDO_SC_DELTAT_L (D0h) and PEDO_SC_DELTAT_H (D1h) embedded advanced features (page 1) registers, this bit is kept at 0. Read-only bit.

11.48 EMB_FUNC_INIT_A (66h)

Embedded functions initialization register (R/W)

Table 299. EMB_FUNC_INIT_A register

MLC_BEFORE_FSM_INIT	0[(1)]	SIG_MOT_INIT	TILT_INIT	STEP_DET_INIT	0[(1)]	SFLP_GAME_INIT	0[(1)]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 300. EMB_FUNC_INIT_A register description

MLC_BEFORE_FSM_INIT	Machine learning core initialization request (MLC executed before FSM). Default value: 0
SIG_MOT_INIT	Significant motion detection algorithm initialization request. Default value: 0
TILT_INIT	Tilt algorithm initialization request. Default value: 0
STEP_DET_INIT	Pedometer step counter/detector algorithm initialization request. Default value: 0
SFLP_GAME_INIT	SFLP game algorithm initialization request. Default value: 0

11.49 EMB_FUNC_INIT_B (67h)

Embedded functions initialization register (R/W)

Table 301. EMB_FUNC_INIT_B register

0[(1)]	0[(1)]	0[(1)]	MLC_INIT	FIFO_COMPR_INIT	PT_INIT	0[(1)]	FSM_INIT

1. *This bit must be set to 0 for the correct operation of the device.*

Table 302. EMB_FUNC_INIT_B register description

MLC_INIT	Machine learning core initialization request (MLC executed after FSM). Default value: 0
FIFO_COMPR_INIT	FIFO compression feature initialization request. Default value: 0
PT_INIT	High-*g* peak tracking initialization request. Default value: 0
FSM_INIT	FSM initialization request. Default value: 0

11.50 EMB_FUNC_SENSOR_CONV_EN (6Eh)

Embedded functions sensor conversion enable/disable register (R/W)

Table 303. EMB_FUNC_SENSOR_CONV_EN register

0[(1)]	0[(1)]	0[(1)]	0[(1)]	EXT_SENSOR_CONV_EN	TEMP_CONV_EN	GYRO_CONV_EN	XL_HG_CONV_EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 304. EMB_FUNC_SENSOR_CONV_EN register description

EXT_SENSOR_CONV_EN	Enables/disables the external sensor data conversion for the embedded functions. Default value: 1 (0: data conversion disabled; 1: data conversion enabled)
TEMP_CONV_EN	Enables/disables the temperature data conversion for the embedded functions. Default value: 1 (0: data conversion disabled; 1: data conversion enabled)
GYRO_CONV_EN	Enables/disables the gyroscope data conversion for the embedded functions. Default value: 1 (0: data conversion disabled; 1: data conversion enabled)
XL_HG_CONV_EN	Enables/disables the high-*g* accelerometer data conversion for the embedded functions. Default value: 1 (0: data conversion disabled; 1: data conversion enabled)

11.51 MLC1_SRC (70h)

Machine learning core source register (R)

Table 305. **MLC1_SRC register**

MLC1_ SRC_7	MLC1_ SRC_6	MLC1_ SRC_5	MLC1_ SRC_4	MLC1_ SRC_3	MLC1_ SRC_2	MLC1_ SRC_1	MLC1_ SRC_0

Table 306. **MLC1_SRC register description**

MLC1_SRC_[7:0]	Output value of MLC1 decision tree

11.52 MLC2_SRC (71h)

Machine learning core source register (R)

Table 307. **MLC2_SRC register**

MLC2_ SRC_7	MLC2_ SRC_6	MLC2_ SRC_5	MLC2_ SRC_4	MLC2_ SRC_3	MLCS2_ SRC_2	MLC2_ SRC_1	MLC2_ SRC_0

Table 308. **MLC2_SRC register description**

MLC2_SRC_[7:0]	Output value of MLC2 decision tree

11.53 MLC3_SRC (72h)

Machine learning core source register (R)

Table 309. **MLC3_SRC register**

MLC3_ SRC_7	MLC3_ SRC_6	MLC3_ SRC_5	MLC3_ SRC_4	MLC3_ SRC_3	MLC3_ SRC_2	MLC3_ SRC_1	MLC3_ SRC_0

Table 310. **MLC3_SRC register description**

MLC3_SRC_[7:0]	Output value of MLC3 decision tree

11.54 MLC4_SRC (73h)

Machine learning core source register (R)

Table 311. **MLC4_SRC register**

MLC4_ SRC_7	MLC4_ SRC_6	MLC4_ SRC_5	MLC4_ SRC_4	MLC4_ SRC_3	MLC4_ SRC_2	MLC4_ SRC_1	MLC4_ SRC_0

Table 312. **MLC4_SRC register description**

MLC4_SRC_[7:0]	Output value of MLC4 decision tree

11.55 MLC5_SRC (74h)

Machine learning core source register (R)

Table 313. **MLC5_SRC register**

MLC5_ SRC_7	MLC5_ SRC_6	MLC5_ SRC_5	MLC5_ SRC_4	MLC5_ SRC_3	MLC5_ SRC_2	MLC5_ SRC_1	MLC5_ SRC_0

Table 314. **MLC5_SRC register description**

MLC5_SRC_[7:0]	Output value of MLC5 decision tree

11.56 MLC6_SRC (75h)

Machine learning core source register (R)

Table 315. **MLC6_SRC register**

MLC6_ SRC_7	MLC6_ SRC_6	MLC6_ SRC_5	MLC6_ SRC_4	MLC6_ SRC_3	MLC6_ SRC_2	MLC6_ SRC_1	MLC6_ SRC_0

Table 316. **MLC6_SRC register description**

MLC6_SRC_[7:0]	Output value of MLC6 decision tree

11.57 MLC7_SRC (76h)

Machine learning core source register (R)

Table 317. **MLC7_SRC register**

MLC7_ SRC_7	MLC7_ SRC_6	MLC7_ SRC_5	MLC7_ SRC_4	MLC7_ SRC_3	MLC7_ SRC_2	MLC7_ SRC_1	MLC7_ SRC_0

Table 318. **MLC7_SRC register description**

MLC7_SRC_[7:0]	Output value of MLC7 decision tree

11.58 MLC8_SRC (77h)

Machine learning core source register (R)

Table 319. **MLC8_SRC register**

MLC8_ SRC_7	MLC8_ SRC_6	MLC8_ SRC_5	MLC8_ SRC_4	MLC8_ SRC_3	MLC8_ SRC_2	MLC8_ SRC_1	MLC8_ SRC_0

Table 320. **MLC8_SRC register description**

MLC8_SRC_[7:0]	Output value of MLC8 decision tree

12 Embedded advanced features pages

The table given below provides a list of the registers for the embedded advanced features page 0. These registers are accessible when PAGE_SEL[3:0] are set to 0000 in PAGE_SEL (02h).

Note: External sensor offset compensation registers and transformation matrix correction registers affect FSM data only. When these registers are set with their default values, no compensation is applied.

Table 321. **Register address map - embedded advanced features page 0**

Name	Type	Register address		Default	Comment
		Hex	Binary		
FSM_EXT_SENSITIVITY_L	R/W	BA	10111010	00100100	
FSM_EXT_SENSITIVITY_H	R/W	BB	10111011	00010110	
FSM_EXT_OFFX_L	R/W	C0	11000000	00000000	
FSM_EXT_OFFX_H	R/W	C1	11000001	00000000	
FSM_EXT_OFFY_L	R/W	C2	11000010	00000000	
FSM_EXT_OFFY_H	R/W	C3	11000011	00000000	
FSM_EXT_OFFZ_L	R/W	C4	11000100	00000000	
FSM_EXT_OFFZ_H	R/W	C5	11000101	00000000	
FSM_EXT_MATRIX_XX_L	R/W	C6	11000110	00000000	
FSM_EXT_MATRIX_XX_H	R/W	C7	11000111	00111100	
FSM_EXT_MATRIX_XY_L	R/W	C8	11001000	00000000	
FSM_EXT_MATRIX_XY_H	R/W	C9	11001001	00000000	
FSM_EXT_MATRIX_XZ_L	R/W	CA	11001010	00000000	
FSM_EXT_MATRIX_XZ_H	R/W	CB	11001011	00000000	
FSM_EXT_MATRIX_YY_L	R/W	CC	11001100	00000000	
FSM_EXT_MATRIX_YY_H	R/W	CD	11001101	00111100	
FSM_EXT_MATRIX_YZ_L	R/W	CE	11001110	00000000	
FSM_EXT_MATRIX_YZ_H	R/W	CF	11001111	00000000	
FSM_EXT_MATRIX_ZZ_L	R/W	D0	11010000	00000000	
FSM_EXT_MATRIX_ZZ_H	R/W	D1	11010001	00111100	
EXT_CFG_A	R/W	D4	11010100	00000101	
EXT_CFG_B	R/W	D5	11010101	00000010	

The following table provides a list of the registers for the embedded advanced features page 1. These registers are accessible when PAGE_SEL[3:0] are set to 0001 in PAGE_SEL (02h).

Table 322. Register address map - embedded advanced features page 1

Name	Type	Register address		Default	Comment
		Hex	Binary		
XL_HG_SENSITIVITY_L	R/W	58	01011000	00011111	
XL_HG_SENSITIVITY_H	R/W	59	01011001	00000101	
FSM_LC_TIMEOUT_L	R/W	7A	01111010	00000000	
FSM_LC_TIMEOUT_H	R/W	7B	01111011	00000000	
FSM_PROGRAMS	R/W	7C	01111100	00000000	
FSM_START_ADD_L	R/W	7E	01111110	00000000	
FSM_START_ADD_H	R/W	7F	01111111	00000000	
PEDO_CMD_REG	R/W	83	10000011	00000000	
PEDO_DEB_STEPS_CONF	R/W	84	10000100	00001010	
PEDO_SC_DELTAT_L	R/W	D0	11010000	00000000	
PEDO_SC_DELTAT_H	R/W	D1	11010001	00000000	
MLC_EXT_SENSITIVITY_L	R/W	E8	11101000	00000000	
MLC_EXT_SENSITIVITY_H	R/W	E9	11101001	00111100	

The following table provides a list of the registers for the embedded advanced features page 2. These registers are accessible when PAGE_SEL[3:0] are set to 0010 in PAGE_SEL (02h).

Table 323. Register address map - embedded advanced features page 2

Name	Type	Register address		Default	Comment
		Hex	Binary		
EXT_FORMAT	R/W	00	00000000	00000000	
EXT_3BYTE_SENSITIVITY_L	R/W	02	00000010	00000000	
EXT_3BYTE_SENSITIVITY_H	R/W	03	00000011	00001100	
EXT_3BYTE_OFFSET_XL	R/W	06	00000110	00000000	
EXT_3BYTE_OFFSET_L	R/W	07	00000111	01010100	
EXT_3BYTE_OFFSET_H	R/W	08	00001000	00111111	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

Write procedure example: write value 06h in register at address 84h (PEDO_DEB_STEPS_CONF) in Page 1

1. Write bit EMB_FUNC_REG_ACCESS = 1 in FUNC_CFG_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE_WRITE = 1 in PAGE_RW (17h) register // Select write operation mode
3. Write 0001 in PAGE_SEL[3:0] field of register PAGE_SEL (02h) // Select page 1
4. Write 84h in PAGE_ADDR register (08h) // Set address
5. Write 06h in PAGE_DATA register (09h) // Set value to be written
6. Write bit PAGE_WRITE = 0 in PAGE_RW (17h) register // Write operation disabled

7. Write bit EMB_FUNC_REG_ACCESS = 0 in FUNC_CFG_ACCESS (01h) // Disable access to embedded functions registers

Read procedure example: read value of register at address 84h (PEDO_DEB_STEPS_CONF) in Page 1

1. Write bit EMB_FUNC_REG_ACCESS = 1 in FUNC_CFG_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE_READ = 1 in PAGE_RW (17h) register // Select read operation mode
3. Write 0001 in PAGE_SEL[3:0] field of register PAGE_SEL (02h) // Select page 1
4. Write 84h in PAGE_ADDR register (08h) // Set address
5. Read value of PAGE_DATA register (09h) // Get register value
6. Write bit PAGE_READ = 0 in PAGE_RW (17h) register // Read operation disabled
7. Write bit EMB_FUNC_REG_ACCESS = 0 in FUNC_CFG_ACCESS (01h) // Disable access to embedded functions registers

Note: *Steps 1 and 2 of both procedures are intended to be performed at the beginning of the procedure. Steps 6 and 7 of both procedures are intended to be performed at the end of the procedure. If the procedure involves multiple operations, only steps 3, 4 and 5 must be repeated for each operation. If, in particular, the multiple operations involve consecutive registers, only step 5 can be performed.*

13 Embedded advanced features register description

13.1 Page 0 - embedded advanced features registers

13.1.1 FSM_EXT_SENSITIVITY_L (BAh) and FSM_EXT_SENSITIVITY_H (BBh)

External sensor sensitivity value register for the finite state machine (R/W)

This register corresponds to the conversion value of the external sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Default value of FSM_EXT_S_[15:0] bits is 0x1624 (when using an external magnetometer this value corresponds to 0.0015 gauss/LSB).

Table 324. **FSM_EXT_SENSITIVITY_L register**

FSM_EXT_S_7	FSM_EXT_S_6	FSM_EXT_S_5	FSM_EXT_S_4	FSM_EXT_S_3	FSM_EXT_S_2	FSM_EXT_S_1	FSM_EXT_S_0

Table 325. **FSM_EXT_SENSITIVITY_L register description**

FSM_EXT_S_[7:0]	External sensor sensitivity (LSbyte). Default value: 00100100

Table 326. **FSM_EXT_SENSITIVITY_H register**

FSM_EXT_S_15	FSM_EXT_S_14	FSM_EXT_S_13	FSM_EXT_S_12	FSM_EXT_S_11	FSM_EXT_S_10	FSM_EXT_S_9	FSM_EXT_S_8

Table 327. **FSM_EXT_SENSITIVITY_H register description**

FSM_EXT_S_[15:8]	External sensor (MSbyte). Default value: 00010110

13.1.2 FSM_EXT_OFFX_L (C0h) and FSM_EXT_OFFX_H (C1h)

External sensor X-axis offset

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 328. FSM_EXT_OFFX_L register

FSM_EXT_ OFFX_7	FSM_EXT_ OFFX_6	FSM_EXT_ OFFX_5	FSM_EXT_ OFFX_4	FSM_EXT_ OFFX_3	FSM_EXT_ OFFX_2	FSM_EXT_ OFFX_1	FSM_EXT_ OFFX_0

Table 329. FSM_EXT_OFFX_L register description

FSM_EXT_OFFX_[7:0]	External sensor X-axis offset (LSbyte). Default value: 00000000

Table 330. FSM_EXT_OFFX_H register

FSM_EXT_ OFFX_15	FSM_EXT_ OFFX_14	FSM_EXT_ OFFX_13	FSM_EXT_ OFFX_12	FSM_EXT_ OFFX_11	FSM_EXT_ OFFX_10	FSM_EXT_ OFFX_9	FSM_EXT_ OFFX_8

Table 331. FSM_EXT_OFFX_H register description

FSM_EXT_OFFX_[15:8]	External sensor X-axis offset (MSbyte). Default value: 00000000

13.1.3 FSM_EXT_OFFY_L (C2h) and FSM_EXT_OFFY_H (C3h)

External sensor Y-axis offset

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 332. FSM_EXT_OFFY_L register

FSM_EXT_ OFFY_7	FSM_EXT_ OFFY_6	FSM_EXT_ OFFY_5	FSM_EXT_ OFFY_4	FSM_EXT_ OFFY_3	FSM_EXT_ OFFY_2	FSM_EXT_ OFFY_1	FSM_EXT_ OFFY_0

Table 333. FSM_EXT_OFFY_L register description

FSM_EXT_OFFY_[7:0]	External sensor Y-axis offset (LSbyte). Default value: 00000000

Table 334. FSM_EXT_OFFY_H register

FSM_EXT_ OFFY_15	FSM_EXT_ OFFY_14	FSM_EXT_ OFFY_13	FSM_EXT_ OFFY_12	FSM_EXT_ OFFY_11	FSM_EXT_ OFFY_10	FSM_EXT_ OFFY_9	FSM_EXT_ OFFY_8

Table 335. FSM_EXT_OFFY_H register description

FSM_EXT_OFFY_[15:8]	External sensor Y-axis offset (MSbyte). Default value: 00000000

13.1.4 FSM_EXT_OFFZ_L (C4h) and FSM_EXT_OFFZ_H (C5h)

External sensor Z-axis offset register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 336. **FSM_EXT_OFFZ_L register**

FSM_EXT_ OFFZ_7	FSM_EXT_ OFFZ_6	FSM_EXT_ OFFZ_5	FSM_EXT_ OFFZ_4	FSM_EXT_ OFFZ_3	FSM_EXT_ OFFZ_2	FSM_EXT_ OFFZ_1	FSM_EXT_ OFFZ_0

Table 337. **FSM_EXT_OFFZ_L register description**

FSM_EXT_OFFZ_[7:0]	External sensor Z-axis offset (LSbyte). Default value: 00000000

Table 338. **FSM_EXT_OFFZ_H register**

FSM_EXT_ OFFZ_15	FSM_EXT_ OFFZ_14	FSM_EXT_ OFFZ_13	FSM_EXT_ OFFZ_12	FSM_EXT_ OFFZ_11	FSM_EXT_ OFFZ_10	FSM_EXT_ OFFZ_9	FSM_EXT_ OFFZ_8

Table 339. **FSM_EXT_OFFZ_H register description**

FSM_EXT_OFFZ_[15:8]	External sensor Z-axis offset (MSbyte). Default value: 00000000

13.1.5 FSM_EXT_MATRIX_XX_L (C6h) and FSM_EXT_MATRIX_XX_H (C7h)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 340. **FSM_EXT_MATRIX_XX_L register**

FSM_EXT_ MAT_XX_7	FSM_EXT_ MAT_XX_6	FSM_EXT_ MAT_XX_5	FSM_EXT_ MAT_XX_4	FSM_EXT_ MAT_XX_3	FSM_EXT_ MAT_XX_2	FSM_EXT_ MAT_XX_1	FSM_EXT_ XX_0

Table 341. **FSM_EXT_MATRIX_XX_L register description**

FSM_EXT_MAT_XX_[7:0]	Transformation matrix row1 col1 coefficient (LSbyte). Default value: 00000000

Table 342. **FSM_EXT_MATRIX_XX_H register**

FSM_EXT_ MAT_XX_15	FSM_EXT_ MAT_XX_14	FSM_EXT_ MAT_XX_13	FSM_EXT_ MAT_XX_12	FSM_EXT_ MAT_XX_11	FSM_EXT_ MAT_XX_10	FSM_EXT_ XX_9	FSM_EXT_ XX_8

Table 343. **FSM_EXT_MATRIX_XX_H register description**

FSM_EXT_MAT_[15:8]	Transformation matrix row1 col1 coefficient (MSbyte). Default value: 00111100

13.1.6 FSM_EXT_MATRIX_XY_L (C8h) and FSM_EXT_MATRIX_XY_H (C9h)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 344. FSM_EXT_MATRIX_XY_L register

FSM_EXT_ MAT_XY_7	FSM_EXT_ MAT_XY_6	FSM_EXT_ MAT_XY_5	FSM_EXT_ MAT_XY_4	FSM_EXT_ MAT_XY_3	FSM_EXT_ MAT_XY_2	FSM_EXT_ MAT_XY_1	FSM_EXT_ MAT_XY_0

Table 345. FSM_EXT_MATRIX_XY_L register description

FSM_EXT_MAT_XY_[7:0]	Transformation matrix row1 col2 (and row2 col1) coefficient (LSbyte). Default value: 00000000

Table 346. FSM_EXT_MATRIX_XY_H register

FSM_EXT_ XY_15	FSM_EXT_ XY_14	FSM_EXT_ XY_13	FSM_EXT_ XY_12	FSM_EXT_ XY_11	FSM_EXT_ XY_10	FSM_EXT_ XY_9	FSM_EXT_ XY_8

Table 347. FSM_EXT_MATRIX_XY_H register description

FSM_EXT_MAT_XY_[15:8]	Transformation matrix row1 col2 (and row2 col1) coefficient (MSbyte). Default value: 00000000

13.1.7 FSM_EXT_MATRIX_XZ_L (CAh) and FSM_EXT_MATRIX_XZ_H (CBh)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 348. FSM_EXT_MATRIX_XZ_L register

FSM_EXT_ MAT_XZ_7	FSM_EXT_ MAT_XZ_6	FSM_EXT_ MAT_XZ_5	FSM_EXT_ MAT_XZ_4	FSM_EXT_ MAT_XZ_3	FSM_EXT_ MAT_XZ_2	FSM_EXT_ MAT_XZ_1	FSM_EXT_ MAT_XZ_0

Table 349. FSM_EXT_MATRIX_XZ_L register description

FSM_EXT_MAT_XZ_[7:0]	Transformation matrix row1 col3 (and row3 col1) coefficient (LSbyte). Default value: 00000000

Table 350. FSM_EXT_MATRIX_XZ_H register

FSM_EXT_ MAT_XZ_15	FSM_EXT_ MAT_XZ_14	FSM_EXT_ MAT_XZ_13	FSM_EXT_ MAT_XZ_12	FSM_EXT_ MAT_XZ_11	FSM_EXT_ MAT_XZ_10	FSM_EXT_ MAT_XZ_9	FSM_EXT_ MAT_XZ_8

Table 351. FSM_EXT_MATRIX_XZ_H register description

FSM_EXT_MAT_XZ_[15:8]	Transformation matrix row1 col3 (and row3 col1) coefficient (MSbyte). Default value: 00000000

13.1.8 FSM_EXT_MATRIX_YY_L (CCh) and FSM_EXT_MATRIX_YY_H (CDh)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 352. FSM_EXT_MATRIX_YY_L register

FSM_EXT_ MAT_YY_7	FSM_EXT_ MAT_YY_6	FSM_EXT_ MAT_YY_5	FSM_EXT_ MAT_YY_4	FSM_EXT_ MAT_YY_3	FSM_EXT_ MAT_YY_2	FSM_EXT_ MAT_YY_1	FSM_EXT_ MAT_YY_0

Table 353. FSM_EXT_MATRIX_YY_L register description

FSM_EXT_MAT_YY_[7:0]	Transformation matrix row2 col2 coefficient (LSbyte). Default value: 00000000

Table 354. FSM_EXT_MATRIX_YY_H register

FSM_EXT_ MAT_YY_15	FSM_EXT_ MAT_YY_14	FSM_EXT_ MAT_YY_13	FSM_EXT_ MAT_YY_12	FSM_EXT_ MAT_YY_11	FSM_EXT_ MAT_YY_10	FSM_EXT_ MAT_YY_9	FSM_EXT_ MAT_YY_8

Table 355. FSM_EXT_MATRIX_YY_H register description

FSM_EXT_MAT_YY_[15:8]	Transformation matrix row2 col2 coefficient (MSbyte). Default value: 00111100

13.1.9 FSM_EXT_MATRIX_YZ_L (CEh) and FSM_EXT_MATRIX_YZ_H (CFh)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 356. FSM_EXT_MATRIX_YZ_L register

FSM_EXT_ MAT_YZ_7	FSM_EXT_ MAT_YZ_6	FSM_EXT_ MAT_YZ_5	FSM_EXT_ MAT_YZ_4	FSM_EXT_ MAT_YZ_3	FSM_EXT_ MAT_YZ_2	FSM_EXT_ MAT_YZ_1	FSM_EXT_ MAT_YZ_0

Table 357. FSM_EXT_MATRIX_YZ_L register description

FSM_EXT_MAT_YZ_[7:0]	Transformation matrix row2 col3 (and row3 col2) coefficient (LSbyte). Default value: 00000000

Table 358. FSM_EXT_MATRIX_YZ_H register

FSM_EXT_ MAT_YZ_15	FSM_EXT_ MAT_YZ_14	FSM_EXT_ MAT_YZ_13	FSM_EXT_ MAT_YZ_12	FSM_EXT_ MAT_YZ_11	FSM_EXT_ MAT_YZ_10	FSM_EXT_ MAT_YZ_9	FSM_EXT_ MAT_YZ_8

Table 359. FSM_EXT_MATRIX_YZ_H register description

FSM_EXT_MAT_YZ_[15:8]	Transformation matrix row2 col3 (and row3 col2) coefficient (MSbyte). Default value: 00000000

13.1.10 FSM_EXT_MATRIX_ZZ_L (D0h) and FSM_EXT_MATRIX_ZZ_H (D1h)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 360. FSM_EXT_MATRIX_ZZ_L register

FSM_EXT_MAT_ZZ_7	FSM_EXT_MAT_ZZ_6	FSM_EXT_MAT_ZZ_5	FSM_EXT_MAT_ZZ_4	FSM_EXT_MAT_ZZ_3	FSM_EXT_MAT_ZZ_2	FSM_EXT_MAT_ZZ_1	FSM_EXT_MAT_ZZ_0

Table 361. FSM_EXT_MATRIX_ZZ_L register description

FSM_EXT_MAT_ZZ_[7:0]	Transformation matrix row3 col3 coefficient (LSbyte). Default value: 00000000

Table 362. FSM_EXT_MATRIX_ZZ_H register

FSM_EXT_MAT_ZZ_15	FSM_EXT_MAT_ZZ_14	FSM_EXT_MAT_ZZ_13	FSM_EXT_MAT_ZZ_12	FSM_EXT_MAT_ZZ_11	FSM_EXT_MAT_ZZ_10	FSM_EXT_MAT_ZZ_9	FSM_EXT_MAT_ZZ_8

Table 363. FSM_EXT_MATRIX_ZZ_H register description

FSM_EXT_MAT_ZZ_[15:8]	Transformation matrix row3 col3 coefficient (MSbyte). Default value: 00111100

13.1.11 EXT_CFG_A (D4h)

External sensor coordinates (Z and Y axes) rotation register (r/w).

Table 364. EXT_CFG_A register

0(1)	EXT_Y_ AXIS2	EXT_Y_ AXIS1	EXT_Y_ AXIS0	0(1)	EXT_Z_ AXIS2	EXT_Z_ AXIS1	EXT_Z_ AXIS0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 365. EXT_CFG_A description

EXT_Y_AXIS[2:0]	External sensor Y-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation) (000: Y = Y; (default) 001: Y = -Y; 010: Y = X; 011: Y = -X; 100: Y = -Z; 101: Y = Z; Others: Y = Y)
EXT_Z_AXIS[2:0]	External sensor Z-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation) (000: Z = Y; 001: Z = -Y; 010: Z = X; 011: Z = -X; 100: Z = -Z; 101: Z = Z; (default) Others: Z = Y)

13.1.12 EXT_CFG_B (D5h)

External sensor coordinates (X-axis) rotation register (r/w).

Table 366. EXT_CFG_B register

0(1)	0(1)	0(1)	0(1)	0(1)	EXT_X_ AXIS2	EXT_X_ AXIS1	EXT_X_ AXIS0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 367. EXT_CFG_B description

EXT_X_AXIS[2:0]	External sensor X-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation) (000: X = Y; 001: X = -Y; 010: X = X; (default) 011: X = -X; 100: X = -Z; 101: X = Z; Others: X = Y)

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13.2.1 XL_HG_SENSITIVITY_L (58h) and XL_HG_SENSITIVITY_H (59h)

High-*g* accelerometer sensitivity value register for the finite state machine and machine learning core (R/W)

This register corresponds to the conversion value of the high-*g* accelerometer sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

The default value of XL_HG_S_[15:0] is 0x051F (expressed in hundreds of *g*, then 7.8e-5 * [100*g*]).

Table 368. XL_HG_SENSITIVITY_L register

XL_HG_S_7	XL_HG_S_6	XL_HG_S_5	XL_HG_S_4	XL_HG_S_3	XL_HG_S_2	XL_HG_S_1	XL_HG_S_0

Table 369. XL_HG_SENSITIVITY_L register description

XL_HG_S_[7:0]	High-*g* accelerometer sensitivity (LSbyte). Default value: 00011111

Table 370. XL_HG_SENSITIVITY_H register

XL_HG_S_15	XL_HG_S_14	XL_HG_S_13	XL_HG_S_12	XL_HG_S_11	XL_HG_S_10	XL_HG_S_9	XL_HG_S_8

Table 371. XL_HG_SENSITIVITY_H register description

XL_HG_S_[15:8]	High-*g* accelerometer sensitivity (MSbyte). Default value: 00000101

13.2.2 FSM_LC_TIMEOUT_L (7Ah) and FSM_LC_TIMEOUT_H (7Bh)

FSM long counter timeout register (R/W)

The long counter timeout value is an unsigned integer value (16-bit format). When the long counter value reached this value, the FSM generates an interrupt.

Table 372. FSM_LC_TIMEOUT_L register

FSM_LC_TIMEOUT7	FSM_LC_TIMEOUT6	FSM_LC_TIMEOUT5	FSM_LC_TIMEOUT4	FSM_LC_TIMEOUT3	FSM_LC_TIMEOUT2	FSM_LC_TIMEOUT1	FSM_LC_TIMEOUT0

Table 373. FSM_LC_TIMEOUT_L register description

FSM_LC_TIMEOUT[7:0]	FSM long counter timeout value (LSbyte). Default value: 00000000

Table 374. FSM_LC_TIMEOUT_H register

FSM_LC_TIMEOUT15	FSM_LC_TIMEOUT14	FSM_LC_TIMEOUT13	FSM_LC_TIMEOUT12	FSM_LC_TIMEOUT11	FSM_LC_TIMEOUT10	FSM_LC_TIMEOUT9	FSM_LC_TIMEOUT8

Table 375. FSM_LC_TIMEOUT_H register description

FSM_LC_TIMEOUT[15:8]	FSM long counter timeout value (MSbyte). Default value: 00000000

13.2.3 FSM_PROGRAMS (7Ch)

FSM number of programs register (R/W)

Table 376. **FSM_PROGRAMS register**

FSM_N_ PROG7	FSM_N_ PROG6	FSM_N_ PROG5	FSM_N_ PROG4	FSM_N_ PROG3	FSM_N_ PROG2	FSM_N_ PROG1	FSM_N_ PROG0

Table 377. **FSM_PROGRAMS register description**

FSM_N_PROG[7:0]	Number of FSM programs; must be less than or equal to 8. Default value: 00000000

13.2.4 FSM_START_ADD_L (7Eh) and FSM_START_ADD_H (7Fh)

FSM start address register (R/W). First available address is 0x2F0.

Table 378. **FSM_START_ADD_L register**

FSM_ START7	FSM_ START6	FSM_ START5	FSM_ START4	FSM_ START3	FSM_ START2	FSM_ START1	FSM_ START0

Table 379. **FSM_START_ADD_L register description**

FSM_START[7:0]	FSM start address value (LSbyte). Default value: 00000000

Table 380. **FSM_START_ADD_H register**

FSM_ START15	FSM_ START14	FSM_ START13	FSM_ START12	FSM_ START11	FSM_ START10	FSM_ START9	FSM_ START8

Table 381. **FSM_START_ADD_H register description**

FSM_START[15:8]	FSM start address value (MSbyte). Default value: 00000000

13.2.5 PEDO_CMD_REG (83h)

Pedometer configuration register (R/W)

Table 382. PEDO_CMD_REG register

0(1)	0(1)	0(1)	0(1)	CARRY_ COUNT_EN	FP_ REJECTION_EN	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 383. PEDO_CMD_REG register description

CARRY_COUNT_EN	Set when user wants to generate interrupt only on count overflow event.
FP_REJECTION_EN(1)	Enables the false-positive rejection feature

1. *This bit is activated if the MLC_EN bit of EMB_FUNC_EN_B (05h) or the MLC_BEFORE_FSM_EN bit in the EMB_FUNC_EN_A (04h) register is set to 1.*

13.2.6 PEDO_DEB_STEPS_CONF (84h)

Pedometer debounce configuration register (R/W)

Table 384. PEDO_DEB_STEPS_CONF register

DEB_ STEP7	DEB_ STEP6	DEB_ STEP5	DEB_ STEP4	DEB_ STEP3	DEB_ STEP2	DEB_ STEP1	DEB_ STEP0

Table 385. PEDO_DEB_STEPS_CONF register description

DEB_STEP[7:0]	Debounce threshold. Minimum number of steps to increment the step counter (debounce). Default value: 00001010

13.2.7 PEDO_SC_DELTAT_L (D0h) and PEDO_SC_DELTAT_H (D1h)

Time period register for step detection on delta time (R/W)

Table 386. PEDO_SC_DELTAT_L register

PD_SC_7	PD_SC_6	PD_SC_5	PD_SC_4	PD_SC_3	PD_SC_2	PD_SC_1	PD_SC_0

Table 387. PEDO_SC_DELTAT_H register

PD_SC_15	PD_SC_14	PD_SC_13	PD_SC_12	PD_SC_11	PD_SC_10	PD_SC_9	PD_SC_8

Table 388. PEDO_SC_DELTAT_H/L register description

PD_SC_[15:0]	Time period value (1LSB = 6.4 ms)

13.2.8 MLC_EXT_SENSITIVITY_L (E8h) and MLC_EXT_SENSITIVITY_H (E9h)

External sensor sensitivity value register for the machine learning core (R/W)

This register corresponds to the conversion value of the external sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Default value of MLC_EXT_S_[15:0] is 0x3C00 (when using an external magnetometer this value corresponds to 1 gauss/LSB).

Table 389. MLC_EXT_SENSITIVITY_L register

MLC_ EXT_S_7	MLC_ EXT_S_6	MLC_ EXT_S_5	MLC_ EXT_S_4	MLC_ EXT_S_3	MLC_ EXT_S_2	MLC_ EXT_S_1	MLC_ EXT_S_0

Table 390. MLC_ EXT_SENSITIVITY_L register description

MLC_EXT_S_[7:0]	External sensor sensitivity (LSbyte). Default value: 00000000

Table 391. MLC_EXT_SENSITIVITY_H register

MLC_ EXT_S_15	MLC_ EXT_S_14	MLC_ EXT_S_13	MLC_ EXT_S_12	MLC_ EXT_S_11	MLC_ EXT_S_10	MLC_ EXT_S_9	MLC_ EXT_S_8

Table 392. MLC_EXT_SENSITIVITY_H register description

MLC_EXT_S_[15:8]	External sensor sensitivity (MSbyte). Default value: 00111100

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13.3.1 EXT_FORMAT (00h)

External sensor data format (2-byte or 3-byte) for the finite state machine and machine learning core (R/W)

Table 393. **EXT_FORMAT register**

0[(1)]	0[(1)]	0[(1)]	0[(1)]	0[(1)]	0[(1)]	EXT_FORMAT_SEL	0[(1)]

1. This bit must be set to 0 for the correct operation of the device.

Table 394. **EXT_FORMAT register description**

EXT_FORMAT_SEL	Selects the format of the external sensor data for FSM and MLC processing. Default value: 0 (0: 2-byte format; 1: 3-byte format)

13.3.2 EXT_3BYTE_SENSITIVITY_L (02h) and EXT_3BYTE_SENSITIVITY_H (03h)

External sensor (3-byte output data) sensitivity value register for the finite state machine and machine learning core (R/W)

This register corresponds to the conversion value of the external sensor having 3-byte output data. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

The default value of EXT_3BYTE_S_[15:0] is 0x0C00 (when using an external pressure sensor this value corresponds to 2.441e-04 hPa/LSB).

Table 395. **EXT_3BYTE_SENSITIVITY_L register**

EXT_3BYTE_S_7	EXT_3BYTE_S_6	EXT_3BYTE_S_5	EXT_3BYTE_S_4	EXT_3BYTE_S_3	EXT_3BYTE_S_2	EXT_3BYTE_S_1	EXT_3BYTE_S_0

Table 396. **EXT_3BYTE_SENSITIVITY_L register description**

EXT_3BYTE_S_[7:0]	External sensor (3-byte output data) sensitivity (LSbyte). Default value: 00000000

Table 397. **EXT_3BYTE_SENSITIVITY_H register**

EXT_3BYTE_S_15	EXT_3BYTE_S_14	EXT_3BYTE_S_13	EXT_3BYTE_S_12	EXT_3BYTE_S_11	EXT_3BYTE_S_10	EXT_3BYTE_S_9	EXT_3BYTE_S_8

Table 398. **EXT_3BYTE_SENSITIVITY_H register description**

EXT_3BYTE_S_[15:8]	External sensor (3-byte output data) sensitivity (MSbyte). Default value: 00001100

13.3.3 EXT_3BYTE_OFFSET_XL (06h), EXT_3BYTE_OFFSET_L (07h) and EXT_3BYTE_OFFSET_H (08h)

External sensor (3-byte output data) offset value register for the finite state machine and machine learning core (R/W)

This register corresponds to the offset value applied to external sensor output data (3-byte) before being processed in FSM and MLC. The value is expressed as a 24-bit word in two's complement.

The default value of EXT_3BYTE_OFF_[23:0] is 0x3F5400, which corresponds to 4150272 LSB. This offset is subtracted from the external output data (in LSB) before the sensitivity (configured in the EXT_3BYTE_SENSITIVITY_L (02h) and EXT_3BYTE_SENSITIVITY_H (03h) registers) is internally applied.

Table 399. EXT_3BYTE_OFFSET_XL register

EXT_3BYTE_ OFF_7	EXT_3BYTE_ OFF_6	EXT_3BYTE_ OFF_5	EXT_3BYTE_ OFF_4	EXT_3BYTE_ OFF_3	EXT_3BYTE_ OFF_2	EXT_3BYTE_ OFF_1	EXT_3BYTE_ OFF_0

Table 400. EXT_3BYTE_OFFSET_XL register description

EXT_3BYTE_OFF_[7:0]	External sensor (3-byte output data) offset (low byte). Default value: 00000000

Table 401. EXT_3BYTE_OFFSET_L register

EXT_3BYTE_ OFF_15	EXT_3BYTE_ OFF_14	EXT_3BYTE_ OFF_13	EXT_3BYTE_ OFF_12	EXT_3BYTE_ OFF_11	EXT_3BYTE_ OFF_10	EXT_3BYTE_ OFF_9	EXT_3BYTE_ OFF_8

Table 402. EXT_3BYTE_OFFSET_L register description

EXT_3BYTE_OFF_[15:8]	External sensor (3-byte output data) offset (mid byte). Default value: 01010100

Table 403. EXT_3BYTE_OFFSET_H register

EXT_3BYTE_ OFF_23	EXT_3BYTE_ OFF_22	EXT_3BYTE_ OFF_21	EXT_3BYTE_ OFF_20	EXT_3BYTE_ OFF_19	EXT_3BYTE_ OFF_18	EXT_3BYTE_ OFF_17	EXT_3BYTE_ OFF_16

Table 404. EXT_3BYTE_OFFSET_H register description

EXT_3BYTE_OFF_[23:16]	External sensor (3-byte output data) offset (high byte). Default value: 00111111

14 Sensor hub register mapping

The table given below provides a list of the registers for the sensor hub functions available in the device and the corresponding addresses. The sensor hub registers are accessible when bit SHUB_REG_ACCESS is set to 1 in FUNC_CFG_ACCESS (01h).

Table 405. Register address map - sensor hub registers

Name	Type	Register address		Default	Comment
		Hex	Binary		
SENSOR_HUB_1	R	02	00000010	output	
SENSOR_HUB_2	R	03	00000011	output	
SENSOR_HUB_3	R	04	00000100	output	
SENSOR_HUB_4	R	05	00000101	output	
SENSOR_HUB_5	R	06	00000110	output	
SENSOR_HUB_6	R	07	00000111	output	
SENSOR_HUB_7	R	08	00001000	output	
SENSOR_HUB_8	R	09	00001001	output	
SENSOR_HUB_9	R	0A	00001010	output	
SENSOR_HUB_10	R	0B	00001011	output	
SENSOR_HUB_11	R	0C	00001100	output	
SENSOR_HUB_12	R	0D	00001101	output	
SENSOR_HUB_13	R	0E	00001110	output	
SENSOR_HUB_14	R	0F	00001111	output	
SENSOR_HUB_15	R	10	00010000	output	
SENSOR_HUB_16	R	11	00010001	output	
SENSOR_HUB_17	R	12	00010010	output	
SENSOR_HUB_18	R	13	00010011	output	
CONTROLLER_CONFIG	R/W	14	00010100	00000000	
TGT0_ADD	R/W	15	00010101	00000000	
TGT0_SUBADD	R/W	16	00010110	00000000	
TGT0_CONFIG	R/W	17	00010111	10000000	
TGT1_ADD	R/W	18	00011000	00000000	
TGT1_SUBADD	R/W	19	00011001	00000000	
TGT1_CONFIG	R/W	1A	00011010	00010000	
TGT2_ADD	R/W	1B	00011011	00000000	
TGT2_SUBADD	R/W	1C	00011100	00000000	
TGT2_CONFIG	R/W	1D	00011101	00000000	
TGT3_ADD	R/W	1E	00011110	00000000	
TGT3_SUBADD	R/W	1F	00011111	00000000	
TGT3_CONFIG	R/W	20	00100000	00000000	
DATAWRITE_TGT0	R/W	21	00100001	00000000	
STATUS_CONTROLLER	R	22	00100010	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

15 Sensor hub register description

15.1 SENSOR_HUB_1 (02h)

Sensor hub output register (R)

First byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 406. **SENSOR_HUB_1 register**

Sensor Hub1_7	Sensor Hub1_6	Sensor Hub1_5	Sensor Hub1_4	Sensor Hub1_3	Sensor Hub1_2	Sensor Hub1_1	Sensor Hub1_0

Table 407. **SENSOR_HUB_1 register description**

SensorHub1_[7:0]	First byte associated to external sensors

15.2 SENSOR_HUB_2 (03h)

Sensor hub output register (R)

Second byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 408. **SENSOR_HUB_2 register**

Sensor Hub2_7	Sensor Hub2_6	Sensor Hub2_5	Sensor Hub2_4	Sensor Hub2_3	Sensor Hub2_2	Sensor Hub2_1	Sensor Hub2_0

Table 409. **SENSOR_HUB_2 register description**

SensorHub2_[7:0]	Second byte associated to external sensors

15.3 SENSOR_HUB_3 (04h)

Sensor hub output register (R)

Third byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 410. **SENSOR_HUB_3 register**

Sensor Hub3_7	Sensor Hub3_6	Sensor Hub3_5	Sensor Hub3_4	Sensor Hub3_3	Sensor Hub3_2	Sensor Hub3_1	Sensor Hub3_0

Table 411. **SENSOR_HUB_3 register description**

SensorHub3_[7:0]	Third byte associated to external sensors

15.4 SENSOR_HUB_4 (05h)

Sensor hub output register (R)

Fourth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 412. SENSOR_HUB_4 register

Sensor Hub4_7	Sensor Hub4_6	Sensor Hub4_5	Sensor Hub4_4	Sensor Hub4_3	Sensor Hub4_2	Sensor Hub4_1	Sensor Hub4_0

Table 413. SENSOR_HUB_4 register description

SensorHub4_[7:0]	Fourth byte associated to external sensors

15.5 SENSOR_HUB_5 (06h)

Sensor hub output register (R)

Fifth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 414. SENSOR_HUB_5 register

Sensor Hub5_7	Sensor Hub5_6	Sensor Hub5_5	Sensor Hub5_4	Sensor Hub5_3	Sensor Hub5_2	Sensor Hub5_1	Sensor Hub5_0

Table 415. SENSOR_HUB_5 register description

SensorHub5_[7:0]	Fifth byte associated to external sensors

15.6 SENSOR_HUB_6 (07h)

Sensor hub output register (R)

Sixth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 416. SENSOR_HUB_6 register

Sensor Hub6_7	Sensor Hub6_6	Sensor Hub6_5	Sensor Hub6_4	Sensor Hub6_3	Sensor Hub6_2	Sensor Hub6_1	Sensor Hub6_0

Table 417. SENSOR_HUB_6 register description

SensorHub6_[7:0]	Sixth byte associated to external sensors

15.7 SENSOR_HUB_7 (08h)

Sensor hub output register (R)

Seventh byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 418. SENSOR_HUB_7 register

Sensor Hub7_7	Sensor Hub7_6	Sensor Hub7_5	Sensor Hub7_4	Sensor Hub7_3	Sensor Hub7_2	Sensor Hub7_1	Sensor Hub7_0

Table 419. SENSOR_HUB_7 register description

SensorHub7_[7:0]	Seventh byte associated to external sensors

15.8 SENSOR_HUB_8 (09h)

Sensor hub output register (R)

Eighth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 420. SENSOR_HUB_8 register

Sensor Hub8_7	Sensor Hub8_6	Sensor Hub8_5	Sensor Hub8_4	Sensor Hub8_3	Sensor Hub8_2	Sensor Hub8_1	Sensor Hub8_0

Table 421. SENSOR_HUB_8 register description

SensorHub8_[7:0]	Eighth byte associated to external sensors

15.9 SENSOR_HUB_9 (0Ah)

Sensor hub output register (R)

Ninth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 422. SENSOR_HUB_9 register

Sensor Hub9_7	Sensor Hub9_6	Sensor Hub9_5	Sensor Hub9_4	Sensor Hub9_3	Sensor Hub9_2	Sensor Hub9_1	Sensor Hub9_0

Table 423. SENSOR_HUB_9 register description

SensorHub9_[7:0]	Ninth byte associated to external sensors

15.10 SENSOR_HUB_10 (0Bh)

Sensor hub output register (R)

Tenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 424. SENSOR_HUB_10 register

Sensor Hub10_7	Sensor Hub10_6	Sensor Hub10_5	Sensor Hub10_4	Sensor Hub10_3	Sensor Hub10_2	Sensor Hub10_1	Sensor Hub10_0

Table 425. SENSOR_HUB_10 register description

SensorHub10_[7:0]	Tenth byte associated to external sensors

15.11 SENSOR_HUB_11 (0Ch)

Sensor hub output register (R)

Eleventh byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 426. SENSOR_HUB_11 register

Sensor Hub11_7	Sensor Hub11_6	Sensor Hub11_5	Sensor Hub11_4	Sensor Hub11_3	Sensor Hub11_2	Sensor Hub11_1	Sensor Hub11_0

Table 427. SENSOR_HUB_11 register description

SensorHub11_[7:0]	Eleventh byte associated to external sensors

15.12 SENSOR_HUB_12 (0Dh)

Sensor hub output register (R)

Twelfth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 428. SENSOR_HUB_12 register

Sensor Hub12_7	Sensor Hub12_6	Sensor Hub12_5	Sensor Hub12_4	Sensor Hub12_3	Sensor Hub12_2	Sensor Hub12_1	Sensor Hub12_0

Table 429. SENSOR_HUB_12 register description

SensorHub12_[7:0]	Twelfth byte associated to external sensors

15.13 SENSOR_HUB_13 (0Eh)

Sensor hub output register (R)

Thirteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 430. **SENSOR_HUB_13 register**

Sensor Hub13_7	Sensor Hub13_6	Sensor Hub13_5	Sensor Hub13_4	Sensor Hub13_3	Sensor Hub13_2	Sensor Hub13_1	Sensor Hub13_0

Table 431. **SENSOR_HUB_13 register description**

SensorHub13_[7:0]	Thirteenth byte associated to external sensors

15.14 SENSOR_HUB_14 (0Fh)

Sensor hub output register (R)

Fourteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 432. **SENSOR_HUB_14 register**

Sensor Hub14_7	Sensor Hub14_6	Sensor Hub14_5	Sensor Hub14_4	Sensor Hub14_3	Sensor Hub14_2	Sensor Hub14_1	Sensor Hub14_0

Table 433. **SENSOR_HUB_14 register description**

SensorHub14_[7:0]	Fourteenth byte associated to external sensors

15.15 SENSOR_HUB_15 (10h)

Sensor hub output register (R)

Fifteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 434. **SENSOR_HUB_15 register**

Sensor Hub15_7	Sensor Hub15_6	Sensor Hub15_5	Sensor Hub15_4	Sensor Hub15_3	Sensor Hub15_2	Sensor Hub15_1	Sensor Hub15_0

Table 435. **SENSOR_HUB_15 register description**

SensorHub15_[7:0]	Fifteenth byte associated to external sensors

15.16 SENSOR_HUB_16 (11h)

Sensor hub output register (R)

Sixteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 436. **SENSOR_HUB_16 register**

Sensor Hub16_7	Sensor Hub16_6	Sensor Hub16_5	Sensor Hub16_4	Sensor Hub16_3	Sensor Hub16_2	Sensor Hub16_1	Sensor Hub16_0

Table 437. **SENSOR_HUB_16 register description**

SensorHub16_[7:0]	Sixteenth byte associated to external sensors

15.17 SENSOR_HUB_17 (12h)

Sensor hub output register (R)

Seventeenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 438. **SENSOR_HUB_17 register**

Sensor Hub17_7	Sensor Hub17_6	Sensor Hub17_5	Sensor Hub17_4	Sensor Hub17_3	Sensor Hub17_2	Sensor Hub17_1	Sensor Hub17_0

Table 439. **SENSOR_HUB_17 register description**

SensorHub17_[7:0]	Seventeenth byte associated to external sensors

15.18 SENSOR_HUB_18 (13h)

Sensor hub output register (R)

Eighteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 440. **SENSOR_HUB_17 register**

Sensor Hub18_7	Sensor Hub18_6	Sensor Hub18_5	Sensor Hub18_4	Sensor Hub18_3	Sensor Hub18_2	Sensor Hub18_1	Sensor Hub18_0

Table 441. **SENSOR_HUB_17 register description**

SensorHub18_[7:0]	Eighteenth byte associated to external sensors

15.19 CONTROLLER_CONFIG (14h)

Controller configuration register (R/W)

Table 442. CONTROLLER_CONFIG register

RST_CONTROLLER_REGS	WRITE_ONCE	START_CONFIG	PASS_THROUGH_MODE	0[1]	CONTROLLER_ON	AUX_SENS_ON1	AUX_SENS_ON0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 443. CONTROLLER_CONFIG register description

RST_CONTROLLER_REGS	Resets controller logic and output registers. Must be set to 1 and then set to 0. Default value: 0
WRITE_ONCE	Target 0 write operation is performed only at the first sensor hub cycle. Default value: 0 (0: write operation for each sensor hub cycle; 1: write operation only for the first sensor hub cycle)
START_CONFIG	Sensor hub trigger signal selection. Default value: 0 (0: sensor hub trigger signal is the accelerometer/gyro data-ready; 1: sensor hub trigger signal external from INT2 pin)
PASS_THROUGH_MODE	I²C interface pass-through. Default value: 0 (0: pass-through disabled; 1: pass-through enabled, primary I²C line is short-circuited with the sensor hub line)
CONTROLLER_ON	Enables sensor hub I²C controller. Default: 0 (0: I²C controller of sensor hub disabled; 1: I²C controller of sensor hub enabled)
AUX_SENS_ON[1:0]	Number of external sensors to be read by the sensor hub. (00: one sensor (default); 01: two sensors; 10: three sensors; 11: four sensors)

15.20 TGT0_ADD (15h)

I²C target address of the first external sensor (sensor 0) register (R/W)

Table 444. TGT0_ADD register

target0_add6	target0_add5	target0_add4	target0_add3	target0_add2	target0_add1	target0_add0	rw_0

Table 445. TGT0_ADD register description

target0_add[6:0]	I²C target address of sensor 0 that can be read by the sensor hub. Default value: 0000000
rw_0	Read/write operation on sensor 0. Default value: 0 (0: write operation; 1: read operation)

15.21 TGT0_SUBADD (16h)

Address of register on the first external sensor (sensor 0) register (R/W)

Table 446. TGT0_SUBADD register

target0_reg7	target0_reg6	target0_reg5	target0_reg4	target0_reg3	target0_reg2	target0_reg1	target0_reg0

Table 447. TGT0_SUBADD register description

target0_reg[7:0]	Address of register on sensor 0 that has to be read/written according to the rw_0 bit value in TGT0_ADD (15h). Default value: 00000000

15.22 TGT0_CONFIG (17h)

First external sensor (sensor 0) configuration and sensor hub settings register (R/W)

Table 448. TGT0_CONFIG register

SHUB_ODR_2	SHUB_ODR_1	SHUB_ODR_0	0[(1)]	BATCH_EXT_SENS_0_EN	target0_numop2	target0_numop1	target0_numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 449. TGT0_CONFIG register description

SHUB_ODR_[2:0]	Rate at which the controller communicates. (000: 1.875 Hz; 001: 15 Hz; 010: 30 Hz; 011: 60 Hz; 100: 120 Hz (default); 101: 240 Hz; 110: 480 Hz; 111: reserved
BATCH_EXT_SENS_0_EN	Enables FIFO data batching of first target. Default value: 0
target0_numop[2:0]	Number of read operations on sensor 0. Default value: 000

15.23 TGT1_ADD (18h)

I²C target address of the second external sensor (sensor 1) register (R/W)

Table 450. TGT1_ADD register

target1_add6	target1_add5	target1_add4	target1_add3	target1_add2	target1_add1	target1_add0	r_1

Table 451. TGT1_ADD register description

target1_add[6:0]	I²C target address of sensor 1 that can be read by the sensor hub. Default value: 0000000
r_1	Enables read operation on sensor 1. Default value: 0 (0: read operation disabled; 1: read operation enabled)

15.24 TGT1_SUBADD (19h)

Address of register on the second external sensor (sensor 1) register (R/W)

Table 452. TGT1_SUBADD register

target1_reg7	target1_reg6	target1_reg5	target1_reg4	target1_reg3	target1_reg2	target1_reg1	target1_reg0

Table 453. TGT1_SUBADD register description

target1_reg[7:0]	Address of register on sensor 1 that has to be read/written according to the r_1 bit value in TGT1_ADD (18h).

15.25 TGT1_CONFIG (1Ah)

Second external sensor (sensor 2) configuration register (R/W)

Table 454. TGT1_CONFIG register

0[(1)]	0[(1)]	0[(1)]	1[(2)]	BATCH_EXT_ SENS_1_EN	target1_ numop2	target1_ numop1	target1_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 455. TGT1_CONFIG register description

BATCH_EXT_SENS_1_EN	Enables FIFO data batching of second target. Default value: 0
target1_numop[2:0]	Number of read operations on sensor 2. Default value: 000

15.26 TGT2_ADD (1Bh)

I²C target address of the third external sensor (sensor 2) register (R/W)

Table 456. TGT2_ADD register

target2_add6	target2_add5	target2_add4	target2_add3	target2_add2	target2_add1	target2_add0	r_2

Table 457. TGT2_ADD register description

target2_add[6:0]	I²C target address of sensor 2 that can be read by the sensor hub.
r_2	Enables read operation on sensor 2. Default value: 0 (0: read operation disabled; 1: read operation enabled)

15.27 TGT2_SUBADD (1Ch)

Address of register on the third external sensor (sensor 2) register (R/W)

Table 458. TGT2_SUBADD register

target2_reg7	target2_reg6	target2_reg5	target2_reg4	target2_reg3	target2_reg2	target2_reg1	target2_reg0

Table 459. TGT2_SUBADD register description

target2_reg[7:0]	Address of register on sensor 2 that has to be read/written according to the r_2 bit value in TGT2_ADD (1Bh).

15.28 TGT2_CONFIG (1Dh)

Third external sensor (sensor 2) configuration register (R/W)

Table 460. TGT2_CONFIG register

0[(1)]	0[(1)]	0[(1)]	0[(1)]	BATCH_EXT_SENS_2_EN	target2_numop2	target2_numop1	target2_numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 461. TGT2_CONFIG register description

BATCH_EXT_SENS_2_EN	Enables FIFO data batching of third target. Default value: 0
target2_numop[2:0]	Number of read operations on sensor 2. Default value: 000

15.29 TGT3_ADD (1Eh)

I²C target address of the fourth external sensor (sensor 3) register (R/W)

Table 462. TGT3_ADD register

target3_add6	target3_add5	target3_add4	target3_add3	target3_add2	target3_add1	target3_add0	r_3

Table 463. TGT3_ADD register description

target3_add[6:0]	I²C target address of sensor 3 that can be read by the sensor hub.
r_3	Enables read operation on sensor 3. Default value: 0 (0: read operation disabled; 1: read operation enabled)

15.30 TGT3_SUBADD (1Fh)

Address of register on the fourth external sensor (sensor 3) register (R/W)

Table 464. TGT3_SUBADD register

target3_reg7	target3_reg6	target3_reg5	target3_reg4	target3_reg3	target3_reg2	target3_reg1	target3_reg0

Table 465. TGT3_SUBADD register description

target3_reg[7:0]	Address of register on sensor 3 that has to be read according to the r_3 bit value in TGT3_ADD (1Eh).

15.31 TGT3_CONFIG (20h)

Fourth external sensor (sensor 3) configuration register (R/W)

Table 466. TGT3_CONFIG register

0[1]	0[1]	0[1]	0[1]	BATCH_EXT_SENS_3_EN	target3_numop2	target3_numop1	target3_numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 467. TGT3_CONFIG register description

BATCH_EXT_SENS_3_EN	Enables FIFO data batching of fourth target. Default value: 0
target3_numop[2:0]	Number of read operations on sensor 3. Default value: 000

15.32 DATAWRITE_TGT0 (21h)

Data to be written into the target device (R/W)

Table 468. **DATAWRITE_TGT0 register**

target0_ dataw7	target0_ dataw6	target0_ dataw5	target0_ dataw4	target0_ dataw3	target0_ dataw2	target0_ dataw1	target0_ dataw0

Table 469. **DATAWRITE_TGT0 register description**

target0_dataw[7:0]	Data to be written into the target 0 device according to the rw_0 bit in register TGT0_ADD (15h). Default value: 00000000

15.33 STATUS_CONTROLLER (22h)

Sensor hub source register (R)

Table 470. **STATUS_CONTROLLER register**

WR_ONCE _DONE	TARGET3_ NACK	TARGET2_ NACK	TARGET1_ NACK	TARGET0_ NACK	0	0	SENS_HUB _ENDOP

Table 471. **STATUS_CONTROLLER register description**

WR_ONCE_DONE	When the bit WRITE_ONCE in CONTROLLER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on target 0 has been performed and completed. Default value: 0
TARGET3_NACK	This bit is set to 1 if not acknowledge occurs on target 3 communication. Default value: 0
TARGET2_NACK	This bit is set to 1 if not acknowledge occurs on target 2 communication. Default value: 0
TARGET1_NACK	This bit is set to 1 if not acknowledge occurs on target 1 communication. Default value: 0
TARGET0_NACK	This bit is set to 1 if not acknowledge occurs on target 0 communication. Default value: 0
SENS_HUB_ENDOP	Sensor hub communication status. Default value: 0 (0: sensor hub communication not concluded; 1: sensor hub communication concluded)

16 Soldering information

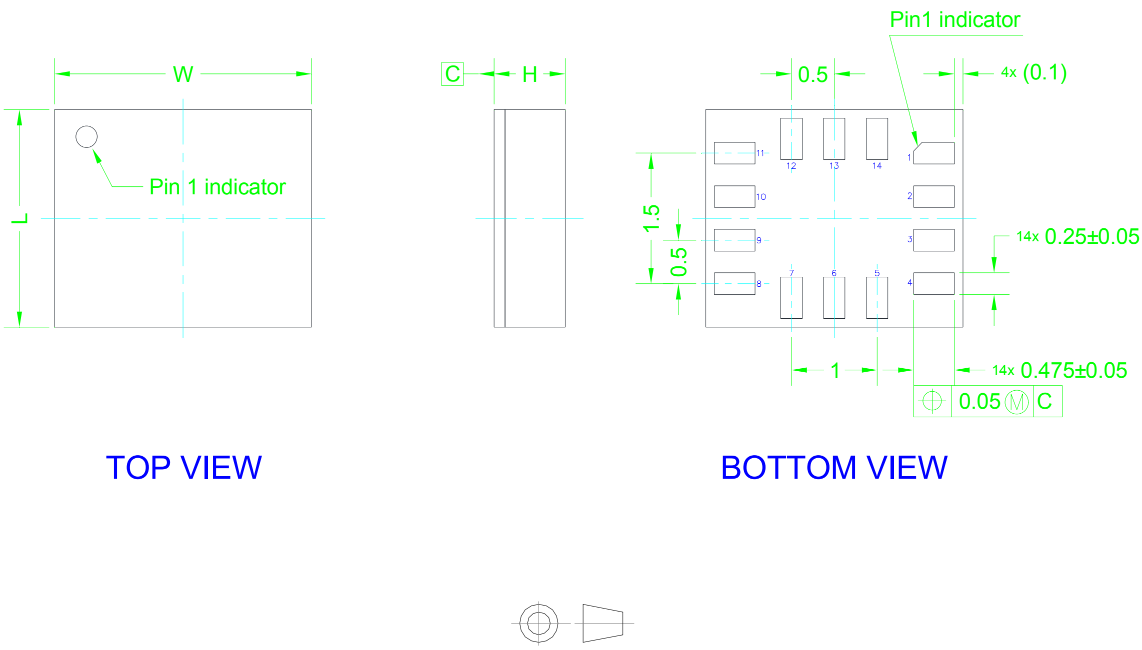
The LGA package is compliant with the ECOPACK and RoHS standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.
For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

17 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

17.1 LGA-14L package information

Figure 24. **LGA-14L 2.5 x 3.0 x 0.83 mm package outline and mechanical data**



Dimensions are in millimeters unless otherwise specified.
General tolerance is +/-0.1mm unless otherwise specified.

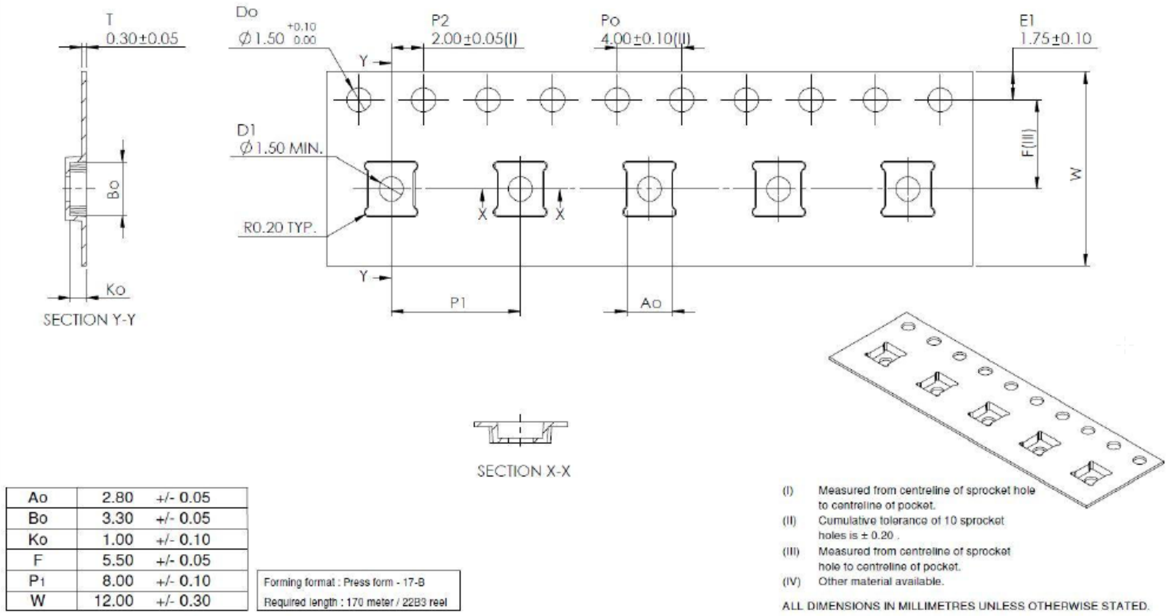
OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.05
Width [W]	3.00	±0.05
Height [H]	0.83	±0.03

DM01021587_2

17.2 LGA-14L packing information

Figure 25. **Carrier tape information for LGA-14L package**



Ao	2.80	+/- 0.05
Bo	3.30	+/- 0.05
Ko	1.00	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Figure 26. **LGA-14L package orientation in carrier tape**

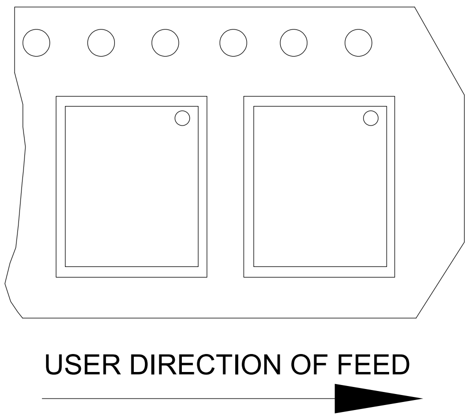


Figure 27. Reel information for carrier tape of LGA-14L package

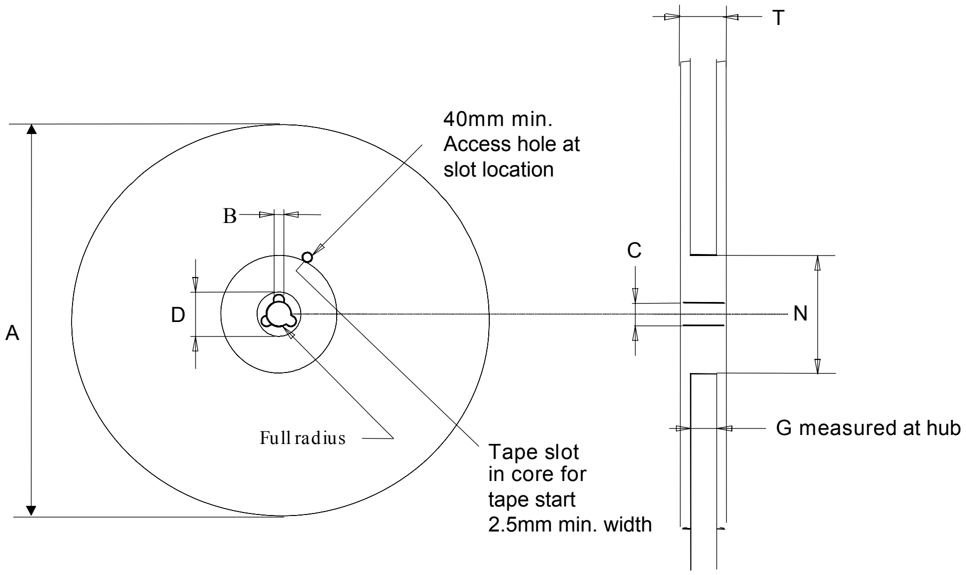


Table 472. Reel dimensions for carrier tape of LGA-14L package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

Revision history

Table 473. **Document revision history**

Date	Revision	Changes
19-Mar-2025	1	Initial release
10-Apr-2025	2	Updated Section 6.1.1: Low-*g* accelerometer and Section 6.1.2: High-*g* accelerometer Added Section 6.2.2: Block diagram of the high-*g* accelerometer filter Renamed Figure 23. Low-*g* accelerometer composite filter

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