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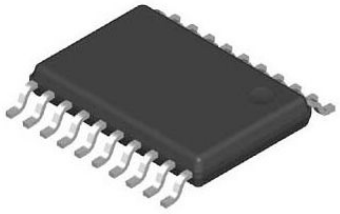
LEOAD128

Datasheet

Rad-hard plastic 8-channel, 1 Msps 12-bit ADC

TSSOP-20



Product status link
LEOAD128

Features

- 12-bit SAR architecture
- 1 Msps conversion rate
- 8-to-1-channel input MUX
- 3.3 V operating supply
- SPI, serial digital output
- Power-down function
- Nickel/palladium/gold-lead-finished (NiPdAu), whisker-free
- Gold-wires
- RML <1% and CVCM <0.1% guaranteed outgassing
- 50 krad (Si) total ionizing dose
- SEL-free up to 62.5 MeV.cm²/mg
- Mass: 80 mg
- Compliant with ST-LEO-specification

Applications

- Low earth orbit (LEO) applications, telemetry, housekeeping

Description

The LEOAD128 is a low power, multiplexed 8-input pure CMOS 12-bit analog-to-digital converter specified for conversion from 50 ksps to 1 Msps. The architecture is based on a successive-approximation register with internal track-and-hold. The output serial data is straight binary and is compatible with SPI™.

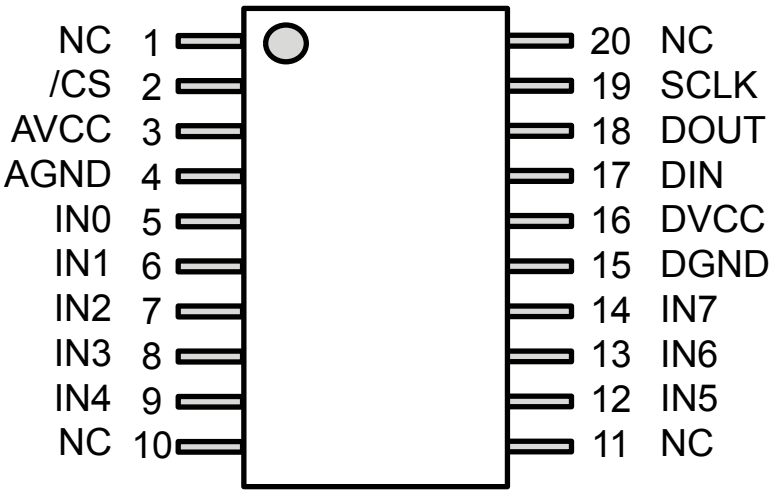
The analog and digital power supplies operate from 2.7 V to 3.6 V, drawing a current consumption of only 2 mA maximum.

The LEOAD128 can operate over a large temperature range of -40 °C to +125 °C and it is housed in plastic TSSOP-20, thin-shrink small outline package, 20 leads, using golden bonding and nickel/palladium/golden-lead-finishing to prevent from whiskers.

The LEOAD128 is compliant with the ST-LEO-specification, dedicated specification for space-ready rad-hard plastic products. This AEC-Q100-based specification offers a specific trade-off among footprint size savings, cost of ownership and quality assurance together with radiation hardness and large quantity capability.

1 Functional description

Figure 1. **Pin connections (top view)**



NC: not internally connected.
The pin can be externally connected to any potential.

Figure 2. **Block diagram**

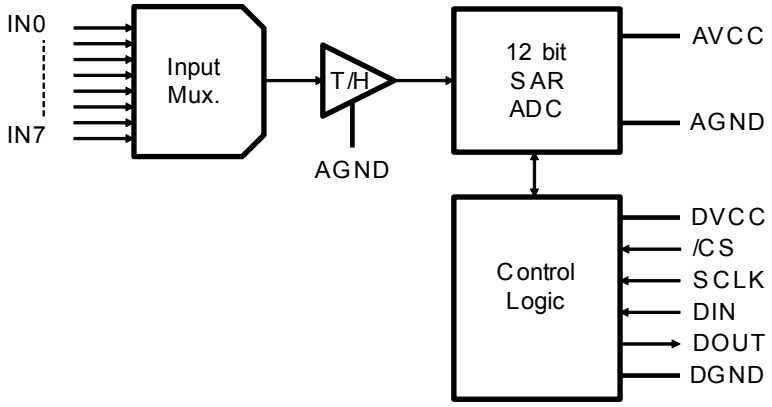


Table 1. Control register bits

Bit	7 (MSB)	6	5	4	3	2	1	0
Symbol	Any code except 11		ADD2	ADD1	ADD0	Any code except 001		

Table 2. Control register bit description

Bit	Symbol	Description
7, 6, 2, 1, 0	DONTC	Do not care, except forbidden codes provided in Table 1. Control register bits
5	ADD2	They determine which input channel to be converted, as per Table 3. Input channel description.
4	ADD1	
3	ADD0	

Table 3. Input channel description

ADD2	ADD1	ADD0	Input channel
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

2 Maximum ratings and operating conditions

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
AVCC(1)	Maximum analog power supply between AVCC and AGND	-0.3 to 4.8	V
DVCC(1)	Maximum digital power supply between DVCC and DGND	-0.3 to AVCC+0.3 (and 4.8 V max.)	V
Vi(2)	Max. voltage on any pin vs. GND	-0.3 to AVCC+0.3 (and 4.8 V max.)	V
Ii	Max input current at any pin	+/-10	mA
T_{stg}	Maximum temperature storage	-65 to +150	°C
T_j	Maximum junction temperature	+150	°C
R_{th}(3)	Junction-to-ambient thermal resistance (Θja)	80	°C/W
	Junction-to-case thermal resistance (Θjc)	17	°C/W
ESD	HBM (human body model)	4 k	V
	CDM (charged device model)	1 k	

1. *All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.*
2. *When the input voltage at any pin exceeds the power supplies (that is VIN < AGND or VIN > AVCC or DVCC), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.*
3. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 5. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
AVCC	Analog supply voltage	2.7	3.6	V
DVCC	Digital supply voltage	AVCC - 0.15 V	AVCC + 0.15 V	V
VINA	Analog input voltage range	0	AVCC	V
VIND	Digital input voltage	0	AVCC	V
SCLK	Clock frequency	0.8	16	MHz
T_a	Ambient temperature range	-40	+125	°C

Note: All unused inputs must be held at VCC or GND to ensure proper device operation.

3 Electrical characteristics

AVCC = DVCC = +3.3 V, AGND = DGND = 0 V, f_{SCLK} = 16 MHz, f_{SAMPLE} = 1 Msps, CL = 25 pF, typ. values at +25 °C, min./max. values at -40 °C and 125 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Static characteristics						
	Resolution with no missing codes				12	Bits
INL	Integral non-linearity (end point method)		−1.1	±0.4	1.1	LSB
DNL	Differential non-linearity		-0.9	±0.4	0.9	LSB
VOFF	Offset error		−2.3	0.8	2.3	LSB
OEM	Offset error match			0.8		LSB
FSE	Full scale error		−2.3	0.8	2.3	LSB
FSEM	Full scale error match			0.8		LSB
Dynamic characteristics						
ENOB	Effective number of bits	FIN = 40.2 kHz, −0.02 dBFS	11.1	11.7		Bits
SINAD	Signal-to-noise plus distortion ratio (0 to Fs/2)	FIN = 40.2 kHz, −0.02 dBFS	68.9	72		dB
SNR	Signal-to-noise ratio (0 to Fs/2)	FIN = 40.2 kHz, −0.02 dBFS	71	73		dB
THD	Total harmonic distortion	FIN = 40.2 kHz, −0.02 dBFS		−80	−73	dB
SFDR	Spurious-free dynamic range (0 to Fs/2)	FIN = 40.2 kHz, −0.02 dBFS	74	81		dB
ISO	Channel-to-channel isolation	FIN = 20 kHz, −0.02 dBFS		84		dB
IM2	2nd order intermodulation	fa = 19.5 kHz, fb = 20.5 kHz VINA = VINB = -6.02 dBFS		−90		dB
IM3	3rd order intermodulation	fa = 19.5 kHz, fb = 20.5 kHz VINA = VINB = -6.02 dBFS		−90		dB
Analog input characteristics						
IDCL			-1		+1	µA
CINA	Input capacitance	Track mode		45		pF
		Hold mode		4.5		
Digital input characteristics						
VIH	Input high voltage	AVCC = DVCC = +2.7 V to +3.6 V	2.1			V
VIL	Input low voltage	AVCC = DVCC = +2.7 V to +3.6 V			0.8	V
IIN	Digital input current	VIN = 0V or DVCC	-1		+1	µA
CIND	Digital input capacitance			4.5		pF
Digital output characteristics (output coding: straight (natural) binary)						
VOH	Output high voltage	I_{source} = 200 µA AVCC = DVCC = +2.7 V to +3.6 V	2.8			V
VOL	Output low voltage	Isink = 200 µA to 1.0 mA,			0.4	V

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
		AVCC = DVCC = +2.7 V to +3.6 V				
IOZH, IOZL	High impedance output leakage current	AVCC = DVCC = +2.7 V to +3.6 V	-1		+1	µA
COUT	High-impedance output capacitance			4.5		pF
Power supply characteristics, CL=10 pF						
IAVCC + IDVCC	Total supply current, normal mode (/CS low)	AVCC = DVCC = +2.7 V to +3.6 V, f_S = 1 MSPS, FIN = 40 kHz		0.9	2	mA
	Total supply current,shutdown mode (/CS high)	AVCC = DVCC = +2.7 V to +3.6 V, f_S = 0		0.11	10	µA
Clocking characteristics, AVCC = DVCC = +2.7 V to +3.6 V						
$t_{CONVERT}$	Conversion (hold) time				13	SCLK cycles
DC	SCLK duty cycle		40		60	%
t_{ACQ}	Acquisition (track) time cycles	See Section 4: Timing diagrams			3	SCLK cycles
	Throughput time acquisition time + conversion time				16	SCLK cycles
t_{AD}	Aperture delay			4		ns
Timing specifications, AVCC = DVCC = +2.7 V to +3.6 V						
t_{CSH}(2)	/CS hold time after SCLK rising edge		10			ns
t_{CSS}(2)	/CS setup time prior SCLK rising edge		10			
t_{EN}	/CSfalling edge to DOUT enabled				30	ns
t_{DACC}	DOUT access time after SCLK falling edge				27	ns
t_{DHLD}	DOUT hold time after SCLK falling edge		7			ns
t_{DS}	DIN set-up time prior to SCLK rising edge		10			ns
t_{DH}	DIN hold time after SCLK rising edge		10			ns
t_{CH}	Min. SCLK high time		0.4 x t_{SCLK}			ns
t_{CL}	Min. SCLK low time		0.4 x t_{SCLK}			ns
t_{DIS}	/CS rising edge to DOUT high-impedance	DOUT falling			20	ns
		DOUT rising			20	ns

1. *Limits are guaranteed by functional test.*
2. *Clock may be in any state (high or low) when /CS goes high. Set-up and hold time restrictions apply only to /CS going low.*

4 Timing diagrams

Figure 3. **Operational timing diagram**

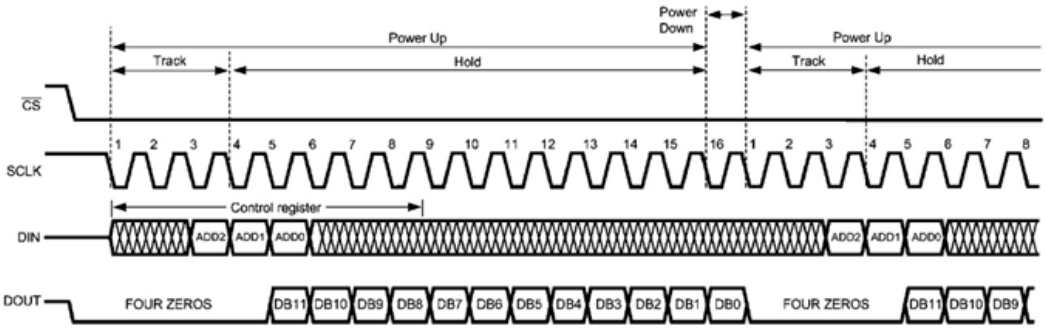


Figure 4. **Serial timing diagram**

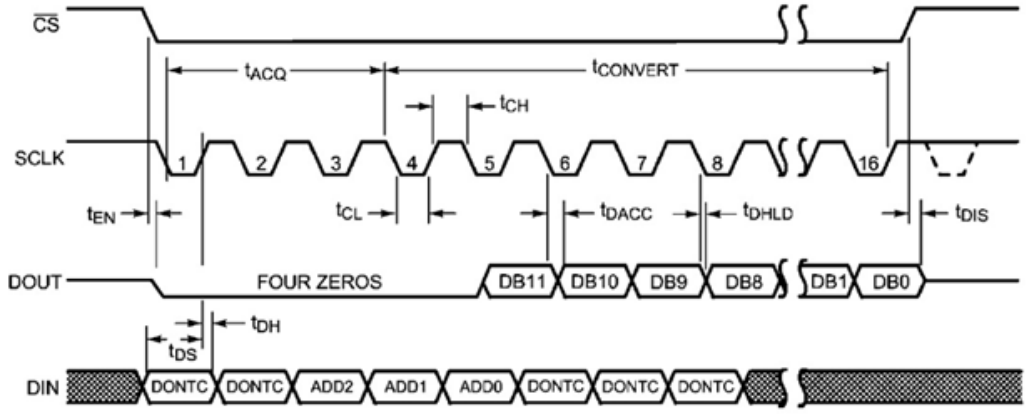
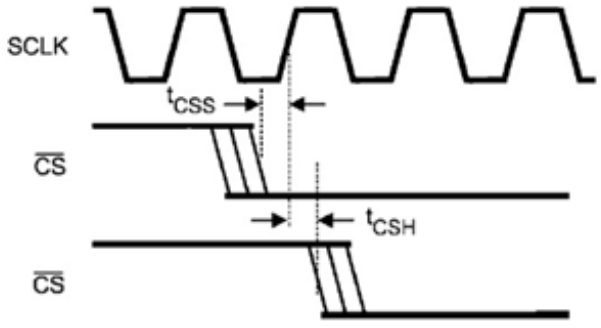


Figure 5. **SCLK and /CS timing parameters**



5 Radiations

Total ionizing dose (TID):

For the qualification, the product is characterized in TID as per MIL-STD-883 TM 1019 up to 50 krad(Si) on 5 biased parts at high dose rate (between 50 and 300 rad(Si)/s), such a rate being the worst condition for a pure CMOS technology.

All parameters provided in Table 6. Electrical characteristics apply to both pre- and post-irradiation.

Each new production lot is tested at high dose rate as per MIL-STD-883 TM 1019 on 5 parts.

Heavy-ions:

Single event latchup (SEL) is characterized at 125 °C at a LET of 62.5 MeV.cm2/mg. The test shows the product is immune to heavy ions at this LET. Heavy-ion trials are performed on qualification lots only.

The results in radiation are summarized in Table 7. Radiations as follows:

Table 7. Radiations

Symbol	Characteristics	Value
TID (1)	• High-dose rate (50-to-300 rad (Si)/s) • Temperature: 25 °C • Performed on 5 biased parts	Within Table 6. Electrical characteristics up to 50 krad(Si)
SEL(2)	• LET: 62.5 MeV.cm2/mg (Xenon ions) • Temperature: 125 °C • Fluence: 1 x 10^7 ions/cm^2 (10 million of particles per cm^2) • Normal incidence	Immune to SEL up to 62.5 MeV.cm^2/mg

1. *A total ionizing dose (TID) of 50 krad(Si) is equivalent to 500 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latchup.*

6 Outgassing

Specification (tested per ASTM E 595)	Value	Unit
Recovered mass loss (RML)[1]	0.06	%
Collected volatile condensable material (CVCM)[2]	0.00	%

1. *RML < 1%.*
2. *CVCM < 0.1%.*

7 PCB precautions

- A ground plane on each layer of the PCB with multiple vias dedicated for interconnexion is recommended for high-speed circuit applications to provide low parasitic inductance and resistance. The goal is to have a “common ground plane” where AGND and DGND are connected with the lowest DC resistance and lowest AC impedance.
- The separation of the analog signal from the digital output is mandatory to prevent noise from coupling onto the input signal.
- Power supply bypass capacitors must be placed as close as possible to the IC pins to improve high-frequency bypassing and reduce harmonic distortion.
- All leads must be as short as possible, especially for the analog input, so to decrease parasitic capacitance and inductance.
- To minimize the transition current when the output changes, the capacitive load at the digital outputs must be reduced as much as possible by using the shortest possible routing tracks. One way to reduce capacitive load is to remove the ground plane under the output digital pins and layers at high sampling frequencies.
- Choose the smallest possible component sizes (SMD).

8 Definitions

The "acquisition time" is the time required to get the input voltage. During this time, the hold capacitor is charged by the input voltage.

The "aperture delay" is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion.

Channel-to-channel isolation is the residual noise injected on the selected channel by other unselected channels.

The "conversion time" is the time required, after the input voltage is acquired, to convert the input voltage to a digital word.

"Differential non-linearity" (DNL) is the maximum deviation from the ideal step size of 1 LSB.

Duty cycle is the ratio, for a periodic digital signal, of the high level duration divided by the total period.

Effective number of bits (ENOB) is a method of specifying signal-to-noise and distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

Full power bandwidth is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

Full scale error (single-ended input) is the deviation of the last code transition (111...110) to (111...111) from the ideal (AVCC -1LSB), after offset error is fixed.

Positive full scale error (differential input) is the deviation of the last code transition (111...110) to (111...111) from the ideal (AVCC -1LSB), after offset error is fixed.

Negative full scale error (differential input) is the deviation of the last code transition (111...110) to (111...111) from the ideal (-AVCC +1LSB), after offset error is fixed.

Integral non-linearity (INL) is the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

Intermodulation distortion (IMD) is the result of the product of two pure sinewaves at frequency fa and fb applied to the ADC input. To avoid clipping when the sinewave is in phase, the level must be just below -6 dBFS. Assuming that the level of the two tones is equal, IMD2 is the difference in dBc between level(fa or fb) and level(fa ± fb). IMD3 is is the difference in dBc between level(fa or fb) and level(2fa ± fb) or level(fa ± 2fb).

Missing codes are those output codes that never appear at the ADC outputs. The RH-AD128 is guaranteed not to have any missing code.

Offset error (single-ended input) is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND +1 LSB).

Offset error (differential input) is the deviation of the mid-code transition (01…111) to (10…000) from the ideal (i.e. AVCC/2 +1 LSB).

Signal-to-noise ratio (SNR) is the ratio, expressed in dB, of the rms value of the fundamental of input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC-component.

Signal-to-noise plus distortion (S/N+D or SINAD) is the ratio of the rms value of the fundamental of input signal to the rms value of all of the other spectral components below half the sampling frequency, including harmonics but excluding DC-component.

Spurious free dynamic range (SFDR) is the difference, expressed in dB, between the desired signal amplitude of fundamental to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

Total harmonic distortion (THD) is the ratio, expressed in dBc, of the rms total of the first nine harmonic components at the output to the rms level of fundamental of the input signal frequency as seen at the output. THD is calculated as

THD=20log10[sqrt((Af2²+…+Af10²)/Af1²)] where Af1 is the RMS power of the fundamental at the output and Af2 to Af10 are the RMS power in the first nine harmonic frequencies.

Throughput time is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion time.

9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 TSSOP-20 package information

Figure 6. TSSOP-20 Mechanical drawing

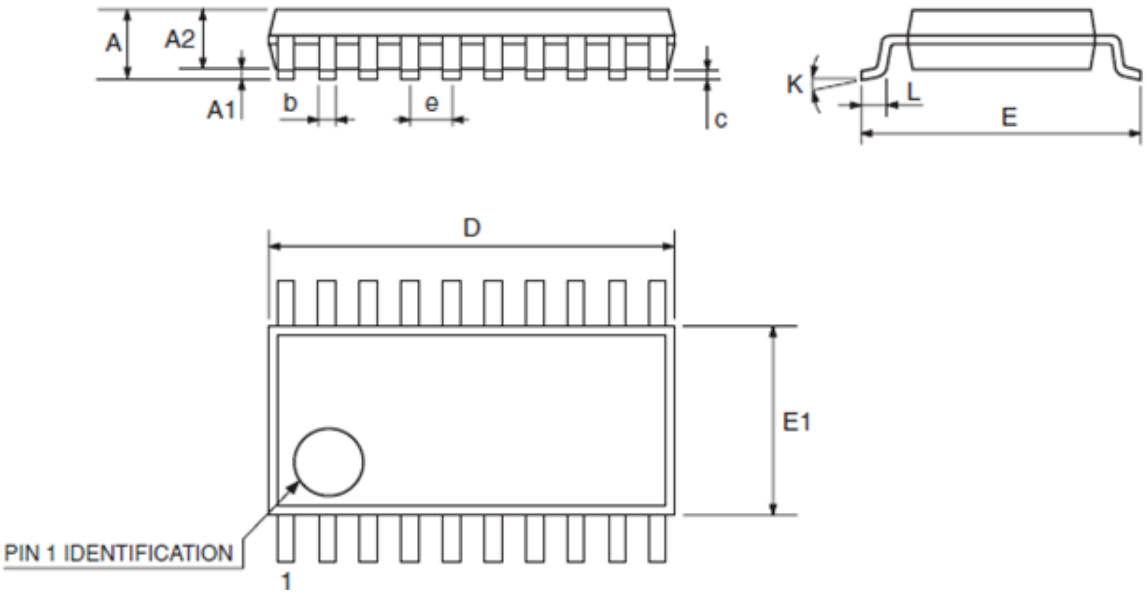


Table 8. TSSOP-20 package mechanical data

Symbol	Milimeters			Inches(1)		
	Min.	Typ.	Max.	Min	Typ	Max
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		
c	0.09		0.20	0.004		
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Note: TSSOP: Thin-Shrink Small Outline Package, using golden bonding and Nickel/Palladium/Golden-lead-finishing.

9.2 TSSOP-20 packing information

Figure 7. **TSSOP-20 Carrier tape (dimensions in mm)**

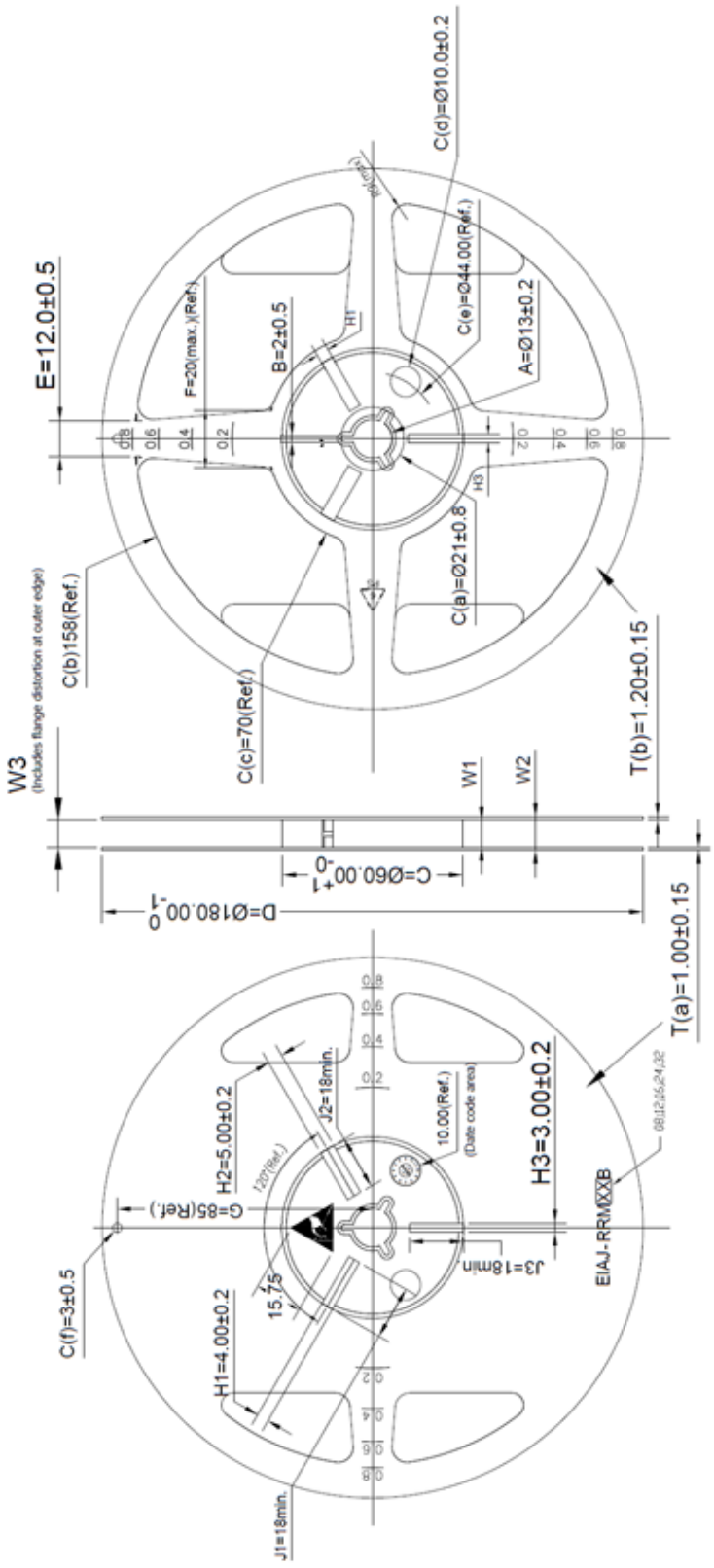
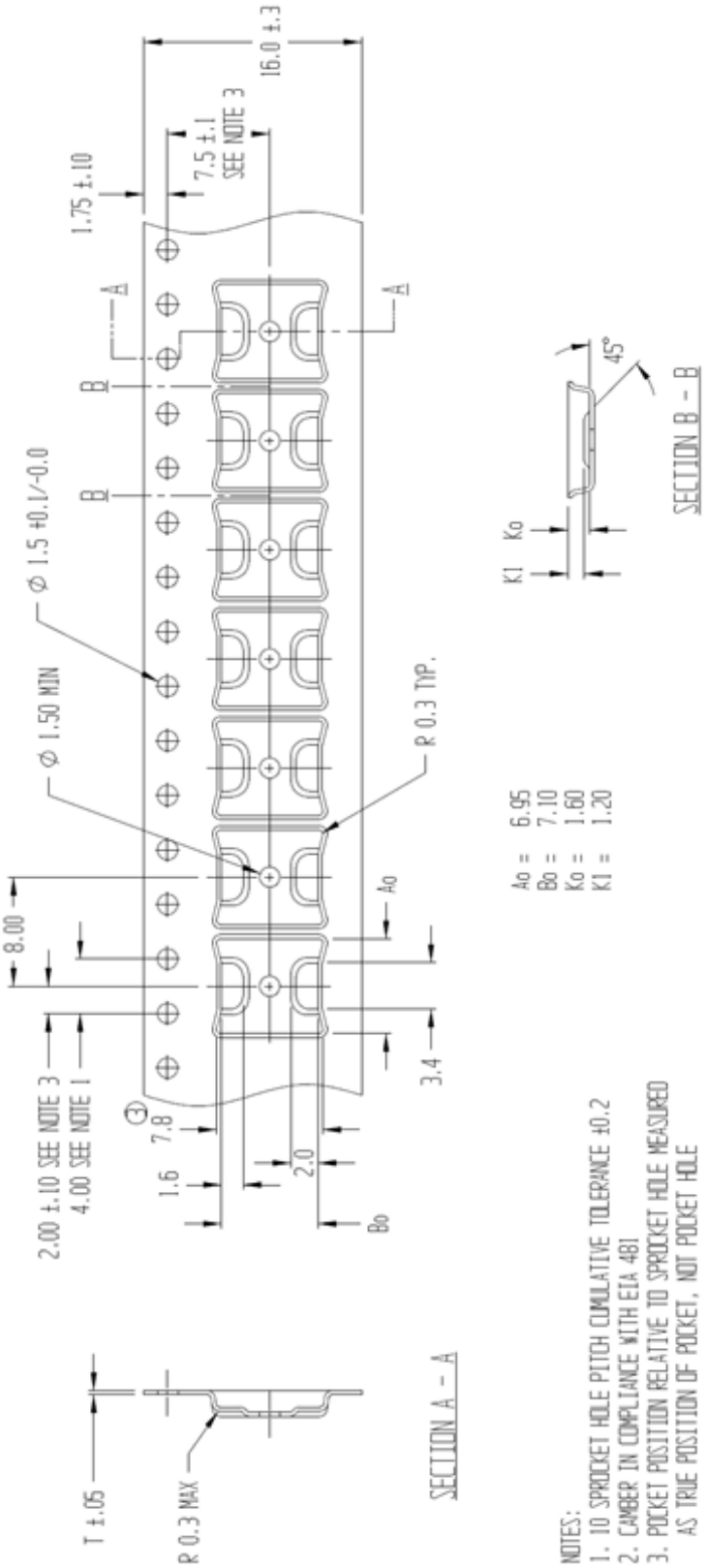


Figure 8. **Tape drawing for TSSOP-20 (dimensions in mm)**



10 Ordering information

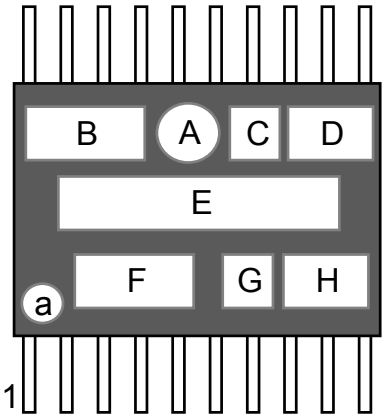
Table 9. Ordering information

Order code	Quality Level	Package	Lead-finish	Marking	Packing
LEOAD128PT-D	Development sample	TSSOP-20	NiPdAu	DLEOAD128	Tape and reel
LEOAD128PT	Flight model	TSSOP-20	NiPdAu	LEOAD128	Tape and reel

Table 10. Order code

LEO	AD128	P	T
LEO qualification	Name	TSSOP-20 package	Tape and reel

Figure 9. TSSOP-20 marking



a: pin-1 reference
A : Second Level of interconnexion (type of lead-finishing)
B: ST logo
C: Assy plant
D: Lot code
E: Marking area
F: Country of origin
G: Assy year
H: Assy week

Revision history

Table 11. **Document revision history**

Date	Version	Changes
01-Mar-2021	1	Initial release.
16-Sep-2021	2	Updated Section 5 Radiations. Removed note and footnote in Table 9. Ordering information.
24-Oct.2024	3	Adjusted timing specifications in Table 6 (typ. values removed).

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