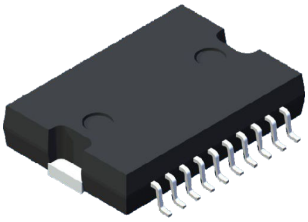
LEO3910

Datasheet

Rad-hard plastic 2 A positive low drop voltage regulator



Power-SO 20
slug-down

Product status link
LEO3910

Features

- Operating input voltage from 3 V to 12 V
- Adjustable output voltage from 1.23 V to 9 V
- Low-dropout voltage: 0.35 V @ I_O = 400 mA
- Overtemperature protection
- Overcurrent protection
- Adjustable current limitation
- Inhibit pin
- High dissipation Power-SO20 package: Rthjc < 2 °C/W
- Operating temperature range: -40 to +125 °C
- Compliant with ST's LEO specification, including
  - Wisker free Nickel/Palladium/Gold lead finishing
  - Gold wires
  - Characterized outgassing: RML < 1% - CVCM < 0.1%
- Radiation performance:
  - 50 krad(Si) Total Ionizing Dose
  - TNID immune at 3.10^{11} proton/cm²
  - SEL free up to 62 MeV.cm²/mg

Application

- LEO satellites power management
- Power supply of FPGA, MPU, ASIC, and MCU
- Power management in radiative and other harsh environments

Description

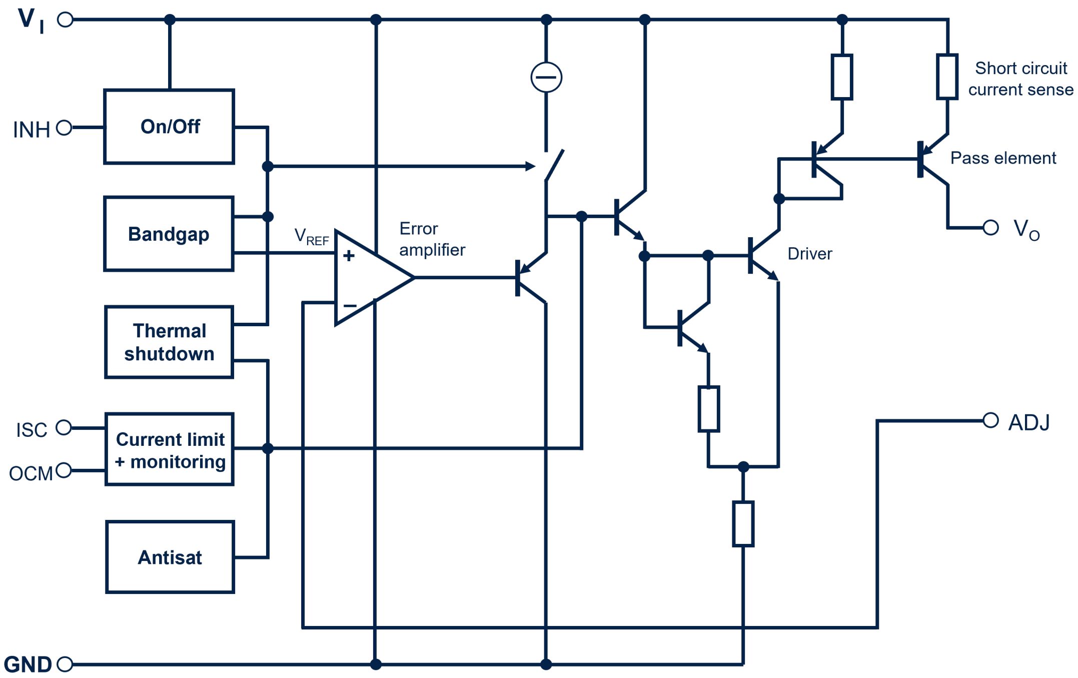
The LEO3910 is a positive adjustable voltage regulator housed into a Power-SO 20 slug-down package, which is able to provide in regulation a maximum output current up to 2 A.

It can operate over a large temperature range of -40 °C to +125 °C.

The LEO3910 is compliant with the ST-LEO-specification, dedicated specifications for space-ready rad-hard plastic products. This AEC-Q100-based specidfication offers radiation hardness and the capability to support large quantities, together with a trade-off optimized for LEO space crafts between quality assurance and cost of ownership (details on the ST LEO generic specification can be found in TN1432).

1 Block diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin configuration

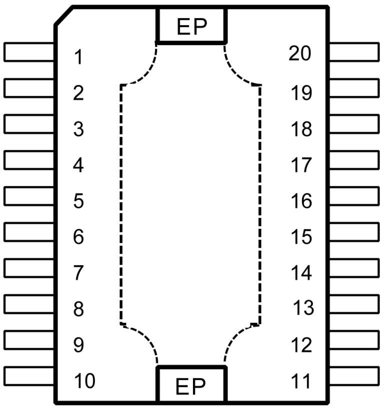
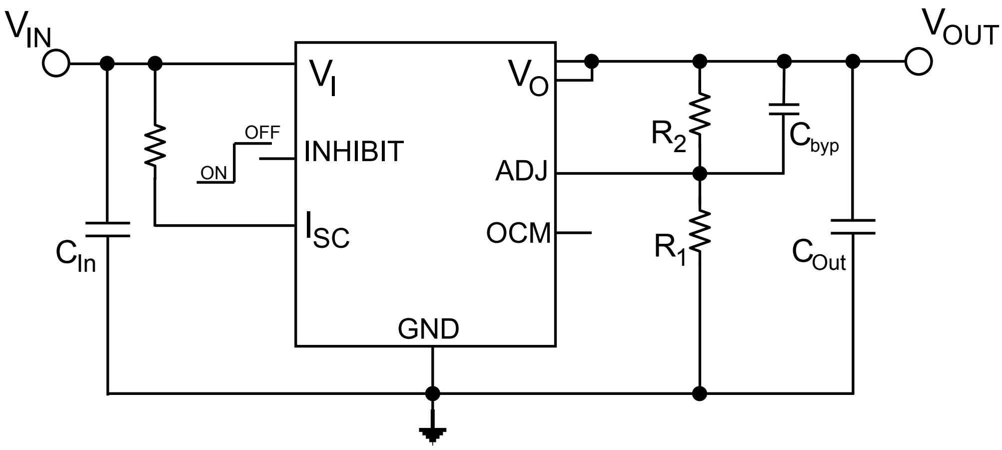


Table 1. Pinout configuration

Pin number	Pin name	Description
EP	EP	Slug down exposed pad, internally connected to pins 1, 10, 11 and 20 The Exposed pad should be grounded to maximize dissipation
1	EP	Internally connected to EP
2, 3	NC	Not connected
4, 6	V_O	Output voltage
5	V_I	Input voltage
6, 4	V_O	Output voltage
7	ISC	Current limit setting
8, 9	NC	Not connected
10, 11	EP	Internally connected to EP
12	OCM	Over-current monitoring
13, 14, 15	NC	Not connected
16	GND	Ground
17	INH	Inhibit
18	NC	Not connected
19	ADJ	Output voltage feedback error adjustment
20	EP	Internally connected to EP

3 Application circuit

Figure 3. Typical application circuit



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	-0.3 to 14	V
V_O	DC output voltage range	-0.3 to V_I + 0.3	V
V_{ADJ}	ADJ pin voltage	See note 1	V
V_{OCM}	Over current monitor pin voltage	-0.3 to V_I + 0.3	V
V_{ISC}	Current limit pin voltage	See note 2	V
V_{INH}	INHIBIT input voltage	-0.3 to V_I + 0.3	V
T_{stg}	Storage temperature range	-65 to +150	°C
ESD	Electrostatic discharge HBM	2	kV
	Electrostatic discharge CDM	750	V

- **Note 1:** V_{ADJ} is internally maintained at 1.23 Volt. A forced excursion below - 0.3 Volt or above the smallest of (V_I + 0.3) and 3.93 Volt may permanently damage the product.
- **Note 2:** V_{ISC} may be pulled-up to V_I or left floating. A forced excursion below the lowest of -0.3 Volt and (V_I - 2.7) or above (V_I + 0.3) may permanently damage the product.

Table 3. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_I	DC input voltage V_I - V_{GROUND}		3 to 12	V
V_O	DC output voltage range		1.23 to 9	V
I_{OMAX}	Maxium output current		2	A
Top	Operating junction temperature		-40 to +125	°C
P_D	TC = 25 °C power dissipation		15	W

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2	°C/W
R_{thJA}	Thermal resistance junction-ambient	25	°C/W

5 Electrical characteristics

$V_I = V_O + 2.5$ V, $T_j = -40$ to 125 °C, $C_I = 10$ µF, $C_O = 10$ µF tantalum, unless otherwise specified.

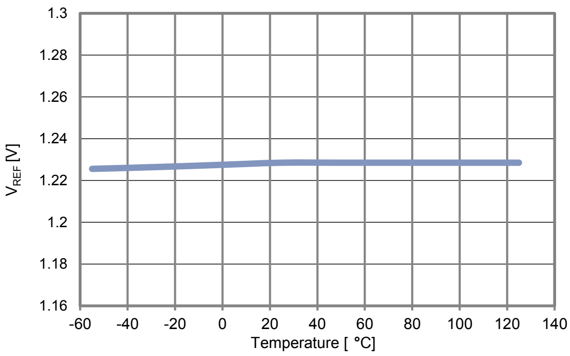
Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Input voltage	$I_O = 2$ A	3		12	V
V_O	Reference voltage	$I_O = 5$ mA, $V_O = V_{ADJ}$	1.19	1.23	1.27	V
I_{OLIM}	Overcurrent protection lilimation [1]	$V_O = 0$ V	0.8		2	A
$\Delta V_O/\Delta V_i$	Line regulation	$V_I = V_O$+2.5 V to 12 V, $I_O = 5$ mA	-	0.07	0.35	%
$\Delta V_O/\Delta I_O$	Load regulation	$V_I = V_O$+2.5 V, $I_O = 5$ mA to 1 A	-	0.4	0.6	%
Z_{OUT}	Output impedance	$I_O = 100$ mA DC and 20 mA rms		100		mΩ
V_d	Dropout voltage	$I_O = 400$ mA, $V_{out} = 3$ V	-	0.35	0.7	V
		$I_O = 1$ A, $V_{out} = 3$ V	-	0.5	1	V
		$I_O = 2$ A, $V_{out} = 3$ V	-	0.75	1.5	V
I_q	Quiescent current	$V_I = V_O$+2.5 V to 12 V, $I_O = 5$ mA	-	1.6	6	mA
		$V_I = V_O$+2.5 V to 12 V, $I_O = 30$ mA	-	2.7	8	mA
		$V_I = V_O$+2.5 V to 12 V, $I_O = 300$ mA	-	11	25	mA
		$V_I = V_O$+2.5 V to 12 V, $I_O = 1$ A	-	32	62	mA
		$V_I = 12$ V $V_{INH} = 3$ V, off mode	-	0.3	-	mA
SVR	Supply voltage rejection[1]	$V_I = V_O$+2.5 V ± 1 V, $I_O = 5$ mA, V_O=3 V, f = 33 kHz Tj = 25 °C	-	50	-	dB
$V_{INH\ (OFF)}$	Inhibit turn-off voltage	$I_O = 5$ mA	2.4	-	-	V
$V_{INH\ (ON)}$	Inhibit turn-on voltage	$I_O = 5$ mA	-	-	0.8	V
I_{INH}	Shutdown input current	$V_{INH} = 5$ V	-	120	-	µA
V_{OCML}	Overcurrent monitor voltage low	$I_{OCM} = 10$ mA (sunk current), $V_I = 12$ V	-	0.4	-	V
V_{OCMH}	Overcurrent monitor voltage high	$I_{OCM} = -10$ µA (sourced current) $V_I = V_O$+2.5 V to 12 V	-	V_I	-	V
eN	Output noise voltage[1]	B= 10 Hz to 100 kHz $I_O = 5$ mA to 2 A Tj = 25 °C	-	40	-	µVrms/V

1. *These values are guaranteed by design, not tested in production.*

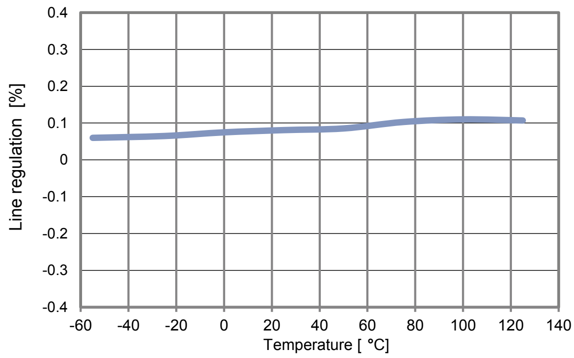
6 Typical characteristics

Figure 4. **Reference voltage vs. temperature (V_{IN}=V_{OUT}+2.5 V)**



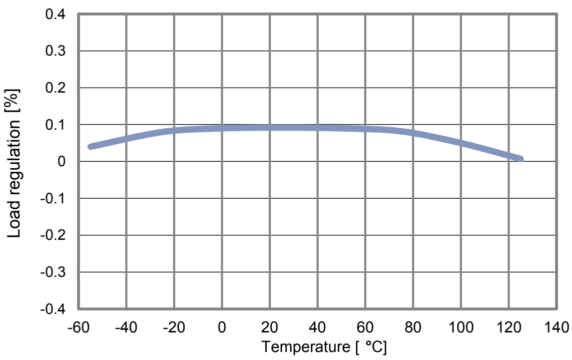
Vin=Vout+2.5V, Vout= Vadj, Cin=0.1Fμ,
Cout=1μF (tantalum), Iout = 5 mA

Figure 5. **Line regulation vs. temperature**



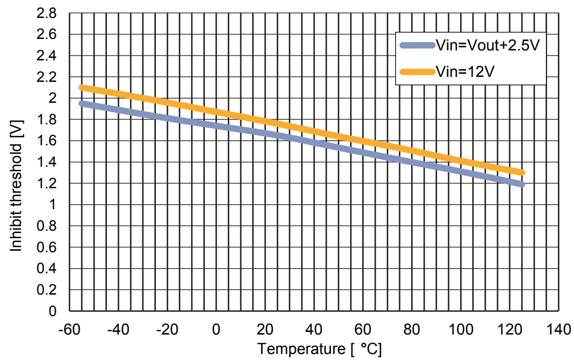
Vout+2.5 V<Vin <12V, Vout= Vadj, Cin=0.1Fμ
Cout=1μF (tantalum),Iout=5mA

Figure 6. **Load regulation vs. temperature (I_{OUT}= 5 mA to 1 A)**



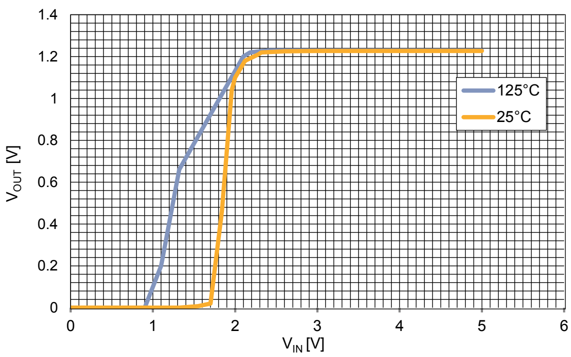
Vin=Vout+2.5V, Vout=Vadj, Cin=0.1μF,
Cout=1μF (tantalum),5mA<Iout<1 A

Figure 7. **Inhibit threshold vs. temperature**



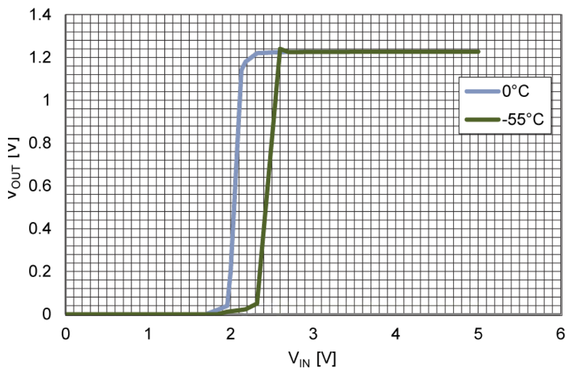
Vout =Vadj, Cin=0.1 μF, Cout =1 μF(tantalum), No load

Figure 8. **Output voltage vs input voltage (I_{OUT}=0 mA,T=25 °C and T=125 °C)**



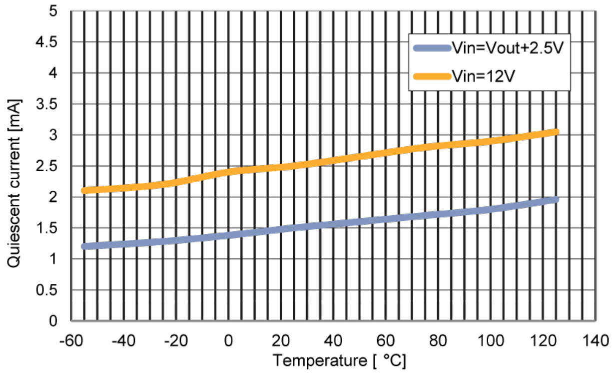
Vout = Vadj, Cin =0.1μF, Cout=1μF(tantalum), No load,
T=25 °C, T=125 °C

Figure 9. **Output voltage vs input voltage (I_{OUT}=0 mA,T=0 °C and T=-55 °C)**



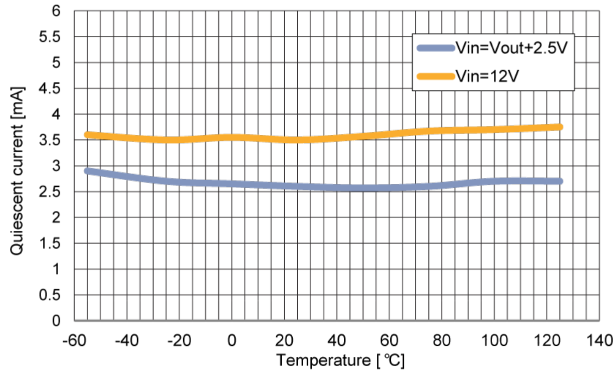
Vout = Vadj, Cin =0.1μF, Cout=1μF(tantalum),
No load, T=0 °C, T= 55 °C

Figure 10. Quiescent current vs. temperature (no load)



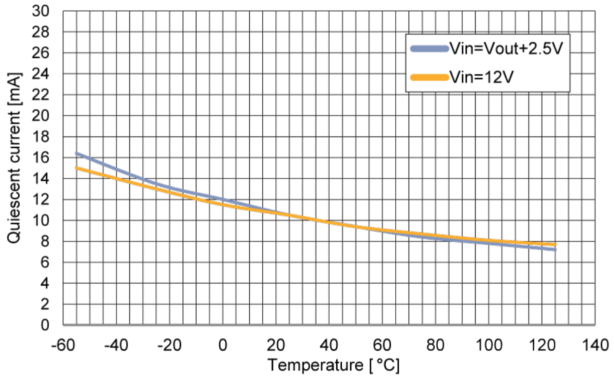
Vout = Vadj, Cin = 0.1 µF, Cout = 1 µF(tantalum), no load

Figure 11. Quiescent current vs. temperature (I_{OUT} = 30 mA)



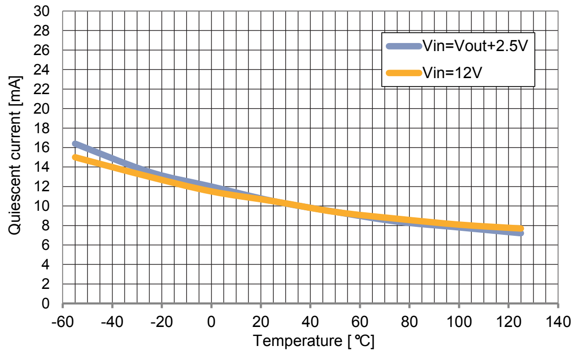
Vout = Vadj, Cin = 0.1 µF, Cout = 1 µF(tantalum), Iout=30 mA

Figure 12. Quiescent current vs. temperature (I_{OUT} = 300 mA)



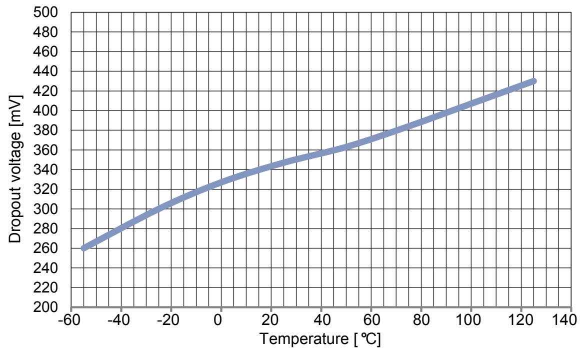
Vout = Vadj, Cin = 0.1 µF, Cout = 1 µF(tantalum), Iout=300 mA

Figure 13. Quiescent current vs. temperature (I_{OUT} = 1 A)



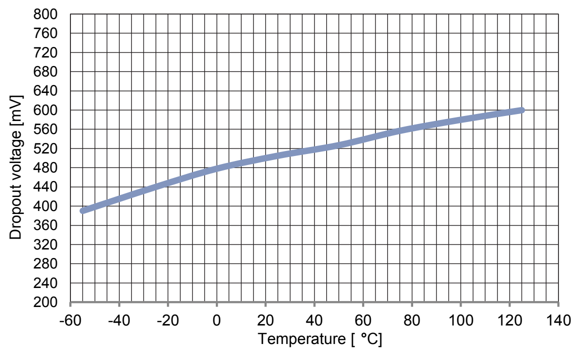
Vout = Vadj, Cin = 0.1 µF, Cout = 1 µF(tantalum), Iout=1A

Figure 14. Dropout voltage vs. temperature (V_{OUT}=3 V, I_{OUT}=400 mA)



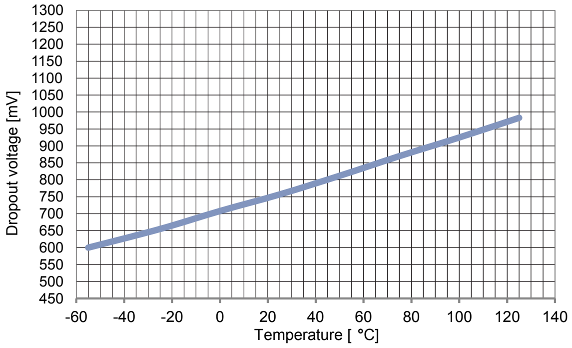
Vout = 3V, Cin = 0 1. µF, Cout = 1 µF(tantalum), Iout=400 mA

Figure 15. Dropout voltage vs. temperature (V_{OUT}=3 V, I_{OUT}=1 A)



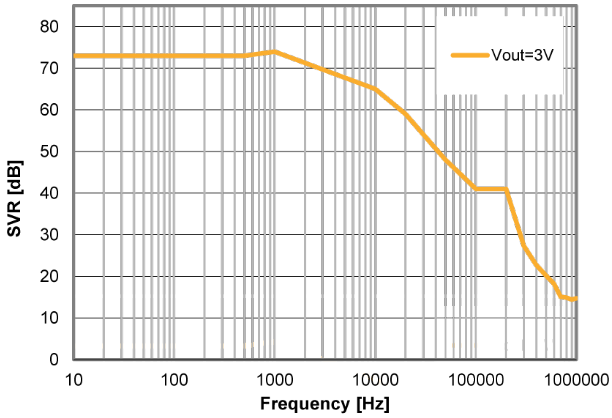
Vout = 3V, Cin = 0 1. µF, Cout = 1 µF(tantalum), Iout=1 A

Figure 16. Dropout voltage vs. temperature (V_{OUT}=3 V, I_{OUT}=2 A)



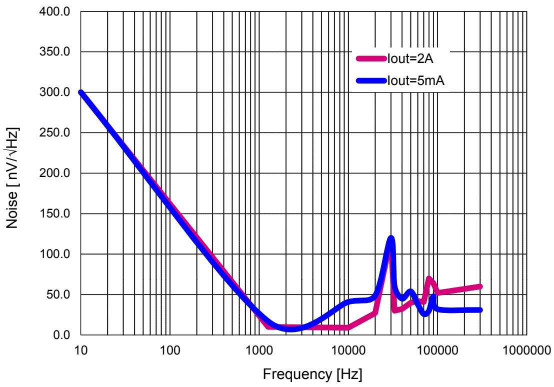
Vout = 3V, Cin = 0 1. μF, Cout = 1 μF(tantalum),Iout=2 A

Figure 17. SVR vs. frequency



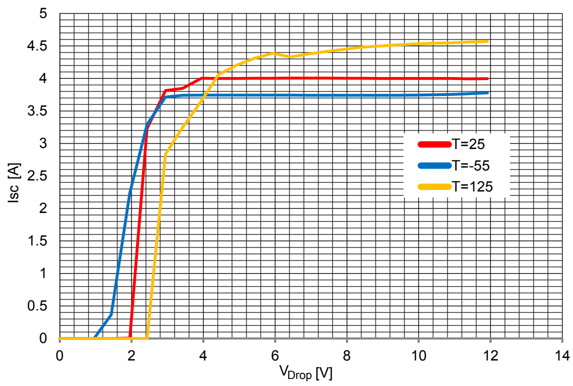
Vripple = ± 1 V, Cin= 0.1 μF, Cout = 1 μF (tant),
Iout = 5 mA, T= 25 °C

Figure 18. Output noise spectrum (V_{OUT}=V_{adj}, C_{OUT}=1 μF)



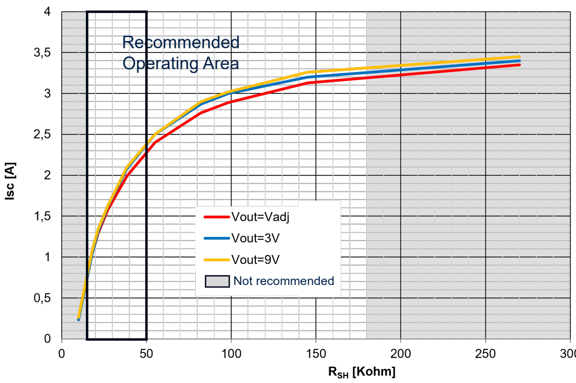
VIN = 3.5V, Vout=VADJ, Cin = 220μF, Cout = 1 μF(tantalum)

Figure 19. Short-circuit current vs. dropout voltage, (V_{OUT}=V_{adj})



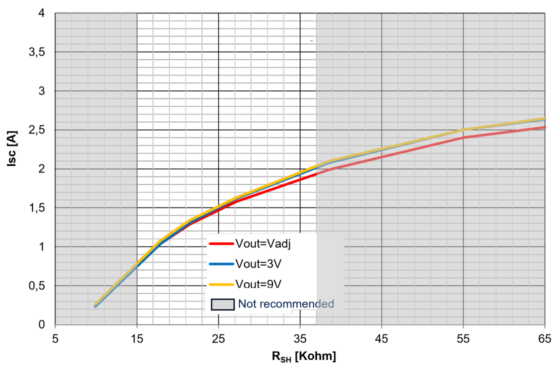
CIN = 0.1 μ F, Cout = 1 μF(tantalum), T=25°C, No RSH

Figure 20. Short-circuit current vs. R_{SH}



C_{IN} = 0.1μF, C_{OUT} = 1μF (tantalum)
I_{OLIM} = I_{SH} ÷ 1.6

Figure 21. I_{SH} vs. R_{SH}



C_{IN} = 0.1μF, C_{OUT} = 1μF (tantalum)
I_{OLIM} = I_{SH} ÷ 1.6

Figure 22. Current limitation principle

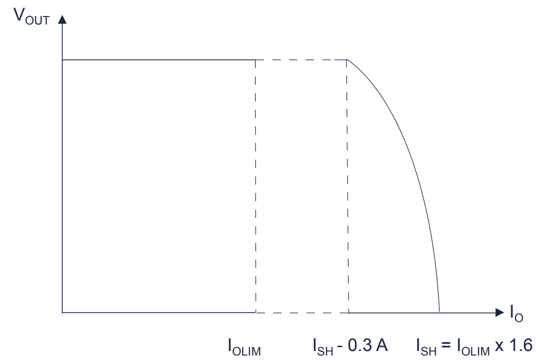
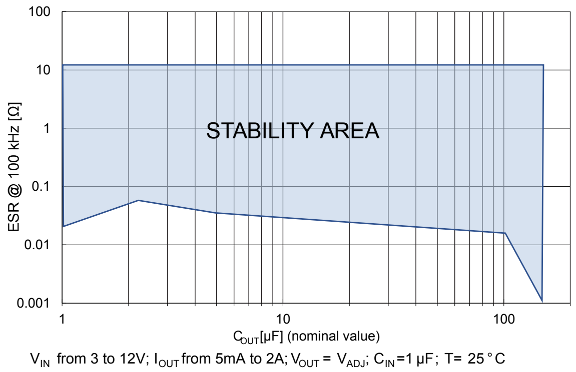


Figure 23. Stability plan



7 Radiations

7.1 Total ionizing dose (TID)

The LEO3910 is RHA guaranteed and ELDRS immune up to 50 krad(Si) as per MIL-STD-883 TM 1019 condition A and D.

The total ionization dose has been characterized in high and low dose rate on 5 biased and 5 unbiased pieces. This test has shown that the product is immune to ELDRS and that the worst-case configuration is with biased parts.

All parameters provided in Table 5. Electrical characteristics apply to both pre- and post-irradiation.

On top of the characterization, each wafer lot is submitted to a wafer lot acceptance with a TID test at a high dose rate on 5 biased parts per wafer lot with an acceptance criterion of 0 fail.

7.2 Total non-ionizing dose (TNID)

The total non-ionizing dose is tested with 50 MeV protons.

The test is performed during the product characterization and as part of the wafer lot acceptance test on 5 pieces per wafer lot with an acceptance criterion of 0 fail.

7.3 Heavy-ions

The LEO3910 is characterized under heavy ions up to 62 MeV.cm²/mg as summarized below:

- Tests performed: SEL, SET, SEU / SEFI

- Each test is performed on 3 samples of the final silicon in the worst-case conditions.

Table 6. Radiation summary

Type	Conditions	Value
TID	Up to 50 krad(Si) at 25 °C 40 krad(Si) / hour (HDR) and 36 rad(Si) / hour (LDR)	RHA guaranted and ELDRS free at 50 krad(Si)
TNID	Up to 3x10^{11} protons.cm² 50 MeV protons	Post TNID characteristics compliant with Table 5
SESB	Test up to 62.5 MeV.cm²/mg at 25 °C Fluence: 1.10^{7} ion/cm² Normal incidence	Immune to SEL up to 62 MeV.cm²/mg
SET	$T_{ambient}$ = 25 °C	Characterized up to 62 MeV.cm²/mg

8 Device description

The LEO3910 adjustable voltage regulator contains a PNP type power element controlled by a signal resulting from an amplified comparison between the internal temperature-compensated band-gap and the fraction of the desired output voltage value obtained from an external resistor divider bridge. The device is protected by several functional blocks.

8.1 ADJ pin

The output voltage feedback comes through an external resistor divider (R1, R2 as in the typical application schematic), whose mid-point connected to the ADJ pin (allowing to set the output voltage at the desired level).

8.2 Inhibit ON-OFF control

By setting the INHIBIT pin high, the device switches off the output current and voltage. The device is ON when the INHIBIT pin is set low. Since the INHIBIT pin is pulled down internally, it can be left floating in cases where the inhibit function is not used.

8.3 OCM pin

In the event of an overcurrent at the output, a voltage level of 0.4 V is present at the OCM pin. In other conditions, this voltage equals V_I. The OCM pin is internally pulled up by a 5 kΩ resistor up to V_I. It is buffered and can sink up to 10 mA.

8.4 Overtemperature protection

A temperature detector internally monitors the power element junction temperature. The device turns off when a temperature of approximately 175 °C is reached, returning to ON mode when back to approximately 135 °C. Combined with the other protection blocks, the device is protected from destructive junction temperature excursions in all load conditions. Prolonged operation under these conditions far exceeds the maximum operating ratings and device reliability cannot be guaranteed.

8.5 Overcurrent protection

An internal non-fold-back short circuit over-current limitation limits by default the short circuit output current ISH at typically 3.6 A when pin ISC is left floating. This overcurrent limitation is primarily designed to protect the device itself.

In the Power So 20 packaged version, the overcurrent limitation can be used as a basic adjustable overcurrent protection of the load. However, to secure proper startup of the regulator in all conditions, the current limit must comply with the guidelines provided below.

The overcurrent protection must be set above the maximum current required by the load in worst case conditions, including temperature and radiations, but low enough to be an effective protection. Furthermore, this I_{OLIM} value must be within the limits specified in the electrical specification in Table 5.

Once I_{OLIM} is defined, I_{SHADJ} is calculated by applying the formula $I_{SHADJ} = I_{OLIM} \times 1.6$ to account for the 0.3 A where the protection is active (see Section 6), for the temperature and radiation drifts as well as for the part to part variations of the default ISH and the protection circuits.

Figure 20 allow to define the typical value of the RSH resistors to be connected between pins ISC and V_I to set I_{SHADJ} at the desired value.

9 Application information

To adjust the output voltage, the R_2 resistor must be connected between the V_O and ADJ pins. The R_1 resistor must be connected between ADJ and ground. Resistor values can be derived from the following formula:

$V_O = V_{ADJ} (R_1 + R_2) / R_1$

The V_{ADJ} is typically 1.23 V, controlled by the internal temperature-compensated band gap block.

The minimum input voltage is 3 V. The LEO3910 is designed to operate for V_I - V_O > of the minimum specified dropout. The value of R_1, the resistance between ADJ pin and GND, must not be greater than 10 kΩ, in order to keep the output feedback error below 0.2%. A minimum of 0.5 mA I_O must be set to ensure perfect no-load regulation. It is advisable to dissipate this current into the divider bridge resistor.

The inhibit function switches off the output current very quickly. According to Lenz’s law, the external circuitry reacts with LdI/dt terms which can be of high amplitude in case somewhere a serial coil inductance exists. Large transient voltage would develop on both device terminals. It is advisable to protect the device with Schottky diodes to prevent negative voltage excursions. In the worst case, a 14 V Zener diode could protect the device input.

All available V_I and V_O pins must be externally interconnected, to ensure stability and reliability of the device.

To ensure regulator stability, input and output capacitors with a minimum 10 μF are mandatory. These capacitors must be connected as close as possible to the device terminals.

In the case of high-current operation, an important factor to look at for the reliability target of the space application is the sustainable surge current of the capacitors used. The surge current is known to be one of the major failure mechanisms for these parts, especially when the equipment is turned ON.

Derating is a means for application engineers of space systems to further reduce the probability of failures by limiting the level of stresses to capacitors during application. Typical derating requirements for solid tantalum capacitors limit the maximum applied voltage to 50% of the rated voltage (VR) and the inrush currents are bounded by additional resistors used in series with the capacitors.

In addition, a ceramic capacitor of at least 100nF in parallel to the input and output bulk capacitors must be used for decoupling purposes. A 470 nF polyester capacitors, put close to the regulator between input and ground, helps further improving the LEO3910 reliability by filtering potentially dangerous over voltages spikes coming out during particular conditions.

A separate kelvin voltage sensing line provides the ADJ pin with exact load "high potential" information (see Figure 4. Application diagram for remote sensing operation). But variable remote load current consumption induces variable Iq current (Iq is roughly the IO current divided by the hFE of the internal PNP series power element) routed through the parasitic series line resistor RW2. To compensate for this parasitic voltage, resistor RW1 can be introduced to provide the necessary compensating voltage signal to the ADJ pin. A ceramic or polyester 47nF CBYP capacitor between ADJ and V_O pins is recommended when the remote sensing technique is implemented.

Since the LEO3910 adjustable voltage regulator is manufactured with very high speed bipolar technology (6 GHz fT transistors), the PCB layout must be designed with exceptional care, with very low inductance and low mutually coupling lines. Otherwise, high frequency parasitic signals may be picked up by the device resulting in system self-oscillation. The benefit is an SVR performance extended to far higher frequencies.

10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 PowerSO-20 package information

Figure 24. PowerSO-20 package outline

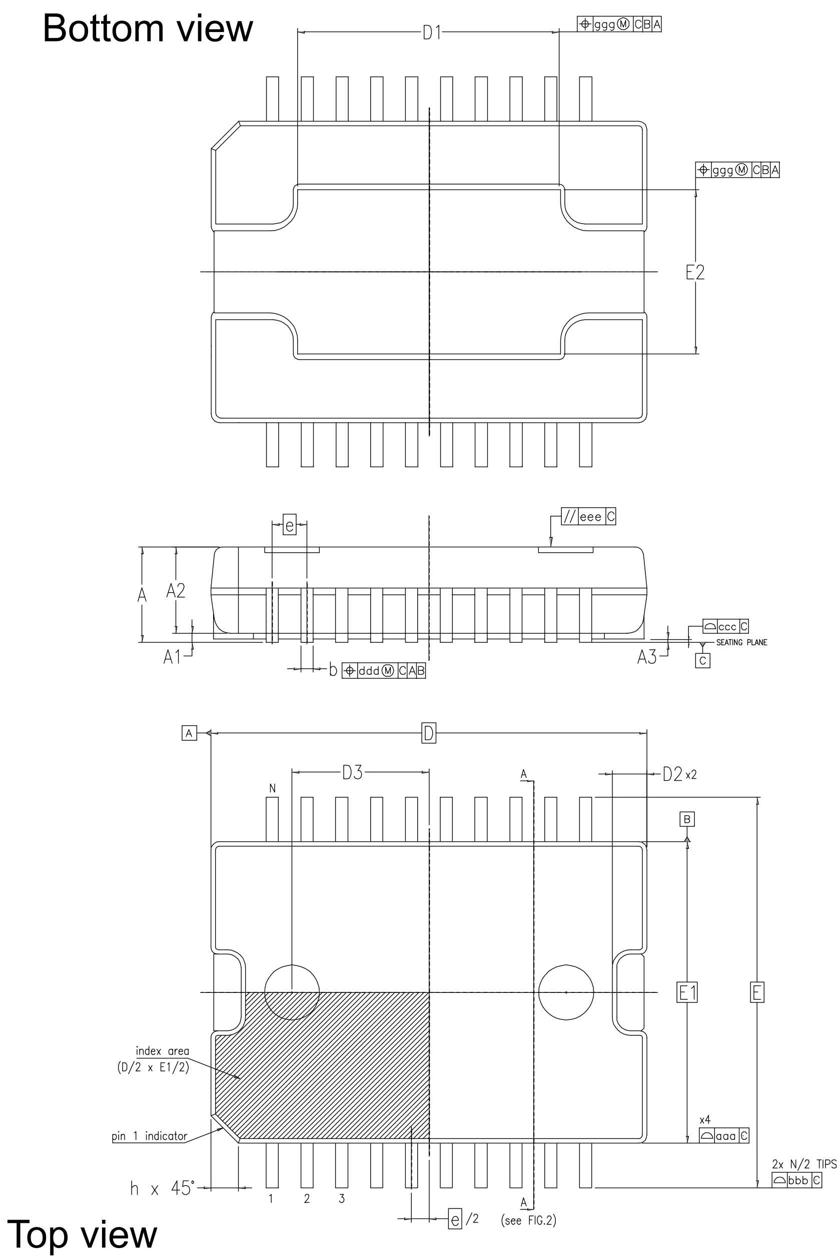


Figure 25. PowerSO-20 detail A

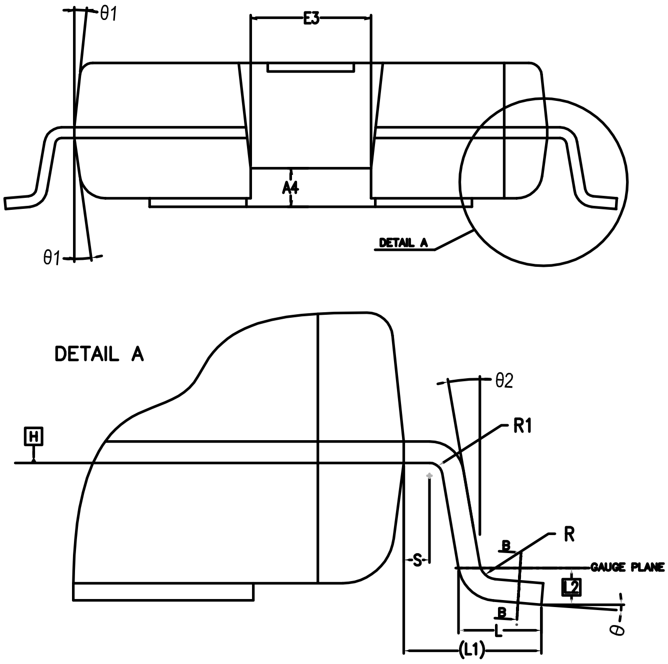


Figure 26. PowerSO-20 detail B

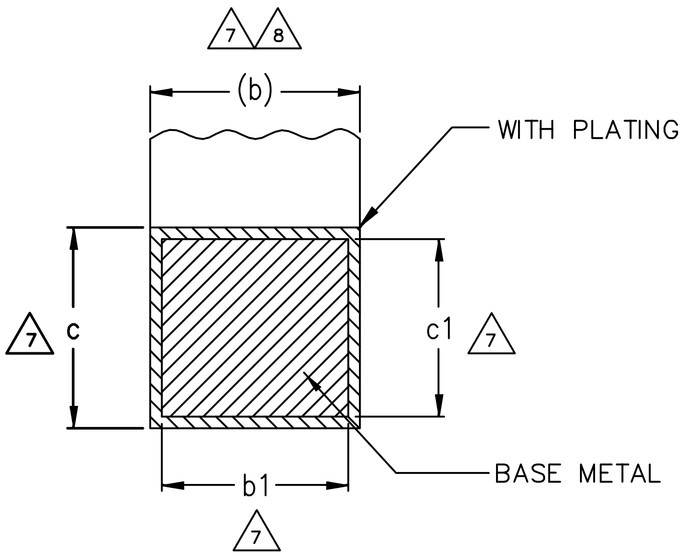


Table 7. **PowerSO-20 mechanical data**

Symbol	Milimeters		
	Min.	Typ.	Max.
θ	0°	-	8°
θ1	5°	-	10°
θ2	0°	-	-
A	-	-	3.50
A1	0.20	-	0.275
A2	3.10	-	3.20
A3	0.00	-	0.075
A4	0.83	-	0.95
b	0.40	-	0.53
b1	0.40	0.45	0.50
c	0.23	-	0.32
D	15.90 BSC		
D1	Variation		
D2	-	-	1.10
D3	-	5.00	-
e	1.27 BSC		
E	14.20 BSC		
E1	11.00 BSC		
E2	Variation		
E3	-	-	2.85
h	-	-	1.10
L	0.85	-	1.05
L1	1.60 REF		
L2	0.35 BSC		
N	20		
R	0.20	-	-
R1	0.20	-	-
S	0.25	-	-

Table 8. **Tolerance of form and position**

Symbol	Drawing
aaa	0.10
bbb	0.30
ccc	0.10
ddd	0.25
eee	0.10
ggg	0.25
Note	1.2

Table 9. Variations

Symbol	Drawing			Opt.
	Min.	Typ.	Max.	
D1	9.00	-	13.00	A
D2	5.60	-	6.20	

10.2 PowerSO-20 packing information

The flight models are delivered in a 600 position tape, out of which 100 consecutive ones are filled with a product, the others being left empty. The carrier tape and tape are described in the figures below.

The development samples are delivered in 7-position sticks of the same tape.

Figure 27. PowerSO-20 carrier tape outline

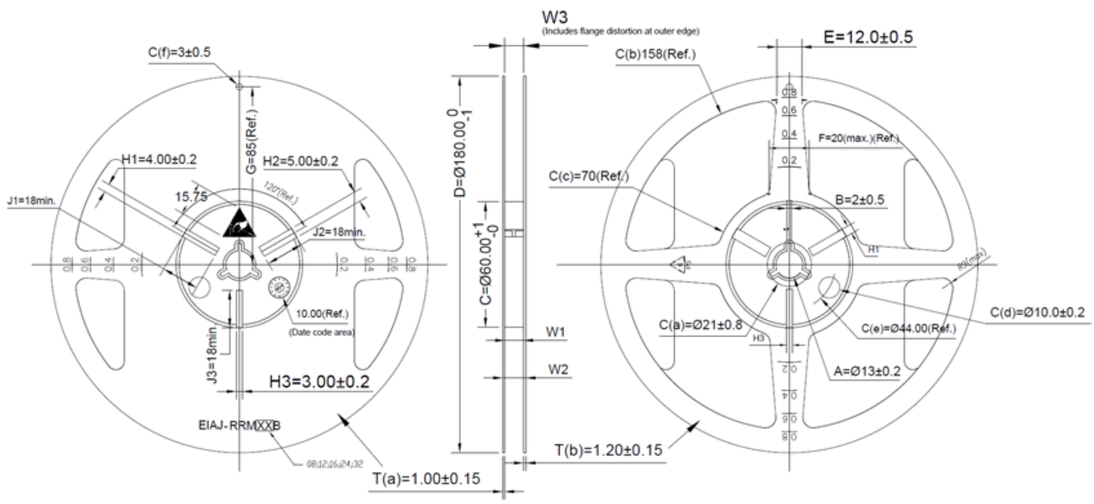
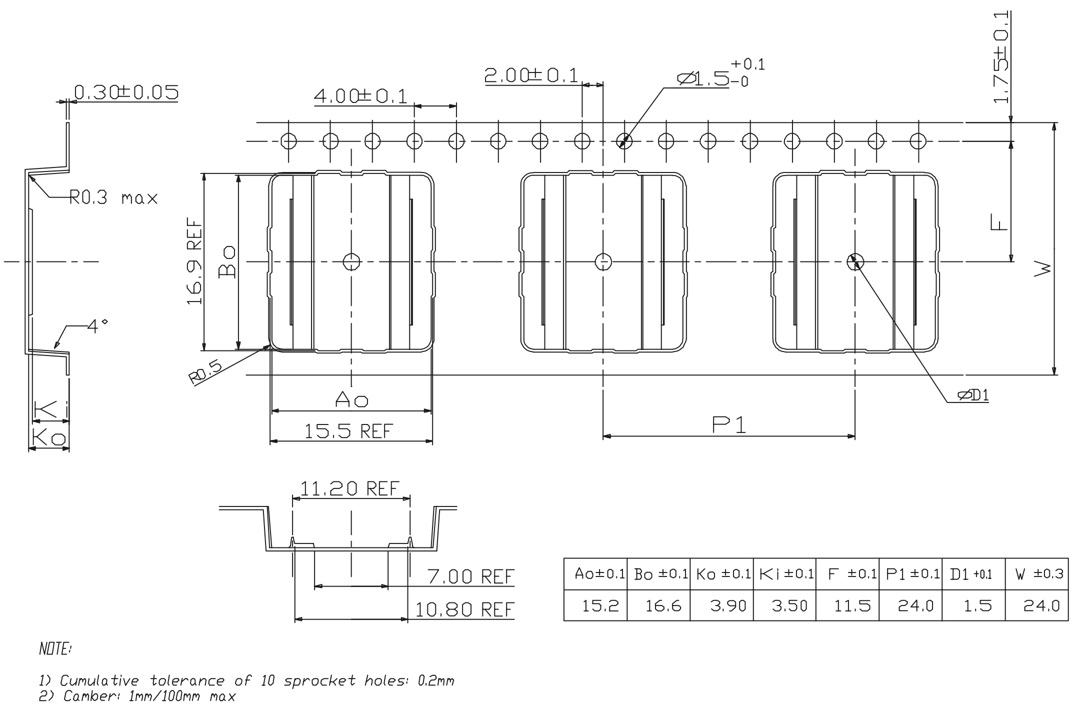


Figure 28. PowerSO-20 tape outline



10.3 Outgassing

The outgassing data of the PowerSO-20, measured as per ASTM-E-595, are provided in Table 10. They are compliant with the LEO generic specification setting the maximum limits for the recovered mass loss at 1% and for the collected volatile condensable material at 0.1%

Table 10. Outgassing

Specification (tested per ASTM E 595)	Value	Unit
Recovered mass loss (RML)[1]	0.06	%
Collected volatile condensable material (CVCM)[2]	0.00	%

1. *RML < 1%.*
2. *CVCM < 0.1%.*

11 Ordering information

Quality level	Quality level	Package	Lead-finish	Marking	Packing	Mass
LEO3910PDB	Flight model	PS0-20	NiPdAu	LEO3910	Tube	1.9
LEO3910PDT					Tape and reel	

1. Product specific marking. See figure Figure 29 for the descrption of the comlete marking.

11.1 Marking

The marking of the parts is summarized for the LEO flight models and in Table 11 for the development samples (refer to TN1418 for the description of the development samples quality level).

Figure 29. PSO marking

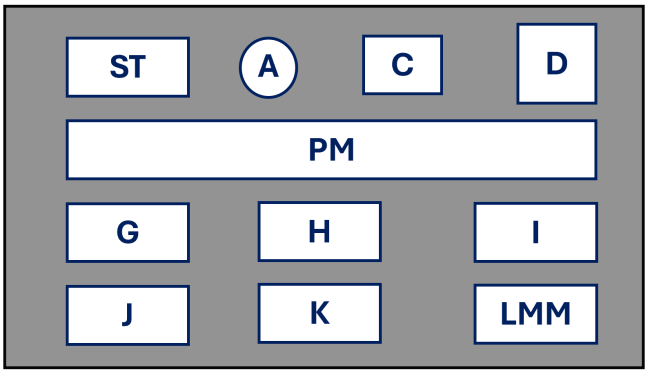


Table 11. Product marking description

Field	Description	LEO3910 values
ST	ST logo	
A	Pb free logo	e4 (1)
C	Sublot assembly index	Lot dependent
D	QR code	Lot dependent
PM	Specific product marking	See
G	Assembly plant	99 (Muar) (3)
H	Back end sequence (2)	xxx
I	Diffusion traceability	VA (Agrate) (3)
J	Country of origin	MYS (Malaysia) (3)
K	Test and finishing plant	99 (Muar) (3)
L	Date code year (last digit)	0 to 9
MM	Date code week	01 to 52

1. Package code as per Jedec J-STD-609. - e4 : precious metal, e.g. Ag, Au, NiPd, NiPdAu... excluding Sn.
2. Assembly flow reference.
3. Different value should denote that a product change notice has been issued.

11.2 Product documentation

The flight models are delivered with a certificate of conformance enclosed in the shipment box. Refer to TN1432 for the list of information it provides.

Table 12. Documentation LEO

Quality level	Documentation
Flight parts	Certificate of conformance [1]

1. *See TN1432 for details on the information provided in the certificate of conformance.*

Revision history

Table 13. Document revision history

Date	Version	Changes
17-May-2021	1	Initial release.
22-Feb-2022	2	Updated Section 5: Electrical characteristics and Section 6: Application information.
20-Jun-2024	3	Minor text changes.
02-Dec-2025	4	Updated features and description on the cover page. Updated Figure 1, Figure 2, Table 1, Added Section 11.1 and Product documentation.

Contents

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