L99VR01

Datasheet

Automotive low dropout linear voltage regulator with configurable output voltage having 200 mA current capability

Product status link
L99VR01

Features

Max. supply voltage (load dump)	V_S	40 V
Max. output voltage tolerance	ΔV_O	+/-2%
Output current	I_O	200 mA
Quiescent current	I_{qn}	≤1 µA [(1)]

1. *Maximum value with regulator disabled*

- AEC-Q100 qualified
- Operating DC power supply voltage range from 2.15 V to 28 V
- Battery and post regulation operating modes are allowed
- Low dropout voltage
- Low quiescent current consumption
- User-selectable output voltage (0.8 V; 1.2 V; 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V or 5 V)
- Output voltage precision ±2%
- Enable input for enabling/disabling the voltage regulator
- Output voltage monitoring with reset output
- Negligible ESR effect on output voltage stability for load capacitor
- Undervoltage lockout UVLO
- Fast output discharge
- Thermal shutdown and short-circuit current limitation
- Advanced thermal warning and output overvoltage diagnostic (L99VR01J only)
- Programmable short-circuit output current (L99VR01J only)
- Wide operating temperature range (T_J = -40°C to 175°C L99VR01J only)
- Limited documentation available for customers that need support when dealing with ASIL requirements as per ISO 26262

Description

L99VR01 is a low dropout linear voltage regulator designed for automotive applications available in SO-8 and in PowerSSO-12 packages. The LDO delivers up to 200 mA of load current and consumes as low as 1 µA of quiescent current when the regulator is disabled. The input is 40 V tolerant to withstand load dump, while the operating input voltage range is between 2.15 V and 28 V. The L99VR01 can be configured, through SELx pins, to generate a fixed selectable output voltage (0.8 V; 1.2 V; 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V or 5 V). High output voltage accuracy (±2%) is kept over wide temperature range, line and load variation. The L99VR01 features enable, reset, advanced thermal warning, fast output discharge and IShort control (IShort control and advanced thermal warning are available only for the L99VR01J). The regulator output current is internally limited so that the device is protected against short-circuit and overload, besides it features over temperature protection; the short current value is configurable by an external resistance in the L99VR01J version. The L99VR01 can operate both in post regulation, attached to a pre-regulated voltage or directly connected to battery.

1 Block diagram and pins description

Figure 1. Functional block diagram of L99VR01S

Figure 2. Functional block diagram of L99VR01J

Table 1. Pins description

Pin name	SO-8 pin	PowerSSO-12 pin	Function
V_S	1	1	Supply voltage. Block directly to ground with ceramic capacitor ≥ 4.7 µF and a 100 nF capacitator as close as possible to the pin
SEL1	2	2	Output voltage selectors.
SEL2	3	3	

Pin name	SO-8 pin	PowerSSO-12 pin	Function
SEL3	4	4	Output voltage selectors.
TW		5	Advanced thermal warning output. If the device detects a junction temperature above the warning threshold, the pin is pulled low. If an overvoltage condition occurs, a square wave is provided through the TW output. Leave floating if not used.
I_{Short}		6	Programmable short circuit output current input pin. A resistor between Ishort pin and GND sets the short circuit output current value.
EN	5	7	Enable input. With the Enable high, regulator and reset are operating. With the Enable low, regulator and reset are shutdown, while the fast discharge circuit is turned on. Connect the Enable to Vs to keep the device always enabled
GND	6	8	Ground reference.
T1		9	Reserved to test, connect the pin to Vo.
T2		10	Reserved to test, connect the pin to GND.
RST	7	11	Reset output. It is pulled down when output voltage goes below Vo_th. Leave floating if not used.
V_O	8	12	Voltage regulator output. Block to ground with a capacitor ≥ 3.3 µF (needed for regulator stability).
TAB		TAB	Connected to ground

Figure 3. Pins configuration

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the Table 2. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
V_S	Single pulse / tmax < 400 ms “transient load dump”	40	V
I_S	Input current	internally limited	
V_O	DC output voltage	-0.3 to 6.7	V
I_O	DC output current	internally limited	
V_{rst}	Reset output voltage	-0.3 to V_O + 0.3	V
T1, T2	Test pins	-0.3 to V_O + 0.3	V
I_{rst}	Reset output current	Internally limited	
V_{tw}	Thermal warning output voltage	-0.3 to V_O + 0.3	V
I_{tw}	Thermal warning output current	Internally limited	
V_{sh_ctrl}	“Short current” control voltage	-0.3 to 3.6	V
V_{EN}	Enable input	-0.3 to V_S + 0.3	V
V_{SELx}	Selectors input voltage	-0.3 to V_S + 0.3	V
VESD HBM	ESD HBM voltage level (HBM-MIL STD 883C)	±2	kV
VESD CDM	ESD CDM voltage level (CDM AEC-Q100-011)	±500	V
	ESD CDM voltage level on corner pins (CDM AEC-Q100-011)	±750	V

2.2 Thermal data

2.2.1 Thermal resistance

Table 3. Operation junction temperature

Item	Symbol	Parameter	Value		Unit
			PowerSSO-12	SO-8	
A.001	$R_{thj\text{-}case}$	Junction to case thermal resistance	8.5		°C/W
A.057	$R_{thj\text{-}lead}$	Junction to lead thermal resistance (1)		54.5	°C/W
A.002	$R_{thj\text{-}amb}$	Junction to ambient thermal resistance	27.4	71	°C/W

1. *Measured on Vs*

Note: the values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, four layers; Cu thickness 0.070 mm (outer layers) . Cu thickness 0.035 mm (inner layers), Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm.

2.2.2 Thermal protection

Table 4. Temperature threshold

Item	Symbol	Parameter		Test condition	Min.	Typ.	Max.	Unit
A.003	T_{prot_s} (1)	Thermal protection temperature		L99VR01S	150		180	°C
A.004	T_{prot_j} (1)	Thermal protection temperature		L99VR01J	175		200	°C
A.005	T_{prot_hyst}	Thermal protection hysteresis				11		°C
A.006	T_J	Operating junction temperature	SO-8	T_J	-40		150	°C
			Power-SSO-12		-40		175	
A.007	T_{stg}	Storage temperature		T_{stg}			150	°C

1. *Thermal protection is guaranteed by design and characterization.*

2.3 Electrical characteristics

Values specified in this section are for V_S = 2.15 V to 18 V, T_J = - 40 °C to +150 °C, unless otherwise stated.

Table 5. Electrical characteristics

Item	Pin	Symbol	Parameter		Test condition	Min.	Typ .	Max.	Unit
A.008	V_O	V_O	Output voltage		V_S = 2.15 to 18 V I_O = 1 to 200 mA SEL_CONF=[0;0;0]	0.784	0.8	0.816	V
					V_S = 2.15 to 18 V I_O = 1 to 200 mA SEL_CONF=[0;0;1]	1.176	1.2	1.224	
					V_S = 2.15 to 18 V I_O = 1 to 200 mA SEL_CONF=[0;1;0]	1.470	1.5	1.530	
					V_S = 2.45 to 18 V I_O = 1 to 200 mA SEL_CONF=[0;1;1]	1.764	1.8	1.836	
					V_S = 3.15 to 18 V I_O = 1 to 200 mA SEL_CONF=[1;0;0]	2.450	2.5	2.550	
					V_S = 3.45 to 18 V I_O = 1 to 200 mA SEL_CONF=[1;0;1]	2.744	2.8	2.856	
					V_S = 3.95 to 18 V I_O = 1 to 200 mA SEL_CONF=[1;1;0]	3.234	3.3	3.366	
					V_S = 5.65 to 18 V I_O = 1 to 200 mA SEL_CONF=[1;1;1]	4.9	5	5.1	
A.009	V_O	I_O	DC output current		V_O=0.8 V; 1.2 V, 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V; 5 V			200	mA
A.010	V_O	I_{short}	Short-circuit current lower value (1)	L99VR01J	V_S = 4V for V_O=3.3 V V_S = 5.8 V for V_O=5 V with I_{short} pin connected to GND	30	65	100	mA
A.011	V_O	I_{short}	Short-circuit current upper value	L99VR01S	V_S = 4 V for V_O=3.3 V V_S = 5.8 V for V_O=5 V I_{short}> I_O	240	360	480	mA
				L99VR01J	V_S = 4 V for V_O=3.3 V V_S = 5.8 V for V_O=5 V with Ishort pin floating; Ishort > I_O				
A.012	V_S, V_O	ΔV_O / V_O	Static line regulation		V_S is from V_{s_low} (2) to 18 V; I_O = 1 mA; 100 mA; 200 mA V_O=3.3 V; V_O=5 V			1	%
			Dynamic line regulation (3)		V_S is from V_{S_low} (2) to 18 V,Tr,f=1ms; I_O = 1 mA; 50 mA; 200 mA; V_O= 3.3 V; V_O=5 V			3	%
A.013	V_O	ΔV_O / V_O	Static load regulation (4)		I_O = 1 mA to 100 mA			1	%

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ .	Max.	Unit
A.013	V_O	$\Delta V_O / V_O$		V_O= 3.3 V for V_S=5 V; V_O= 5 V for V_S= 6 V				
			Dynamic load regulation(3) (4)	I_O = 10 mA to 100 mA, Tr, f=10 us V_O=3.3 V for V_S=5 V; V_O= 5 V for V_S= 6 V			3	%
A.014	V_S, V_O	V_{dp}	Drop voltage (5)	I_O = 150 mA V_O = 5 V			500	mV
				I_O = 150 mA V_O = 3.3 V				
				I_O = 150 mA V_O = 2.8 V				
				I_O = 150 mA V_O = 2.5 V				
				I_O = 150 mA V_O = 1.8 V				
				I_O = 200 mA V_O = 5 V			530	mV
				I_O = 200 mA V_O = 3.3 V				
				I_O = 200 mA V_O = 2.8 V				
				I_O = 200 mA V_O = 2.5 V				
				I_O = 200 mA V_O = 1.8 V				
A.015	V_S, V_O	PSRR	Power supply rejection ratio	V_S = 13.5 V; V_O = 5 V; I_O = 200 mA fr = 1 kHz		75(3)		dB
A.017	V_S, V_O	I_{qn}	Current consumption with regulator disabled $I_{qn} = I_S - I_O$	VS = 3.5V; 13.5 V, EN = low			1	µA
A.058	V_S, V_O	I_{qn_LL}	Current consumption with regulator enabled $I_{qn_LL} = I_S - I_O$	V_S = 3.5 V; 13.5 V, I_O = 0 µA; EN = high		75	100	µA
A.018	V_S, V_O	I_{qn_O}	Current consumption with regulator enabled $I_{qn_O} = I_s - I_O$	V_S = 3.5 V; 13.5 V, 0 < I_O ≤100 µA; EN = high		100	130	µA
A.019	V_S, V_O	I_{qn_50}	Current consumption with regulator enabled $I_{qn_50} = I_s - I_O$	V_S = 3.5 V; 13.5 V, I_O = 50 mA EN = high		1	1.3	mA
A.020	V_S, V_O	I_{qn_100}	Current consumption with regulator enabled $I_{qn_100} = I_s - I_O$	V_S = 3.5 V; 13.5 V, I_O= 100 mA EN = high		1.7	2.0	mA
A.021	V_S, V_O	I_{qn_200}	Current consumption with regulator enabled $I_{qn_200} = I_s - I_O$	V_S = 3.5 V; 13.5 V, I_O= 200 mA EN = high		3.1	3.5	mA
A.022	V_S	V_{UVLO_fall}	Undervoltage lockout, falling	V_O= 0.8 V; 1.2 V; 1.5 V; 1.8 V	1.5	1.6	1.7	V
				V_O = 2.5 V; 2.8 V; 3.3 V	2.3	2.4	2.55	

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ .	Max.	Unit
A.022	V_S	V_{UVLO_fall}	Undervoltage lockout, falling	V_O = 5 V	4.6	4.8	4.9	V
A.023	V_S	V_{UVLO_rise}	Undervoltage lockout, rising	V_O = 0.8 V; 1.2 V; 1.5 V; 1.8 V	1.7	1.8	2.1	V
				V_O=2.5 V; 2.8 V; 3.3 V	2.6	2.7	2.8	
				V_O=5 V	4.9	5.1	5.3	

1. *Ishort typical value of 120 mA for t= 400 µs during the power on*
2. *V_{s_Low} = 3.5 V@V_O = 0.8 V, 1.2 V,1.5 V,1.8 V& 2.5 V; V_{s_Low}=5 V@ V_O= 2.8 V & 3.3 V, V_{s_Low}= 6 V@V_O = 5 V*
3. *Parameters are guaranteed by design*
4. *Referred to Figure 26. Maximum load variation response*
5. *Considering that the minimum operating input voltage is 2.15 V, the dropout voltage (V_{dp}) is not defined for output voltages below 1.8 V.*

Table 6. Fast output discharge

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.024	V_O	R_{FD}	Fast discharge - pull down resistor	V_S= 3.95 V; 13.5 V; V_O = 3.3 V, V_O = 5 V EN = low	50	75	120	Ω

Table 7. Reset

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.025	RST	V_{rst_l}	Reset output low voltage	V_S = 5 V; 13.5 V Rext ≥ 4.7 KΩ to V_O V_O = 3.3 V, V_O = 5 V			0.2 x V_O	V
A.026	RST	I_{rst_lkg}	Reset output high leakage current	V_{rst} = 0.8 V			1	µA
A.027	RST	V_{O_th}	V_O out of regulation – low threshold	V_S = 5 V; 13.5 V V_O decreasing V_O=3.3 V, V_O=5 V	13.5%	10%	6.5%	Below V_O
A.055	RST	$V_{O_th_hyst}$	V_O out of regulation – low threshold hysteresis	V_S = 5 V; 13.5 V; V_O increasing; V_O=3.3 V ; V_O=5 V		2%		V_{O_th}
A.028	RST	T_{rr}	Reset reaction time	V_S = 5 V; 13.5 V; V_O=3.3 V ; V_O=5 V	10	16	37	µs
A.029	RST	T_{rd}	Reset delay time	V_S = 5 V; 13.5 V ; V_O=3.3 V ; V_O = 5 V	160[1]	250	300	µs

1. *T_{rd} = 120 µs for Vs < 3.5V.*

Table 8. Enable

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.042	EN	V_{En_low}	EN input low voltage				0.6	V
A.043	EN	V_{En_high}	EN input high voltage		1.5			V
A.045	EN	I_{En}	Pull down current	V_S = 13.5 V		4	12	µA

Table 9. Output voltages selectors

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.046	SELx	V_{SELx_low}	SELx input low voltage				0.3	V
A.047	SELx	V_{SELx_high}	SELx input high voltage		0.7			V
A.048	SELx	I_{SELx}	Pull down current	V_S = 3.5V; 13.5 V		0.1	0.4	µA

Table 10. Thermal warning and protection (only for L99VR01J)

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.049	TW	V_{Tw_low}	Thermal warning output low voltage	R_{ext} ≥ 4.7 kΩ to V_O V_O=3.3 V; V_O=5 V			0.2xVo	V
A.050	TW	T_{warn}	Thermal warning temperature		140	150	165	°C
A.051	TW	T_{warn_hyst}	Thermal warning hysteresis		3	11	15	°C
A.052	V_O	OV	V_O overvoltage	V_S = 5 V; 13.5 V; V_O increasing V_O=3.3 V; V_O=5 V	6.5%	10%	13.5%	Above VO
A.056	V_O	$O_{V__hyst}$	V_O overvoltage hysteresis	V_S = 5 V; 13.5 V; Vo decreasing V_O=3.3 V; V_O=5 V		2%		Below OV
A.054	TW	T_{w_per}	Thermal warning square wave period	V_S = 5V; 13.5 V V_O=3.3 V; V_O=5 V	160[1]	250	335	µs

1. *T_{w_per} = 130 µs for Vs < 3.5V.*

Note: all parameters are guaranteed in the junction temperature range -40 °C to 150 °C (unless otherwise specified); L99VR01J device is still operative and functional at higher temperatures (up to 175 °C). Parameters limit at higher junction temperature than 150 °C may change respect to what is specified as per the standard temperature range. Device functionality at high junction temperature is guaranteed by characterization.

All parameters are guaranteed by design for Vo not reported in test condition.

Note: minimum input voltage values are achievable adopting an input ceramic capacitator: C5750X7R2A475M230KA – ceramic capacitor multistrate SMD, 4.7 µF, 100 V, ±20%, X7R, C series TDK.

2.4 Electrical characteristics curves

Figure 4. Output voltage vs Tj

Figure 5. Output voltage vs VS

Figure 6. Drop voltage vs output current

Figure 7. Current consumption vs output current

Figure 8. Current consumption vs input voltage (Io < 1mA)

Figure 9. Current consumption vs input voltage (Io = 50 mA)

Figure 10. Current consumption vs input voltage (Io= 100 mA)

Figure 11. Short-circuit current vs Tj (Ishort pin floating)

Figure 12. Short-circuit current vs Tj (Ishort pin tied to GND)

Figure 13. Short-circuit current vs input voltage

Figure 14. Output voltage vs enable voltage (V_O =0.8 V)

Figure 15. Output voltage vs enable voltage (V_O =1.2 V)

Figure 16. Output voltage vs enable voltage (V_O =1.5 V)

Figure 17. Output voltage vs enable voltage (V_O =1.8 V)

Figure 18. Output voltage vs enable voltage (V_O =2.5 V)

Figure 19. Output voltage vs enable voltage (V_O =2.8 V)

Figure 20. Output voltage vs enable voltage (V_O =3.3 V)

Figure 21. Output voltage vs enable voltage (V_O =5 V)

Figure 22. VEn_high vs Tj

Figure 23. VEn_low vs Tj

Figure 24. PSRR

3 Test circuit and waveforms plot

3.1 Load regulation

Figure 25. Load regulation test circuit

Figure 26. Maximum load variation response

Vo=5V	Vo=3.3V

4 Application information

Figure 27. Application schematic

Figure 28. Application schematic – Post regulation

Input ceramic capacitor $C_2 \geq 4.7$ µF is necessary for the regulator to operate properly. The other input capacitor C1 can be used as backup supply for the application. The C_0 capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations.

Suggested value is $C_0 = 3.3$ µF.

The ESR of the SMD output ceramic capacitor has a negligible effect on the stability of the L99VR01 family for capacitors with low ESR. A ceramic SMD capacitor is recommended on Vo pin.

4.1 Voltage regulator

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure, a very low dropout voltage at current up to Io = 200 mA is obtained. The high-precision of the output voltage (±2%) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes down to $I_{qn_LL = 75}$ µA (low consumption mode). L99VR01 operates with reduced input voltage (post regulation) minimizing the internal power dissipation and maximizing the output current.

4.2 Output current limitation

Output current limitation is present to protect the regulator and the application from overload condition, such as short to ground.

Figure 29. Behavior of output current versus regulated voltage Vo

The Ishort current can be set in the range from 65 mA to 360 mA through an external resistor R_{sh} connected between I_{Short} pin and ground (L99VR01J version only).

Figure 30. Ishort versus Rsh

Open pin (no resistance on the Ishort pin), is seen as a max resistance corresponding to the maximum Ishort current.

4.3 Output voltage selection

The L99VR01 can provide one out of 8 different output voltages. The combination of three digital input selectors (SELx) determines the output voltage according to the following truth table.

Table 11. Truth table

V_O	SEL1	SEL2	SEL3
5	1	1	1
3.3	1	1	0
2.8	1	0	1
2.5	1	0	0
1.8	0	1	1
1.5	0	1	0
1.2	0	0	1
0.8 (Default)	0	0	0

The SELx pins configuration is acquired at the device start-up (EN transition from low to high) and once configuration is acknowledged, it cannot be changed until next EN transition.

When all the pins are left not connected, the default configuration will be selected.

Figure 31. **Example of output voltage selection**

SELx pins are internally connected to GND via pull down current source.

4.4 Enable

The L99VR01 is enabled/disabled by the enable input; a high voltage signal switches the regulator ON. When the enable pin is set low, the output is switched off, the current consumption of the device becomes as low as 1 µA and the Fast Output Discharge circuit is activated.

It may happen that the enable pin must be driven by components supplied at a voltage different from the regulator supply voltage. In this case the EN input pin must be set high only once Vs > 1.5 V. A solution to drive the enable pin is depicted in the following figure.

Figure 32. **Typical example of enable control**

In any case, since the enable input voltage is linked to the maximum DC supply voltage (V_S) applied to the L99VR01 (-0.3 V to Vs + 0.3 V), special care must be adopted in driving EN pin to avoid exceeding absolute maximum rating.

Note: A diode (0.25 V < VF < 0.75 V) connected in series with EN pin is requested only if the regulator is directly supplied by car battery.

4.5 Reset

The reset circuit supervises the output voltage V_O. If the output voltage falls below V_{O_th} then RST is pulled low with a reaction time Trr. When the output voltage rises above V_{O_th} + $V_{O_th_hyst}$ then RST is pulled high with a delay time T_{rd}. The delay is generated by an internal circuit. The reset circuit is active when En is high. Being RST an open-drain output an external resistance (Rrst) is needed between the RST pin and the Vo pin. The external resistance value can be in a range between 4.7 KΩ and 20 KΩ. Leave the RST pin floating if not used.

Figure 33. Reset timing diagram

4.6 Thermal warning and thermal shutdown

To warn the microcontroller about a severe temperature increase, a thermal warning output has been implemented (L99VR01J version only). If the device detects a junction temperature above T_{warn}, the advanced thermal warning (TW) output pin is pulled low while the voltage regulator and its features remain all active. The TW pin will return to its high logic level (equal to the Vo output value) once the temperature falls below the threshold T_{warn} - T_{warn_hyst}.

Figure 34. Thermal warning diagram

When junction temperature reaches the $T_{prot_j/s}$ thermal shutdown threshold the regulator output is quickly shut off through the internal Fast Output Discharge circuit; to be reactivated, junction temperature has to decrease below $T_{prot_j/s}$- T_{prot_hyst}. Being TW an open-drain output an external resistance (R_{TW}) is needed between the TW pin and the Vo pin. The external resistance value can be in a range between 4.7 KΩ and 20 KΩ. Leave floating if not used.

4.7 Overvoltage detection by advanced thermal warning read-out

The TW pin also provides diagnostics about output overvoltage (OV); to distinguish between a thermal warning event and an output overvoltage event, two different signals are generated at the same TW output pin. How reported in the previous paragraph a thermal warning event detection sets the TW pin LOW, instead an output overvoltage event generates a square wave at the TW pin (Figure 35. Square wave on TW pin generated during an overvoltage). Overvoltage detection has higher priority than thermal warning detection so that concurrence of thermal warning and over voltage events leads to a square wave like in the case of overvoltage detection (as shown in Figure 36. Warning signal caused by overvoltage and thermal warning on TW pin).

Figure 35. Square wave on TW pin generated during an overvoltage

A typical example of thermal warning and overvoltage failures management is depicted in Figure 36. Warning signal caused by overvoltage and thermal warning on TW pin.

Figure 36. Warning signal caused by overvoltage and thermal warning on TW pin

4.8 Fast output discharge

To assure a quick discharge of the external capacitor tied to the output pin down to around 1.3 V the L99VR01 uses an internal pulldown circuit. Activated each time the EN pin goes low, during thermal shut down and during undervoltage lockout, the output current will flow through the pulldown resistor of the fast output discharge circuit to ground. The fast output discharge feature is available for the output voltages Vo= 2.5 V (SELx = [1;0;0]) Vo= 2.8 V (SELx = [1;0;1]) Vo= 3.3 V (SELx = [1;1;0]) and Vo= 5 V (SELx = [1;1;1]).

4.9 Undervoltage lockout UVLO

The undervoltage lockout (UVLO) circuit allows a fast regulating element to turn off (activating the internal Fast Output Discharge circuit) if the input voltage drops below the threshold, V_{UVLO_fall}, avoiding undesired unknown output state during low input voltage. When the input voltage is above the V_{UVLO_rise} threshold, the regulating element is again turned on.

Figure 37. Undervoltage lockout on output voltage

4.10 Functional safety management

Even if not designed as safety HW element, the device contains some features that can be used to support application that need to fulfill functional safety requirements. Analysis of the IC's capability to reach the required safety level, should be made at system level under user's responsibility.

The following device safety requirements have been considered for a typical application:

Table 12. Safety requirement

ID	Description
SR-001	Operation of the voltage regulator(s) is allowed till over temperature limit.
SR-002	Operation of voltage regulator(s) is enabled until programmed current limit is reached.
SR-003	Output voltage of regulator(s) shall remain within programmed range when RST pin is not asserted.
SR-004	Output voltage of regulator(s) shall remain within programmed range when square wave at TW pin is not generated.

Based on the above requirements list the following safety mechanism has been implemented:

Table 13. Implemented safety mechanism

ID	Description	SR covered
SM1	Thermal sensor acting by TW pin	SR-004
SM2	Overtemperature protection	SR-001
SM3	Limitation on maximum output current	SR-002
SM4	Output voltage V_O monitoring for undervoltage detection	SR-002
SM5	Output voltage V_O monitoring for overvoltage detection	SR-002
SM6	RST reset assertion in case ofV_O undervoltage detection	SR-003

More details about functional safety can be found in the device safety manual, provided on customer request.

5 Application

Figure 38. Typical application

6 Package and PCB thermal data

6.1 PowerSSO-12 thermal data

Figure 39. PowerSSO-12 PC board

Note: The values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, two and four layers; Cu thickness 0.070 mm (outer layers). Cu thickness 0.035 mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 2.2 mm x 2.9 mm.

Figure 40. $R_{thj-amb}$ versus PCB copper area in open box free air condition

Figure 41. PowerSSO-12 thermal impedance junction ambient single pulse

Pulse calculation:

$Z_{TH\delta} = R_{TH}.\delta + Z_{THtp}(1-\delta)$

Where $\delta = tp/T$

Figure 42. Thermal fitting model of a V_{reg} in PowerSSO-12

Table 14. PowerSSO-12 thermal parameter

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	3.8			
R2 (°C/W)	4.2			
R3 (°C/W)	6	6	6	5
R4 (°C/W)	18	9	8	4.5
R5 (°C/W)	22	15	10	4
R6 (°C/W)	26	20	15	4
C1 (W.s/°C)	0.0015			
C2 (W.s/°C)	0.035			
C3 (W.s/°C)	0.15			
C4 (W.s/°C)	0.4	0.4	0.4	0.8
C5 (W.s/°C)	0.27	0.8	1	7
C6 (W.s/°C)	3	6	8	15

6.2 SO-8 thermal data

Figure 43. **SO-8 PC board**

Note: Layout condition of Rth and Zth measurements (PCB: double layer and four layers; FR4 area = 77 mm x 86 mm; PCB thickness = 1.6 mm; Cu thickness = 0.070 mm (front and back side), Cu thickness 0.035mm (inner layers); Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias of 0.025 mm, Footprint dimension 2.2 mm x 2.9 mm.

Figure 44. Rthj-amb vs PCB copper area in open box free air condition

Figure 45. SO-8 thermal impedance junction ambient single pulse

Pulse calculation formula:

$Z_{TH\delta} = R_{TH}.\delta + Z_{THtp}(1-\delta)$

$Z_{TH\delta} = R_{TH}.\delta + Z_{THtp}(1-\delta)$

where $\delta = tp/T$

Figure 46. Thermal fitting model of a Vreg in SO-8

Table 15. SO-8 thermal parameter

Area/island (cm2)	Footprint	2	8	4L
R1 (°C/W)	4.4			
R2 (°C/W)	4.5			
R3 (°C/W)	6			
R4 (°C/W)	28	23	23	23
R5 (°C/W)	30	24	21	19
R6 (°C/W)	41.6	25	21	14
C1 (W.s/°C)	0.0001			
C2 (W.s/°C)	0.002			
C3 (W.s/°C)	0.03			
C4 (W.s/°C)	0.05			
C5 (W.s/°C)	0.15			
C6 (W.s/°C)	1.4	3	5	5.5

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-12 package information

Figure 47. PowerSSO-12 package dimensions

Table 16. **PowerSSO-12 package mechanical data**

Symbol	Millimeters		
	Min	Typ.	Max
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
b	0.230		0.410
c	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

7.2 SO-8 package information

Figure 48. **SO-8 package dimension**

Table 17. SO-8 package mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D[1]	4.80	4.90	5.00
E	5.80	6.00	6.20
E1[2]	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. *Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).*
2. *Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

7.3 PowerSSO-12 packaging information

Figure 49. PowerSSO-12 tape and reel shipment (suffix “TR”)

REEL DIMENSIONS

Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	8
Hole diameter	D (± 0.05)	1.5
Hole diameter	D1 (min)	1.5
Hole position	F (± 0.1)	5.5
Compartment depth	K (max)	4.5
Hole spacing	P1 (± 0.1)	2

All dimensions are in mm.

7.4 SO-8 packaging information

Figure 50. SO-8 tape and reel shipment (suffix "TR")

Reel dimensions

Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+2/-0)	12.4
N (min)	60
T (max)	18.4

All dimensions are in mm.

Tape dimensions

According to electronic industries association (EIA) standard 481 rev.A, feb.1986

Tape width	**W**	12
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	8
Hole diameter	**D (+0.1/-0)**	1.5
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.05)**	5.5
Compartment depth	**K (max)**	4.5
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

8 Order codes

Order codes				
Order code			L99VR01	
Package	Tape & reel		SO-8	L99VR01STR
			PowerSSO-12	L99VR01JTR
P/N	**Enable**	**Reset**	**Advanced thermal warning**	**Ishort CTRL**
L99VR01STR	X	X	-	-
L99VR01JTR	X	X	X	X

Revision history

Table 18. Document revision history

Date	Version	Changes
02-Mar-2021	1	Initial release
13-Apr-2021	2	Updated *Table 11. Thermal warning and protection (only for L99VR01J)* ; *Section 2.4 Electrical characteristics curves..*
22-Aug-2022	3	Updated *Section Features in cover page.* Updated *Table 3. Operation junction temperature.* Updated *Section 4.11 Functional safety management.* Updated *Table 6. Fast output discharge.* Updated *Table 7. Reset.* Updated *Table 11. Thermal warning and protection (only for L99VR01J).* Updated *Figure 45. Rthj-amb vs PCB copper area in open box free air condition (PowerSSO-12).*
09-Feb-2024	4	Updated Features and Description on cover page. Updated Table 1. Pins description and Table 2. Absolute maximum ratings. Removed "Table 8: Watchdog (only for L99VR01J)" Updated Table 2. Absolute maximum ratings. Updated Section 2.4: Electrical characteristics curves. Updated Figure 25. Load regulation test circuit , Figure 27. Application schematic, Figure 28. Application schematic – Post regulation, Figure 31. Example of output voltage selection and Figure 32. Typical example of enable control. Updated Section 4.5: Reset. Removed "Section: Autonomous watchdog". Updated Section 4.6: Thermal warning and thermal shutdown. Updated Section 5: Application. Updated Section 8: Order codes. Minor text changes.

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