L99SP08

Datasheet

Smart octal P-channel for ultra-low current consumption automotive systems

QFN 5x5x0.9 mm 32+4L WF
(with bottom side exposed pad)

Product summary	
Order code	L99SP08TR
Package	QFN 5x5x0.9 mm 32+4L wettable flanks
Packing	Tape and reel

Features

Maximum transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	28 V
Standby ON current (max.)	I_{VCC_Q}	48 µA
SPI I/O supply voltage	V_{DD}	3 V to 5.5 V
SPI standby ON current (max.)	I_{VDD_Q}	5 µA

- AEC-Q100 qualified
- 8x P-channel with R_{ON} = 1 Ω
- Ultra low current consumption:
  - 0 µA in deep standby mode
  - 6 µA in standby on mode per channel
- 4x direct inputs to control channels status in limp-home mode
- 24-bit ST-SPI interface for device full configurability and standalone operation
- Limp-home mode set by dedicated pin
- Integrated ADC block to monitor:
  - Outputs current in on state (both in normal and fail-safe mode)
  - Battery and output voltages in both on and off state (in normal mode)
  - Device junction temperature (T_J) in both on and off state
- Dual range ADC for current sensing
- 500 mA minimum peak current (per channel) to avoid undesired main switch triggering due to inrush transient current (microcontroller peripherals polling, contact monitoring…)
- Built in self test (BIST), actionable on demand, to monitor correct device behavior during its working life:
  - Current ADC
  - Voltage ADC
  - Standby on current sense chain
  - P-channel stuck-on protection
- Non-volatile memory (NVM) to configure current thresholds (I_{THRx}) automatically to exit standby ON state - two few times programmable (FTP) bits per channel
- Capacitive charging mode (CCM) in normal operation
- Protection–whose triggering generates main switch enable:
  - Overtemperature shutdown (latch-off)
  - Current shutdown (based on VDS monitoring)
- Integrated ESD protection
- QFN 5x5x0.9 mm 32+4L package with wettable flanks
- Compliant with European directive 2002/95/EC

Description

The L99SP08 Smart P-channel is an octa channel device made using STMicroelectronics BCD9sL technology, housed in a small QFN 5x5x0.9 mm 32+4L wettable flanks package. It is designed to support standby on functionality, when interacting with hybrid and monolitich STi²Fuse product family, as well as to drive loads in standalone mode, up to I_{OUTX} DC current per channel.

Integrating a deep standby mode, the device fulfills highly stringent requirements for all those always active battery lines, providing ultra-low current consumption with the car in parking mode.

Real time diagnostic is available through the SPI bus (communication error, oscillator stuck, overtemperature, V_{CC} and V_{OUT} monitoring). In case of overtemperature, VDS overvoltage or I_{PEAK} triggering, the device sets high EN pin, allowing the turn on of external devices, like STi²Fuse hybrid and monolithic devices (for further information on the usage of the L99SP08 in combination with the hybrid and monolithic STi2Fuse devices for parking mode functionality refer to the related application notes AN6025 and AN6371).

Built-in self-tests (BIST) are integrated to check the correct behavior of the device during its working life, allowing customer on demand activation, testing current ADC, voltage ADC, standby on current sense chain and P-channel stuck-on protection.

The device is also equipped with a nonvolatile memory (NVM) to allow the customer to set current thresholds (I_{THRx}) parameters, managing the standby on exit strategy.

Limp-home mode is enabled in case of reset of watchdog monitoring time-out event or LH (limp-home) pin is set to high. In this state each output is controlled by dedicated direct inputs (DIx).

1 Block diagram and pin description

Figure 1. **Block diagram**

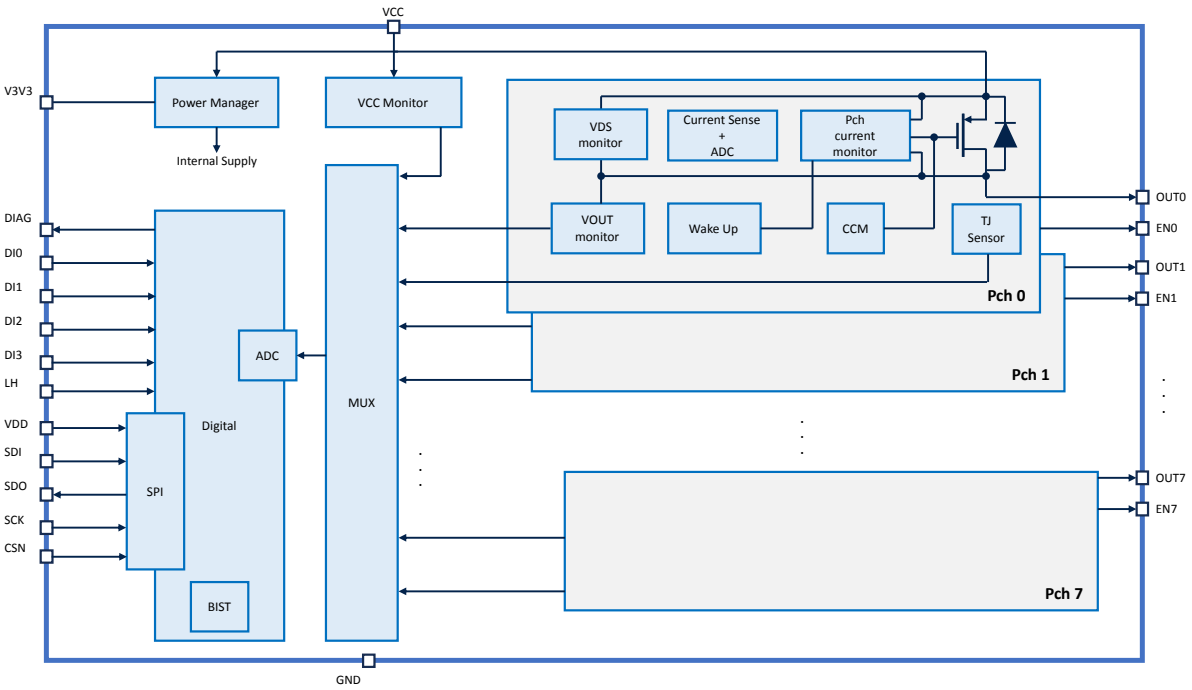
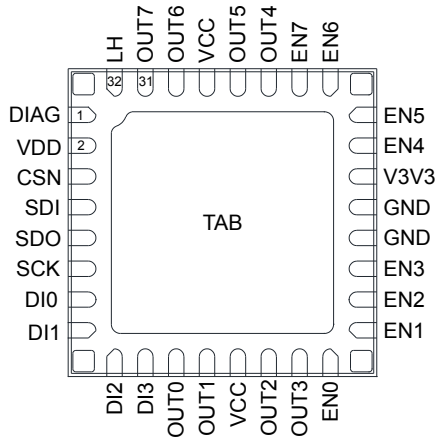


Figure 2. Device pin connection diagram (top through view - not in scale)



Note: the corner leads are electrically connected to the TAB. Those pins are intended for thermo-mechanical purpose only. They have to be soldered, but must be electrically isolated at PCB level.

Table 1. Pin functions

Name	Function
VCC	Input supply pin. Connect to the 12 V battery voltage
DIx	4 direct inputs for fail-safe operation
ENx	Open drain logic outputs, active high. 8 enable pins (1 per channel)
OUTx	8 output pins (1 per channel)
GND	Ground connection
VDD	DC supply input for the SPI interface. 3.3 V and 5 V compatible
V3V3	Output of the 3.3 V internal LDO voltage regulator (logic and I/O supply) Connect a low ESR capacitor (1 µF) close to this pin
CSN	Chip select not (active low) for SPI communication. It is the selection pin of the device. CMOS compatible input
SDO	Serial data output for SPI communication. Data is transferred serially out of the device on SCK falling edge
SDI	Serial data input for SPI communication. Data is transferred serially into the device on SCK rising edge
SCK	Serial clock for SPI communication. It is a CMOS compatible input
DIAG	Open drain logic output, active low. Diagnostic feedback
LH	Active high input pin compatible with 3 V and 5 V CMOS; it activates limp-home mode
TAB	Pin connected to internal ground through high resistive path. To be connect to GND

2 Electrical specification

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.3 to 40	V
I_{GND}	DC reverse ground pin current	10	mA
V_{DD}	DC input voltage	-0.3 to 6.5	V
V_{SDO}	SPI pins DC input voltage	-0.3 to V_{DD}	V
V_{3V3}	DC output voltage	-0.3 to 4.6	V
V_{CSN}, V_{SDI}, V_{SCK},	SPI pins DC input voltage	-0.3 to 6.5	V
V_{LH}	DC input voltage	-0.3 to 40	V
V_{DIAG}	DC output voltage	-0.3 to V_{3v3}	V
I_{DIAG}	DC input current	10	mA
V_{OUTx}	DC output voltage	(V_{CC} - 45) to V_{CC}	V
V_{DIx}	DC input voltage	-0.3 to 40	V
V_{ENx}	DC input voltage	-0.3 to V_{3V3}	V
I_{ENx}	DC input current	-10	mA
VESD	Electrostatic discharge (JEDEC 22A-114F) local pin	±2000	V
	Electrostatic discharge (JEDEC 22A-114F) global pin	±4000	V
	Charge device model (CDM-AEC-Q100-011) corner pin	±750	V
	Charge device model (CDM-AEC-Q100-011) all pin	±500	V
T_J	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	
N_{FTP}	Number of FTP writing cycles	1000	Cycles

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Typ. value	Unit
R_{thJA}	Thermal resistance, junction-to-ambient (JEDEC JESD 51-2) (1)	25.5	°C/W

1. *Device mounted on four-layer 2s2p PCB.*

2.3 Main electrical characteristics

5 V < V_{CC} < 40 V; -40 °C < T_J < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 12 V; T_J = 25 °C, unless otherwise specified.

Table 4. Supply specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
1.1	V_{CC}	Operating supply voltage		5	12	28	V
1.2	V_{CC_EXT}	Extended operating supply voltage		3		40	V
1.3	V_{CC_USD}	Undervoltage shutdown		3.9			V
1.4	$V_{CC\_USD\_RES}$	Undervoltage shutdown reset				4.5	V
1.5	$V_{CC\_USD\_HYST}$	Undervoltage shutdown hysteresis			0.3		V
1.6	V_{CC_OV}	V_{CC} overvoltage	Normal or fail-safe mode	15.6	16	16.4	V
1.7	$V_{CC\_OV\_RES}$	V_{CC} overvoltage reset	Normal or fail-safe mode	14.7	15.4	16.1	V
1.8	$V_{CC\_OV\_HYST}$	V_{CC} overvoltage hysteresis	Normal or fail-safe mode		0.5		V
1.9	V_{DD}	SPI I/Os supply voltage		3		5.5	V
1.10	V_{DD_UV}	SPI I/Os undervoltage		1.5	1.7	1.9	V
1.11	$V_{DD\_UV\_RES}$	SPI I/Os undervoltage reset		1.7	2.1	2.3	V
1.12	$V_{DD\_UV\_HYST}$	SPI I/Os undervoltage hysteresis			0.4		V
1.13	V_{V3V3}	3.3 V output regulator	Normal or fail-safe mode	3.1	3.25	3.4	V
1.14	I_{VDD}	SPI supply current in normal mode	1 SPI frame (24-bit) at 1 MHz		1.5	3	mA
1.15	I_{VDD_Q}	SPI supply current in standby ON state		0.2	1	3	µA
1.16	I_{VCC_ON}	Supply current (includes logic)	V_{CC} = 12 V, I_{OUT} = 0A T_J = 130°C, Normal mode	11	12	13	mA
1.17	I_{VCC_Q}	V_{CC} quiescent current (not including I_{OUT} current)	V_{CC} = 12 V, all I_{OUT} ≤ 30 mA, V_{OUT} = V_{Batt},T_J = 25°C Standby ON mode		35	48	µA
			V_{CC} = 12 V, all I_{OUT} = 100 mA, T_J = 130°C, Standby on mode		1.25	1.8	mA
			V_{CC} = 12 V, Deep standby mode			1	µA
1.18	I_{OUTX}	DC output current per channel	V_{CC} = 12 V, T_A = 85 °C, All channel ON			300	mA
			V_{CC} = 12 V, T_A = 85 °C, One channel ON			500	mA
1.19	$V_{CC\_POR\_H}$	Power ON reset threshold. Device leaves the Reset mode. Supply of digital part is reset		2.4	2.5	2.7	V

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
1.20	$V_{CC\_POR\_L}$	Power ON shutdown threshold. Device enters Reset mode. Supply of digital part in shutdown		2.2	2.3	2.5	V
1.21	$V_{CC\_POR\_HYST}$	Power ON reset hysteresis			0.2		V
1.22	$V_{V3V3\_POR\_H}$	Power ON digital threshold. Device leaves the Standby ON mode. Digital part is waking up		2.7	2.85	3.0	V
1.23	$V_{V3V3\_POR\_L}$	Shutdown digital threshold. Device enters in Standby ON mode. Digital part is frozen		2.4	2.5	2.65	V
1.24	$V_{V3V3\_POR\_HYST}$	Digital part wake up hysteresis			0.3		V
1.25	$V_{POR\_LH\_H}$	Power-on wake-up threshold. Device leaves the deep standby state		2.2	2.5	2.8	V
1.26	$V_{POR\_LH\_L}$	Shutdown threshold. Device enters in deep standby state		2.0	2.3	2.6	V
1.27	$V_{POR\_LH\_HYST}$	Device wake-up hysteresis			0.2		V

Table 5. SPI logic inputs (CSN, SCK and SDI) specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
2.1	I_{IL_CSN}	Low level Input current CSN PAD	CSN = 1.5 V	-5	-2.5	-1	µA
2.2	I_{IH_CSN}	High level Input current in CSN PAD	CSN = 2.31 V	-15	-10	-5	µA
2.3	$I_{IH\_SCK, SDI}$	High level input current SCK, SDI PAD	SCK, SDI = 2.31 V	-15	-5	-1	µA
2.4	$I_{IL\_SCK, SDI}$	Low level input current SCK, SDI PAD	SCK, SDI = 1.5 V	1	2.5	5	µA
2.5	V_{IL}	Low level Input voltage				1.35	V
2.6	V_{IH}	High level input voltage		2.3			V
2.7	V_{I_HYST}	Input hysteresis voltage			0.4		V

Table 6. SPI logic outputs (SDO) specification

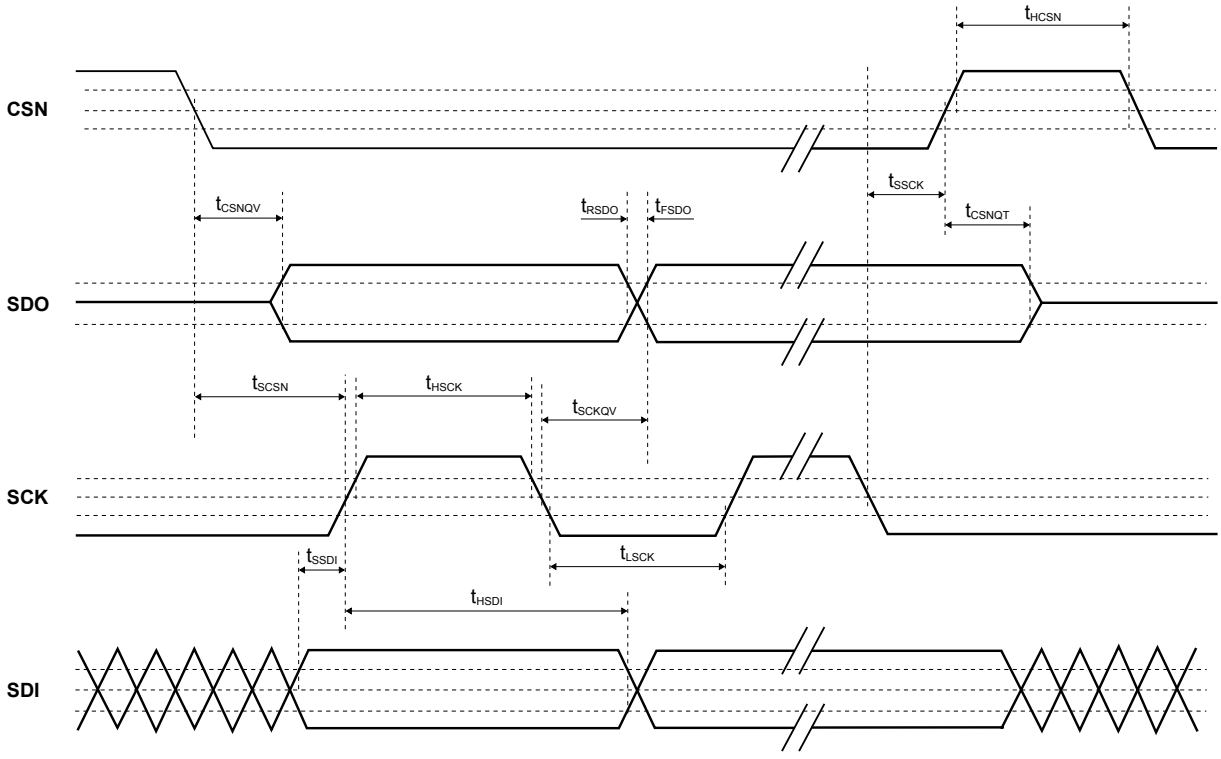
ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
3.1	V_{OL}	Low level output voltage				$0.2*V_{DD}$	V
3.2	V_{OH}	High level output voltage		$0.8*V_{DD}$			V
3.3	I_{LO}	Output leakage current				1	µA

Table 7. SPI timing specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
4.1	f_{SCK}	SPI clock frequency		-	-	8	MHz
4.2	t_{HSCK}	SCK high time		55	-	-	ns
4.3	t_{LSCK}	SCK low time		55	-	-	ns
4.4	t_{HCSN}	CSN high time		1	-	-	µs
4.5	t_{SCSN}	CSN setup time–CSN low before SCK rising edge		100	-	-	ns
4.6	t_{SSCK}	SCK setup time–SCK low before CSN rising edge		100	-	-	ns

ID	Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
4.7	t_{SSDI}	SDI setup time before SCK rising edge			25	-	-	ns
4.8	t_{HSDI}	SDI hold time			20	-	-	ns
4.9	t_{CSNQV}	CSN falling edge until SDO valid			-	-	70	ns
4.10	t_{CSNQT}	CSN rising edge until SDO tristate			-	220	-	ns
4.11	t_{SCKQV}	SCK falling edge until SDO valid			-	-	50	ns
4.12	t_{RSDO}	SDO rise time			-	-	25	ns
4.13	t_{FSDO}	SDO fall time			-	-	25	ns
4.14	t_{WHCH}	CSN low timeout			-10%	50	+10%	ms
4.15	t_{WDTB}	Watchdog toggle bit timeout	WD_TIME configuration:	00	-10%	50	+10%	ms
				01		100		
				10		150		
				11	Disabled			-

Figure 3. SPI dynamic characteristics



t_{HCSN} : CSN high time
t_{CSNQV} : CSN falling until SDO valid
t_{RSDO} : SDO fall time
t_{FSDO} : SDO rise time
t_{SSCK} : SCK setup time before CSN rising
t_{CSNQT} : CSN rising until SDO tristate
t_{SCSN} : CSN setup time before SCK rising
t_{HSCK} : SCK high time
t_{SCKQV} : SCK falling until SDO valid
t_{SSDI} : SDI setup time before SCK rising
t_{HSDI} : SDI hold time
t_{LSCK} : SCK low time

Table 8. ENx pin specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
5.1	V_{ENx_PU}	Channel x enable pin - pull up voltage		3			V
5.2	I_{ENx_CC}	Channel x enable pin – current capability	V_{ENX} = V_{ENx_PU}			300	µA
5.3	I_{ENx_LEAK}	Channel x enable pin - leakage current				1	µA

Table 9. DIx pin specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
6.1	I_{IL}	Low level Input current	DIx = 1.5 V	1	2.5	5	µA
6.2	I_{IH}	High level Input current	DIx = 2.31 V	-10	-5	-1	µA
6.3	V_{IL}	Low level input voltage				1.35	V
6.4	V_{IH}	High level input voltage		2.3			V
6.5	V_{I_HYST}	Input hysteresis voltage			0.4		V

Table 10. Digital timings specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
7.1	f_C	Clock frequency	Dithering configuration = 000 (see Table 20)	19	20	21	MHz
7.2	t_{WHCH}	CSN low timeout	Covered by SCAN		50		ms
7.3	t_{STBY_OUT}	Minimum time during which CSN must be low or LH must be high to exit Standby ON mode		1	5	10	µs
7.4	t_{STBY_IN}	Minimum time during which CSN must be high and LH must be low to go to Standby ON mode	Covered by SCAN		14		ms
7.5	$t_{STARTUP}$	Startup time from initialization to Standby ON	V_{CC} > $V_{CC\_POR\_H}$, V3V3 external cap. = 1 µF, LH > $V_{POR\_LH\_H}$			1.2	ms
7.6	$t_{STBY\_LOW\_to\_MID}$	Transition time from Standby ON low to high consumption	I_{OUT} > $I_{STBYON\_TH\_H}$	150	300	550	µs
7.7	$t_{STBY\_LOW\_to\_FS}$	Transition time from Standby ON low consumption to fail-safe	V3V3 external cap. = 1 µF, (I_{OUT} > I_{Peak} OR I_{OUT} < $I_{STDBY\_ON\_TH\_H}$) OR (LH “high” OR CSN “low” OR VDS_OV “high”)	150	350	550	µs
7.8	$t_{STBY\_MID\_to\_FS}$	Transition time from Standby ON high consumption to fail-safe	V3V3 external cap. = 1 µF, (I_{OUT} > I_{Peak} OR I_{OUT} > $I_{STDBY\_ON\_TH\_H}$) OR	10	25	40	µs

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
7.8	$t_{STBY\_MID\_to\_FS}$	Transition time from Standby ON high consumption to fail-safe	(LH “high” OR CSN “low” OR TSD “high”)				µs
			V3V3 external cap. = 1 µF, (I_{OUT} > I_{Peak} OR I_{OUT} > $I_{STDBY\_ON\_TH\_H}$) OR (LH “high” OR CSN “low” OR TSD “high”) AND V3V3 > V3V3_POR_H	0.1	0.5	1	
7.9	t_{MAX}	Digital counter to manage the standby ON exit strategy		0		255	ms
7.10	t_{NVM_READ}		Covered by SCAN	30			µs
7.11	t_{NVM_WRITE}		Covered by SCAN	10			ms
7.12	t_{ENhigh}	ENx delay from fault rise time	Standby ON - low consumption mode, no exsternal resistive load on ENx pin	3		5	µs
			All states except standby ON - low consumption mode, no exsternal resistive load on ENx pin	0.05		1	

Table 11. LH logic input pin specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
8.1	I_{IL}	Low level Input current	V_{IL} = 1.5 V	1			µA
8.2	I_{IH}	High level Input current	V_{IH} = 2.31 V			15	µA
8.3	V_{IL}	Low level Input voltage				1.5	V
8.4	V_{IH}	High level input voltage		2.31			V
8.5	V_{I_HYST}	Input hysteresis voltage			0.4		V
8.6	t_{LH}	LH filtering time			32		µs

Table 12. DIAG logic output pin specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
9.1	V_{DIAG_PD}	DIAG pin pull down voltage	I_{DIAG_PD} = 1mA		-	0.25	V
9.2	I_{DIAG_PD}	DIAG pin input current	V_{DIAG} = V_{DIAG_PD}		-	1	mA
9.3	I_{DIAG_LEAK}	DIAG pin leakage current	V_{DIAG} = V3V3	0	-	1	µA

Table 13. Thermal specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
10.1	T_{TSD}	Junction temperature thermal shutdown threshold		160	175	190	°C

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
10.2	T_{TSD_HYS}	Junction temperature thermal shutdown hysteresis			15		°C
10.3	T_W	Junction temperature thermal warning threshold			140		

Table 14. Current sense amplifier with integrated ADC

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
11.1	ADC_{RES_IOUTx}	ADC resolution			10		bit
11.2	$ADC_{REFRESH\_RATE\_IOUTx}$	ADC refresh rate			3.3		µs
11.3	ADC_{FS}	ADC full scale for I_{OUTx}			0.55		A
11.4	ADC_{STEP_IOUTx}	ADC step for I_{OUTx}			0.55/ 1023		A
11.5	ADC_FS_DIAG	ADC full scale for I_{OUTx} in leak mode			37		mA
11.6	ADC_STEP_DIAG	ADC step for I_{OUTx} in leak mode			37/ 1023		mA
11.7	$C_{S\_PRECISION}$	Digital current sense accuracy	0.04 A ≤ I_{OUT} < 0.1 A	-20		20	%
			0.1 A ≤ I_{OUT} < 0.2 A	-10		10	%
			0.2 A ≤ I_{OUT} < 0.5 A	-5		+5	%
11.8	$C_{S\_PRECISION\_DIAG}$		1 mA < I_{OUT} < 5 mA	-35		35	%
			5 mA ≤ I_{OUT} < 10 mA	-10		10	%
			10 mA ≤ I_{OUT} < 37 mA	-8		8	%

Table 15. P-channel bypass switch specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
12.1	$V_{DS\_BYPASS\_SAT}$	Bypass switch V_{DS} saturation protection threshold		0.4		1.2	V
12.2	R_{ON}	Internal bypass resistance	T_J = 25°C	0.7	1	1.3	Ω
12.3	$R_{ON\_STBY\_LC}$	Internal bypass resistance in Standby ON low consumption	T_J = 25°C	7	14	16	Ω
12.4	$I_{STBYON\_TH\_H}$	Current threshold for transition from Standby ON low to high consumption	V_S - V_{OUT} = $V_{DS\_BYPASS\_SAT}$, Standby ON low consumption	30		85	mA
12.5	I_{PEAK_STBY}	Peak current	Standby on state, T_J = -40 °C	0.8		1.2	A
			Standby on state, T_J = 25 °C	0.6		0.9	
			Standby on state, T_J = 130 °C	0.5		0.7	
12.6	$I_{STBYON\_TH\_L}$	Output current to go in Standby ON low consumption state		8	15	25	mA
12.7	I_{THRx}	Output current threshold		-10%	100	10%	mA

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
12.7	I_{THRx}	Output current threshold		-10%	200	10%	mA
				-10%	300	10%	
				-10%	400	10%	
12.8	I_{PEAK}	Peak current in normal or fail-safe mode	Normal or fail-safe mode	-5%	500	5%	mA

Table 16. Overvoltage specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
13.1	$V_{DS\_OV\_L}$	Drain-source overvoltage threshold-rising edge of V_{OUT}		1.3	1.4	1.5	V
13.2	$V_{DS\_OV\_H}$	Drain-source overvoltage threshold-falling edge of V_{OUT}		1.9	2.1	2.3	V
13.3	V_{DSOV_HYST}				700		mV

Table 17. Capacitive Charging Mode (CCM) Specification

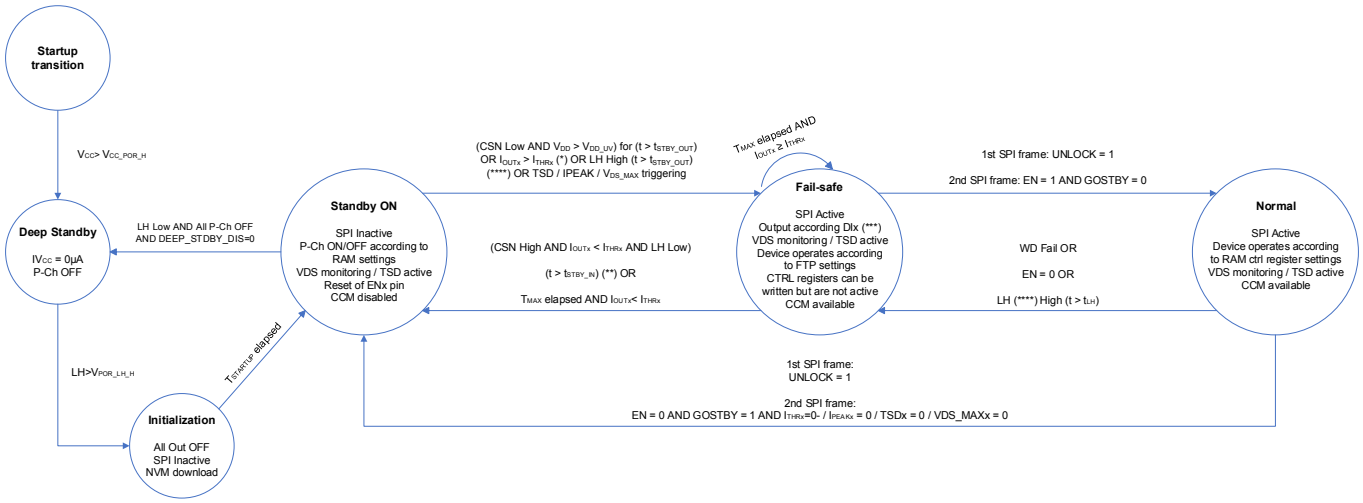
ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S = 12 V; -40°C < T_J < 150°C, unless otherwise specified							
14.1	I_{OUT_CCM}	Output current in CCM	V_{OUT} = 0 V	12	20	25	mA
14.2	t_{CCM}	Time to charge OUT voltage to V_{CC}	C_{OUT} = 180 µF, V_{CC} = 16V			200	ms

Table 18. Voltage and temperature monitoring with integrated ADC

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC} = 13 V; -40°C < T_J < 150°C, unless otherwise specified							
15.1	ADC_{RES}	ADC resolution			10		bit
15.2	$ADC_{REFRESH\_RATE}$	ADC refresh rate			47.6		µs
15.3	ADC_{FS_VOUTx}	ADC full scale for V_{OUTx}			25		V
15.4	ADC_{STEP_VOUTx}	ADC step for V_{OUTx}			24.5		mV
15.5	ADC_{FS_Vcc}	ADC full scale for V_{CC}			25		V
15.6	ADC_{STEP_Vcc}	ADC step for V_{CC}			24.5		mV
15.7	ADC_{FS_Tjx}	ADC full scale for T_{J_X}			2.5		V
15.8	ADC_{STEP_Tjx}	ADC step for T_{J_X}			2.45		mV
15.9	$ADC_{ACCURACY}$	ADC reading accuracy	$V_{OUTx} \geq 1.5V$ $V_{CC} \geq V_{CC\_POR\_L}$	-5		5	%

3 Functional description

Figure 4. Device state diagram



NOTES:

(*) Only if transition from standby on to fail-safe is triggered by the following condition: $I_{THRx} < I_{OUTx} < I_{PEAK}$, then T_{MAX} timer is enabled.
(**) t_{STBY_IN} timer is reset if T_{MAX} timer is enabled.
(***) Output according to OUT_CTRL if T_{MAX} time is enabled.
(****) If NVM bit DEEP_STDBY_DIS = 1, the contribution of LH signal to this transition of the device FSM is disabled.

3.1 Operating modes

The L99SP08 features different operating modes:

- Deep standby on mode
- Standby on mode
- Normal mode
- Fail-safe mode

Nevertheless, there is a transition startup phase which is not an operation mode for the device.

When the voltage on VCC pin exceeds the power on or reset threshold ($V_{CC\_POR\_H}$) and LH > $V_{POR\_LH\_H}$, the device enters in the initialization phase, during which:

- the FTP registers values are downloaded into corresponding RAM registers
- the internal bypass switches are OFF

The transition to standby ON state is triggered after the end of FTP download ($t_{STARTUP}$).

Table 19. Operating modes

Operating mode	Entering conditions	Leaving conditions	Characteristics
Startup transition (Not considered as an operating mode)		Deep Standby: V_{CC} > 0	
Deep standby mode	Startup transition: V_{CC} > 0	Initialization: LH > $V_{POR\_LH\_H}$	• Outputs: off • SPI: inactive • Diagnostics: not available • IV_{CC} = 0 µA
	Standby on: LH low AND all P-channel off AND DEEP_STDBY_DIS = 0		
Initialization (Not considered as an operating mode)	Deep Standby: LH > $V_{POR\_LH\_H}$	Standby on: T_{STARUP} elapsed	• Outputs: off • SPI: inactive • NVM download
Standby ON mode	Initialization: $T_{STARTUP}$ elapsed	Deep standby: LH low AND all P-channel off AND DEEP_STDBY_DIS = 0	• SPI: inactive • P-channel on/off according to RAM settings • VDS monitoring/TSD active • Reset of ENx pin • CCM disabled
	Fail-safe: (CSN high AND I_{OUTx} < I_{THRx} and LH low) (t > t_{STBY_IN}) (**) OR T_{MAX} elapsed AND I_{OUTx} < I_{THRx}		
	Normal: 1st SPI frame: UNLOCK = 1 2nd SPI frame: EN = 0 AND GOSTBY = 1 AND I_{THRx}= 0- / IPEAKx = 0 / TSDx = 0 / VDS_MAXx = 0	Fail-safe: CSN low (t > t_{STBY_OUT}) OR I_{OUTx} > I_{THRx} (*) OR LH high (t > t_{STBY_OUT}) (****) OR TSD / IPEAK / VDS_MAX triggering	
Fail-safe	Standby on: CSN Low (t > t_{STBY_OUT}) OR I_{OUTx} > I_{THRx} (*) OR LH High (t > t_{STBY_OUT}) (****) OR TSD/IPEAK/VDS_MAX triggering	Standby on: (CSN High AND I_{OUTx} < I_{THRx} and LH Low) (t > t_{STBY_IN}) (**) OR T_{MAX} elapsed AND I_{OUTx}<I_{THRx}	• SPI: inactive • Output according to DIx (***) • VDS monitoring/TSD active • Device operates according to FTP settings • CTRL registers can be written but are not active • CCM available • Reset =1 after SW reset
	Normal: WD fail OR EN = 0 OR LH(****) high (t > t_{LH})	Normal: 1st SPI frame: UNLOCK = 1 2nd SPI frame: EN = 1 AND GOSTBY = 0	
Normal	Fail-safe: 1st SPI frame: UNLOCK = 1 2nd SPI frame: EN = 1 AND GOSTBY = 0	Standby on: 1st SPI frame: UNLOCK=1 2nd SPI frame: EN = 0 AND GOSTBY = 1 AND I_{THRx}=0- / IPEAKx = 0 / TSDx = 0 / VDS_MAXx = 0	• SPI Active • Device operates according to RAM CTRL register settings • VDS monitoring/TSD active • CCM available
		Fail-safe: WD fail OR EN = 0 OR LH(****) high (t > t_{LH})	

3.1.1 Deep standby mode

The deep standby mode is a state with the following characteristics:

- The device consumption is below 1 µA;
- NO SPI response;
- NO device features are available;

The device enters this state:

- From startup:
  $V_{CC} > V_{CCPOR\_H}$
- From standby ON:
  LH < $V_{POR\_LH\_L}$ AND (ALL P-Channel OFF) AND (DEEP_STDBY_DIS = 0)

The device leaves this state:

- LH > $V_{POR\_LH\_H}$ for t > 600 µs

If LH is maintained > $V_{POR\_LH\_H}$ for t > $T_{startup}$ the device enters automatically in fail-safe.

3.1.2 Standby on mode

The L99SP08 device features a standby on operation mode, with the following characteristics:

- The SPI interface is inactive–the digital part is supplied (but the clock is off) and the registers are frozen to the latest state;
- the bypass switches can be on or off depending on dedicated BIT on control register CR3 "Output control Register";
- The capacitive charging mode is disabled;
- The bypass drain-source voltage and the junction temperature are monitored to ensure the device protected while keeping the lowest current consumption from the supply voltage.

The device enters this state:

- From initialization phase, after the FTP download (and within $t_{STARTUP}$ timing);
- From normal mode by sending two dedicated SPI frames (see Figure 4):
  - First SPI frame: 02x0009
  - Second SPI frame: 01x8001
- From fail-safe when:
  - CSN goes high for t> t_{STBY_IN} AND
  - I_{OUTX} < I_{THRX} (for all the output currents) AND
  - LH goes low for t> t_{STBY_IN}

The standby ON exit strategy is deeply described in the Section 3.2: Standby on state exit strategy.

3.1.3 Fail-safe mode

The device enters the fail-safe operation from standby ON if:

- If CSN goes low for a time t> t_{STBY_OUT} OR
- If I_{OUTX}>I_{THRX} (it is enough the current of one channel only is higher than its configured threshold) OR
- If LH goes high a time t> t_{STBY_OUT} AND DEEP_STDBY_DIS = 1 OR
- If a fault occurs in at least one channel:
  - Goes in thermal shutdown (TSDx is triggered)
  - The drain-source voltage of the P-channel bypass is exceeding a fixed threshold (V_{DSMAXx} is triggered)
  - The output current overcome the Ipeak fixed threshold (I_{PEAKx} is triggered)

When the device enters from standby ON to fail-safe mode, the DIAG goes down for 1 ms. In case of transition triggered from a fault the DIAG is latched down.

The device enters the fail-safe operation from normal mode when:

- WD_FAIL bit set (the microcontroller connection is lost, and the watchdog is not anymore served) OR
- EN bit is set to 0, OR

- LH pin is set in high state.

The fail-safe state characteristics are:

- SPI active - with control registers locked and values corresponding to the latest ones;
- Capacitive charging mode enabled;
- Bypass switches handled according to the direct inputs (4x DIx);
- Diagnostic active.

3.1.4 Normal mode

The device enters the normal operation, only from fail-safe, through two dedicated SPI frames (see Figure 4):

- First SPI frame: 02x0009
- Second SPI frame: 01x4001

The characteristics of the normal mode are:

- SPI active (until the watchdog, regularly toggled, is served);
- Capacitive charging mode is enabled;
- Bypass switches handled according to the values stored in the dedicated registers or to the direct inputs (4x DI_x in total);
- Diagnostic active.

If NVM bit DEEP_STDBY_DIS = 0, the L99SP08 leaves the normal mode to enter the fail-safe under the following conditions:

- WD_FAIL bit set (the microcontroller connection is lost, and the watchdog is not anymore served) OR
- EN bit is set to 0, OR
- LH pin is set in high state.

The normal mode leaving conditions to enter the standby ON state are managed by sending two dedicated SPI frames (see Figure 4).

3.2 Standby on state exit strategy

The standby on is a key state for the L99SP08. This section is dedicated to the strategy implemented to leave this device operation.

The standby on is the state during which the L99SP08 delivers the required current to the outputs.

The key requirement in this phase is to minimize the current consumption from the supply voltage. Then, this state can be split in two sub states, depending on the IOUTx values (see Figure 5): the first one with a very low consumption (see I_{VCC_Q}); the second one, with medium consumption (see I_{VCC_Q}).

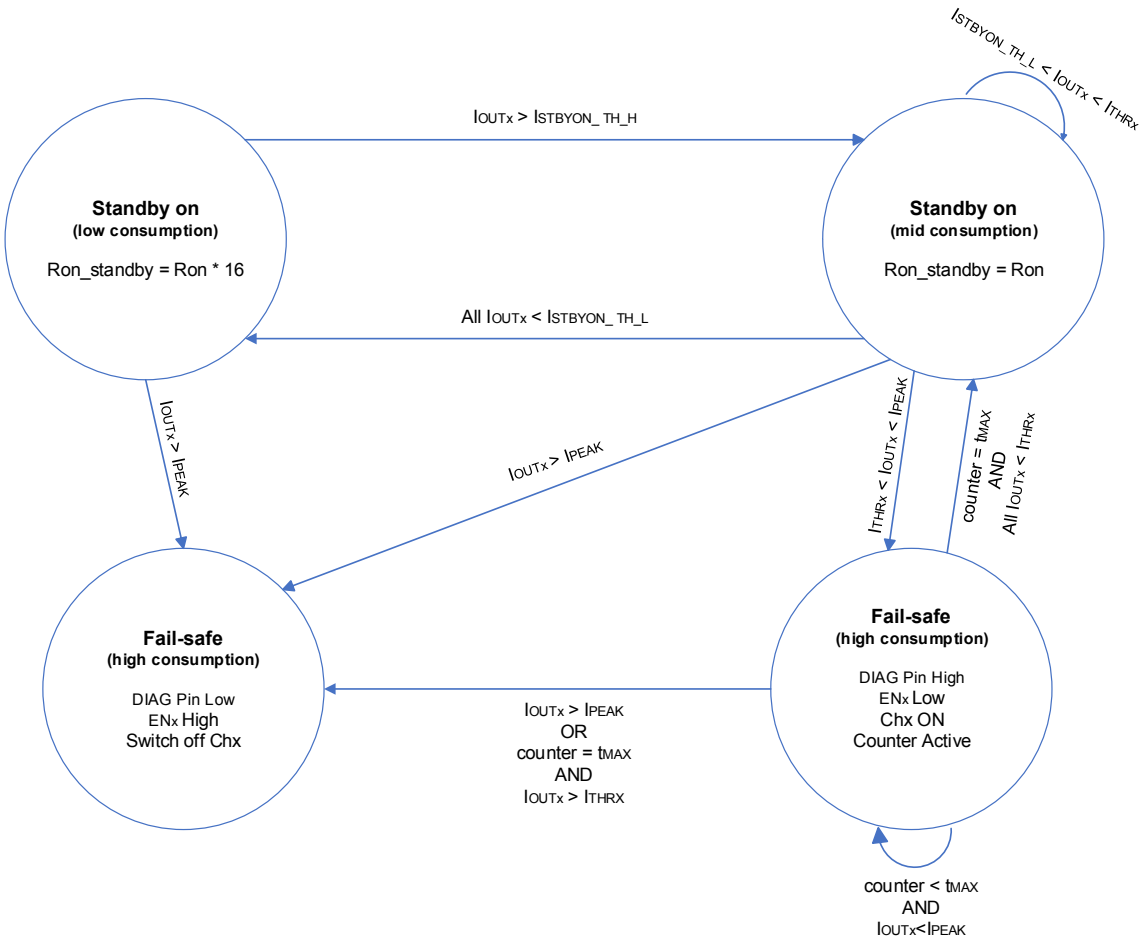
The transition between these two phases, is handled according to the current required by the output: if below than $I_{STBYON\_TH\_L}$, the device is in low consumption sub state, then if the current is above than $I_{STBYON\_TH\_H}$, the device moves to standby on high consumption sub state.

The L99SP08 leaves the standby on state when the channel output current is exceeding the configurable threshold (per channel) I_{THRx}.

In that case, the device goes in fail-safe and a digital counter starts counting until a configurable t_{MAX} timing. When the programmed t_{MAX} is reached, the L99SP08 compares the output current I_{OUTx} against the I_{THRx} threshold:

- If the output current I_{OUTx} is higher than the threshold I_{THRx}, the enable pin (ENx) of the channel x is raised, and the relative P-channel is switched OFF. Meanwhile, the DIAG pin is pulled down;
- If the output current I_{OUTx} is lower than the threshold I_{THRx}: the channel x come back to standby on state (see Figure 5).

Figure 5. **Standby on exit strategy**



3.3 Channel enable (ENx) pin behavior

The L99SP08 features one EN pin per channel. These are open drain outputs active high.

They are used to wake up or enable external devices, like the STi²Fuse hybrid and monolithic devices.

The ENx pin is raised in case of at least one of the following trigger condition is verified:

- $I_{OUTx} > I_{PEAK}$
- TSD_x is triggered
- $V_{DSx} > V_{DS\_OV}$
- $I_{OUTx} > I_{THRx}$ AND t_{MAX} expired

The L99SP08 implements the possibility to drive, during normal mode operation, the ENx through control register (CR8 "Direct External EN Control Register") even if the cases mentioned above are not triggered.

On top of this, the device allows to configure the ENx pin through the NVM bits.

In standby mode:

- EN_CONF_STDBY
  [1]: ENx pin internally set to ENCTRL_STDBYx NVM bits (8 bits, one per channel), even if the trigger condition is not present.
  [0]: ENx pin depends on the trigger conditions previously listed.

In fail-safe mode:

- DIS_CONF_FS
  [0]: ENx pin internally set to the ENCTRL_FSx bits (8 bits, one per channel) in logical OR combination with the faults occurring on the channels.
  [1]: the ENCTRL_FSx bits are not acting

3.4 DIAG pin behavior

The L99SP08 has one diagnostic pin called DIAG. This is an open drain output active low, used to provide an information hard wire to the microcontroller. The DIAG pin is pulled down when the device goes from standby ON to fail-safe; the pin is pulled down for 1ms, then it is released in case anyone of the below listed fault is triggered:

- $I_{OUTx} > I_{PEAK}$
- TSD_X triggering
- $V_{DSx} > V_{DS\_OV}$
- $I_{OUTx} > I_{THRx}$ AND t_{MAX} expired

In normal mode, the fault is cleared through the SPI frame; while in fail-safe, the DIAG pin is released upon a falling edge on DIN (after a filtering time of 20 µs).

3.5 OUTPUT control in fail-safe mode

In fail-safe mode the OUTPUT channel driving depends on the DIx mapping (refer to the Section 5: DIx input management) and the two dedicated NVM registers (OUTCTRL and OUTCTRL_FS).

DIS_CONF_OUT_FS

[1]: OUTPUT pins depend on the OUTCTRL register content, while the content of OUTCTRL_FS and the DIx pin levels are ignored.

[0]: OUTPUT pins internally set to the logical OR combination of DIx pins and OUTCTRL_FS NVM bits.

3.6 Oscillator 20 MHz

The L99SP08 embeds a 20 MHz oscillator and a dithering block, for the relevant parameter of modulation, aimed to improve the EMC performances of the device.

There are three dedicated bits to program the desired frequency modulation and deviation to be applied (see Table 20).

Table 20. 20 MHz oscillator, dithering-modulation parameters

DITH_STEP [2:0]	N_STEP	Fosc_Mod [kHz]	Fosc_Dev [%]	Rejection [dB]
000 disable	0	0	0	0
001	8	156	1.6	-7.38
010	16	78	3.2	-11.68
011	24	52	4.8	-13.28
100	32	39	6.4	-14.58
101	40	32	8	-15.48
110	48	25	9.6	-16.28
111	56	22	11.2	-16.78

3.7 P-channel bypass

The L99SP08 embeds eight bypass switches, aimed to feed the load during standby ON state.

The switches are P-channel Power MOSFET, with an I_{PEAK} maximum current capability.

A dedicated driver controls each bypass switch, with zero current consumption in DC mode. The P-channel driver is put in high-Z when capacitive charging mode is enabled: in this latter case, a dedicated circuitry overtakes the gate control.

The device features the P-channel current monitoring in both standby ON state low and mid consumption.

3.7.1 Output current monitoring in standby ON low consumption mode

To keep the lowest current consumption from the battery, the current monitoring is performed through an analog current sense: this is used to manage the transition from standby ON low to mid consumption, occurring as soon as the output current exceeds the $I_{STBY\_ON\_TH\_H}$ threshold (see Figure 5).

When the device is in standby ON low consumption, the P-channel Ron is augmented at $R_{ON\_STBY\_LC}$.

When the output current I_{OUTx} overcomes the threshold $I_{STDBY\_ON\_TH\_H}$ (configurable via SPI), the bypass switch Ron is reduced to its typical value.

Finally, if the output current increases, exceeding the I_{PEAK}, the enable pin (ENx) is raising and the bypass switch is turned off.

3.7.2 Output current monitoring in standby ON mid consumption mode

In this case, the current monitoring is still performed through analog current sense but with higher accuracy. It is used to manage:

- The transition from standby ON mid consumption to fail-safe, occurring as soon as the output current of one channel (at least) exceeds the configured I_{THRx} threshold;
- The transition from standby ON mid to low consumption in the case of all the output current I_{OUTx} is lower than $I_{STBYON\_TH\_L}$.

A built-in self-test is implemented to check the whole P-channel monitoring circuitry. A dedicated bit per channel in the status register is set if the self-test is passed.

3.8 Bypass drain-source overvoltage

The L99SP08 features a regular monitoring of the drain-source voltage (V_{DS}) to avoid P-channel switches overheating. As soon as the V_{DSx} voltage overcomes the $V_{DS\_OV\_H}$ threshold, the enable pin (ENx) is forced high, and the relative channel x is switched off.

The $V_{DS\_OV\_H}$ threshold is a fixed value, far enough from the worst case conditions of the maximum current on the P-channel multiplied by its R_{on}.

3.9 ADC current sense

The device integrates eight 10-bit successive approximation register (SAR) analog-to-digital converters (ADCs) dedicated to current measurement. These ADCs provide digital information of the output current, which are stored in dedicated registers, 0x20 for Channel 0 to 0x27 for Channel 7, specifically in bits 13 to 4.

The update of the current sense registers is disabled when the corresponding channel is in the off state. Nevertheless, the device is capable of detecting potential malfunctions in the channels even when they are off, by employing alternative mechanisms based on the voltage measurement across the P-channels, as detailed in Section 3.11: Voltage ADC.

The ADC operates under both fail-safe and normal conditions. After each conversion, an update flag bit, UPDTIxSR, is set to indicate the availability of new conversion data. This bit is cleared following the reading of the corresponding RAM register.

$I_{OUTx} = ADC_{Xconv} * 550 / 1024$

In normal state, the ADC can be configured into a diagnostic mode by setting the bit CS_DIAGx in the control register of each channel. In this diagnostic mode, the ADC's full-scale range is scaled to ADC_FS_DIAG, enabling the measurement of output currents up to 1 mA.

$I_{OUTx} = ADC_{Xconv} * 37 / 1024$

3.10 Capacitive charging mode (CCM)

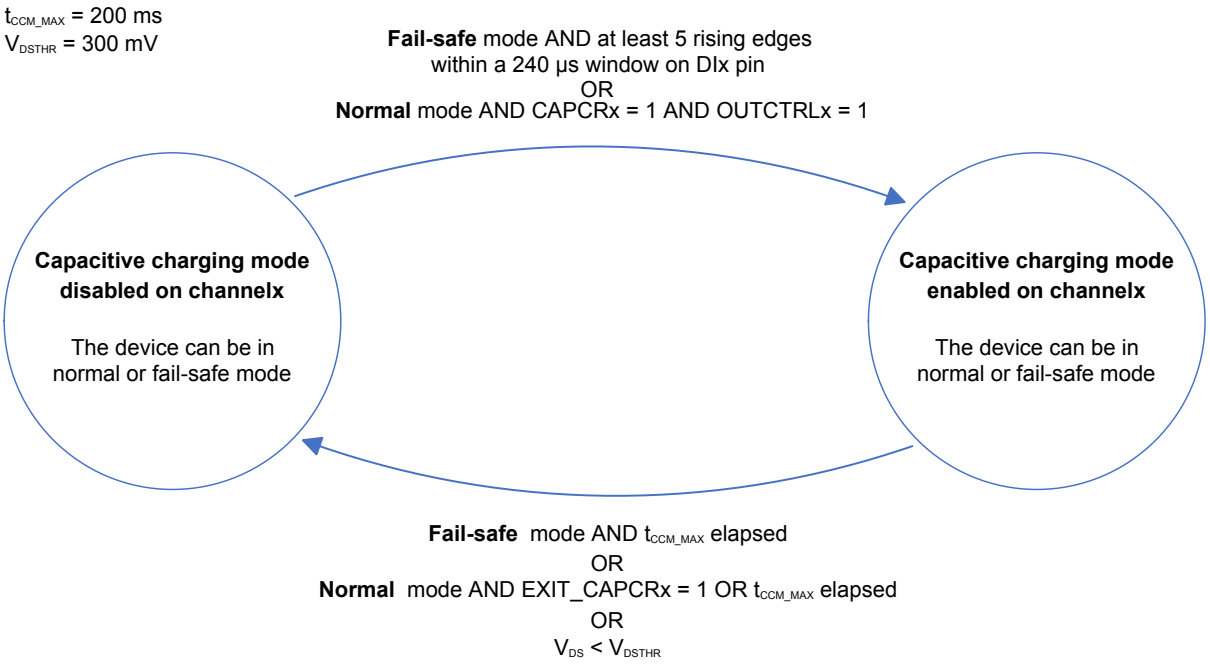
The capacitive charging mode (CCM) feature is used to precharge the output voltage to V_{CC} in case of a capacitive load is present. Thanks to this functionality, the turn on of the bypass switch with a capacitive load not leads to an inrush current through the P-channel, avoiding device potential switching off due to high dissipation and overheating, the CCM feature is disabled in case of V_{CCOV}.

The CCM is configured by means bit "CAPCRx" in the channels control register, moreover when the CCM is ended the P-channel driver could be left in generator current mode (CCM setting) or in ON/OFF mode depending on bit OUTCTRL.

Once CCM is configured the capacitive load is sustained by an I_{OUT_CCM} as per Table 17.

Hereafter the state diagram of CCM mode.

Figure 6. **CCM mode state diagram**



3.11 Voltage ADC

The device embeds one multiplexed voltage 10-bit successive approximation register (SAR) analog-to-digital converter. The parameters converted by the voltage ADC through MUX are: 8 V_{OUT} - 8 T_J - 1 V_{CC}. The conversion are stored in the dedicated registers (from 0x28 to 0x2F for VOUTxSR; from 0x30 to 0x37 for TJxSR and 0x38 for VCCSR).

The ADC works both in fail-safe and normal conditions, moreover both in channels ON or OFF, after each conversion, an updated bit "UPDTIxSR" is set to advise about the new conversion data. This bit is reset after the read process of the dedicated RAM register.

4 Protections and diagnostics

4.1 Oscillator stuck

The 20 MHz oscillator integrated in the L99SP08 implements a safety redundancy, consisting in a second oscillator activated by a dedicated IP that monitors any potential stuck of the main oscillator.

Then, the main oscillator stuck fault is used for functional safety: until the fault is not reached, the secondary oscillator is switched off; as soon as the main oscillator is in stuck, the second one is woken up (and the fault signal is sent to the digital part, in a dedicated status register SR1 bit[12]).

4.2 Bandgap stuck

The bandgap integrated in the L99SP08 implements a safety redundancy, consisting in a second bandgap activated by a dedicated IP that monitors any potential stuck low of the main bandgap.

Then, the main bandgap stuck fault is used for functional safety: until the fault is not reached, the secondary bandgap is switched off; as soon as the main bandgap is in stuck, the second one is woken up (and the fault signal is sent to the digital part, in a dedicated status register SR1 bit[13]).

4.3 Overtemperature

The device integrates eight thermal sensors, one per channel: each sensor is used to monitor the die junction temperature (T_J). The thermal sensors are positioned close to the P-channel (thermal sources).

Two thermal thresholds are implemented on the device:

- T_{Wx}, one per channel, it is a flag highlighted in the GSB just as warning for a temperature increasing. No action from the device in case of this threshold exceeding;
- T_{SDx}, one per channel, this is a thermal shutdown, the device will switch off the channel x related to the thermal sensor detecting the T_{SDx} event for safety reasons.

The T_J is converted through an ADC in Failsafe and Normal state, instead in standby ON condition, the output of the thermal sensor is compared with a fixed threshold (T_{SDx}, one per channel) for thermal shutdown.

In fail-safe or normal operations, the thermal sensor output is sent to the voltage ADC.

A dedicated bit in the channels status register from SR2 to SR5 bit[15:14] is set in case of fault.

The T_J ADC conversion is stored from SR30h to SR37h. The conversion formula is the following one:

$$\mathrm{TJ}[°\mathrm{C}] = -\frac{\frac{\mathrm{TJxSR}}{1023} * 2.5 - 2.136}{0.006} \quad (1)$$

4.4 Output and battery voltages monitoring

The L99SP08 embeds a voltage ADC used to monitor both the output voltage for each channel (V_{OUTx}) and the battery voltage at the VCC pin.

This monitoring is active only in fail-safe and normal mode operation, both channel on or off. It is disable in standby on to keep the lowest current consumption from the battery that is the key requirement in this standby on operation.

If the V_{CC} goes below V_{CC_USD}, will be flagged the VCC_undervoltage, a dedicated bit in the status register SR1 bit[10] is set in case of undervoltage of VCC and all the outputs will be switched off for safety reasons.

The V_{OUTx} ADC conversion is stored from SR28h to SR2Fh. The conversion formula is the following one:

$$\mathrm{VOUTx}[\mathrm{V}] = \frac{\mathrm{VOUTxSR}}{1023} * 25 \quad (2)$$

The V_{CC} ADC conversion is stored in SR38h. The conversion formula is the following one:

$$\mathrm{VCC}[\mathrm{V}] = \frac{\mathrm{VCCSR}}{1023} * 25 \quad (3)$$

4.5 Current sense standby on self-test

The self-test is intended to check the status of one of the most important chains of the device. The whole current sense chain of standby on can be tested through an on demand self-test and it is actionable by means TRIG_CS_TEST bit in the control register 0x02h.

The self-test configures the device with the lowest ITHR for each channel and simulates an output current of about 200 mA for 50 µs. So, during the self-test, the ITHR is overcome and the bit CSx_FAIL in SR8–CSBSR at address 0x17h is maintained low. In this way, the status of the internal chain of current sense in standby ON mid consumption is completely checked.

4.6 Output current leakage

A very low output current can be monitored through an on demand feature. The current ADC is set to have as maximum value of ADC_FS_DIAG with a step of ADC_STEP_DIAG. In this way the device can read an eventual leakage current on the output.

4.7 NVM FTP programming mode

The L99SP08 is equipped with a 2-kbit EEPROM, used also to store device configuration data. Part of this memory is managed by the customer. The device can operate in standalone mode (no microcontroller used) thanks to full configurability by FTPs. In application, the FTPs can be programmed (up to NFTP cycles) via the SPI interface–the device integrates a counter to take note about the FTP writing cycles [bits 9:0 of ROW 0].

The customer can write the data in the NVM following the steps described in the Figure 7.

The CRC field in the customer data map is used to read the 15th byte when a read operation is requested, while it doesn't care for a write operation (since the CRC will be automatically calculated and written into the NVM by the device itself).

In the NVM there are 15 rows. Row 0 (customer data map) is dedicated to user settings while the other 14 rows are ST restricted. Each row has 16 bytes. The 16th byte of each row contains the CRC calculated basing on the other 15 data bytes of the row. The polynomial is 0x7h.

The CRC check BIST is automatically launched after power-ON and the BIST results are stored in SR10-NVMCRCSR bits from 15 to 1 named NVMCRC[14:0]. For each row, the corresponding bit in this register is set to '1' if there was a CRC error during the download of NVM.

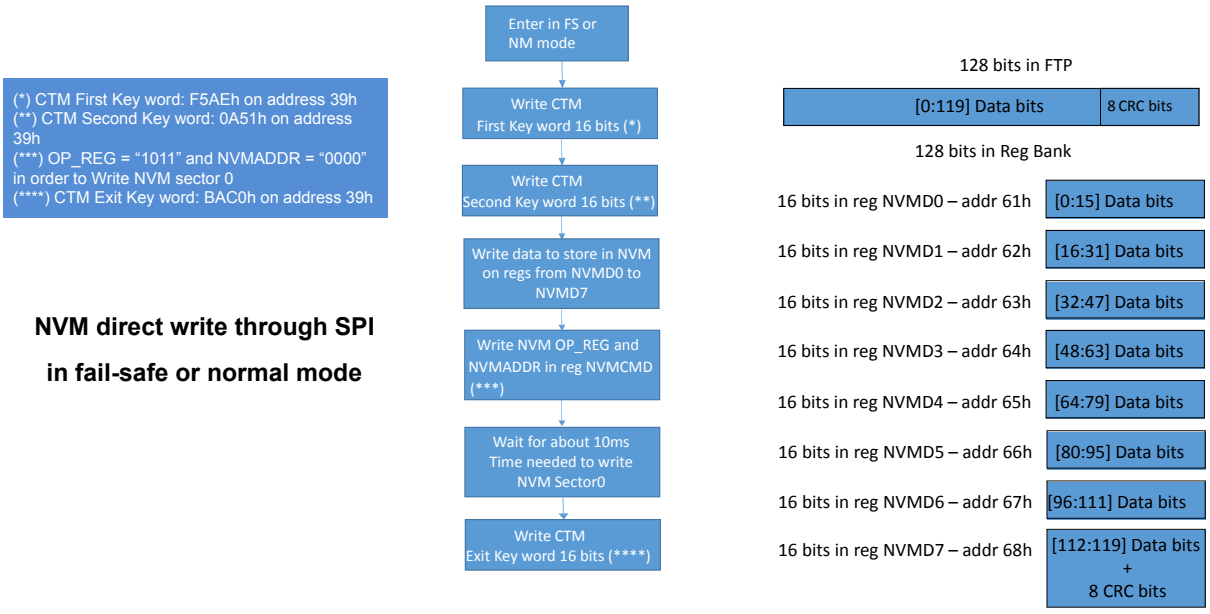
The "Shadow Register BIST" is an on-demand BIST and its execution can be launched through TRIG_NVMSH_TEST bit 6 inside CR2-CTRLR2 with device in normal or Fail Safe. For each row the CRC is recalculated and compared with the stored one. The BIST result is stored in SR9-NVMSHSR bits from 15 to 1 named NVMSHB[14:0]. For each row, the corresponding bit in this register is set to '1' if there was a CRC error during the BIST execution.

Table 21. Customer data map

Byte#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte0	WrCount [7:0]							
Byte1	DITH_STEP [2:0]			WD_TIME		DEEP_STANDBY_DIS	WrCount [9:8]	
Byte2	IOUT threshold [5:0]						EMPTY	
Byte3	IOUT threshold [13:6]							
Byte4	ENCTRL_STDBY [3:0]				IOUT threshold [15:14]		EMPTY	
Byte5	OUT_CTRL [7:0]							
Byte6	ENCTRL_STDBY [7:4]				EN_CONF_STDBY	EMPTY		
Byte7	TMAX [7:0]							
Byte8	ENCTRL_FS [3:0]				DIS_CONF_FS	DIS_CONF_OUT_FS	EMPTY	
Byte9	DIN Mask [7:0]							
Byte10	ENCTRL [7:4]				EMPTY			
Byte11	DIN Mask [15:8]							
Byte12	EMPTY							

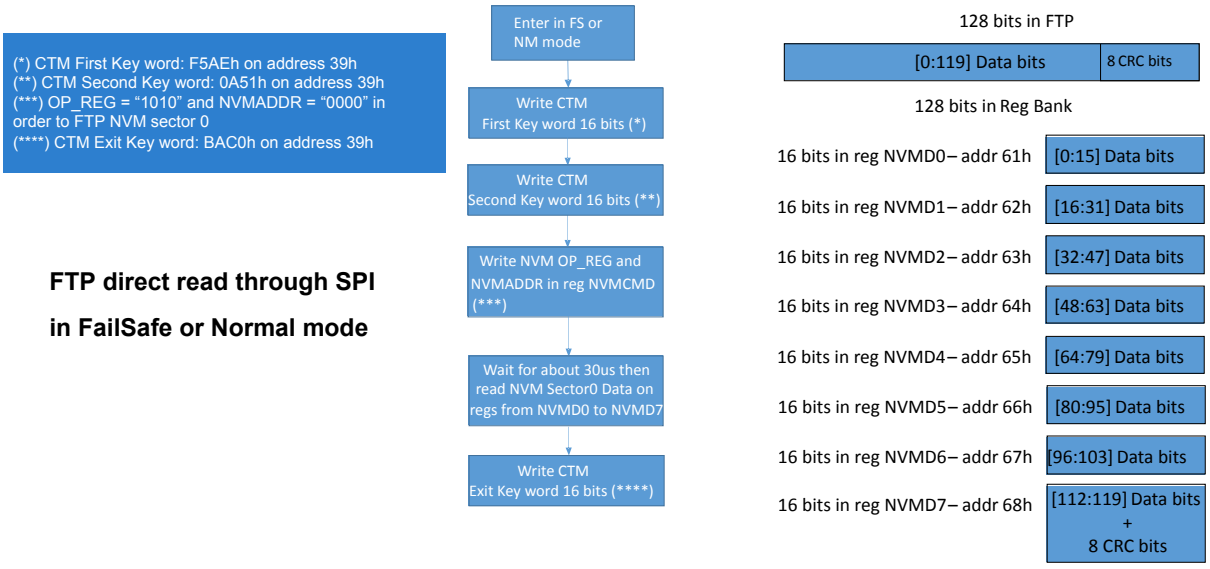
Byte#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte13	OUTCTRL_FS [7:0]							
Byte14	EMPTY							
Byte15	CRC							

Figure 7. NVM direct write



The customer can read the NVM data following the steps described in the Figure 8:

Figure 8. NVM direct read



5 DIx input management

The device allows output control directly by hardware, through four dedicated input pins (DIx), in addition to software control by the SPI interface. Through these pins it is possible, while the device is in fail-safe or in normal mode if bit DIENx = 1 (in channels control registers from CR4 to CR7), to turn-on/turn-off directly the outputs, providing an alternative to application host management, as requested by safety requirements and by application use cases in which the device could operate without the SPI interface being active. Clearly, DIx control is superseded by fault occurrence.

Every output can be mapped to each DIx through NVM registers byte 9 and byte 11 as follows:

Table 22. DIx pins output mapping

Output mapping	Bit 1, bit 0	Bit 1, bit 0	Bit 1, bit 0	Bit 1, bit 0
	00	01	10	11
CH7	DI0	DI1	DI2	DI3
CH6	DI0	DI1	DI2	DI3
CH5	DI0	DI1	DI2	DI3
CH4	DI0	DI1	DI2	DI3
CH3	DI0	DI1	DI2	DI3
CH2	DI0	DI1	DI2	DI3
CH1	DI0	DI1	DI2	DI3
CH0	DI0	DI1	DI2	DI3

DIx toggling

DIx pins can be used to enable capacitive charging mode functionality, while the device operates in a fail-safe state. To do that, at least five DIx pulses rising edge within a 240 µs window shall be executed.

Each pulse duration shall be t > 20 µs.

Voltages and current thresholds of DIx pins are reported in the Table 9. DIx pin specification.

6 Built-in self-test

The device integrates a built-in self-test (BIST), implemented to check device health during its working life monitoring voltage and current ADC conversion, standby on the current sense chain.

Voltage ADC BIST

Voltage ADC BIST can be activated through the SPI frame by means of the bit “TRIG_ADC_TEST” in the control register 0x02h. During the execution, a multiplexer passes to the ADC three voltages references, ADC_{VLOW_BIST} - ADC_{VMID_BIST} - ADC_{VHIGH_BIST}.

The result of the comparison will be stored into three distinct registers R&C:

- Address 0x59h: digital voltage for the low-level self-test (VADCLSR)
- Address 0x5Ah: digital voltage for the mid-level self-test (VADCMSR)
- Address 0x5Bh: digital voltage for the high-level self-test (VADCHSR)
  When the value of the registers is updated, an updated bit UPDTHxSR is set.

Table 23. Voltage ADC BIST conversion results

Symbol	Parameter	Test conditions	Min.	Typ.	Max.
ADC_{VLOW_BIST}	Conversion result for the low-level voltage self-test	V_{CC}=13 V	-20%	100	20%
ADC_{VMID_BIST}	Conversion result for the medium-level voltage self-test	V_{CC}=13 V	-10%	491	10%
ADC_{VHIGH_BIST}	Conversion result for the high-level voltage self-test	V_{CC}=13 V	-10%	900	10%

The microcontroller validates the expected conversions.

Current ADC BIST

Current ADC BIST can be activated for each channel through the SPI frame by means of the bit “TRIG_ADC_TEST” in the control register 0x02h. During the execution, a multiplexer passes to the ADC three current references, ADC_{ILOW_BIST} - ADC_{IMID_BIST} - ADC_{IHIGH_BIST}.

The result of the comparison will be stored into three distinct registers from 0x41h to 0x58h:

- Digital current for the low-level self-test (CSADCLxSR)
- Digital current for the mid-level self-test (CSADCMxSR)
- Digital current for the high-level self-test (CSADCHxSR)

When the value of the registers is updated, the bit UPDTHxSR is set.

Table 24. Current ADC BIST conversion results

Symbol	Parameter	Test conditions	Min.	Typ.	Max.
ADC_{ILOW_BIST}	Conversion result for the low-level current self-test	V_{CC}=13 V	-25%	88	25%
ADC_{IMID_BIST}	Conversion result for the medium-level current self-test	V_{CC}=13 V	-12%	519	12%
ADC_{IHIGH_BIST}	Conversion result for the high-level current self-test	V_{CC}=13 V	-12%	960	12%

The microcontroller validates the expected conversions.

Stuck-on BIST

The stuck-on BIST can be activated independently for each channel through the SPI frame by means of the bit TRIG_STUCKON_TEST bit in the control register 0x02h.

It is used to check the status of each P-Channel, detecting an eventual output stuck-on. As it is shown in the Figure 9, this check could be implemented by calculating ΔV_{OUT} between an initial V_{OUT} measure, sampled before the start of the self-test, and a final V_{OUT} measurement, sampled during the self-test.

During the self-test, a current generator is activated to discharge a capacitive load: this implies that the test duration is dependent on load capacitor, ΔV_{OUT} and $I_{selftest}$ as follows:

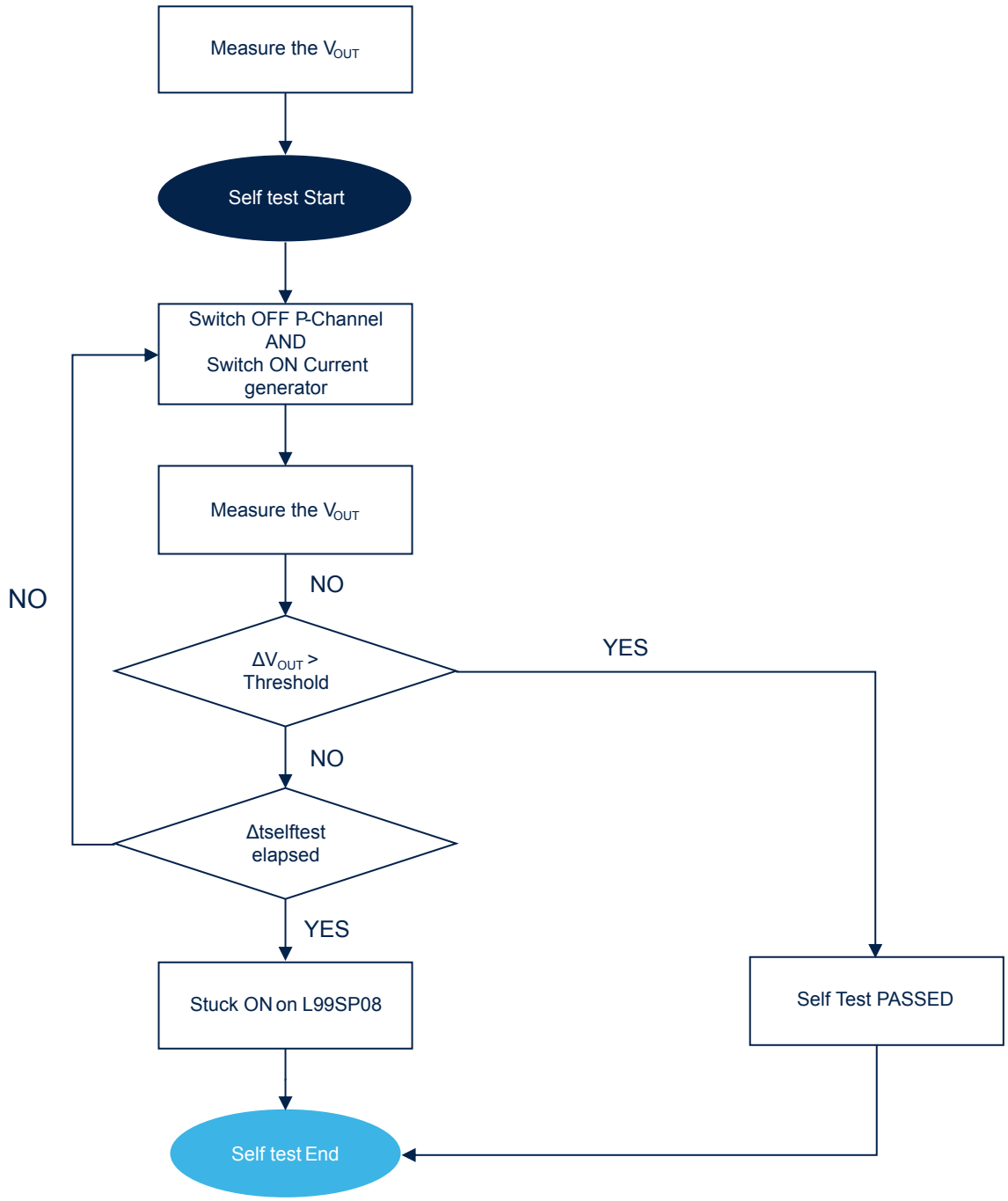
$$\Delta t_{selftest} = \frac{C_{load} * \Delta V_{OUT}}{I_{selftest}} \quad (4)$$

Where $I_{selftest}$ depends on the number of activated stuck-on test as follows:

$$I_{selftest} = \frac{10mA}{n°activatedchannels} \quad (5)$$

ΔV_{OUT} can be calculated by the microcontroller reading in the status register VOUTxSR (21-28) bit [13:4].

Figure 9. Stuck-on self-test–flow sequence



7 SPI functional description

7.1 SPI communication

The SPI communication is based on the “ST-SPI specification”.

The device operates in slave mode on a bus configuration through CSN, SDI, SDO, and SCK signal lines, with 24-bit SPI frames.

A SPI master device (host microcontroller) initiates the communication. The SPI Master device must be configured in the following mode:

CPOL = 0, CPHA = 0

Input data are shifted into SDI, MSB first while output data are shifted out on SDO, MSB first.

7.2 Signal description

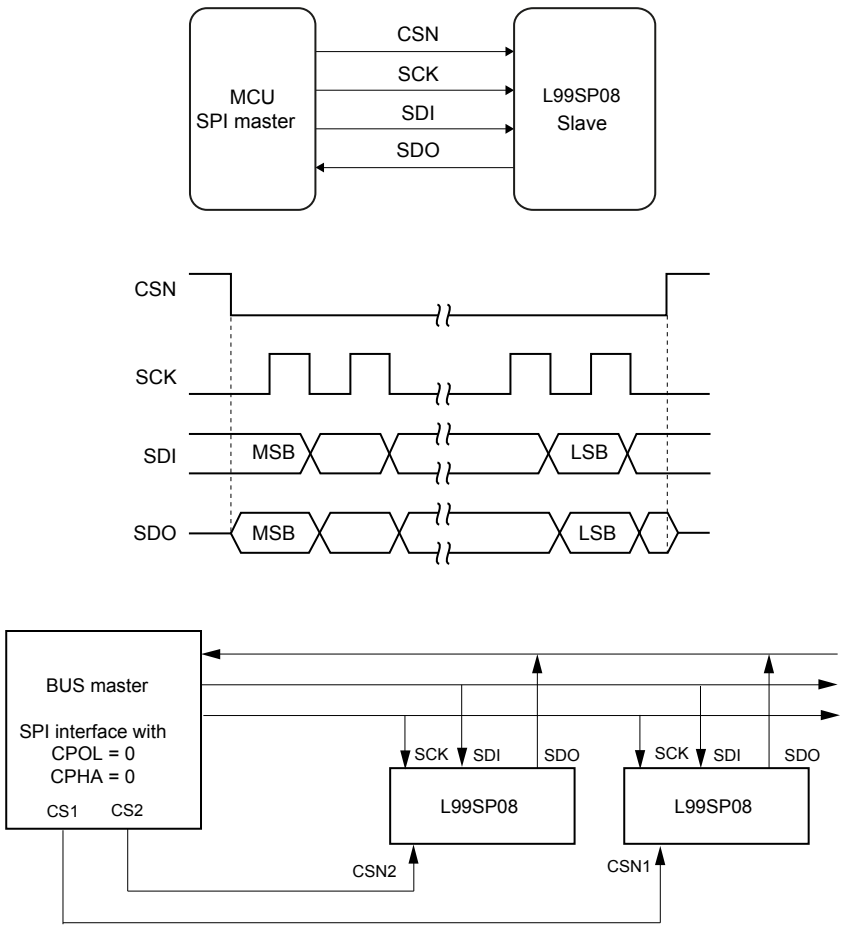
During all operations, V_{DD} must be held stable and within the specified valid range: V_{DD} min. to V_{DD} max.

Table 25. SPI signal description

Name	Function
Serial clock SCK	This input signal provides the timing of the serial interface. Data present at serial data input (SDI) are latched on the rising edge of the serial clock (SCK). Data on serial data output (SDO) change after the falling edge of the serial clock (SCK).
Serial data input SDI	This input signal is used to transfer data serially into the device. It receives data to be written. Values are sampled on the rising edge of the serial clock (SCK).
Serial data output SDO	This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of the serial clock (SCK).
Chip select CSN	When this input signal is high, the device is deselected, and serial data output (SDO) is high-Z. Driving this input low enables the communication. The communication must start on a low level of serial clock (SCK). Data are accepted only if exactly 24 bits have been shifted in. As per the ST_SPI standard, in case of failing communication: • CSN stuck at high: – If the device is in normal mode, a WDTB timeout forces the device into fail-safe mode. The serial data output (SDO) remains in high-Z (high-Z). The device accepts any valid communications received after this event. • CSN stuck at low: – in this case and whatever the mode of the device, a CSN timeout protection is activated and force the device to release the SPI bus. Then the serial data output (SDO) goes into high-Z (high-Z) A reset of the CSN timeout is activated with a transition low to high on the CSN pin (or with a power-on reset or software reset). With this reset, the serial data output (SDO) is released and the device accepts each valid communication. Without this reset, the device does not consider next communication.

A schematic view of the architecture between the bus and devices can be seen in the below figure. All input data bytes are shifted into the device, MSB first. The serial data input (SDI) is sampled on the first rising edge of the serial clock (SCK) after chip select (CSN) goes low. All output data bytes are shifted out of the device on the falling edge of SCK, MSB first on the first falling edge of the chip select (CSN).

Figure 10. **SPI functional diagram**



7.3 SPI protocol

SDI format during each communication frame starts with a command byte. It begins with two bits of operating code (OC1, OC0) which specify the type of operation (read, write, read and clear status, read device information). It is followed by a 6-bit address (A5: A0). The command byte is followed by two input data bytes: (D15: D8) and (D7:D0).

Table 26. **Command byte**

MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 27. **Input data byte 1**

MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 28. **Input data byte 2**

MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB
D7	D6	D5	D4	D3	D2	D1	D0[1]

1. *D0 is the parity bit.*

SDO format during each communication frame starts with a specific byte called global status byte (see GSB byte for more details on bit0 - bit7). This byte is followed by two output data bytes (D15: D8) and (D7: D0).

Table 29. Global status byte

MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Table 30. Output data byte 1

MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB
D23	D22	D21	D20	D19	D18	D17	D16

Table 31. Output data byte 2

MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB
D15	D14	D13	D12	D11	D10	D9	D8

7.4 Operating code definition

The SPI interface features four different addressing modes that are listed in the table below.

Table 32. Operating codes

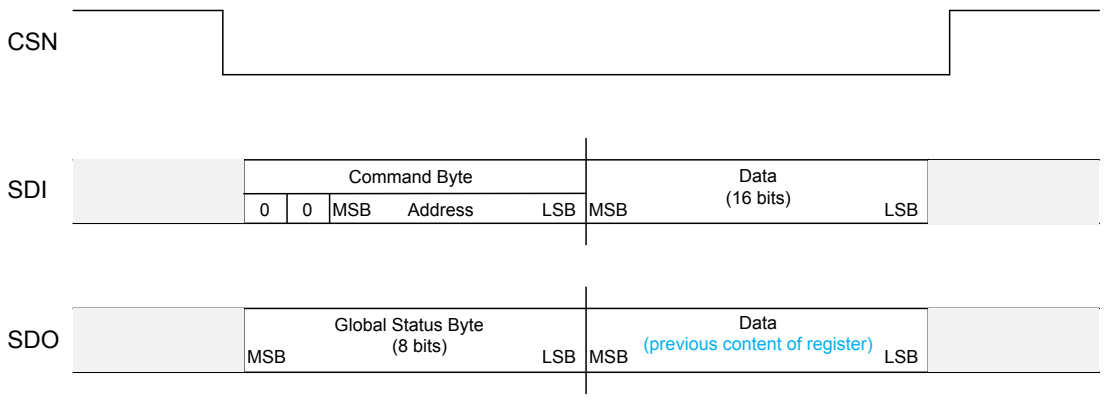
OC1	OC0	Meaning
0	0	Write operation
0	1	Read operation
1	0	Read and clear status operation
1	1	Read device information

7.4.1 Write mode

The write mode of the device allows writing the content of the input data byte into the addressed register (see list of registers in Table 38. RAM memory map). Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence, outgoing data are shifted out MSB first on the falling edge of the CSN pin and subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the global status byte, the second, and third bytes to the previous content of the addressed register. Unused bits are always read as 0.

Figure 11. SPI write operation



GADG1010171330PS

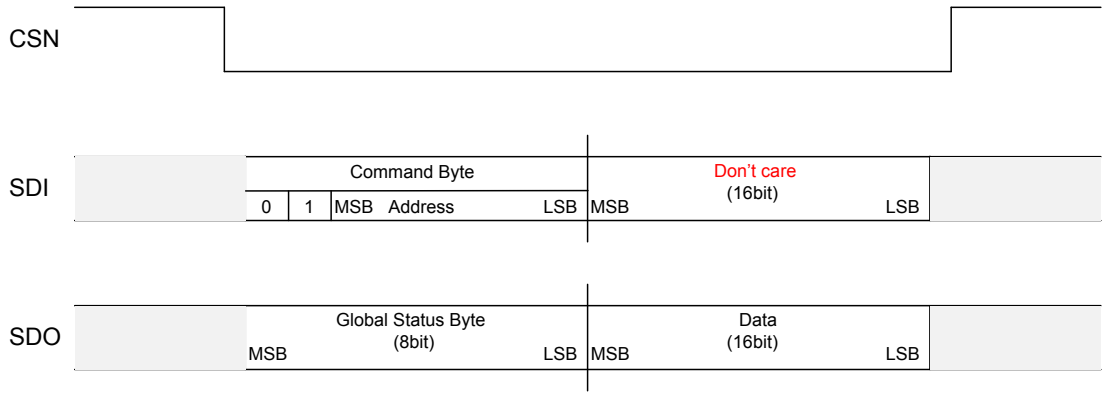
7.4.2 Read mode

The read mode of the device allows to read and to check the state of any registers. Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte, second and third byte to the content of the addressed register. Unused bits are always read as 0.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 12. SPI read operation



7.4.3 Read and clear status command

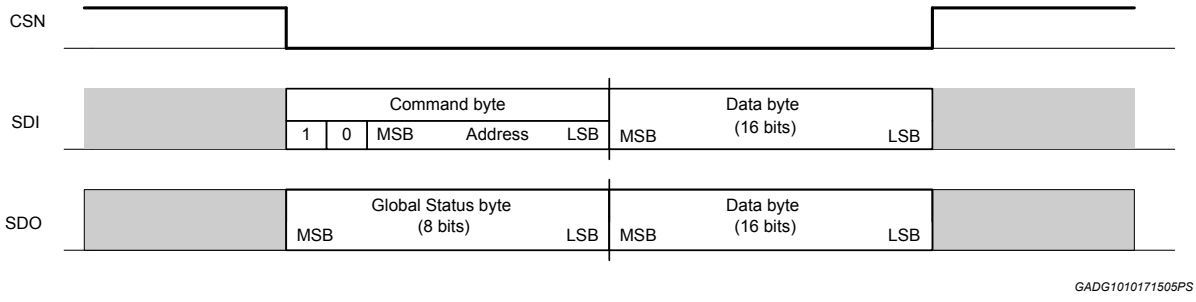
The read and clear status operation is used to clear the content of the addressed status register (see Table 38. RAM memory map). A read and clear status operation with address 3Fh clears all status registers simultaneously.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read and the payload bits set to 1 into the data byte determine the bits into the register that have to be cleared.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the global status byte, the second and third byte to the content of the addressed register. Unused bits are always read as 0.

In order to avoid inconsistency between the global status byte and the status register, the status register contents are frozen during SPI communication.

Figure 13. SPI read and clear operation



7.4.4 SPI device information

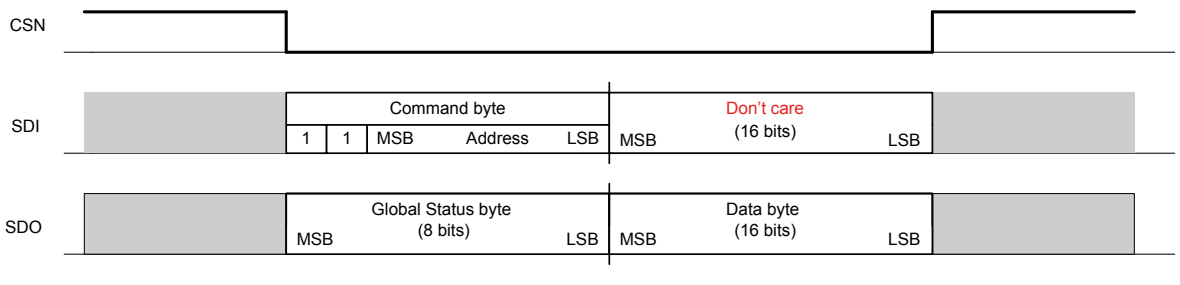
Specific information can be read but not modified during this mode.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read, while the other three data bytes are “don’t care”.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the global status byte, the second byte to the content of the addressed register, the third, and fourth bytes are 0x00.

Note: ROM is based on the 8-bit registers, then even if 16 bits are returned, only the second byte contains the addressed ROM register.

Figure 14. SPI read device information



7.4.5 Special commands

0xFF–SWReset: set all control registers to default and clears all status register.

An OpCode ‘11’ (read device information) addressed at ‘111111’ forces a software reset of the device, second and third bytes are "don't care" provided that at least one bit is zero.

Note: An OpCode '11' at address '111111' with data field equal to '1111111111111111' the SPI frame is recognized as a frame error and the SPIE bit of GSB is set.

Table 33. 0xFF (SW_Reset)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Command							
OC1	OC0	Address					
1	1	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care.*

0xBF–clear all status registers (RAM access)

When an OpCode ‘10’ (read and clear operation) at address b’111111 is performed.

Table 34. **Clear all status registers (RAM access)**

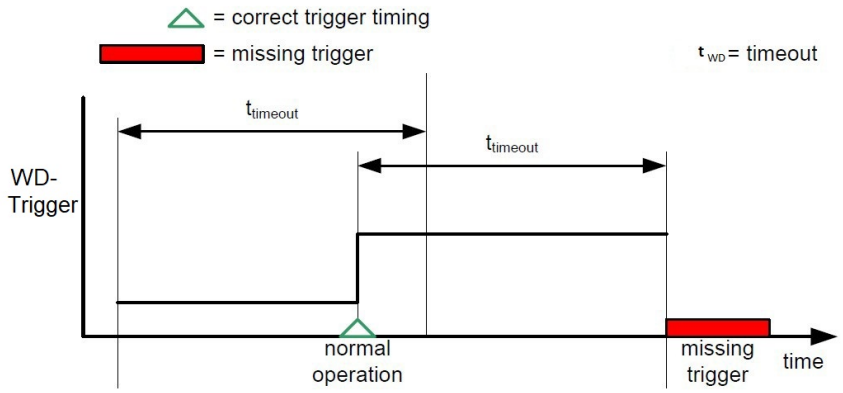
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Command							
OC1	OC0	Address					
1	0	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care.*

7.5 Timeout watchdog

In order to serve the timeout watchdog, the watchdog trigger bit must be toggled within a given timeout window.

Figure 15. **Timeout watchdog**



8 SPI registers

8.1 Global status byte

The device features an in-frame response mechanism.

The data shifted out on SDO during each communication starts with a specific byte called the global status byte. This one is used to inform the microcontroller about global faults, which can happen at channel-side level (that is like thermal shutdown, IPEAK...) or on the SPI interface (like watchdog monitoring timeout event, communication error...).

This specific register has the following format:

Table 35. Global status byte

MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB
GSBN	RSTB	SPIE	FE2	FE1	DE	GW	FS

Table 36. Global status byte - bit description

Bit#	Name	Description
7	Global status bit not	The GSBN is a logically NOR combination of bit 0 to bit 6. This bit can also be used as global status flag without starting a complete communication frame as it is present directly after pulling CSN low.
6	Reset bit	The RSTB indicates a device reset. In case this bit is set, all internal control registers are set to default and kept in that state until the bit is cleared. The reset bit is automatically cleared by any valid SPI communication
5	SPI error	The SPIE is a logical OR combination of errors related to a wrong SPI communication (SCK count and SDI stuck at errors). The SPIE bit is automatically set when SDI is stuck at High or Low. The SPIE is automatically cleared by a valid SPI communication.
4	FE2	ITHRx (x in 0 to 7)
3	FE1	VDS_MAXx or IPEAKx (x in 0 to 7)
2	DE	TSDx (x in 0 to 3) or BG_FAIL or OSC_FAIL or NVMSHBy or NVMCRCy (y in 1 to 9)
1	GW	VCC_OV or VCC_UV or TWx (x in 0 to 7)
0	Fail-safe	The bit is set in case the device operates in fail-safe mode. A detailed description of these root-causes and the fail-safe state itself is specified in the paragraph “Fail-safe mode”

8.2 Address map

8.2.1 Register map pages management

Due to the complexity of device control, the number of needed bits to store the device configuration exceeds the addressable registers (3Fh) with six bits address vector, so has been added a paging strategy to the registers addressment. The register map is divided in two pages, the first one includes the registers with address less than 40h, the second one the register with an address between 40h and 7Fh. In order to manage the current page two control registers have been inserted respectively with address 00h and 40h whose bit two sets the *CURR_PAGE*.

The following table shows the correlation between the *SPI_reg_address Ax* set in the SPI frame and the *Complete_reg_map_address*.

Table 37. Register map pages management

CURR_PAGE	SPI_reg_address Ax	Complete_reg_map_address
0	xxxxxx	0xxxxxx
1	xxxxxx	1xxxxxx

The default value of the *CURR_PAGE* bit is set to “0”, in this way, at the switch on, the device is set to address the page “0”, to move to the page “1”, in order to address a register between 40h and 7Fh, is needed to set a write operation on register 00h to set *CURR_PAGE* bit(bit2) to “1”. Then using the regular SPI protocol is possible to address the second page registers in the following way.

To operate on register with address 1xxxxxx you need to load two SPI frames:

- First SPI frame to set to “1” bit2 of *Page control register*(00h);
- Second SPI frame to operate on register with address 1xxxxxx using, in the SPI frame, the address xxxxxx.

8.2.2 RAM

RAM register can be separated according to the frequency of usage:

- Init–register is read/written during the initialization phase (single shot action)
- Continuos–read/write/read and clear registers often accessed, applying outputs control and diagnostic
- Rare–read/read and clear status of device registers accessed on demand (in case of failure)

Table 38. RAM memory map

Address	Name	Access	Content	Access type	Reset value
CONTROL REGISTERS					
00h/40h	CR0–PAGECR	Read/Write	Page control register	Init	0x0000
01h	CR1–CTRLR1	Read/Write	Central control register 1	Init	0x0000
02h	CR2–CTRLR2	Read/Write	Central control register 2	Init	0x0000
03h	CR3–OUTCR	Read/Write	Outputs control register	Init	0x0000
04h	CR4–CHCR1	Read/Write	Channels 0-1 control register	Init	0x0000
05h	CR5–CHCR2	Read/Write	Channels 2-3 control register	Init	0x0000
06h	CR6–CHCR3	Read/Write	Channels 4-5 control register	Init	0x0000
07h	CR7–CHCR4	Read/Write	Channels 6-7 control register	Init	0x0000
08h	CR8–ENCR	Read/Write	Direct external EN control register	Init	0x0000
…	…	…	…	…	…
1Fh	CR20–WDTCR0/1	Read/Write	WD toggling control register	Init	0x0000
STATUS REGISTERS					
10h	SR1–SREG	Read/Clear	Central status register	Rare	0x0000
11h	SR2–CHSR1	Read/Clear	Channels 0-1 status register 1	Rare	0x0000
12h	SR3–CHSR2	Read/Clear	Channels 2-3 status register 2	Rare	0x0000
13h	SR4–CHSR3	Read/Clear	Channels 4-5 status register 3	Rare	0x0000
14h	SR5–CHSR4	Read/Clear	Channels 6-7 status register 4	Rare	0x0000
15h	SR6–TMAXSR	Read/Clear	TMAX status register	Rare	0x0000
16h	SR7–CSDIAGSR	Read/Clear	CS_DIAG status register	Rare	0x0000
17h	SR8–CSBSR	Read/Clear	CS bist status register	Rare	0x0000
18h	SR9–NVMSHSR	Read/Clear	NVM Shadow bist status register	Rare	0x0000
19h	SR10–NVMCRCSR	Read/Clear	NVM CRC status register	Rare	0x0000
1Ah	SR11–DINVMSR1	Read/Clear	DINVM (channels 0-3) status register	Rare	0x0000
1Bh	SR12–DINVMSR2	Read/Clear	DINVM (channels 4-7) status register	Rare	0x0000
…	…	…	…	…	…
20h	SR13–IOUT0SR	Read/Clear	Current value register for channel 0	Rare	0x0000
21h	SR14–IOUT1SR	Read/Clear	Current value register for channel 1	Rare	0x0000
22h	SR15–IOUT2SR	Read/Clear	Current value register for channel 2	Rare	0x0000

Address	Name	Access	Content	Access type	Reset value
23h	SR16–IOUT3SR	Read/Clear	Current value register for channel 3	Rare	0x0000
24h	SR17–IOUT4SR	Read/Clear	Current value register for channel 4	Rare	0x0000
25h	SR18–IOUT5SR	Read/Clear	Current value register for channel 5	Rare	0x0000
26h	SR19–IOUT6SR	Read/Clear	Current value register for channel 6	Rare	0x0000
27h	SR20–IOUT7SR	Read/Clear	Current value register for channel 7	Rare	0x0000
28h	SR21–VOUT0SR	Read/Clear	Output voltage register for channel 0	continuous	0x0000
29h	SR22–VOUT1SR	Read/Clear	Output voltage register for channel 1	continuous	0x0000
2Ah	SR23–VOUT2SR	Read/Clear	Output voltage register for channel 2	continuous	0x0000
2Bh	SR24–VOUT3SR	Read/Clear	Output voltage registers for channel 3	continuous	0x0000
2Ch	SR25–VOUT4SR	Read/Clear	Output voltage register for channel 4	continuous	0x0000
2Dh	SR26–VOUT5SR	Read/Clear	Output voltage registers for channel 5	continuous	0x0000
2Eh	SR27–VOUT6SR	Read/Clear	Output voltage register for channel 6	continuous	0x0000
2Fh	SR28–VOUT7SR	Read/Clear	Output voltage registers for channel 7	continuous	0x0000
30h	SR29–TJ0SR	Read	TJ register for channel 0	continuous	0x0000
31h	SR30–TJ1SR	Read	TJ register for channel 1	continuous	0x0000
32h	SR31–TJ2SR	Read	TJ register for channel 2	continuous	0x0000
33h	SR32–TJ3SR	Read	TJ register for channel 3	continuous	0x0000
34h	SR33–TJ4SR	Read	TJ register for channel 4	continuous	0x0000
35h	SR34–TJ5SR	Read	TJ register for channel 5	continuous	0x0000
36h	SR35–TJ6SR	Read	TJ register for channel 6	continuous	0x0000
37h	SR36–TJ7SR	Read	TJ register for channel 7	continuous	0x0000
38h	SR37–VCCSR	Read	VCC register	continuous	0x0000
41h	SR38–CSADCL0SR	Read/Clear	ADC self-test (low level) current value for channel 0	Init	0x0000
42h	SR39–CSADCM0SR	Read/Clear	ADC self-test (medium level) current value for channel 0	Init	0x0000
43h	SR40–CSADCH0SR	Read/Clear	ADC self-test (high level) current value for channel 0	Init	0x0000
44h	SR41–CSADCL1SR	Read/Clear	ADC self-test (low level) current value for channel 1	Init	0x0000
45h	SR42–CSADCM1SR	Read/Clear	ADC self-test (medium level) current value for channel 1	Init	0x0000
46h	SR43–CSADCH1SR	Read/Clear	ADC self-test (high level) current value for channel 1	Init	0x0000
47h	SR44–CSADCL2SR	Read/Clear	ADC self-test (low level) current value for channel 2	Init	0x0000
48h	SR45–CSADCM2SR	Read/Clear	ADC self-test (medium level) current value for channel 2	Init	0x0000
49h	SR46–CSADCH2SR	Read/Clear	ADC self-test (high level) current value for channel 2	Init	0x0000
4Ah	SR47–CSADCL3SR	Read/Clear	ADC self-test (low level) current value for channel 3	Init	0x0000
4Bh	SR48–CSADCM3SR	Read/Clear	ADC self-test (medium level) current value for channel 3	Init	0x0000
4Ch	SR49–CSADCH3SR	Read/Clear	ADC self-test (high level) current value for channel 3	Init	0x0000

Address	Name	Access	Content	Access type	Reset value
4Dh	SR50–CSADCL4SR	Read/Clear	ADC self-test (low level) current value for channel 4	Init	0x0000
4Eh	SR51–CSADCM4SR	Read/Clear	ADC self-test (medium level) current value for channel 4	Init	0x0000
4Fh	SR52–CSADCH4SR	Read/Clear	ADC self-test (high level) current value for channel 4	Init	0x0000
50h	SR53–CSADCL5SR	Read/Clear	ADC self-test (low level) current value for channel 5	Init	0x0000
51h	SR54–CSADCM5SR	Read/Clear	ADC self-test (medium level) current value for channel 5	Init	0x0000
52h	SR55–CSADCH5SR	Read/Clear	ADC self-test (high level) current value for channel 5	Init	0x0000
53h	SR56–CSADCL6SR	Read/Clear	ADC self-test (low level) current value for channel 6	Init	0x0000
54h	SR57–CSADCM6SR	Read/Clear	ADC self-test (medium level) current value for channel 6	Init	0x0000
55h	SR58–CSADCH6SR	Read/Clear	ADC self-test (high level) current value for channel 6	Init	0x0000
56h	SR59–CSADCL7SR	Read/Clear	ADC self-test (low level) current value for channel 7	Init	0x0000
57h	SR60–CSADCM7SR	Read/Clear	ADC self-test (medium level) current value for channel 7	Init	0x0000
58h	SR61–CSADCH7SR	Read/Clear	ADC self-test (high level) current value for channel 7	Init	0x0000
59h	SR62–VADCLSR	Read/Clear	ADC self-test (low level) voltage value	continuous	0x0000
5Ah	SR63–VADCMSR	Read/Clear	ADC self-test (medium Level) voltage value	continuous	0x0000
5Bh	SR64–VADCHSR	Read/Clear	ADC self-test (high level) voltage value	continuous	0x0000
…	…	…	…	…	…
60h	NVMCMD	Read/Write	NVM CTM/ST programming–CMD		
61h	NVMD0	Read/Write	NVM CTM/ST programming–DATA0 (Byte1 e Byte0)		
62h	NVMD1	Read/Write	NVM CTM/ST programming–DATA1 (Byte3 e Byte2)		
63h	NVMD2	Read/Write	NVM CTM/ST programming–DATA2 (Byte5 e Byte4)		
64h	NVMD3	Read/Write	NVM CTM/ST programming–DATA3 (Byte7 e Byte6)		
65h	NVMD4	Read/Write	NVM CTM/ST programming–DATA4 (Byte9 e Byte8)		
66h	NVMD5	Read/Write	NVM CTM/ST programming–DATA5 (Byte11 e Byte10)		
67h	NVMD6	Read/Write	NVM CTM/ST programming–DATA6 (Byte13 e Byte12)		
68h	NVMD7	Read/Write	NVM CTM/ST programming–DATA7 (Byte15 e Byte14)		

8.2.3 ROM memory map

This memory is used for device identification.

Table 39. ROM memory map

Address	Name	Description	Access	Content
00h	Company code	Indicates the code of STMicroelectronics company	Read only	00H
01h	Device Family	Product family (STi²Fuse) code	Read only	03H
02h	Product code 1	Indicates the first code of the product (**U**)	Read only	55h
03h	Product code 2	Indicates the second code of the product (**R**)	Read only	52h
04h	Product code 3	Indicates the third code of the product (**4**)	Read only	04h
05h	Product code 4	Indicates the fourth code of the product (**C**)	Read only	43h
0Ah	Version	Silicon version	Read only	03H
… not used area				
10h	SPI mode	Different modes of the SPI (see chapter ‘SPI modes’)	Read only	A1H
11h	WD type 1	Indicates the type of watchdog used in the product	Read only	4AH
13h	WD bit position 1	Indicates the address of the register containing the WD toggle bit	Read only	41H
14h	WD bit position 2	Indicates the position of the WD toggle bit	Read only	C1H
… not used area				
20h	SPI CPHA	Indicates the polarity and phase of the SPI interface	Read only	55H
3Eh	GSB options	Options of GSB byte (standard GSB definition)	Read only	00H
3Fh	Advanced OP. Code			

8.2.4 SPI modes

By reading out the <SPI mode> register general information of SPI usage of the device application registers can be read.

Table 40. SPI mode

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Content
BR	DL2	DL1	DL0	SPI8	0	S1	S0	A1H

SPI burst read.

The burst read is implemented in this product, so this bit is enabled.

Table 41. SPI burst read

Bit7	Description
0	BR disabled
1	BR enabled

SPI data length

The SPI data length value indicates the length of the SCK count monitor that is running for all the accesses to the device application registers. In case a communication frame with an SCK count is not equal to the reported one, the device leads to a SPI error and the data are rejected. The Frame length is specified on 3 bits in the SPI mode register located in the ROM part. The 24-bit SPI communication is implemented in this product, so these bits are ‘010’.

Table 42. **SPI data length**

Bit6	Bit5	Bit4	Description
DL2	DL1	DL0	
0	0	0	Invalid
0	0	1	16 bit SPI
0	1	0	24 bit SPI
…			
1	1	1	64 bit SPI

Data consistency check (Parity/CRC)

For some devices, a data consistency check is required. Therefore, either a parity-check or for very sensitive systems a CRC may be implemented. It is defined on 2 bits, in the SPI mode register located in the ROM part. A check is then applied on the incoming frame (SDI) while a calculation elaborated on one/multiple bits is done and integrated on the outgoing frame (SDO).

Table 43. **SPI data consistency check**

Bit 1	Bit 0	Description
S1	S0	
0	0	Not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

In case either the parity or the CRC check is implemented it is always located at the end of the communication. The device is equipped with the parity control check.

8.3 Control registers

8.3.1 Page control register (CR0–PAGECR1/2)

Table 44. **Page control register (CR0–PAGECR1/2)**

Address 0x00h and 0x40h				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	Not used	R	0	
12	Not used	R	0	
11	Not used	R	0	
10	Not used	R	0	
9	Not used	R	0	
8	Not used	R	0	
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	

Address 0x00h and 0x40h				
Bit	Name	Access	Reset	Content
4	Not used	R	0	
3	Not used	R	0	
2	CURR_PAGE	R/W	0	CURR_PAGE bit controls current page number 1: page1 0: page0
1	Not used	R	0	
0	PARITY	R		Parity bit

8.3.2 Central control register (CR1–CTRLR1)

Table 45. Central control register (CR1–CTRLR1)

Address 0x01h				
Bit	Name	Access	Reset	Content
15	GOSTBY	R/W	0	Go to standby It is necessary to perform two writes accesses to enter standby from normal mode: • Write UNLOCK=1 • Write GOSTBY=1 and EN=0
14	EN	R/W	0	1: Normal mode 0: Fail-safe mode It is necessary to perform two writes accesses to enter normal mode: • Write UNLOCK=1 • Write EN=1
13:11	Not used	R	0	
10	Not used	R	0	
9:2	Not used	R	0	
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R		Parity bit

8.3.3 Central control register (CR2–CTRLR2)

Table 46. Central control register (CR2–CTRLR2)

Address 0x02h				
Bit	Name	Access	Reset	Content
15:8	TRIG_STUCKON_TEST	R/W	0	Triggers the stuck-on self-test (a bit x Channel)
7	Not used	R	0	
6	TRIG_NVMSH_TEST	R/W	0	To run the NVM shadow regs stuck-at test. This bit is automatically reset.
5	TRIG_CS_TEST	R/W	0	Triggers the current sense test This bit is automatically reset
4	TRIG_ADC_TEST	R/W	0	Triggers the ADC test This bit is automatically reset

Address 0x02h				
Bit	Name	Access	Reset	Content
3	UNLOCK	R/W	0	UNLOCK bit allows protected SPI transactions. It means that the next SPI communication will automatically clear this bit and prevent any change of protected data (like slope control or bulb/led mode for example). Therefore, modifying a protected data requires to set UNLOCK bit in a first communication and write the protected data during the next communication.
2	Not used	R	0	
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R		

8.3.4 Output control register (CR3–OUTCR)

Table 47. **Output control register (CR3–OUTCR)**

Address 0x03h				
Bit	Name	Access	Reset	Content
15	OUTCTRL7	R/W	0	OUTCTRL7 bit controls output state of channel 7 1: output enabled 0: output disabled
14	OUTCTRL6	R/W	0	OUTCTRL6 bit controls output state of channel 6 1: output enabled 0: output disabled
13	OUTCTRL5	R/W	0	OUTCTRL5 bit controls output state of channel 5 1: output enabled 0: output disabled
12	OUTCTRL4	R/W	0	OUTCTRL4 bit controls output state of channel 4 1: output enabled 0: output disabled
11	OUTCTRL3	R/W	0	OUTCTRL3 bit controls output state of channel 3 1: output enabled 0: output disabled
10	OUTCTRL2	R/W	0	OUTCTRL2 bit controls output state of channel 2 1: output enabled 0: output disabled
9	OUTCTRL1	R/W	0	OUTCTRL1 bit controls output state of channel 1 1: output enabled 0: output disabled
8	OUTCTRL0	R/W	0	OUTCTRL0 bit controls output state of channel 0 1: output enabled 0: output disabled
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	

Address 0x03h				
Bit	Name	Access	Reset	Content
2	Not used	R	0	
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R		Parity bit

8.3.5 Channels 0-1 control register (CR4–CHCR1)

Table 48. Channels 0-1 control register (CR4–CHCR1)

Address 0x04h				
Bit	Name	Access	Reset	Content
15	DINEN1	R/W	0	Channel 1 direct input control bit 1: ON 0: OFF
14	CAPCR1	R/W	0	CAPCR1 bit triggers the capacitive charging mode in normal mode for channel 1 when it is set to 1. This bit is automatically cleared.
13	EXIT_CAPCR1	R/W	0	EXIT_CAPCR1 bit sets the exit from CCM for channel 1 1: CCM exit 0: Holds CCM setting This bit is automatically cleared.
12	I_THR1[1:0]	R/W	0	I_THR1 vector sets the Channel 1 I_THR threshold
11			0	
10	Not used	R	0	
9	CS_DIAG1	R/W	0	1: only a part of the channel 1 Pch is used to reduce the sense ratio and to enhance accuracy at low current levels 0: normal conditions
8	DINEN0	R/W	0	Channel 0 direct input control bit 1: ON 0: OFF
7	CAPCR0	R/W	0	CAPCR0 bit triggers the capacitive charging mode in normal mode for channel 0 when it is set to 1. This bit is automatically cleared.
6	EXIT_CAPCR0	R/W	0	EXIT_CAPCR0 bit sets the exit from CCM for channel 0 1: CCM exit 0: Holds CCM setting This bit is automatically cleared.
5	I_THR0[1:0]	R/W	0	I_THR0 vector sets the Channel 0 I_THR threshold
4			0	
3	Not used	R	0	
2	CS_DIAG0	R/W	0	1: only a part of the Channel 0 P-channel is used to reduce the sense ratio and to enhance accuracy at low current levels 0: normal conditions
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R		Parity bit

8.3.6 Channels 2-3 control register (CR5–CHCR2)

Table 49. Channels 2-3 control register (CR5–CHCR2)

Address 0x05h				
Bit	**Name**	**Access**	**Reset**	**Content**
15	DINEN3	R/W	0	Channel 3 direct input control bit 1: ON 0: OFF
14	CAPCR3	R/W	0	CAPCR3 bit triggers the capacitive charging mode in normal mode for channel 3 when it is set to 1. This bit is automatically cleared.
13	EXIT_CAPCR3	R/W	0	EXIT_CAPCR3 bit sets the exit from CCM for channel 3 1–CCM Exit 0–Holds CCM setting This bit is automatically cleared.
12	I_THR3[1:0]	R/W	0	I_THR3 vector sets the Channel 3 I_THR threshold
11			0	
10	Not used	R	0	
9	CS_DIAG3	R/W	0	1: only a part of the Channel 3 Pch is used to reduce the sense ratio and to enhance accuracy at low current levels 0: normal conditions
8	DINEN2	R/W	0	Channel 2 direct input control bit 1: ON 0: OFF
7	CAPCR2	R/W	0	CAPCR2 bit triggers the capacitive charging mode in normal mode for channel 2 when it is set to 1. This bit is automatically cleared.
6	EXIT_CAPCR2	R/W	0	EXIT_CAPCR2 bit sets the exit from CCM for channel 2 1–CCM exit 0–Holds CCM setting This bit is automatically cleared.
5	I_THR2[1:0]	R/W	0	I_THR2 vector sets the Channel 2 I_THR threshold
4			0	
3	Not used	R	0	
2	CS_DIAG2	R/W	0	1: only a part of the Channel 2 Pch is used to reduce the sense ratio and to enhance accuracy at low current levels 0: normal conditions
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R		Parity bit

8.3.7 Channels 4-5 control register (CR6–CHCR3)

Table 50. Channels 4-5 control register (CR6–CHCR3)

Address 0x06h				
Bit	**Name**	**Access**	**Reset**	**Content**
15	DINEN5	R/W	0	Channel 5 direct input control bit 1: ON 0: OFF
14	CAPCR5	R/W	0	CAPCR5 bit triggers the capacitive charging mode in normal mode for channel 5 when it is set to 1. This bit is automatically cleared.
13	EXIT_CAPCR5	R/W	0	EXIT_CAPCR5 bit sets the exit from CCM for channel 5 1: CCM exit 0: Holds CCM setting This bit is automatically cleared.
12	I_THR5[1:0]	R/W	0	I_THR5 vector sets the Channel 5 I_THR threshold
11			0	
10	Not used	R	0	
9	CS_DIAG5	R/W	0	1: only a part of the Channel 5 Pch is used to reduce the sense ratio and to enhance accuracy at low current levels 0: normal conditions
8	DINEN4	R/W	0	Channel 4 direct input control bit 1: ON 0: OFF
7	CAPCR4	R/W	0	CAPCR4 bit triggers the capacitive charging mode in normal mode for channel 4 when it is set to 1. This bit is automatically cleared.
6	EXIT_CAPCR4	R/W	0	EXIT_CAPCR4 bit sets the exit from CCM for channel 4 1: CCM exit 0: Holds CCM setting This bit is automatically cleared.
5	I_THR4[1:0]	R/W	0	I_THR4 vector sets the Channel 4 I_THR threshold
4			0	
3	Not used	R	0	
2	CS_DIAG4	R/W	0	1: only a part of the Channel 4 Pch is used to reduce the sense ratio and to enhance accuracy at low current levels 0: normal conditions
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R		Parity bit

8.3.8 Channels 6-7 control register (CR7–CHCR4)

Table 51. **Channels 6-7 control register (CR7–CHCR4)**

Address 0x07h				
Bit	**Name**	**Access**	**Reset**	**Content**
15	DINEN7	R/W	0	Channel 7 direct input control bit 1: ON 0: OFF
14	CAPCR7	R/W	0	CAPCR7 bit triggers the capacitive charging mode in normal mode for channel 7 when it is set to 1. This bit is automatically cleared.
13	EXIT_CAPCR7	R/W	0	EXIT_CAPCR7 bit sets the exit from CCM for channel 7 1: CCM Exit 0: Holds CCM setting This bit is automatically cleared.
12	I_THR7[1:0]	R/W	0	I_THR7 vector sets the Channel 7 I_THR threshold
11			0	
10	Not used		0	
9	CS_DIAG7	R/W	0	1: only a part of the Channel 7 Pch is used to reduce the sense ratio and to enhance accuracy at low current levels 0: normal conditions
8	DINEN6	R/W	0	Channel 6 direct input control bit 1: ON 0: OFF
7	CAPCR6	R/W	0	CAPCR6 bit triggers the capacitive charging mode in normal mode for channel 6 when it is set to 1. This bit is automatically cleared.
6	EXIT_CAPCR6	R/W	0	EXIT_CAPCR6 bit sets the exit from CCM for channel 6 1: CCM exit 0: Holds CCM setting This bit is automatically cleared.
5	I_THR6[1:0]	R/W	0	I_THR0 vector sets the Channel 6 I_THR threshold
4			0	
3	Not used	R	0	
2	CS_DIAG6	R/W	0	1: only a part of the Channel 6 Pch is used to reduce the sense ratio and to enhance accuracy at low current levels 0: normal conditions
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R		Parity bit

8.3.9 Direct external EN control register (CR8–ENCR)

Table 52. **Direct external EN control register (CR8–ENCR)**

Address 0x08h				
Bit	**Name**	**Access**	**Reset**	**Content**
15	ENCTRL7	R/W	0	ENCTRL7 bit controls EN state of channel 7 1: EN enabled 0: EN disabled
14	ENCTRL6	R/W	0	ENCTRL6 bit controls EN state of channel 6 1: EN enabled 0: EN disabled
13	ENCTRL5	R/W	0	ENCTRL5 bit controls EN state of channel 5 1: EN enabled 0: EN disabled
12	ENCTRL4	R/W	0	ENCTRL4 bit controls EN state of channel 4 1: EN enabled 0: EN disabled
11	ENCTRL3	R/W	0	ENCTRL3 bit controls EN state of channel 3 1: EN enabled 0: EN disabled
10	ENCTRL2	R/W	0	ENCTRL2 bit controls EN state of channel 2 1: EN enabled 0: EN disabled
9	ENCTRL1	R/W	0	ENCTRL1 bit controls EN state of channel 1 1: EN enabled 0: EN disabled
8	ENCTRL0	R/W	0	ENCTRL0 bit controls EN state of channel 0 1: EN enabled 0: EN disabled
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R		Parity bit

8.3.10 WD toggling control registers (CR20-WDTCR0/1)

Table 53. **WD toggling control registers (CR20-WDTCR0/1)**

Address 0x1Fh and 0x5Fh				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	

Address 0x1Fh and 0x5Fh				
Bit	Name	Access	Reset	Content
14	Not used	R	0	
13	Not used	R	0	
12	Not used	R	0	
11	Not used	R	0	
10	Not used	R	0	
9	Not used	R	0	
8	Not used	R	0	
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	WDTB	R/W	0	Watchdog toggle bit
0	PARITY	R	0	Parity bit

8.4 Status registers

8.4.1 Central status register (SR1–SREG)

Table 54. Central status register (SR1–SREG)

Address 0x10h				
Bit	Name	Access	Reset	Content
15:14	WD_TIME	R	0	WD timer control: 00 → 50 ms 01 → 100 ms 10 → 200 ms 11 → WD disable
13	BG_FAIL	R/C	0	Bandgap fault status bit
12	OSC_FAIL	R/C	0	Oscillator fault status bit
11	Not used	R	0	
10	VCC_OV	R	0	VCC over voltage status bit
9	VCC_UV	R	0	VCC under voltage status bit
8	DEEP_STANDBY	R	0	DEEP_STANDBY_DIS (0 → deep_standby state enabled)
7	LHST	R	0	LH status bit
6	D3ST	R	0	D3 status bit
5	D2ST	R	0	D2 status bit
4	D1ST	R	0	D1 status bit
3	D0ST	R	0	D0 status bit
2	Not used	R	0	
1	WD_FAIL	R/C	0	Watchdog fail status bit

Address 0x10h				
Bit	Name	Access	Reset	Content
0	PARITY	R		

8.4.2 Channels 0-1 status register (SR2–CHSR1)

Table 55. **Channels 0-1 status register (SR2–CHSR1)**

Address 0x11h				
Bit	Name	Access	Reset	Content
15	TSD1	R/C	0	Channel 1 thermal shutdown status bit (switch off the p-channel and turn on the main switch) In NM this bit must be cleared through a R&C command, in FS the bit will be automatically cleared after 50ms (auto restart) This bit is set in two cases: 1) when the analog comparator switches (in standby) 2) when the digital threshold is reached (not in standby)
14	TSD0	R/C	0	Channel 0 thermal shutdown status bit (switch off the p-channel and turn on the main switch) In NM this bit must be cleared through a R&C command, in FS the bit will be automatically cleared after 50ms (auto restart) This bit is set in two cases: 1) when the analog comparator switches (in standby) 2) when the digital threshold is reached (not in standby)
13	TW1	R	0	Channel 1 thermal warning status bit
12	TW0	R	0	Channel 0 thermal warning status bit
11	VDS_MAX1	R/C	0	Channel 1 VDS Max status bit
10	VDS_MAX0	R/C	0	Channel 0 VDS Max status bit
9	IPEAK1	R/C	0	Channel 1 analog IPeak status bit
8	IPEAK0	R/C	0	Channel 0 analog IPeak status bit
7	ITHR1	R/C	0	Channel 1 analog Ithreshold status bit
6	ITHR0	R/C	0	Channel 0 analog Ithreshold status bit
5	CAPSR1	R	0	Channel 1 CCM status bit
4	CAPSR0	R	0	Channel 0 CCM status bit
3	ENABLE1	R	0	Channel 1 Enable output pin status bit
2	ENABLE0	R	0	Channel 0 Enable output pin status bit
1	Not used	R	0	
0	PARITY	R		

8.4.3 Channels 2-3 status register (SR3–CHSR2)

Table 56. **Channels 2-3 status register (SR3–CHSR2)**

Address 0x12h				
Bit	Name	Access	Reset	Content
15	TSD3	R/C	0	Channel 3 thermal shutdown status bit (switch off the p-channel and turn on the main switch)

Address 0x12h				
Bit	Name	Access	Reset	Content
				In NM this bit must be cleared through a R&C command, in FS the bit will be automatically cleared after 50ms (auto restart) This bit is set in two cases: 1) when the analog comparator switches (in standby) 2) when the digital threshold is reached (not in standby)
14	TSD2	R/C	0	Channel 2 thermal shutdown status bit (switch off the p-channel and turn on the main switch) In NM this bit must be cleared through a R&C command, in FS the bit will be automatically cleared after 50ms (auto restart) This bit is set in two cases: 1) when the analog comparator switches (in standby) 2) when the digital threshold is reached (not in standby)
13	TW3	R	0	Channel 3 thermal warning status bit
12	TW2	R	0	Channel 2 thermal warning status bit
11	VDS_MAX3	R/C	0	Channel 3 VDS Max status bit
10	VDS_MAX2	R/C	0	Channel 2 VDS Max status bit
9	IPEAK3	R/C	0	Channel 3 analog IPeak status bit
8	IPEAK2	R/C	0	Channel 2 analog IPeak status bit
7	ITHR3	R/C	0	Channel 3 analog Ithreshold status bit
6	ITHR2	R/C	0	Channel 2 analog Ithreshold status bit
5	CAPSR3	R	0	Channel 3 CCM status bit
4	CAPSR2	R	0	Channel 2 CCM status bit
3	ENABLE3	R	0	Channel 3 Enable output pin status bit
2	ENABLE2	R	0	Channel 2 Enable output pin status bit
1	Not used	R	0	
0	PARITY	R		

8.4.4 Channels 4-5 status register (SR4–CHSR3)

Table 57. Channels 4-5 status register (SR4–CHSR3)

Address 0x13h				
Bit	Name	Access	Reset	Content
15	TSD5	R/C	0	Channel 5 thermal shutdown status bit (switch off the p-channel and turn on the main switch) In NM this bit must be cleared through a R&C command, in FS the bit will be automatically cleared after 50ms (auto restart) This bit is set in two cases: 1) when the analog comparator switches (in standby) 2) when the digital threshold is reached (not in standby)
14	TSD4	R/C	0	Channel 4 thermal shutdown status bit (switch off the p-channel and turn on the main switch) In NM this bit must be cleared through a R&C command, in FS the bit will be automatically cleared after 50ms (auto restart) This bit is set in two cases:

Address 0x13h				
Bit	Name	Access	Reset	Content
				1) when the analog comparator switches (in standby) 2) when the digital threshold is reached (not in standby)
13	TW5	R	0	Channel 5 thermal warning status bit
12	TW4	R	0	Channel 4 thermal warning status bit
11	VDS_MAX5	R/C	0	Channel 5 VDS Max status bit
10	VDS_MAX4	R/C	0	Channel 4 VDS Max status bit
9	IPEAK5	R/C	0	Channel 5 analog IPeak status bit
8	IPEAK4	R/C	0	Channel 4 analog IPeak status bit
7	ITHR5	R/C	0	Channel 5 analog Ithreshold status bit
6	ITHR4	R/C	0	Channel 4 analog Ithreshold status bit
5	CAPSR5	R	0	Channel 5 CCM status bit
4	CAPSR4	R	0	Channel 4 CCM status bit
3	ENABLE5	R	0	Channel 5 Enable output pin status bit
2	ENABLE4	R	0	Channel 4 Enable output pin status bit
1	Not used	R	0	
0	PARITY	R		

8.4.5 Channels 6-7 status register (SR5–CHSR4)

Table 58. Channels 6-7 status register (SR5–CHSR4)

Address 0x14h				
Bit	Name	Access	Reset	Content
15	TSD7	R/C	0	Channel 7 thermal shutdown status bit (switch off the p-channel and turn on the main switch) In NM this bit must be cleared through a R&C command, in FS the bit will be automatically cleared after 50ms (auto restart) This bit is set in two cases: 1) when the analog comparator switches (in standby) 2) when the digital threshold is reached (not in standby)
14	TSD6	R/C	0	Channel 6 thermal shutdown status bit (switch off the p-channel and turn on the main switch) In NM this bit must be cleared through a R&C command, in FS the bit will be automatically cleared after 50ms (auto restart) This bit is set in two cases: 1) when the analog comparator switches (in standby) 2) when the digital threshold is reached (not in standby)
13	TW7	R	0	Channel 7 thermal warning status bit
12	TW6	R	0	Channel 6 thermal warning status bit
11	VDS_MAX7	R/C	0	Channel 7 VDS Max status bit
10	VDS_MAX6	R/C	0	Channel 6 VDS Max status bit
9	IPEAK7	R/C	0	Channel 7 analog IPeak status bit
8	IPEAK6	R/C	0	Channel 6 analog IPeak status bit
7	ITHR7	R/C	0	Channel 7 analog Ithreshold status bit

Address 0x14h				
Bit	Name	Access	Reset	Content
6	ITHR6	R/C	0	Channel 6 analog Ithreshold status bit
5	CAPSR7	R	0	Channel 7 CCM status bit
4	CAPSR6	R	0	Channel 6 CCM status bit
3	ENABLE7	R	0	Channel 7 Enable output pin status bit
2	ENABLE6	R	0	Channel 6 Enable output pin status bit
1	Not used	R	0	
0	PARITY	R		

8.4.6 TMAX status register (SR6–TMAXSR)

Table 59. TMAX status register (SR6–TMAXSR)

Address 0x1Fh and 0x5Fh				
Bit	Name	Access	Reset	Content
15	TSD_THR	R	0	TSD_THR bits set the TSD threshold
14				
13	DITH_STEP[2:0]	R	0	DITH_STEP bits set the dithering step
12				
11				
10	CTM_PROG_MODE	R	0	When high the device is in customer programming mode
9	TMAX	R	0	TMAX vector sets the value of the timer expiration for standby on exit
8				
7				
6				
5				
4				
3				
2				
1	Not used	R	0	
0	PARITY	R		

8.4.7 CS_DIAG status register (SR7–CSDIAGSR)

Table 60. CS_DIAG status register (SR7–CSDIAGSR)

Address 0x16h				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	Not used	R	0	
12	Not used	R	0	
11	Not used	R	0	

Address 0x16h				
Bit	Name	Access	Reset	Content
10	CS_DIAG7	R	0	Ch7 CS_DIAG status bit
9	CS_DIAG6	R	0	Ch6 CS_DIAG status bit
8	CS_DIAG5	R	0	Ch5 CS_DIAG status bit
7	CS_DIAG4	R	0	Ch4 CS_DIAG status bit
6	CS_DIAG3	R	0	Ch3 CS_DIAG status bit
5	CS_DIAG2	R	0	Ch2 CS_DIAG status bit
4	CS_DIAG1	R	0	Ch1 CS_DIAG status bit
3	CS_DIAG0	R	0	Ch0 CS_DIAG status bit
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R		

8.4.8 CS bist status register (SR8–CSBSR)

Table 61. CS bist status register (SR8–CSBSR)

Address 0x17h				
Bit	Name	Access	Reset	Content
15	Not used	R	0	Not used
14	Not used	R	0	Not used
13	Not used	R	0	Not used
12	Not used	R	0	Not used
11	CSADC_TEST	R	0	Current sense ADC test status bit
10	CS7_FAIL	R/C	0	Ch3 current sense fault status bit
9	CS6_FAIL	R/C	0	Ch2 current sense fault status bit
8	CS5_FAIL	R/C	0	Ch1 current sense fault status bit
7	CS4_FAIL	R/C	0	Ch0 current sense fault status bit
6	CS3_FAIL	R/C	0	Ch3 current sense fault status bit
5	CS2_FAIL	R/C	0	Ch2 current sense fault status bit
4	CS1_FAIL	R/C	0	Ch1 current sense fault status bit
3	CS0_FAIL	R/C	0	Ch0 current sense fault status bit
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R		

8.4.9 NVM shadows status register (SR9–NVMSHSR)

Table 62. NVM shadows status register (SR9–NVMSHSR)

Address 0x18h				
Bit	Name	Access	Reset	Content
15:1	NVMSHB[14:0]	R	0	NVM shadow registers BIST (one bit per row): 0 = test ok

Address 0x18h				
Bit	Name	Access	Reset	Content
				1 = test fail
0	PARITY	R		

8.4.10 NVM CRC check status Register (SR10–NVMCRCSR)

Table 63. **NVM CRC check status Register (SR10–NVMCRCSR)**

Address 0x19h				
Bit	Name	Access	Reset	Content
15:1	NVMCRC[14:0]	R	0	NVM single row CRC check: 0 = test ok 1 = test fail
0	PARITY	R		

8.4.11 DINNVM (channel 0-3) status register (SR11–DINVMSR1)

Table 64. **DINNVM (channel 0-3) status register (SR11–DINVMSR1)**

Address 0x1Ah				
Bit	Name	Access	Reset	Content
15 14	DINVM3[1:0]	R	0	Channel 3 DIN Mask: • 00 = din_ch(3) = di_i(0) • 01 = din_ch(3) = di_i(1) • 10 = din_ch(3) = di_i(2) • 11 = din_ch(3) = di_i(3)
13 12	DINVM2[1:0]	R	0	Channel 2 DIN Mask: • 00 = din_ch(2) = di_i(0) • 01 = din_ch(2) = di_i(1) • 10 = din_ch(2) = di_i(2) • 11 = din_ch(2) = di_i(3)
11 10	DINVM1[1:0]	R	0	Channel 1 DIN Mask: • 00 = din_ch(1) = di_i(0) • 01 = din_ch(1) = di_i(1) • 10 = din_ch(1) = di_i(2) • 11 = din_ch(1) = di_i(3)
9 8	DINVM0[1:0]	R	0	Channel 0 DIN Mask: • 00 = din_ch(0) = di_i(0) • 01 = din_ch(0) = di_i(1) • 10 = din_ch(0) = di_i(2) • 11 = din_ch(0) = di_i(3)
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	

Address 0x1Ah				
Bit	Name	Access	Reset	Content
0	PARITY	R		

8.4.12 DINNVM (channel 4-7) status register (SR12–DINVMSR2)

Table 65. DINNVM (channel 4-7) status register (SR12–DINVMSR2)

Address 0x1Bh				
Bit	Name	Access	Reset	Content
15	DINVM7[1:0]	R	0	Channel 7 DIN Mask: • 00 = din_ch(7) = di_i(0) • 01 = din_ch(7) = di_i(1) • 10 = din_ch(7) = di_i(2) • 11 = din_ch(7) = di_i(3)
14				
13	DINVM6[1:0]	R	0	Channel 6 DIN Mask: • 00 = din_ch(6) = di_i(0) • 01 = din_ch(6) = di_i(1) • 10 = din_ch(6) = di_i(2) • 11 = din_ch(6) = di_i(3)
12				
11	DINVM5[1:0]	R	0	Channel 5 DIN Mask: • 00 = din_ch(5) = di_i(0) • 01 = din_ch(5) = di_i(1) • 10 = din_ch(5) = di_i(2) • 11 = din_ch(5) = di_i(3)
10				
9	DINVM4[1:0]	R	0	Channel 4 DIN Mask: • 00 = din_ch(4) = di_i(0) • 01 = din_ch(4) = di_i(1) • 10 = din_ch(4) = di_i(2) • 11 = din_ch(4) = di_i(3)
8				
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R		

8.4.13 Output control in fail-safe shift register (CR65–OUTFSSR)

Table 66. Output control in fail-safe shift register (CR65–OUTFSSR)

Address 0x1Ch				
Bit	Name	Access	Reset	Content
15	OUTCTRL_FS7	R	0	OUTCTRL_FS7 Bit controls output state in FS of channel 7 • 1 = output Enabled • 0 = output Disabled
14	OUTCTRL_FS6	R	0	OUTCTRL_FS6 Bit controls output state in FS of channel 6 • 1 = output Enabled

Address 0x1Ch				
Bit	Name	Access	Reset	Content
				• 0 = output Disabled
13	OUTCTRL_FS5	R	0	OUTCTRL_FS5 Bit controls output state in FS of channel 5 • 1 = output Enabled • 0 = output Disabled
12	OUTCTRL_FS4	R	0	OUTCTRL_FS4 Bit controls output state in FS of channel 4 • 1 = output Enabled • 0 = output Disabled
11	OUTCTRL_FS3	R	0	OUTCTRL_FS3 Bit controls output state in FS of channel 3 • 1 = output Enabled • 0 = output Disabled
10	OUTCTRL_FS2	R	0	OUTCTRL_FS2 Bit controls output state in FS of channel 2 • 1 = output Enabled • 0 = output Disabled
9	OUTCTRL_FS1	R	0	OUTCTRL_FS1 Bit controls output state in FS of channel 1 • 1 = output Enabled • 0 = output Disabled
8	OUTCTRL_FS0	R	0	OUTCTRL_FS0 Bit controls output state in FS of channel 0 • 1 = output Enabled • 0 = output Disabled
7	DIS_CONF_OUT_FS	R	0	Disable Configuration stored in NVM for Outputs pins • 1 = OUTCTRL_FS stored in NVM Disabled • 0 = OUTCTRL_FS stored in NVM Enabled
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R	0	Parity bit

8.4.14 Enable control in fail-safe shift register (CR66–ENFSSR)

Table 67. Enable control in fail-safe shift register (CR66–ENFSSR)

Address 0x1Dh				
Bit	Name	Access	Reset	Content
15	ENCTRL_FS7	R	0	ENCTRL_FS7 Bit controls Enable pin state of channel 7 in Failsafe mode • 1 = EN Enabled • 0 = EN Disabled
14	ENCTRL_FS6	R	0	ENCTRL_FS6 Bit controls Enable pin state of channel 6 in Failsafe mode • 1 = EN Enabled • 0 = EN Disabled
13	ENCTRL_FS5	R	0	ENCTRL_FS5 Bit controls Enable pin state of channel 5 in Failsafe mode • 1 = EN Enabled • 0 = EN Disabled
12	ENCTRL_FS4	R	0	ENCTRL_FS4 Bit controls Enable pin state of channel 4 in Failsafe mode • 1 = EN Enabled

Address 0x1Dh				
Bit	Name	Access	Reset	Content
				• 0 = EN Disabled
11	ENCTRL_FS3	R	0	ENCTRL_FS3 Bit controls Enable pin state of channel 3 in Failsafe mode • 1 = EN Enabled • 0 = EN Disabled
10	ENCTRL_FS2	R	0	ENCTRL_FS2 Bit controls Enable pin state of channel 2 in Failsafe mode • 1 = EN Enabled • 0 = EN Disabled
9	ENCTRL_FS1	R	0	ENCTRL_FS1 Bit controls Enable pin state of channel 1 in Failsafe mode • 1 = EN Enabled • 0 = EN Disabled
8	ENCTRL_FS0	R	0	ENCTRL_FS0 Bit controls Enable pin state of channel 0 in Failsafe mode • 1 = EN Enabled • 0 = EN Disabled
7	DIS_CONF _FS	R	0	Disable Configuration stored in NVM for EN pins • 1 = ENCTRL _FS stored in NVM Disabled • 0 = ENCTRL _FS stored in NVM Enabled
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R	0	Parity bit

8.4.15 Enable control in standby shift register (CR67_01–ENSTDBYSR)

Table 68. Enable control in standby shift register (CR67_01–ENSTDBYSR)

Address 0x1Eh				
Bit	Name	Access	Reset	Content
15	ENCTRL_STDBY7	R	0	ENCTRL_STDBY7 Bit controls Enable pin state of channel 7 in Standby mode • 1 = EN Enabled • 0 = EN Disabled
14	ENCTRL_STDBY6	R	0	ENCTRL_STDBY6 Bit controls Enable pin state of channel 6 in Standby mode • 1 = EN Enabled • 0 = EN Disabled
13	ENCTRL_STDBY5	R	0	ENCTRL_STDBY5 Bit controls Enable pin state of channel 5 in Standby mode • 1 = EN Enabled • 0 = EN Disabled
12	ENCTRL_STDBY4	R	0	ENCTRL_STDBY4 Bit controls Enable pin state of channel 4 in Standby mode • 1 = EN Enabled • 0 = EN Disabled
11	ENCTRL_STDBY3	R	0	ENCTRL_STDBY3 Bit controls Enable pin state of channel 3 in Standby mode • 1 = EN Enabled • 0 = EN Disabled
10	ENCTRL_STDBY2	R	0	ENCTRL_STDBY2 Bit controls Enable pin state of channel 2 in Standby mode • 1 = EN Enabled

Address 0x1Eh				
Bit	Name	Access	Reset	Content
				• 0 = EN Disabled
9	ENCTRL_STDBY1	R	0	ENCTRL_STDBY1 Bit controls Enable pin state of channel 1 in Standby mode • 1 = EN Enabled • 0 = EN Disabled
8	ENCTRL_STDBY0	R	0	ENCTRL_STDBY0 Bit controls Enable pin state of channel 0 in Standby mode • 1 = EN Enabled • 0 = EN Disabled
7	EN_CONF _STDBY	R	0	Enable Configuration stored in NVM for EN pins • 1 = ENCTRL _STDBY stored in NVM Enabled • 0 = ENCTRL _ STDBY stored in NVM Disabled
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R	0	Parity bit

8.4.16 Output current registers from channels 0 to 7 (SR(20:27)–IOUTxSR)

The register contains the digital value of the current flowing on the selected channel. It reports the result of the digital current conversion.

Table 69. Output current registers from channels 0 to 7 (SR(20:27)–IOUTxSR)

Address 0x20h to 0x27h				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	IOUTxSR[9:0]	R	0	The 10 bit register contains the digital value of xChannel IOUT The current sense registers update is disabled when the channel is in off state.
12				
11				
10				
9				
8				
7				
6				
5				
4				
3	Not used	R	0	
2	CS_DIAG	R	0	When 1: xChannel in Diagnostic Mode
1	UPDTIxSR	R	0	Updated status bit. This bit is set when the value is updated and cleared when register is read
0	PARITY	R	0	Parity bit

8.4.17 Output voltage registers from channels 0 to 7 (SR(21:28)–VOUTxSR)

The register contains the digital value of the output voltage on the selected channel. It reports the result of the digital voltage conversion.

Table 70. Output voltage registers from channels 0 to 7 (SR(21:28)–VOUTxSR)

Address 0x28h to 0x2Fh				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	VOUTxSR[9:0]	R	0	The 10 bit register contains the digital value of xChannel VOUT
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTVxSR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

8.4.18 TJ register from channels 0 to 7 (SR(29:36)–TJxSR)

The register contains the result of the digital conversion of the case temperature.

Table 71. TJ register from channels 0 to 7 (SR(29:36)–TJxSR)

Address 0x30h to 0x37h				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	TJxSR[9:0]	R	0	The 10-bit register contains the TJ digital value
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	

Address 0x30h to 0x37h				
Bit	Name	Access	Reset	Content
3	Not used	R	0	
2	Not used	R	0	
1	UPDTTJxSR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

8.4.19 VCC register (SR37–VCCSR)

The register contains the result of the digital conversion of the V_{CC} voltage.

Table 72. VCC register (SR37–VCCSR)

Address 0x38h				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	VCCSR[9:0]	R	0	The 10-bit register contains the VCC digital value
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTVCSR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

8.4.20 ADC self-test (low level) current value for channel 0 (SR38–CSADCL0SR)

Table 73. ADC self-test (low level) current value for channel 0 (SR38–CSADCL0SR)

Address 0x41h: 0x01h page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	CSADCL0SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	

Address 0x41h: 0x01h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
9	CSADCL0SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTCS0LSR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.21 ADC self-test (medium level) current value for channel 0 (SR39–CSADCM0SR)

Table 74. ADC self-test (medium level) current value for channel 0 (SR39–CSADCM0SR)

Address 0x42h: 0x02h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCM0SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTM0SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.22 ADC self-test (high level) current value for channel 0 (SR40–CSADCH0SR)

Table 75. ADC self-test (high level) current value for channel 0 (SR40–CSADCH0SR)

Address 0x43h: 0x03h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCH0SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTH0SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.23 ADC self-test (low level) current value for channel 1 (SR41–CSADCL1SR)

Table 76. ADC self-test (low level) current value for channel 1 (SR41–CSADCL1SR)

Address 0x44h: 0x04h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCL1SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	

Address 0x44h: 0x04h page 1				
Bit	Name	Access	Reset	Content
3	Not used	R	0	
2	Not used	R	0	
1	UPDTL1SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.24 ADC self-test (medium level) current value for channel 1 (SR42–CSADCM1SR)

Table 77. ADC self-test (medium level) current value for channel 1 (SR42–CSADCM1SR)

Address 0x45h: 0x05h page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	CSADCM1SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTM1SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.25 ADC self-test (high level) current value for channel 1 (SR43–CSADCH1SR)

Table 78. ADC self-test (high level) current value for channel 1 (SR43–CSADCH1SR)

Address 0x46h: 0x06h page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	CSADCH1SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test

Address 0x46h: 0x06h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
12	CSADCH1SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTHxSR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.26 ADC self-test (low level) current value for channel 2 (SR44–CSADCL2SR)

Table 79. ADC self-test (low level) current value for channel 2 (SR44–CSADCL2SR)

Address 0x47h: 0x07h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCL2SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTL2SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.27 ADC self-test (medium level) current value for channel 2 (SR45–CSADCM2SR)

Table 80. ADC self-test (medium level) current value for channel 2 (SR45–CSADCM2SR)

Address 0x48h: 0x08h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCM2SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTM2SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.28 ADC self-test (high level) current value for channel 2 (SR46–CSADCH2SR)

Table 81. ADC self-test (high level) current value for channel 2 (SR46–CSADCH2SR)

Address 0x49h: 0x09h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCH2SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	

Address 0x49h: 0x09h page 1				
Bit	Name	Access	Reset	Content
5	CSADCH2SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTH2SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.29 ADC self-test (low level) current value for channel 3 (SR47–CSADCL3SR)

Table 82. ADC self-test (low level) current value for channel 3 (SR47–CSADCL3SR)

Address 0x4Ah: 0x0Ah page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	CSADCL3SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTL3SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.30 ADC self-test (medium level) current value for channel 3 (SR48–CSADCM3SR)

Table 83. ADC self-test (medium level) current value for channel 3 (SR48–CSADCM3SR)

Address 0x4Bh: 0x0Bh page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	

Address 0x4Bh: 0x0Bh page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
14	Not used	R	0	
13	CSADCM3SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTM3SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.31 ADC self-test (high level) current value for channel 3 (SR49–CSADCH3SR)

Table 84. ADC self-test (high level) current value for channel 3 (SR49–CSADCH3SR)

Address 0x4Ch: 0x0Ch page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCH3SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTH3SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.32 ADC self-test (low level) current value for channel 4 (SR50–CSADCL4SR)

Table 85. ADC self-test (low level) current value for channel 4 (SR50–CSADCL4SR)

Address 0x4Dh: 0x0Dh page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCL4SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTL4SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.33 ADC self-test (medium level) current value for channel 4 (SR51–CSADCM4SR)

Table 86. ADC self-test (medium level) current value for channel 4 (SR51–CSADCM4SR)

Address 0x4Eh: 0x0Eh page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCM4SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	

Address 0x4Eh: 0x0Eh page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
5	CSADCM4SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTM4SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.34 ADC self-test (high level) current value for channel 4 (SR52–CSADCH4SR)

Table 87. ADC self-test (high level) current value for channel 4 (SR52–CSADCH4SR)

Address 0x4Fh: 0x0Fh page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCH4SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTH4SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.35 ADC self-test (low level) current value for channel 5 (SR53–CSADCL5SR)

Table 88. ADC self-test (low level) current value for channel 5 (SR53–CSADCL5SR)

Address 0x50h: 0x10h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	

Address 0x50h: 0x10h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
14	Not used	R	0	
13	CSADCL5SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTL5SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.36 ADC self-test (medium level) current value for channel 5 (SR54–CSADCM5SR)

Table 89. ADC self-test (medium level) current value for channel 5 (SR54–CSADCM5SR)

Address 0x51h: 0x11h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCM5SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTM5SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.37 ADC self-test (high level) current value for channel 5 (SR55–CSADCH5SR)

Table 90. ADC self-test (high level) current value for channel 5 (SR55–CSADCH5SR)

Address 0x52h: 0x12h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCH5SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTH5SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.38 ADC self-test (low level) current value for channel 6 (SR56–CSADCL6SR)

Table 91. ADC self-test (low level) current value for channel 6 (SR56–CSADCL6SR)

Address 0x53h: 0x13h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCL6SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	

Address 0x53h: 0x13h page 1				
Bit	Name	Access	Reset	Content
5	CSADCL6SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTL6SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.39 ADC self-test (medium level) current value for channel 6 (SR57–CSADCM6SR)

Table 92. ADC self-test (medium level) current value for channel 6 (SR57–CSADCM6SR)

Address 0x54h: 0x14h page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	CSADCM6SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTM6SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.40 ADC self-test (high level) current value for channel 6 (SR58–CSADCH6SR)

Table 93. ADC self-test (high level) current value for channel 6 (SR58–CSADCH6SR)

Address 0x55h: 0x15h page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	

Address 0x55h: 0x15h page 1				
Bit	Name	Access	Reset	Content
14	Not used	R	0	
13	CSADCH6SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTH6SR	R	0	Updated status bit. This bit is set when the value is updated and cleared when the register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address clears all clearable bits independently on payload content.

8.4.41 ADC self-test (low level) current value for channel 7 (SR59–CSADCL7SR)

Table 94. ADC self-test (low level) current value for channel 7 (SR59–CSADCL7SR)

Address 0x56h: 0x16h page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	CSADCL7SR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTL7SR	R	0	Updated status bit. This bit is set when value is updated and cleared when register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently on payload content.

8.4.42 ADC self-test (medium level) current value for channel 7 (SR60–CSADCM7SR)

Table 95. ADC self-test (medium level) current value for channel 7 (SR60–CSADCM7SR)

Address 0x57h: 0x17h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCM7SR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTM7SR	R	0	Updated status bit. This bit is set when value is updated and cleared when register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently on payload content.

8.4.43 ADC self-test (high level) current value for channel 7 (SR61–CSADCH7SR)

Table 96. ADC self-test (high level) current value for channel 7 (SR61–CSADCH7SR)

Address 0x58h: 0x18h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	CSADCH7SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	

Address 0x58h: 0x18h page 1				
Bit	Name	Access	Reset	Content
5	CSADCH7SR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTH7SR	R	0	Updated status bit. This bit is set when value is updated and cleared when register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently on payload content.

8.4.44 ADC self-test (low level) voltage value (SR62–VADCLSR)

Table 97. ADC self-test (low level) voltage value (SR62–VADCLSR)

Address 0x59h: 0x19h page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	VADCLSR[9:0]	R/C	0	The 10-bit register contains the digital value of low current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTVLSR	R	0	Updated status bit. This bit is set when value is updated and cleared when register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently on payload content.

8.4.45 ADC self-test (medium level) voltage value (SR63–VADCMSR)

Table 98. ADC self-test (medium level) voltage value (SR63–VADCMSR)

Address 0x5Ah: 0x1Ah page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	

Address 0x5Ah: 0x1Ah page 1				
Bit	Name	Access	Reset	Content
14	Not used	R	0	
13	VADCMSR[9:0]	R/C	0	The 10-bit register contains the digital value of medium current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTMSR	R	0	Updated status bit. This bit is set when value is updated and cleared when register is read
0	PARITY	R		

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently on payload content.

8.4.46 ADC self-test (high level) voltage value (SR64–VADCHSR)

Table 99. ADC self-test (high level) voltage value (SR64–VADCHSR)

Address 0x5Bh: 0x1Bh page 1				
Bit	Name	Access	Reset	Content
15	Not used	R	0	
14	Not used	R	0	
13	VADCHSR[9:0]	R/C	0	The 10-bit register contains the digital value of high current level used for self-test
12			0	
11			0	
10			0	
9			0	
8			0	
7			0	
6			0	
5			0	
4			0	
3	Not used	R	0	
2	Not used	R	0	
1	UPDTHSR	R	0	Updated status bit. This bit is set when value is updated and cleared when register is read
0	PARITY	R	1	

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently on payload content.

8.4.47 NVM CTM/ST programming–CMD (NVMCMD)

Table 100. NVM CTM/ST programming–CMD (NVMCMD)

Address 0x60h: 0x20h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	Not used	R	0	
14	Not used	R	0	
13	Not used	R	0	
12	Not used	R	0	
11	OP_REG[3:0]	R/W	0	NVM operation code 1010: Read 1011: Write 1100: Simulation
10			0	
9			0	
8			0	
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R		

8.4.48 NVM CTM/ST programming–data0 (byte1 and byte0) (NVMD0)

Table 101. NVM CTM/ST programming–data0 (byte1 and byte0) (NVMD0)

Address 0x61h: 0x21h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	DITH_STEP[2:0]	R/W	0	Dithering step
14				
13				
12	WD_TIME	R/W	0	Watchdog timer control
11				
10	DEEP_STANDBY_DIS	R/W	0	Disable of return in deep standby state
9	WR_COUNT	R	0	Number of NVM writings
8				
7				
6				
5				
4				
3				

Address 0x61h: 0x21h page 1				
Bit	Name	Access	Reset	Content
2	WR_COUNT	R	0	Number of NVM writings
1				
0	PARITY	R		Parity bit

8.4.49 NVM CTM/ST programming–data1 (byte3 and byte2) (NVMD1)

Table 102. **NVM CTM/ST programming–data1 (byte3 and byte2) (NVMD1)**

Address 0x62h: 0x22h page 1				
Bit	Name	Access	Reset	Content
15	I_THR6	R/W	0	IOUT threshold channel 6
14				
13	I_THR5	R/W	0	IOUT threshold channel 5
12				
11	I_THR4	R/W	0	IOUT threshold channel 4
10				
9	I_THR3	R/W	0	IOUT threshold channel 3
8				
7	I_THR2	R/W	0	IOUT threshold channel 2
6				
5	I_THR1	R/W	0	IOUT threshold channel 1
4				
3	I_THR0	R/W	0	IOUT threshold channel 0
2				
1	Not used	R	0	
0	PARITY	R		Parity bit

8.4.50 NVM CTM/ST programming–data2 (byte5 and byte4) (NVMD2)

Table 103. **NVM CTM/ST programming–data2 (byte5 and byte4) (NVMD2)**

Address 0x63h: 0x23h page 1				
Bit	Name	Access	Reset	Content
15	OUTCTRL7	R/W	0	Output state of channel 7
14	OUTCTRL6	R/W	0	Output state of channel 6
13	OUTCTRL5	R/W	0	Output state of channel 5
12	OUTCTRL4	R/W	0	Output state of channel 4
11	OUTCTRL3	R/W	0	Output state of channel 3
10	OUTCTRL2	R/W	0	Output state of channel 2
9	OUTCTRL1	R/W	0	Output state of channel 1
8	OUTCTRL0	R/W	0	Output state of channel 0
7	ENCTRL_STDBY3	R/W	0	Enable pin state of channel 3 in Standby mode (when EN_CONF_STDBY=1)

Address 0x63h: 0x23h page 1				
Bit	Name	Access	Reset	Content
6	ENCTRL_STDBY2	R/W	0	Enable pin state of channel 2 in Standby mode (when EN_CONF_STDBY=1)
5	ENCTRL_STDBY1	R/W	0	Enable pin state of channel 1 in Standby mode (when EN_CONF_STDBY=1)
4	ENCTRL_STDBY0	R/W	0	Enable pin state of channel 0 in Standby mode (when EN_CONF_STDBY=1)
3 2	I_THR7	R/W	0	IOUT threshold channel 7
1	Not used	R	0	
0	PARITY	R		

8.4.51 NVM CTM/ST programming–data3 (byte7 and byte6) (NVMD3)

Table 104. NVM CTM/ST programming–data3 (byte7 and byte6) (NVMD3)

Address 0x64h: 0x24h page 1				
Bit	Name	Access	Reset	Content
15 14 13 12 11 10 9 8	TMAX[7:0]	R/W	0	Timer expiration for Standby ON exit
7	ENCTRL_STDBY7	R/W	0	Enable pin state of channel 7 in Standby mode (when EN_CONF_STDBY=1)
6	ENCTRL_STDBY6	R/W	0	Enable pin state of channel 6 in Standby mode (when EN_CONF_STDBY=1)
5	ENCTRL_STDBY5	R/W	0	Enable pin state of channel 5 in Standby mode (when EN_CONF_STDBY=1)
4	ENCTRL_STDBY4	R/W	0	Enable pin state of channel 4 in Standby mode (when EN_CONF_STDBY=1)
3	EN_CONF_STDBY	R/W	0	Configuration of Enable pins in Standby mode: • 0 = ENCTRL registers set EN pins in Standby mode • 1 = ENCTRL_STDBY NVM bits set EN pins in Standby mode
2	Not used	R	0	
1	Not used	R	0	

8.4.52 NVM CTM/ST programming–data4 (byte9 and byte8) (NVMD4)

Table 105. NVM CTM/ST programming–data4 (byte9 and byte8) (NVMD4)

Address 0x65h: 0x25h page 1				
Bit	Name	Access	Reset	Content
15 14	DINVM3[1:0]	R/W	0	Channel 3 direct input configuration
13 12	DINVM2[1:0]	R/W	0	Channel 2 direct input configuration
11	DINVM1[1:0]	R/W	0	Channel 1 Direct input configuration

Address 0x65h: 0x25h page 1				
Bit	Name	Access	Reset	Content
10	DINVM1[1:0]	R/W	0	Channel 1 Direct input configuration
9 8	DINVM0[1:0]	R/W	0	Channel 0 direct input configuration
7	ENCTRL_FS3	R/W	0	Enable pin state of channel 3 in fail-safe mode (when DIS_CONF_FS=0)
6	ENCTRL_FS2	R/W	0	Enable pin state of channel 2 in fail-safe mode (when DIS_CONF_FS=0)
5	ENCTRL_FS1	R/W	0	Enable pin state of channel 1 in fail-safe mode (when DIS_CONF_FS=0)
4	ENCTRL_FS0	R/W	0	Enable pin state of channel 0 in fail-safe mode (when DIS_CONF_FS=0)
3	DIS_CONF_FS	R/W	0	Configuration of Enable pins in fail-safe mode: • 1 = ENCTRL registers set EN pins in fail-safe mode OR faults occurring on the channels • 0 = ENCTRL_FS NVM bits set EN pins in fail-safe mode OR faults occurring on the channels
2	DIS_CONF_OUT_FS	R/W	0	Configuration of Output pins in fail-safe mode: • 1 = OUTCTRL registers set OUT pins in fail-safe mode • 0 = OUTCTRL_FS NVM bits set OUT pins in fail-safe mode OR DIx pins based on DIx mapping
1	Not used	R	0	
0	PARITY	R		Parity bit

8.4.53 NVM CTM/ST programming–data5 (byte11 and byte10) (NVMD5)

Table 106. NVM CTM/ST programming–data5 (byte11 and byte10) (NVMD5)

Address 0x66h: 0x26h page 1				
Bit	Name	Access	Reset	Content
15 14	DINVM7[1:0]	R/W	0	Channel 7 direct input configuration
13 12	DINVM6[1:0]	R/W	0	Channel 6 direct input configuration
11 10	DINVM5[1:0]	R/W	0	Channel 5 direct input configuration
9 8	DINVM4[1:0]	R/W	0	Channel 4 direct input configuration
7	ENCTRL_FS7	R/W	0	Enable pin state of channel 7 in fail-safe mode (when DIS_CONF_FS=0)
6	ENCTRL_FS6	R/W	0	Enable pin state of channel 6 in fail-safe mode (when DIS_CONF_FS=0)
5	ENCTRL_FS5	R/W	0	Enable pin state of channel 5 in fail-safe mode (when DIS_CONF_FS=0)
4	ENCTRL_FS4	R/W	0	Enable pin state of channel 4 in fail-safe mode

Address 0x66h: 0x26h page 1				
Bit	Name	Access	Reset	Content
				(when DIS_CONF_FS=0)
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R		Parity bit

8.4.54 NVM CTM/ST programming–data6 (byte13 and byte12) (NVMD6)

Table 107. **NVM CTM/ST programming–data6 (byte13 and byte12) (NVMD6)**

Address 0x67h: 0x27h page 1				
Bit	Name	Access	Reset	Content
15	OUTCTRL_FS7	R/W	0	Output pin state of channel 7 in fail-safe mode (when DIS_CONF_OUT_FS=0)
14	OUTCTRL_FS6	R/W	0	Output pin state of channel 6 in fail-safe mode (when DIS_CONF_OUT_FS=0)
13	OUTCTRL_FS5	R/W	0	Output pin state of channel 5 in fail-safe mode (when DIS_CONF_OUT_FS=0)
12	OUTCTRL_FS4	R/W	0	Output pin state of channel 4 in fail-safe mode (when DIS_CONF_OUT_FS=0)
11	OUTCTRL_FS3	R/W	0	Output pin state of channel 3 in fail-safe mode (when DIS_CONF_OUT_FS=0)
10	OUTCTRL_FS2	R/W	0	Output pin state of channel 2 in fail-safe mode (when DIS_CONF_OUT_FS=0)
9	OUTCTRL_FS1	R/W	0	Output pin state of channel 1 in fail-safe mode (when DIS_CONF_OUT_FS=0)
8	OUTCTRL_FS0	R/W	0	Output pin state of channel 0 in fail-safe mode (when DIS_CONF_OUT_FS=0)
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R		Parity bit

8.4.55 NVM CTM/ST programming–data7 (byte15 and byte14) (NVMD7)

Table 108. **NVM CTM/ST programming–data7 (byte15 and byte14) (NVMD7)**

Address 0x68h: 0x28h page 1				
Bit	**Name**	**Access**	**Reset**	**Content**
15	CRC	R/W	0	NVM single row CRC check
14			0	
13			0	
12			0	
11			0	
10			0	
9			0	
8			0	
7	Not used	R	0	
6	Not used	R	0	
5	Not used	R	0	
4	Not used	R	0	
3	Not used	R	0	
2	Not used	R	0	
1	Not used	R	0	
0	PARITY	R		

9 Application schematic

Figure 16. **Application schematic**

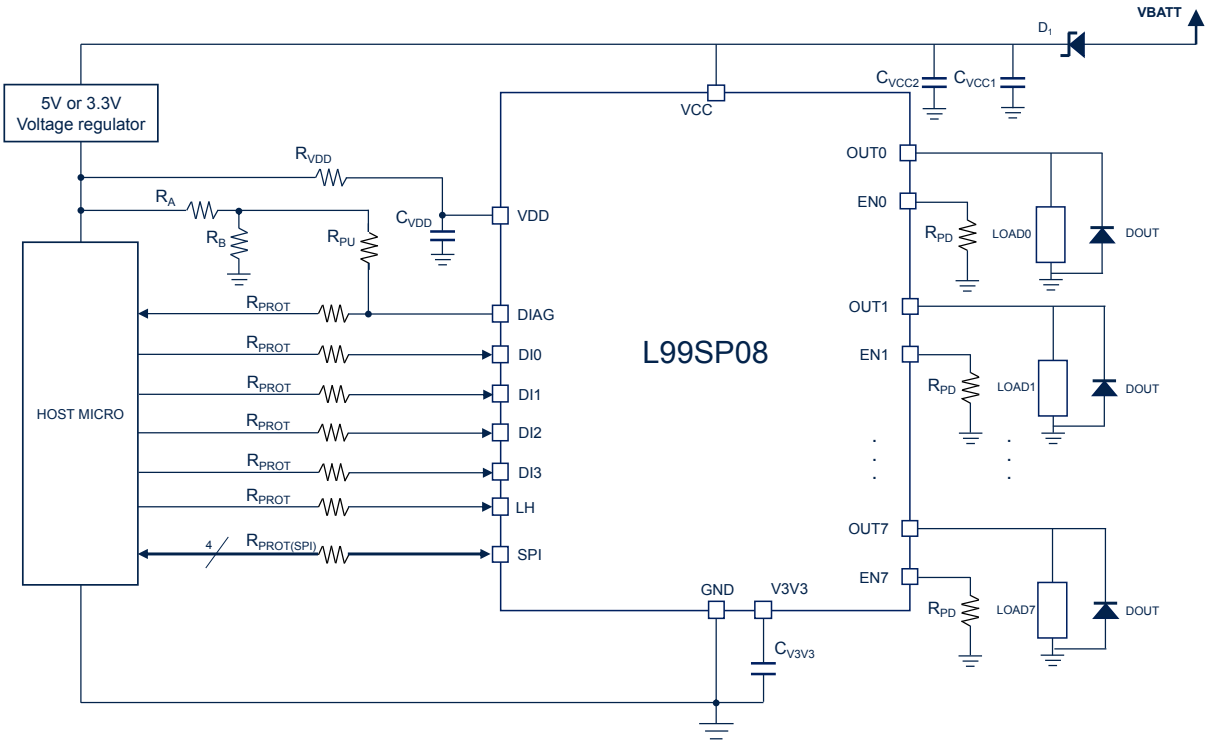


Table 109. **Component value**

Reference		Value
C_{VCC1}		2x 22 µF
C_{VCC2}		100 µF
C_{VDD}		330 nF
C_{V3V3}		1 µF
R_{PU}		4.7 kΩ
R_{VDD}		300 Ω
R_{PROT}		2.2 kΩ
$R_{PROT(SPI)}$	R_{CS}	50 mΩ
	R_{CLK}	50 mΩ
	R_{SDI}	50 mΩ
	R_{SDO}	100 Ω
R_{PD}		N.M. (1) 27 kΩ (2)
D_{OUT}		STPS5H100-Y
D_1		STPS2L60-Y (1)
R_A		0 Ω (3) 8.2 kΩ (4)

Reference	Value
R_B	N.M. (3) 15 kΩ (4)

1. *Stand alone applications.*
2. *Companion applications.*
3. *3.3 V applications.*
4. *5 V applications.*

Figure 17. Application diagram L99SP08 in combination with VNF9DxSF for parking mode functionality

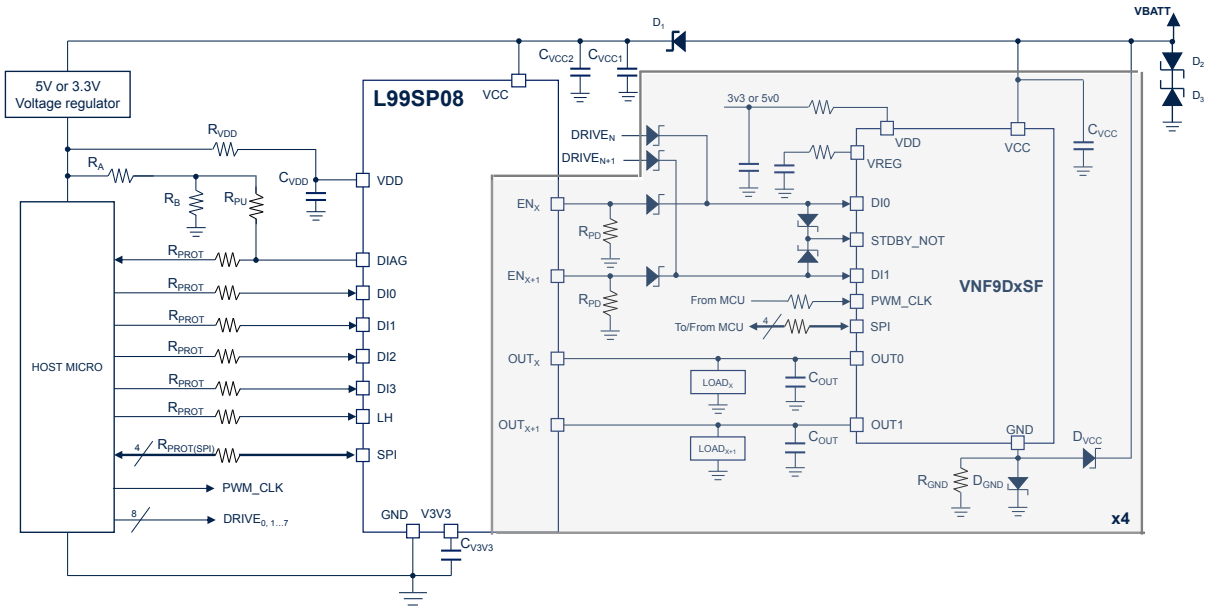
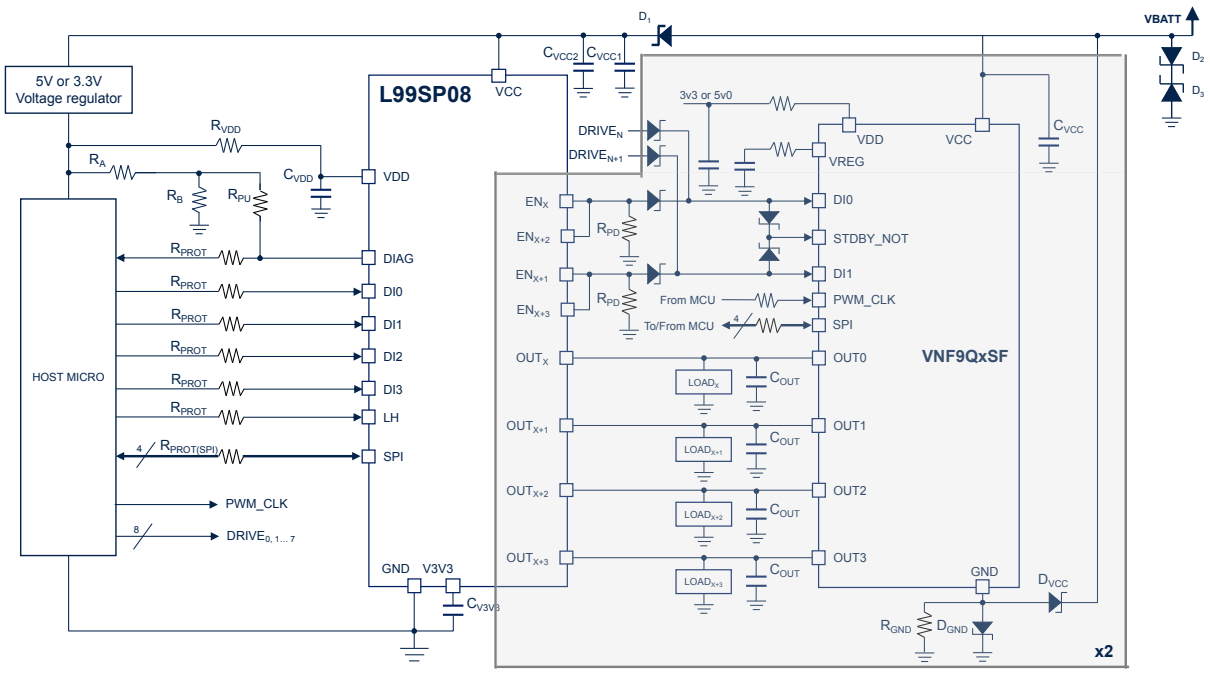


Figure 18. Application diagram L99SP08 in combination with VNF9QxSF for parking mode functionality



Note: The reported connection of EN pins to DI0-DI1 considers the default association of OUT0+OUT2 with DI0 and OUT1+OUT3 to DI1.

The direct control of the DIx pins of the VNF9DxSF (or the VNFQxSF) by the MCU GPIO is optional, as the L99SP08 can activate its ENx pins through appropriate SPI commands.

However, directly connecting the DIx pins of the VNF9DxSF (or the VNFQxSF) to the MCU GPIO ensures control of the VNF9DxSF (or the VNFQxSF) even if the SPI communication between the L99SP08 and the MCU fails.

For further information on the usage of the L99SP08 in combination with the hybrid and monolithic STi^{2}Fuse devices for parking mode functionality refer to the related application notes AN6025 and AN6371.

10 Package and PCB thermal data

10.1 QFN (5x5mm) thermal data

Figure 19. **QFN (5x5 mm) PCB 4 layers**

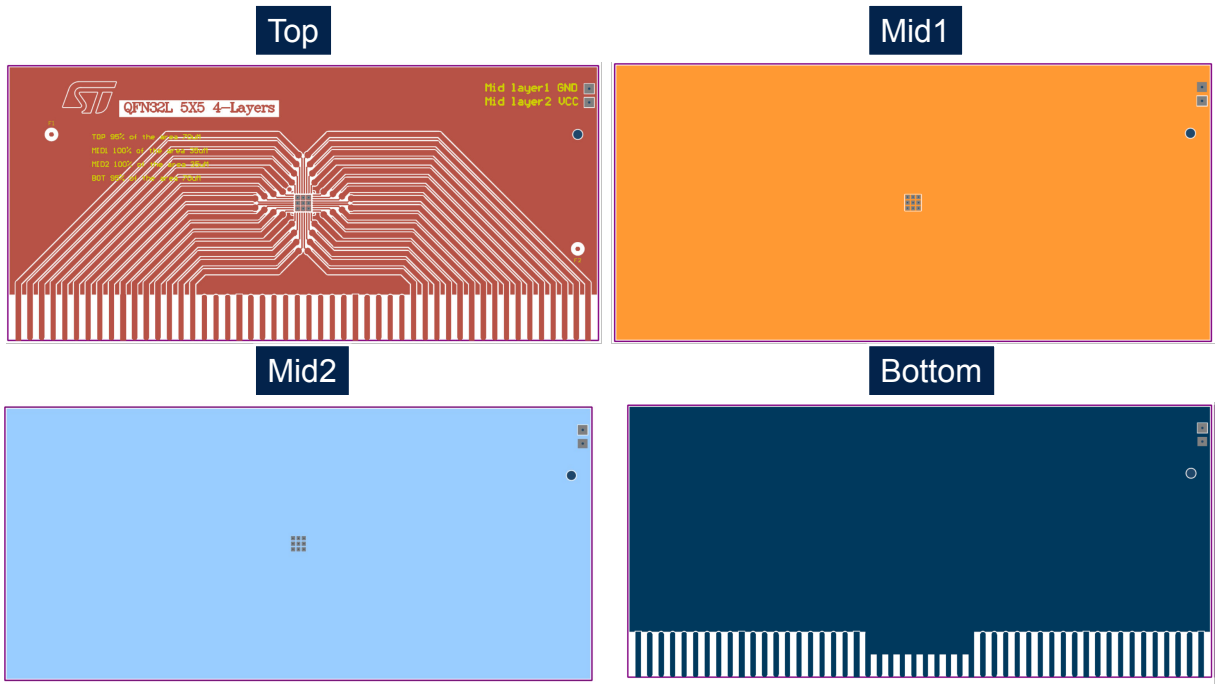


Table 110. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm ±10%
Board dimension	129 mm x 60 mm
Board material	FR4
Cu thickness (top and bottom layers)	0.070 mm
Cu thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal vias diameter	0.3 mm ±0.08 mm
Cu thickness on vias	0.025 mm
Footprint dimension (top layer)	3.5 mm x 3.5 mm

R_{thJA} on 4 layers PCB: 25.5 °C/W, measurement performed according to JESD51.2 in natural convection (still air).

11 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 QFN 5x5x0.9 mm 32+4L wettable flanks package information

Figure 20. QFN 5x5x0.9 mm 32+4L wettable flanks package outline

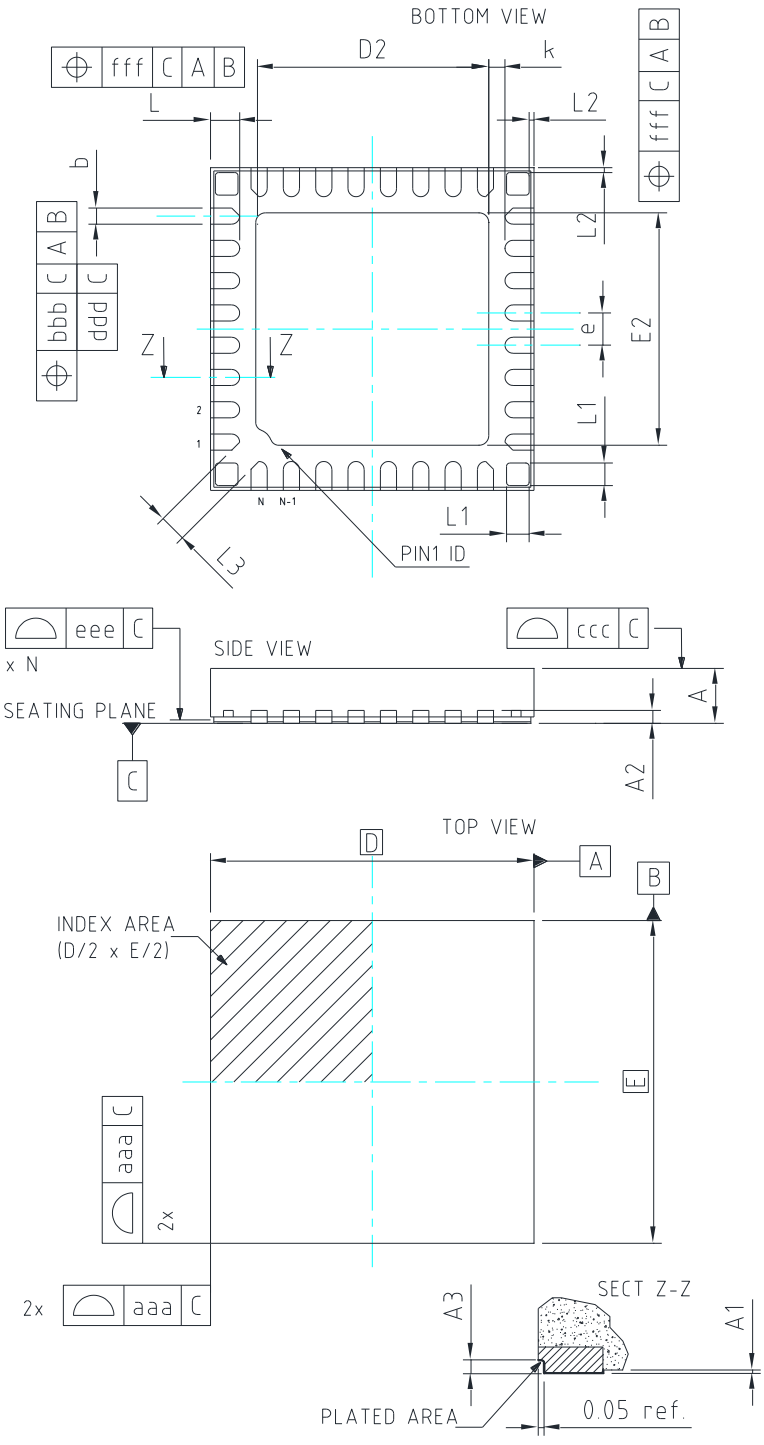


Table 111. **QFN 5x5x0.9 mm 32+4L wettable flanks mechanical data**

	Dimension [mm]		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.2 REF	
A3	0.10		
b	0.20	0.25	0.30
D		5.00	
e		0.50	
E		5.00	
L	0.35	0.45	0.55
L1		0.35	
L2		0.075	
L3		0.42	
k	0.20		
N		32 + 4	

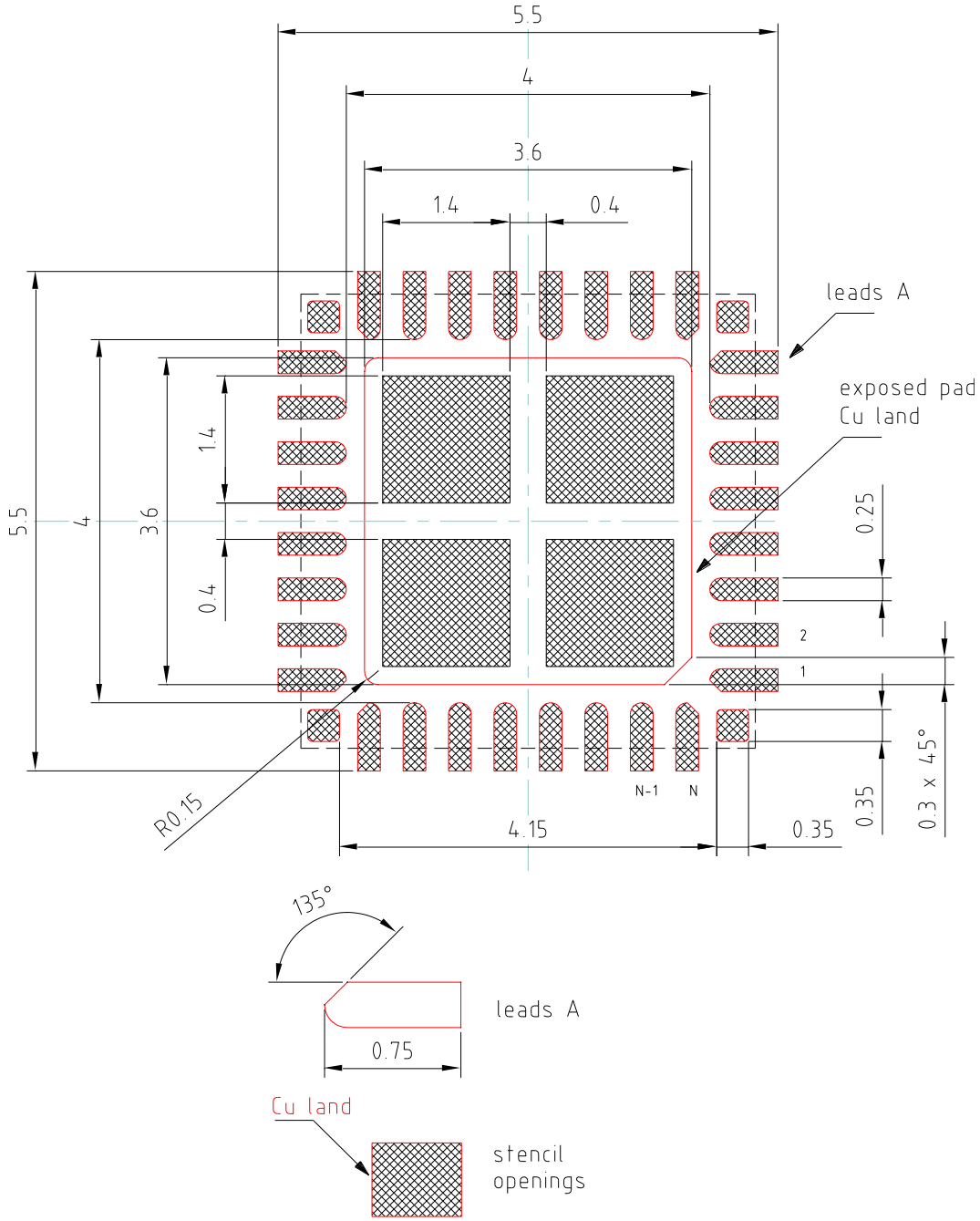
Table 112. **Tolerance of form and position**

Symbol	Tolerance
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Table 113. **Exposed pad variation**

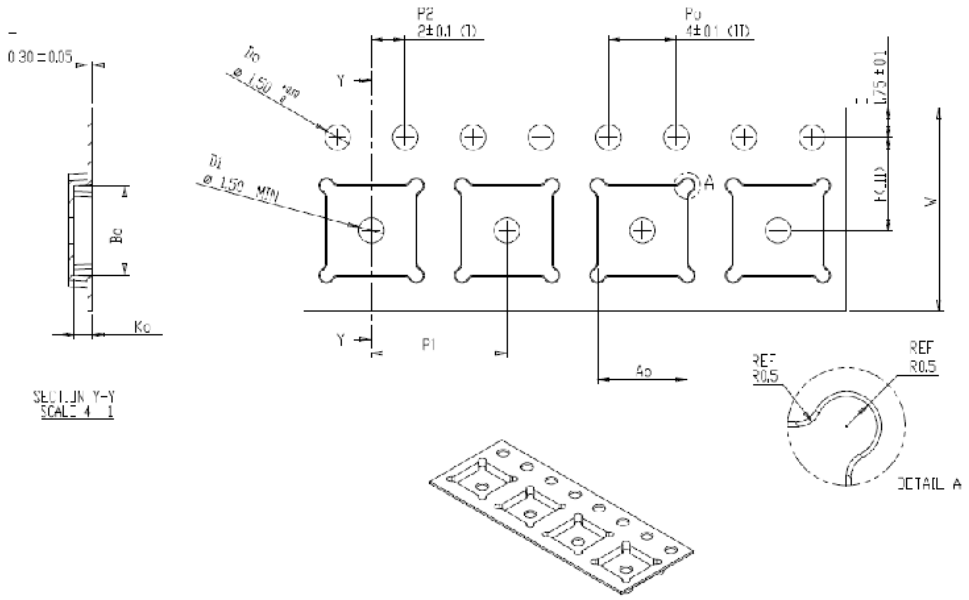
	Dimension [mm]		
	Min.	Typ.	Max.
D2	3.55	3.60	3.65
E2	3.55	3.60	3.65

Figure 21. **QFN 5x5x0.9 mm 32+4L wettable flanks suggested footprint**



11.2 QFN 5x5x0.9 mm 32+4L wettable flanks packing information

Figure 22. **QFN 5x5x0.9 mm 32+4L wettable flanks carrier tape**



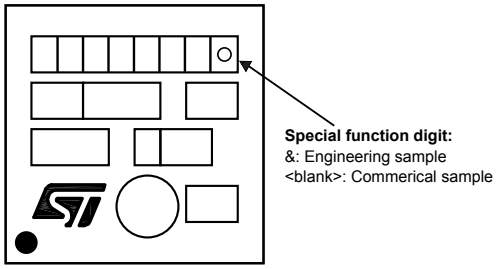
Note: (I) (III) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of sprocket holes is ± 020.

Table 114. **QFN 5x5x0.9 mm 32+4L wettable flanks mm carrier tape**

Description	Value [mm]
A0	5.30 ± 0.1
B0	5.30 ± 0.1
K0	1.10 ± 0.1
F	5.50 ± 0.1
P1	8.00 ± 0.1
W	12.00 ± 0.1

11.3 QFN 5x5x0.9 mm 32+4L wettable flanks marking information

Figure 23. **QFN 5x5x0.9 mm 32+4L wettable flanksmarking information**



Parts marked as '&' are not yet qualified and therefore not approved for use in production. STMicroelectronics is not responsible for any consequences resulting from such use. In no event will STMicroelectronics be liable for the customer using any of these engineering samples in production. STMicroelectronics's quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

12 Ordering information

Table 115. **Ordering information**

Order code	Package	Package marking	Packing
L99SP08TR	QFN 5x5x0.9 mm 32+4L wettable flanks	L99SP08	Tape and reel

Revision history

Table 116. **Document revision history**

Date	Revision	Changes
03-Jul-2023	1	Initial release.
29-Jul-2024	2	Updated Features and Description on cover page. Updated Table 2. Absolute maximum rating, Table 4. Supply specification, Table 6. SPI logic outputs (SDO) specification, Table 7. SPI timing specification, Table 8. ENx pin specification, Table 10. Digital timings specification, Table 14. Current sense amplifier with integrated ADC, Table 15. P-channel bypass switch specification, and Table 16. Overvoltage specification. Updated Figure 4. Device state diagram, Section 3.1: Operating modes, Section 3.1.3: Fail-safe mode, Section 3.1.4: Normal mode, Figure 5. Standby on exit strategy, Section 3.3: Channel enable (ENx) pin behavior, Section 3.4: DIAG pin behavior, Section 3.6: Oscillator 20 MHz, Section 3.9: ADC current sense, Section 3.10: Capacitive charging mode (CCM) and Section 3.11: Voltage ADC. Moved *3.1.3 Fail-safe mode* to Section 3.1.3: Fail-safe mode. Added Section 3.1.1: Deep standby mode and Section 3.5: OUTPUT control in fail-safe mode. Updated title from "*Section 4. Protections*" to Section 4: Protections and diagnostics, added Section 4.2: Bandgap stuck, and Table 21. Customer data map. Updated Section 4.1: Oscillator stuck, Section 4.3: Overtemperature, Section 4.4: Output and battery voltages monitoring, Section 4.5: Current sense standby on self-test, and Figure 8. NVM direct read. Added Section 5: DIx input management and Section 6: Built-in self-test. Added Section 8.2.1: Register map pages management and updated Table 38. RAM memory map, Table 39. ROM memory map, Section 8.3.1: Page control register (CR0–PAGECR1/2), Section 8.3.2: Central control register (CR1–CTRLR1), Section 8.3.3: Central control register (CR2–CTRLR2), Section 8.3.5: Channels 0-1 control register (CR4–CHCR1), Section 8.3.6: Channels 2-3 control register (CR5–CHCR2), Section 8.3.7: Channels 4-5 control register (CR6–CHCR3), Section 8.3.8: Channels 6-7 control register (CR7–CHCR4), and added Section 8.3.10: WD toggling control registers (CR20-WDTCR0/1). Updated Section 8.4.1: Central status register (SR1–SREG), Section 8.4.3: Channels 2-3 status register (SR3–CHSR2),Section 8.4.4: Channels 4-5 status register (SR4–CHSR3), Section 8.4.5: Channels 6-7 status register (SR5–CHSR4), Section 8.4.6: TMAX status register (SR6–TMAXSR). Updated title "*Section 6.4.7 CS ADC status register (SR7–CSADCSR)*" and its content to Section 8.4.7: CS_DIAG status register (SR7–CSDIAGSR). Updated Section 8.4.8: CS bist status register (SR8–CSBSR),Section 8.4.9: NVM shadows status register (SR9–NVMSHSR), and Section 8.4.10: NVM CRC check status Register (SR10–NVMCRCSR). Added Section 8.4.13: Output control in fail-safe shift register (CR65–OUTFSSR), Section 8.4.14: Enable control in fail-safe shift register (CR66–ENFSSR), Section 8.4.15: Enable control in standby shift register (CR67_01–ENSTDBYSR), and Section 8.4.16: Output current registers from channels 0 to 7 (SR(20:27)–IOUTxSR). Updated Section 8.4.18: TJ register from channels 0 to 7 (SR(29:36)–TJxSR), Section 8.4.37: ADC self-test (high level) current value for channel 5 (SR55–CSADCH5SR), Section 8.4.47: NVM CTM/ST programming–CMD (NVMCMD), Section 8.4.48: NVM CTM/ST programming–data0 (byte1 and byte0) (NVMD0), Section 8.4.49: NVM CTM/ST programming–data1 (byte3 and byte2) (NVMD1), Section 8.4.50: NVM CTM/ST programming–data2 (byte5 and byte4) (NVMD2), Section 8.4.51: NVM CTM/ST programming–data3 (byte7 and byte6) (NVMD3), Section 8.4.52: NVM CTM/ST programming–data4 (byte9 and byte8) (NVMD4), Section 8.4.53: NVM CTM/ST programming–data5 (byte11 and byte10) (NVMD5), Section 8.4.54: NVM CTM/ST programming–data6 (byte13 and byte12) (NVMD6), and Section 8.4.55: NVM CTM/ST programming–data7 (byte15 and byte14) (NVMD7). Added Section 9: Application schematic. Minor text changes.
08-Oct-2025	3	Update Section cover image and all package information with QFN 5x5x0.9 mm 32+4L wettable flanks data. Updated Description, Section 3.3, Section 3.1, Section 3.9, Section 3.10, Section 4.3, Section 4.4, Section 8.1. Added Section 10, Section 11.2, Section 11.3, Section 12. Updated Figure 1, Figure 2 (add note), Figure 3, Figure 4, Figure 16, and added Figure 17, Figure 18.

Date	Revision	Changes
		Updated Table 3, Table 4, Table 5, Table 7, Table 9, Table 10, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 21, Table 23, Table 24, Table 36, Table 38, Table 39, Table 64, Table 65, Table 69, Table 105, Table 106, Table 107, Table 109; updated address information in the header from Table 73 to Table 108.
13-Oct-2025	4	Updated Features, Table 111, and added Table 113.
17-Oct-2025	5	Updated Section 4.3 andSection 4.7; Table 62 and Table 63.

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