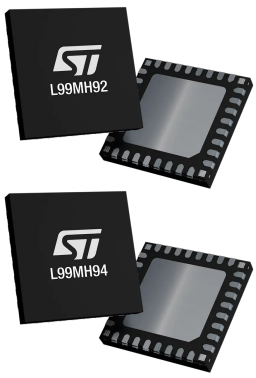
L99MH94, L99MH92

Datasheet

Automotive quad and dual half-bridge pre-driver



VFQFN32+4L WF
exposed pad down

VFQFN48L WF
exposed pad down

Product status link
L99MH94
L99MH92

Product summary		
Order code	**Package**	**Packing**
L99MH92Q5-TR L99MH94Q5-TR	VFQFN32+4L WF 5x5x0.9 mm	Tape and reel
L99MH94Q7-TR	VFQFN48L WF 7x7x0.9 mm	Tape and reel

Features

- AEC-Q100 qualified
- ISO26262 compliant, covering ASIL-B safety integrity level
- Quad (L99MH94) and dual (L99MH92) half-bridge, or dual (L99MH94) and single (L99MH92) H-Bridge, pre-driver
- Independent channel driver up to 4 (L99MH94) and 2 (L99MH92) high-side or 4 (L99MH94) and 2 (L99MH92) low-side
- Driving logic permits any H-bridge configuration, pairing different half-bridges, using the internal gate drivers (GHx/SHx/GLx can be associated to any GHy/SHy/GLy)
- Support logic level and standard level MOSFETs
- Control of reverse battery protection MOSFET
- Fully configurable half-bridge driver in case of fault occurrence
- Generator mode for power trunk/tailgate applications
- Supporting indirect current measurement of external MOSFETs
- SPI configurable overvoltage threshold
- Adaptive MOSFET gate control
  - Three steps gate control of external HS/LS
  - Improved electromagnetic emission
  - Programmable gate current up to 120 mA
  - Reduced switching losses in PWM mode
- V_{ds} monitoring
- Low IQ (1.05 µA) in reset mode
- High-side and low-side capable of protection and diagnosis
- Two external diodes control, needed for assisting calibration of indirect current measurement, can be used for steady - temperature monitoring
- Drain-source monitoring for short circuit detection
- Overtemperature warning and shutdown
- Timeout watchdog for MCU control
- Detailed off-state diagnostic (open load, short circuit to battery or short circuit to GND) via SPI
- Three PWM inputs
  - High-side and low-side PWM capable
  - Active freewheeling
  - Up to 50 kHz PWM frequency
- Out-of-frame serial peripheral interface (SPI), 24 bits
- QFN package with wettable flanks
- Green product (RoHS compliant)

Applications

- Seat control
- Steering column adjustment, gas pedal adjustment

- Sunroof, sliding doors, window lift, seat-belt pre-tensioners, cargo cover, washer pump
- Engine vibrations compensation system
- Power lift gate
- Central door lock

Description

The L99MH94 and L99MH92 integrate respectively a quad and a dual half-bridge pre-driver dedicated to control up to eight and four N-channel MOSFETs.

It is intended for DC motor control applications such as automotive power seat control or other applications.

A 24-bit serial peripheral interface (SPI) is used for configuring and controlling the eight half-bridges or four H-bridge. SPI status registers provide high-level diagnostic information such as supply voltage monitoring, the charge pump voltage monitoring, temperature warning and overtemperature shutdown.

Each gate driver monitors independently its external MOSFET drain-source voltage for fault conditions.

The L99MH94 / L99MH92 support indirect current measurement on external MOSFETs, allowing cost saving and lower system complexity, avoiding the usage of shunt resistors.

A more efficient gate current control of the external MOSFETs, called “three stages gate current”, decreases and optimizes electromagnetic interference (EMI).

Protection features (drain-source monitoring for short circuit detection, overtemperature warning and shutdown, timeout watchdog for MCU control, detailed off-state diagnostic via SPI) ensure the ASIL-B achievement according to ISO 26262 standard.

The L99MH94 is housed in VFQFN48L and VFQFN32L packages with an exposed pad, the L99MH92 is housed in a VFQFN32L package with exposed pad. These packages have wettable flanks for easy visual inspection of the solder joint.

1 Block diagram and pin description

1.1 Block diagram

Figure 1. **L99MH94 block diagram**

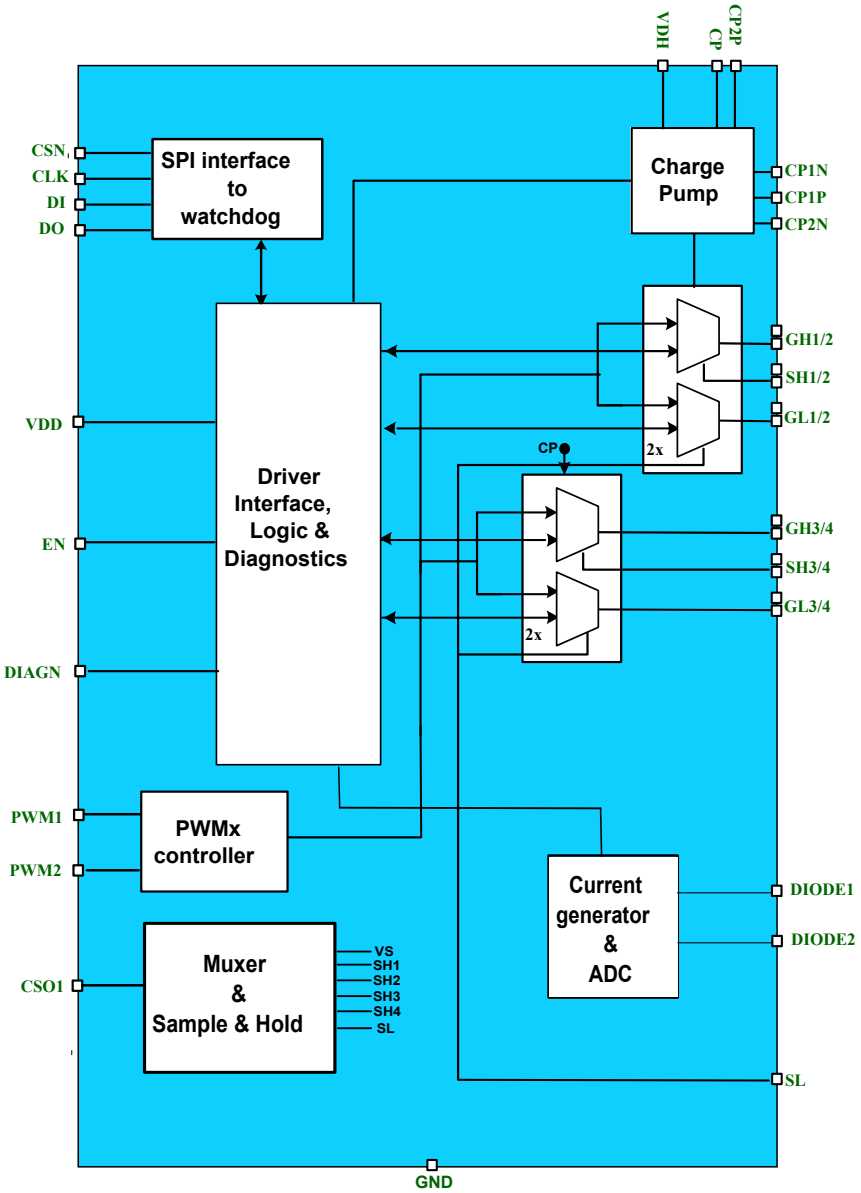
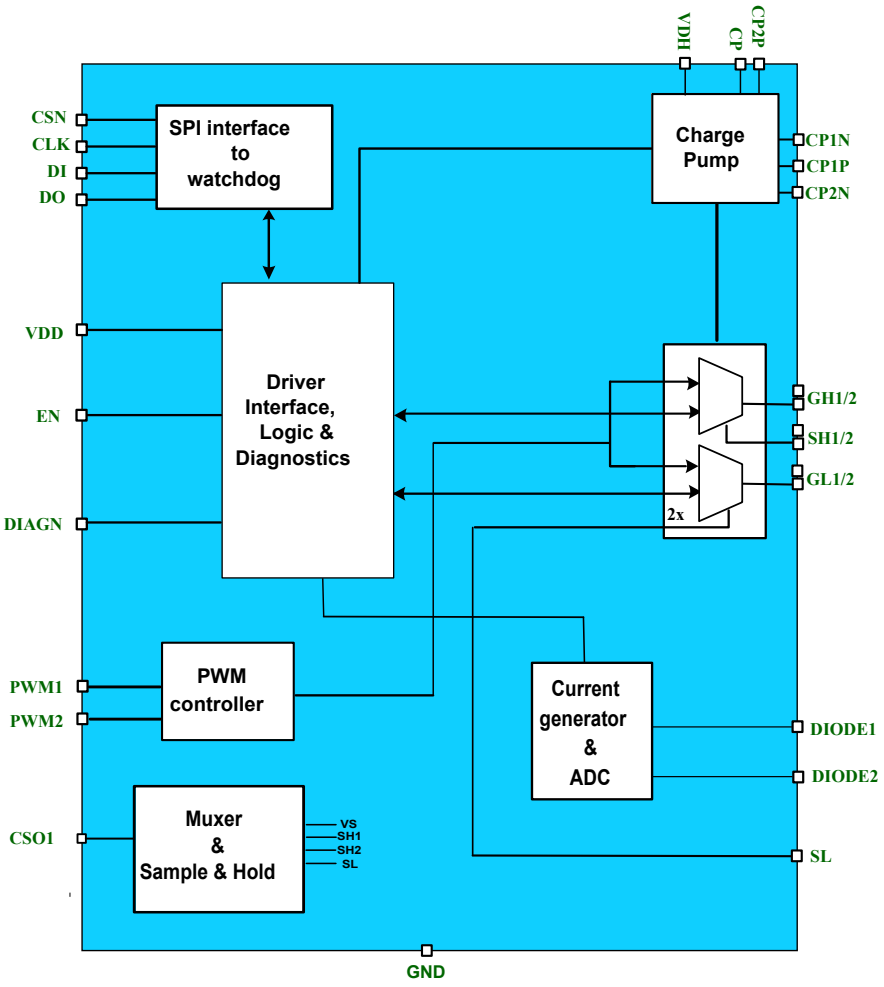


Figure 2. **L99MH92 block diagram**



1.2 Pin description

Figure 3. L99MH94 pin connection - VFQFN32 (top view)

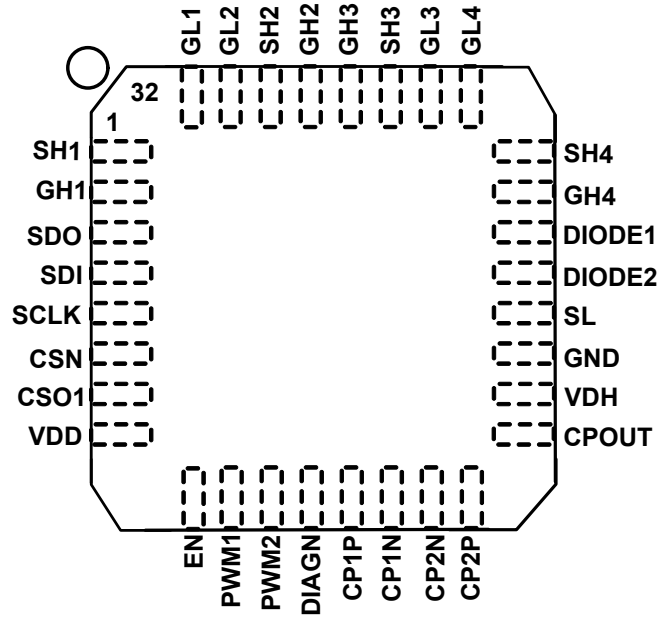


Figure 4. L99MH94 pin connection - VFQFN48 (top view)

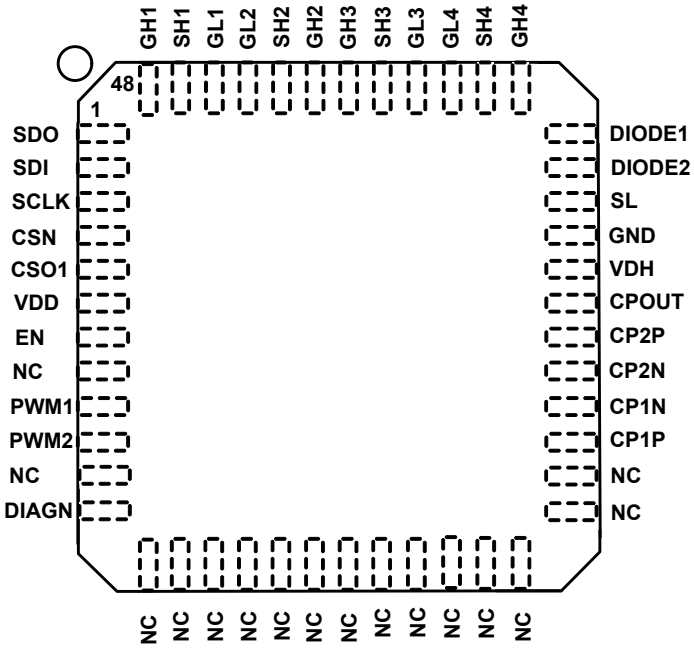


Figure 5. **L99MH92 pin connection (top view)**

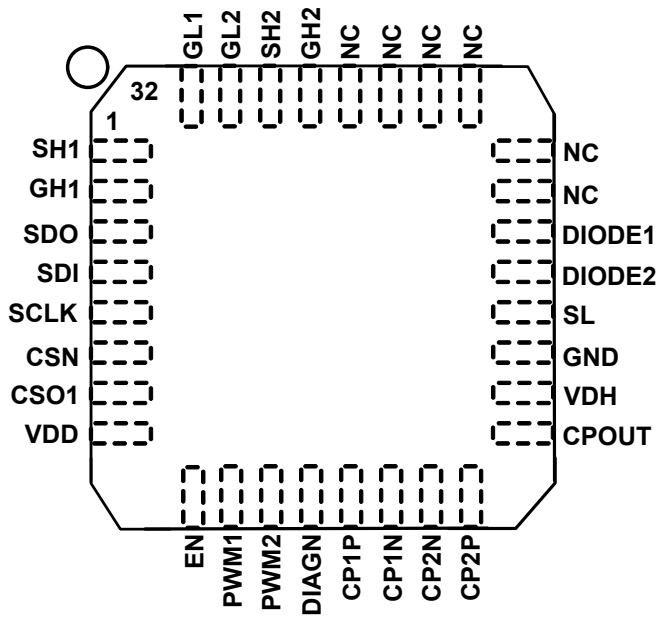


Table 1. **Pin function - VFQFN32**

Pin	L99MH94	L99MH92	Function
1	SH1		SH1 Source high-side 1: Connection to source of high-side MOSFET 1
2	GH1		GH1 Gate high-side 1: Analog output pin to turn on/off high-side MOSFET 1. Connect to the gate of high side
3	SDO		SDO Serial Data Output
4	SDI		SDI Serial Data Input with internal pull-down
5	SCLK		SCLK Serial Clock Input with internal pull-down
6	CSN		CSN Chip Select Not with internal pull-up
7	CSO1		CSO1 Current Sense Amplifier Output1
8	VDD		VDD Logic supply
9	EN		EN Enable input with internal pull-down
10	PWM1		PWM1: PWM input 1
11	PWM2		PWM2: PWM input 2
12	DIAGN		Diagnostic output NOT (Active Low)
13	CP1P		NC: Not Connected CP1P: Positive connection to Charge Pump Capacitor 1
14	CP1N		NC: Not Connected CP1N: Negative connection to Charge Pump Capacitor 1
15	CP2N		NC: Not Connected CP2N: Negative connection to Charge Pump Capacitor 2
16	CP2P		NC: Not Connected CP2P: Positive connection to Charge Pump Capacitor 2
17	CPOUT		CP: Charge Pump Output

Pin	L99MH94	L99MH92	Function
18	VDH		VDH input pin
19	GND		GND Ground connection
20	SL		SL Source low-side: Common connection to the source of the low-side MOSFETs.
21	DIODE2		External diode control 2
22	DIODE1		External diode control 1
23	GH4	NC	GH4 Gate high-side 4: Analog output pin to turn on/off high-side MOSFET 4. Connect to the gate of high side NC: Not Connected
24	SH4	NC	SH4 Source high-side 4: Connection to source of high-side MOSFET 4 NC: Not Connected
25	GL4	NC	GL4 Gate low-side 4: Analog output pin to turn on/off low-side MOSFET 4. Connect to the gate of low side NC: Not Connected
26	GL3	NC	GL3 Gate low-side 3: Analog output pin to turn on/off low-side MOSFET 3. Connect to the gate of low side NC: Not Connected
27	SH3	NC	SH3 Source high-side 3: Connection to source of high-side MOSFET 3 NC: Not Connected
28	GH3	NC	GH3 Gate high-side 3: Analog output pin to turn on/off high-side MOSFET 3. Connect to the gate of high side NC: Not Connected
29	GH2		GH2 Gate high-side 2: Analog output pin to turn on/off high-side MOSFET 2. Connect to the gate of high side
30	SH2		SH2 Source high-side 2: Connection to source of high-side MOSFET 2
31	GL2		GL2 Gate low-side 2: Analog output pin to turn on/off low-side MOSFET 2. Connect to the gate of low side
32	GL1		GL1 Gate low-side 1: Analog output pin to turn on/off low-side MOSFET 1. Connect to the gate of low side
	E.P. Exposed pad connected to ground on the application board		

Table 2. Pin function - VFQFN48

#	Name	Function
1	SDO	SDO serial data output
2	SDI	SDI serial data input with internal pull-down
3	SCLK	SCLK serial clock input with internal pull-down
4	CSN	CSN chip select not with internal pull-up
5	CSO1	CSO1 current sense amplifier output1
6	VDD	VDD logic supply
7	EN	EN enable input with internal pull-down
8, 11, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26	NC	Not Connected
9	PWM1	PWM1: PWM input 1
10	PWM2	PWM2: PWM input 2

#	Name	Function
12	DIAGN	DIAGN: Diagnostic output NOT (active low)
27	CP1P	CP1P:positive connection to charge pump capacitor 1
28	CP1N	CP1N: negative connection to charge pump capacitor 1
29	CP2N	CP2N: negative connection to charge pump capacitor 2
30	CP2P	CP2P: Positive connection to charge pump capacitor 2
31	CPOUT	CPOUT: Charge pump output
32	VDH	VDH input pin
33	GND	GND Ground connection
34	SL	SL source low-side: common connection to the source of the low-side MOSFETs
35	DIODE2	External diode control 2
36	DIODE1	External diode control 1
37	GH4	GH4 gate high-side 4: analog output pin to turn on/off high-side MOSFET 4. Connect to the gate of the high side
38	SH4	SH4 source high-side 4: connection to source of high-side MOSFET 4
39	GL4	GL4 gate low-side 4: analog output pin to turn on/off low-side MOSFET 4. Connect to the gate of the low side
40	GL3	GL3 gate low-side 3: analog output pin to turn on/off low-side MOSFET 3. Connect to the gate of the low side
41	SH3	SH3 source high-side 3: connection to source of high-side MOSFET 3
42	GH3	GH3 gate high-side 3: analog output pin to turn on/off high-side MOSFET 3. Connect to the gate of the high side
43	GH2	GH2 gate high-side 2: analog output pin to turn on/off high-side MOSFET 2. Connect to the gate of the high side
44	SH2	SH2 source high-side 2: connection to source of high-side MOSFET 2
45	GL2	GL2 gate low-side 2:analog output pin to turn on/off low-side MOSFET 2. Connect to the gate of the low side
46	GL1	GL1 gate low-side 1: analog output pin to turn on/off low-side MOSFET 1. Connect to the gate of the low side
47	SH1	SH1 source high-side 1: connection to source of high-side MOSFET 1
48	GH1	GH1 gate high-side 1: analog output pin to turn on/off high-side MOSFET 1. Connect to the gate of the high side
-	E.P.	Exposed pad connected to ground on the application board

2 Electrical specifications

Stressing the device above the rating listed in the Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{DH}	Power supply voltage	-0.3	-	28	V
V_{DH}	Single pulse tmax < 400 ms	-	-	40	V
V_{PWM1}	PWM input voltages (PWMx)	-0.3	-	VDD + 0.3	V
V_{PWM2}	PWM input voltages (PWMx)	-0.3	-	VDD + 0.3	V
V_{SDI}	SDI logic input voltages	-0.3	-	VDD + 0.3	V
V_{SCLK}	SCLK logic input voltages	-0.3	-	VDD + 0.3	V
V_{CSN}	CSN logic input voltages	-0.3	-	VDD + 0.3	V
V_{EN}	EN logic input voltages	-0.3	-	20	V
$V_{SDO/DIAGN}$	Voltage range at SDO/DIAGN	-0.3	-	VDD + 0.3	V
V_{SL}	Voltage range at SL	-6.0	-	6	V
V_{SH}	Voltage range at SHx	-6.0	-	VDH	V
V_{GH}	Voltage range at GHx, V_{CPOUT} = +0.3 V	Sxy - 0.3	-	Sxy + 13	V
V_{GL}	Voltage range at GLx, V_{CPOUT} = +0.3 V	Sxy - 0.3	-	Sxy + 13	V
V_{GS_LS}	Voltage difference between GLx and SL	-0.3	-	13	V
V_{GS_HS}	Voltage difference between GHx and SHx	-0.3	-	13	V
V_{CP1-}	CP1 minus	-0.3	-	VDH	V
V_{CP2-}	CP2 minus	-0.3	-	VDH	V
V_{CP1+}	CP1 plus	VDH - 0.3	-	VDH + 13	V
V_{CP2+}	CP2 plus	VDH - 0.6	-	VDH + 13	V
V_{CPOUT}	CP out	VDH - 0.6	-	VDH + 13	V
V_{DIODE}	Voltage at Vdiode pins	-0.3	-	40	V
V_{DD}	Logic supply voltage	-0.3	-	18	V
V_{CSO1}	Voltage at CSO1	-0.3	-	VDD + 0.3	V

Note:

- *All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit.*
- *Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.*

2.2 ESD protection

Table 4. ESD protection

Symbol	Parameter	Min	Typ	Max	Unit
Electrostatic discharge test (AEC-Q100-002-E) all pins (HBM)	-	-2	-	+2	kV
Electrostatic discharge test (AEC-Q100-002-E) output pins SHx (X = 1...8) and V_{DH} versus GND (HBM)	-	-4	-	+4	kV
Charge device model (CDM-AEC-Q100-011) all pins	-	-500	-	+500	V
Charged device model (CDM-AEC-Q100-011) corner pins	-	-750	-	+750	V

2.3 Thermal data

Table 5. Operation junction temperature

Symbol	Parameter	Min	Typ	Max	Unit
T_j	Operating junction temperature	-40	-	150	°C
T_{stg}	Storage temperature	-55	-	150	°C

All parameters are guaranteed in the temperature range -40 to 150 °C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to 165 °C).

Note:
- *Parameters limits at higher temperatures than 150 °C may change with respect to what is specified as per the standard temperature range.*
- *Device functionality at high temperature is guaranteed by characterization.*

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
T_{jTW_ON}	Junction temperature thermal warning threshold	T_j increasing	140	150	160	°C
T_{jSD_ON}	Junction temperature thermal shutdown threshold	T_j increasing	170	180	190	°C
T_{jSD_OFF}	Junction temperature thermal shutdown threshold	T_j decreasing	160	170	180	°C
$t_{fTjTW/TSD}$	Temperature warning/shutdown filtering time	Tested by scan	24	-	43	µs

Note: Those parameters are guaranteed at hot only.

2.3.1 Packages thermal data

Table 7. Packages thermal resistance

Symbol	Parameter	Test condition	Value	Unit
$R_{thj\text{-}amb}$ (1)	VFQFN32 thermal resistance junction to ambient (max.)		28.6	°C/W
$R_{thj\text{-}amb}$ (1)	VFQFN48 thermal resistance junction to ambient (max.)		26	°C/W
$R_{thj\text{-}case}$ (2)	VFQFN32 thermal resistance junction to case (max.)		7.6	°C/W
$R_{thj\text{-}case}$ (2)	VFQFN48 thermal resistance junction to case (max.)		4.5	°C/W

1. *The parameter is retrieved according to JEDEC 51.2. Device mounted on a four-layer 2s2p PCB.*
2. *The $R_{thj\text{-}case}$ is retrieved according to MIL-STD-883E referring to thermal testing method.*

2.4 Electrical characteristics

2.4.1 Supply, supply monitoring and current consumption

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, all voltages are referred to ground and currents are assumed positive when flow into the pin (unless otherwise specified).

Table 8. Supply, supply monitoring and current consumption

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{DH}	High-side drain voltage		6	-	28	V
V_{SL}	SL operative voltage range		-0.3	-	0.5	V
V_{SH}	SH operative voltage range		-0.3	-	VDH	V
V_{DH_ext}	High-side drain voltage extended range(1)		5	-	6	V
V_{DD}	I/O supply voltage		3	-	5.5	V
I_{DD}	V_{DD} DC supply current	V_{DH} = 13.5 V V_{DD} = 5 V Active mode	3.5	-	7.5	mA
I_{DD_SDN}	V_{DD} quiescent supply current	V_{DD} = 5 V Reset mode	-	-	0.5	µA
I_{DH}	V_{DH} current consumption in active mode	V_{DH} = 13 V V_{DD} = 5 V Active mode Outputs floating	-	40	50	mA
I_{DH}	V_{DH} current consumption in active mode	V_{DH} = 6 V to 28 V V_{DD} = 5.0 V Active mode Outputs floating	-	48	60	mA
I_{DH_SDN}	V_{DH} quiescent supply current	V_{DH} = 13 V V_{DD} = 0 V Reset mode Outputs floating	-	-	0.55	µA
V_{DHUV}	V_{DH} undervoltage threshold	V_{DH}increasing/decreasing	4	-	4.5	V
V_{DHUV_hyst}	V_{DH} undervoltage hysteresis		0.04	-	0.2	V
V_{DHOVT1_LH}	V_{DH} overvoltage threshold 1 LH	V_{DH} increasing	19	-	21	V
V_{DHOVT1_HL}	V_{DH} overvoltage threshold 1 HL	V_{DH} decreasing	18.4	-	20.4	V
V_{DHOVT2_LH}	V_{DH} overvoltage threshold 2 LH	V_{DH} increasing	29	-	33	V
V_{DHOVT2_HL}	V_{DH} overvoltage threshold 2 HL	V_{DH} decreasing	28.5	-	32.5	V
V_{DHOV2_hyst}	V_{DH} overvoltage threshold 2 hysteresis	Guaranteed by design	-	0.8	-	V
V_{DHOV1_hyst}	V_{DH} overvoltage threshold 1 hysteresis	Guaranteed by design	-	0.65	-	V
t_{UV_FILT}	V_{DH} undervoltage filter time		7	10	13	µs
t_{OV_FILT}	V_{DH}/V_{DD} overvoltage filter time		7	10	13	µs
V_{DDOVT_LH}	V_{DD} overvoltage threshold LH		5.4	-	5.9	V
V_{DDOVT_HL}	V_{DD} overvoltage threshold HL		5.3	-	5.8	V
V_{DDhyst_OV}	V_{DD} overvoltage hysteresis		0.07	-	0.2	V
V_{DDPOR_OFF}	V_{DD} power-on-reset	V_{DD} increasing	2.40	2.60	2.80	V

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{DDPOR_ON}	V_{DD} power-off-reset	V_{DD} decreasing	2.30	2.50	2.70	V

1. *Only functionality guaranteed.*

2.4.2 Logic inputs PWMx, EN

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, all voltages are referred to ground and currents are assumed positive when flow into the pin (unless otherwise specified).

Table 9. PWMx, EN

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{ENH}	EN high voltage		0.9	-	2	V
V_{ENL}	EN low voltage		0.4	-	0.95	V
V_{ENHY}	EN hysteresis	(1)	0.45	-	0.95	V
$R_{PD\_OFF\_EN}$	EN pull-down resistor	EN pin below EN threshold	150	200	250.5	kΩ
$I_{PD\_ON\_EN}$	EN pull-down current	EN pin above EN threshold, additional current, pull down resistor still present. Expected 80 µA + 25 µA with 5 V at EN pin	8.5	15	25	µA
V_{PWMH}	PWMx high voltage	(2)	1	-	2	V
V_{PWML}	PWMx low voltage	(3)	0.75	-	1.65	V
V_{PWMHY}	PWMx hysteresis	(1)	0.1	-	0.5	V
R_{PD_PWMx}	PWMx pull-down resistor		20	30	40	kΩ
f_{PWMH}	PWMH switching frequency	VDH = 13.5 V, VSLx = 0 V RG = 0 Ω, CG = 2.7 nF PWMH-duty-cycle = 50%	-	-	50	kHz

1. *Not subject to production test, specified by design.*
2. *High level guaranteed above max voltage.*
3. *Low level guaranteed below min voltage.*

2.4.3 Diagnostic not output (DIAGN)

The voltages are referred to ground and currents are assumed positive when the current flows into the pin. 6 V ≤ V_{DH} ≤ 18 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 10. DIAGN outputs

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage	I_{out} = 1 mA	-	-	0.4	V
V_{OH}	High-level output voltage	I_{out} = 1 mA	VDD - 0.4	-	-	V

2.4.4 Charge pump

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Table 11. Charge pump

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
f_{CP}	Charge Pump frequency	(1)	325	400	475	kHz
V_{CP}	Charge pump output voltage	$V_{DH} \geq 8$ V $I_{CP} \geq -10$ mA(2)	V_{DH} + 8.2	V_{DH} + 11.2	V_{DH} + 13	V
V_{CP_vbmin}	Charge pump output voltage	V_{DH} = 6 V I_{CP} = -5 mA(2)	V_{DH} + 6.2	V_{DH} + 7	-	V
V_{CP_low}	Charge pump low threshold voltage	(2)	V_{DH} + 4.5	V_{DH} + 5	V_{DH} + 5.5	V
I_{CP_lim}	Charge pump output current limitation(3)	V_{CP}= V_{DH} = 13.5 V	-36	-	-	mA
t_{CP}	Charge pump low filter time	Tested by scan	8	10	12	µs
t_{CP_blank}	Charge pump startup blanking time	Tested by scan	500	-	800	µs

1. *Not subject to production test, specified by design.*
2. *C_{CPC1} = C_{CPC2} = 100 nF, C_{CP} = 220 nF.*
3. *In case of short to battery. This pin is not protected from short to ground.*

2.4.5 Gate driver

The electrical characteristics related to the gate driver are valid for $V_{CP} > V_{DH} + 8.5$ V.

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, $V_{CP} > V_{DH} + 8.5$ V, all voltages with respect to ground, positive current flowing into pin except for I_{GLx} and I_{GHx} (unless otherwise specified).

The gate source and sink current level can be affected in case of high SHx/GHx slew rate due to capacitive current injected into the GATE pin from an external MOS miller capacitor. This behavior is described in a dedicated application note.

Table 12. Gate driver

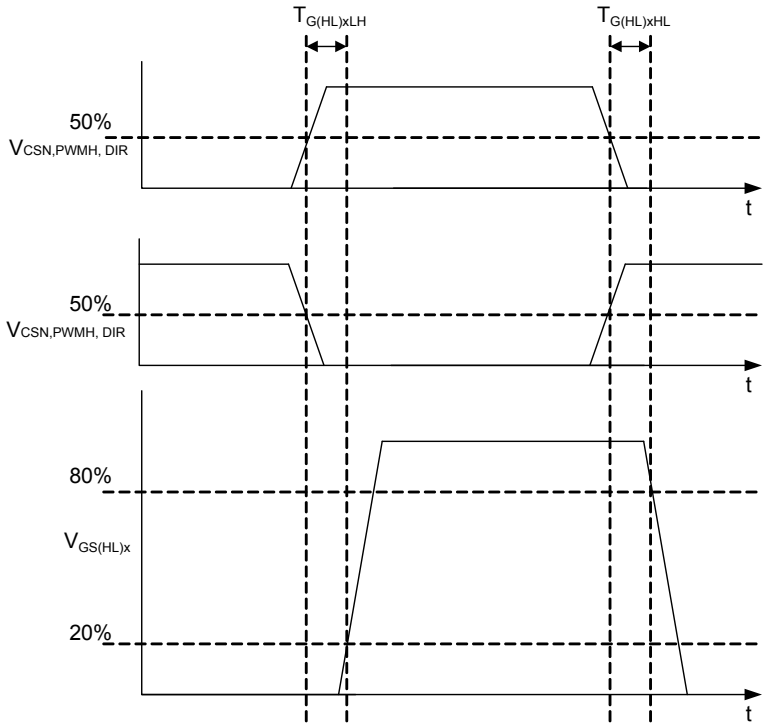
Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 0000	-50%	-0.72	+50%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0000	-50%	0.88	+50%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 0001 ISTEP3_CONFx = 0000	-50%	-1.58	+50%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0001 ISTEP3_CONFx = 0000	-50%	1.77	+50%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 0010	-50%	-2.6	+50%	mA
I_{offx}	Gate Sink Current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFX = ISTEP2_OFF_CONFx = 0010	-50%	2.6	+50%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 0011 ISTEP3_CONFx = 0001	-45%	-3.3	+45%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0011 ISTEP3_CONFx = 0001	-45%	3.5	+45%	mA

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 0100	-45%	-6	+45%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0100	-45%	6	+45%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 0101 ISTEP3_CONFx = 0010	-35%	-8	35%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0101 ISTEP3_CONFx = 0010	-35%	8	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 0110	-35%	-10	35%	mA
I_{offx}	Gate Sink Current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0110	-35%	10	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 0111 ISTEP3_CONFx = 0011	-35%	-12	35%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0111 ISTEP3_CONFx = 0011	-35%	12	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 1000	-35%	-16	35%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1000	-35%	16	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 1001 ISTEP3_CONFx = 0100	-35%	-20	35%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1001 ISTEP3_CONFx = 0100	-35%	20	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 1010	-35%	-24	35%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1010	-35%	24	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 1011 ISTEP3_CONFx = 0101	-35%	-28	35%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1011 ISTEP3_CONFx = 0101	-35%	28	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 1100	-35%	-32	35%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1100	-35%	32	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 1101 ISTEP3_CONFx = 0110	-35%	-36	35%	mA
I_{Toffx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1101 ISTEP3_CONFx = 0110	-35%	36	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 1110	-35%	-40	35%	mA

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1110	-35%	40	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 1111 ISTEP3_CONFx = 0111	-25%	-42	+25%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1111 ISTEP3_CONFx = 0111	-25%	37	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1000	-25%	-52	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1000	-25%	52	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1001	-25%	-60	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1001	-25%	60	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1010	-25%	-68	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1010	-25%	68	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1011	-25%	-76	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1011	-25%	76	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1100	-25%	-84	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1100	-25%	84	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1101	-25%	-92	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1101	-25%	92	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1110	-25%	-104	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1110	-25%	104	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1111	-25%	-120	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1111	-25%	120	+25%	mA
V_{GSHx}	Gate-on voltage	VDH = VSH = 6 V ICP = -5 mA, DC measure GH-SH	VSHx + 6	-	-	V
V_{GSHx}	Gate-on voltage	VDH = VSH >= 8 V ICP = -10 mA, DC measure GH-SH	VSHx +- 8	VSHx + 10	VSHx + 12	V
R_{GHx}	Passive gate-pull-down resistance	Resistance between gate HS and ground when device is ON	-	1	-	MΩ
R_{SHx}	Passive source-pull-down resistance	Resistance between source HS and ground when device is ON	-	1	-	MΩ
V_{GLx}	Gate-on voltage	VSL = 0 V, VDH = 6 V	VSLx + 6	-	-	V

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
		ICP = -5 mA, DC measure GL-SL				
V_{GLx}	Gate-on voltage	VSL = 0 V, VDH ≥ 8 V ICP = -10 mA, DC measure GL-SL	VSLx + 8	VSLx + 10	VSLx + 12	V
R_{GLx}	Passive gate-pull-down resistance	Resistance between gate LS and ground when device is ON	-	1	-	MΩ
R_{SL}	Passive source-pull-down resistance	Resistance between source LS and ground when device is ON	-	125	-	KΩ
$V_{step1xl}$	Step voltage1 for x channel x = 1…8	VSTEP1_CONFx = 00/01 Switch ON, command = 1	-55%	1.1	+55%	V
$V_{step1xh}$	Step voltage1 for x channel x = 1…8	VSTEP1_CONFx = 00/01 Switch OFF command = 0	-47%	1.3	+47%	V
$V_{step1xl}$	Step voltage1 for x channel x = 1...8	VSTEP1_CONFx = 10/11 Switch ON, command = 1	-35%	2.2	+35%	V
$V_{step1xh}$	Step voltage1 for x channel x = 1...8	VSTEP1_CONFx = 10/11 Switch OFF command = 0	-35%	2.6	+35%	V
$V_{step2xl}$	Step voltage2 for x channel x = 1...8	VSTEP2_CONFx = 00 Switch ON, command = 1	-31%	2.67	+31%	V
$V_{step2xh}$	Step voltage2 for x channel x = 1...8	VSTEP2_CONFx = 00 Switch OFF command = 0	-28%	3.33	+28%	V
V_{step2x}	Step voltage2 for x channel x = 1...8	VSTEP2_CONFx = 01 Switch ON, command = 1	-27%	3.56	+27%	V
$V_{step2xh}$	Step voltage2 for x channel x = 1...8	VSTEP2_CONFx = 01 Switch OFF command = 0	-25%	4.44	+25%	V
$V_{step2xl}$	Step voltage2 for x channel x = 1...8	VSTEP2_CONFx = 10 Switch ON, command = 1	-24%	4.45	+24%	V
$V_{step2xh}$	Step voltage2 for x channel x = 1...8	VSTEP2_CONFx = 10 Switch OFF command = 0	-24%	5.55	+24%	V
$V_{step2xl}$	Step voltage2 for x channel x = 1...8	VSTEP2_CONFx = 11 Switch ON, command = 1	-24%	5.34	+24%	V
$V_{step2xh}$	Step voltage2 for x channel x = 1...8	VSTEP2_CONFx = 11 Switch OFF command = 0	-24%	6.66	+24%	V
Gate drivers dynamic parameters						
t_{GLxr}	Rise time LS	VDH = 13.5 V; VSLx = 0 V RG = 0 Ω; CG = 10 nF	-	-	2.1	µs
t_{GHxr}	Rise time HS	VDH = 13.5 V; VSLx = 0 V RG = 0 Ω; CG = 10 nF	-	-	2.1	µs
t_{GLxf}	Fall time LS	VDH = 13.5 V; VSLx = 0 V RG = 0 Ω; CG = 10 nF	-	-	2.1	µs
t_{GHxf}	Fall time HS	VDH = 13.5 V; VSLx = 0 V RG = 0 Ω; CG = 10 nF	-	-	2.1	µs
V_{GSHx}	Gate-on voltage HS	Maximum VGH-VSH in turn-on condition	-	-	VSHx + 13	V
V_{GSLx}	Gate-on voltage LS	Maximum VGL-VSL in turn-on condition	-	-	VSLx + 16	V

Figure 6. **H-driver delay times**

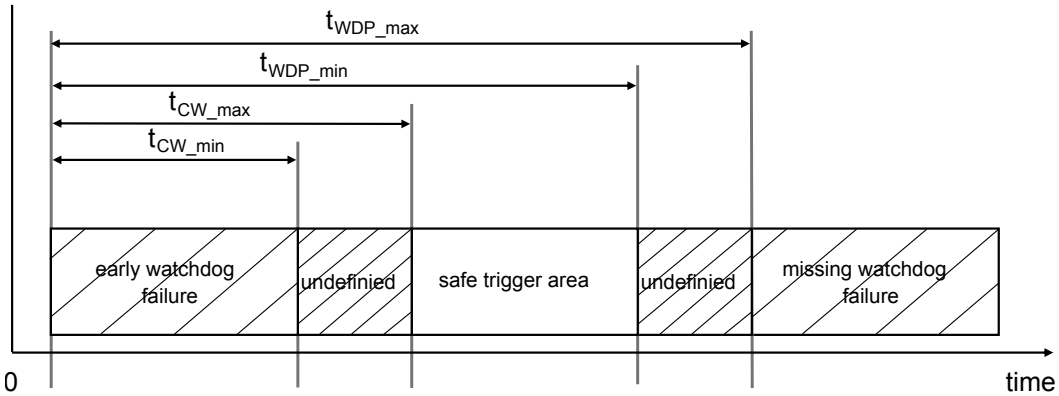


2.4.6 Watchdog

Table 13. **Watchdog**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{LOW}	Long open window	Guaranteed by scan	52	-	87	ms
t_{CW}	Closed window	Guaranteed by scan	11	-	20	ms
t_{WDP}	Watchdog period	Guaranteed by scan	32	-	54	ms
$t_{timeout}$	Timeout period	Guaranteed by scan	90	-	110	ms

Figure 7. **Watchdog early, late and safe window**



2.4.7 Open-load monitoring external

The voltages are referred to power ground and currents are assumed positive when the current flows into the pin. 6 V ≤ V_{DH} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 14. Open-load monitoring threshold

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{ODLS}	Low-side drain-source monitor off state-threshold voltage	VDH = 13.5 V VDS_CONFx = 1xxx or (HB_MODEx = 00, OUTEx = 1)	1.5	1.8	2.1	V
V_{ODHS}	High-side drain-source monitor off state-threshold voltage	VDH = 13.5 V VDS_CONFx = 1xxx or (HB_MODEx = 00, OUTEx = 1)	1.5	1.8	2.1	V
V_{SHx_OL}	Output voltage of selected SHx in open-load test mode	VSLx = 0 V; VDH = 13.5 V	2.1	3	3.9	V
I_{shx_PU}	Pull-up current in DIAG OFF	VSHx = 0 V; VDH = 13.5 V DIAGOFF_CURR_SEL = 0	0.5	0.9	1.25	mA
I_{shx_PU}	Pull-up current in DIAG OFF	VSHx = 0 V; VDH = 13.5 V DIAGOFF_CURR_SEL = 1	1.2	1.6	2.4	mA
I_{shx_PD}	Pull-down current in DIAG OFF	VSHx = 3 V; VDH = 13.5 V DIAGOFF_CURR_SEL = 0	200	300	400	µA
I_{shx_PD}	Pull-down current in DIAG OFF	VSHx = 3 V; VDH = 13.5 V DIAGOFF_CURR_SEL = 1	400	600	800	µA
t_{diag}	DIAG OFF time		130	200	270	µs

2.4.8 Drain-source monitoring threshold

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, V_{CP} > V_{DH} + 8.5 V, all voltages are referred to ground and currents are assumed positive when flow into the pin (unless otherwise specified).

Table 15. Drain-Source monitoring threshold

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{SCd0}	Drain-source monitoring threshold	VDS_CONFx = 0000	0.045	0.08	0.095	V
V_{SCd1}	Drain-source monitoring threshold	VDS_CONFx = 0001	0.12	0.16	0.18	V
V_{SCd2}	Drain-source monitoring threshold	VDS_CONFx = 0010	0.16	0.20	0.24	V
V_{SCd3}	Drain-source monitoring threshold	VDS_CONFx = 0011	0.20	0.25	0.30	V
V_{SCd4}	Drain-source monitoring threshold	VDS_CONFx = 0100	0.24	0.30	0.36	V
V_{SCd5}	Drain-source monitoring threshold	VDS_CONFx = 0101	0.32	0.40	0.48	V
V_{SCd6}	Drain-source monitoring threshold	VDS_CONFx = 0110	0.40	0.50	0.62	V
V_{SCd7}	Drain-source monitoring threshold	VDS_CONFx = 0111	0.48	0.60	0.72	V

2.4.9 Drain source monitoring blanking time

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, V_{CP} > V_{DH} + 8.5 V, all voltages are referred to ground and currents are assumed positive when flow into the pin (unless otherwise specified).

Table 16. Drain source monitoring external H-bridge

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{B0000}	DS monitoring blank time	VDS_BLANKx = 0000	0.5	0.625	0.85	µs
t_{B0001}	DS monitoring blank time	VDS_BLANKx = 0001	0.8	1	1.2	µs
t_{B0010}	DS monitoring blank time	VDS_BLANKx = 0010	1	1.25	1.5	µs
t_{B0011}	DS monitoring blank time	VDS_BLANKx = 0011	1.2	1.5	1.8	µs
t_{B0100}	DS monitoring blank time	VDS_BLANKx = 0100	1.6	2	2.4	µs
t_{B0101}	DS monitoring blank time	VDS_BLANKx = 0101	2.4	3	3.6	µs
t_{B0110}	DS monitoring blank time	VDS_BLANKx = 0110	3.2	4	4.8	µs
t_{B0111}	DS monitoring blank time	VDS_BLANKx = 0111	4	5	6	µs
t_{B1000}	DS monitoring blank time	VDS_BLANKx = 1000	4.8	6	7.2	µs
t_{B1001}	DS monitoring blank time	VDS_BLANKx = 1001	5.6	7	8.4	µs
t_{B1010}	DS monitoring blank time	VDS_BLANKx = 1010	6.4	8	9.6	µs
t_{SCS}	Drain-source comparator propagation delay	VDH = 14 V VDS jump from 10 mV to 1 V, time from filter time end to VGS external FET under threshold without external MOSFETs(1)		-	1	µs

1. *Not subject to production test, specified by design.*

Note: For the VDS_BLANKx = 1x11 the default value (VDS_BLANKx = 0000) will be set.

2.4.10 Drain source monitoring filter time

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, V_{CP} > V_{DH} + 8.5 V, all voltages are referred to ground and currents are assumed positive when flow into the pin (unless otherwise specified).

Table 17. Drain source monitoring filter time

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{FT000}	DS monitoring filter time(1)	VDS_FILTx = 000	0.4	0.5	0.85	µs
t_{FT001}	DS monitoring filter time(1)	VDS_FILTx = 001	0.8	1	1.4	µs
t_{FT010}	DS monitoring filter time(1)	VDS_FILTx = 010	1.6	2	2.4	µs
t_{FT011}	DS monitoring filter time(1)	VDS_FILTx = 011	2.4	3	3.6	µs
t_{FT100}	DS monitoring filter time(1)	VDS_FILTx = 100	3.2	4	4.8	µs
t_{FT101}	DS monitoring filter time(1)	VDS_FILTx = 101	4	5	6	µs
t_{FT110}	DS monitoring filter time(1)	VDS_FILTx = 110	4.8	6	7.2	µs

1. *Not subject to production test, specified by design.*

Note: If the VDS_FILTx = 111 the default value (VDS_FILTx = 000) will be set.

2.4.11 Cross current protection time

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, $V_{CP} > V_{DH}$ + 8.5 V, all voltages are referred to ground and currents are assumed positive when flow into the pin (unless otherwise specified).

Table 18. Cross current protection time

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
tDT000	Cross-current protection time	Tested by scan, DTP_REF = 0(1)	350	500	650	ns
tDT001	Cross-current protection time	Tested by scan, DTP_REF = 0(1)	0.8	1	1.2	µs
tDT010	Cross-current protection time	Tested by scan, DTP_REF = 0(1)	1.6	2	2.4	µs
tDT011	Cross-current protection time	Tested by scan, DTP_REF = 0(1)	2.4	3	3.6	µs
tDT100	Cross-current protection time	Tested by scan, DTP_REF = 0(1)	3.2	4	4.8	µs
tDT101	Cross-current protection time	Tested by scan, DTP_REF = 0(1)	4	5	6	µs
tDT110	Cross-current protection time	Tested by scan, DTP_REF = 0(1)	4.8	6	7.2	µs
tDT111	Cross-current protection time	Tested by scan, DTP_REF = 0(1)	12.8	16	19.2	µs

1. *When DTP_REF = 1 it is necessary to add 850 ns to the maximum value.*

Note: Not subject to production test, specified by design.

2.4.12 External temperature diode

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, $V_{CP} > V_{DH}$ + 8.5 V, all voltages are referred to ground and currents are assumed positive when flow out from the pin (unless otherwise specified).

Table 19. External temperature diode

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{DIODE}	Diode current	IDIODE_CONFx = 00	200	250	300	µA
I_{DIODE}	Diode current	IDIODE_CONFx = 01	400	500	600	µA
I_{DIODE}	Diode current	IDIODE_CONFx = 10	600	750	900	µA
I_{DIODE}	Diode current	IDIODE_CONFx = 11	800	1000	1200	µA
V_{dioinc}	Diode voltage range		0.3	-	2	V
-	ADC nbit		-	11	-	bit
-	ADC offset error		-2	-	+2	mV
-	ADC gain error vs temp		-	-	+1.5	%
-	ADC total gain error		-2.5	-	+2.5	%

2.4.13 SPI

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, $V_{CP} > V_{DH}$ + 8.5 V, all voltages are referred to ground and currents are assumed positive when flow into the pin (unless otherwise specified).

Table 20. SPI parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DC parameters						
V_{IL}	Low-level input voltage		0.75	-	1.65	V
V_{IH}	High-level input voltage		0.85	-	1.75	V
V_{ihyst}	Input voltage hysteresis		0.1	-	0.5	V
$I_{CSN\ in}$	CSN pull-up current input	Probe current on force input pin at VHL voltage in DC conditions	20	40	60	uA
$I_{SDI\ in}$	SCLK, SDI pull down current input	Probe current on force input pin at VIL voltage in DC conditions	20	40	60	µA
$V_{SDO\ low}$	SDO output low voltage	ISDO out = 1 mA	-	-	0.4	V
$V_{SDO\ high}$	SDO output high voltage	ISDO out = 1 mA 3.0 V ≤ VDD ≤ 5.5 V	VDD - 0.4	-	-	V
$I_{SDO\ leak}$	SDO tristate leakage current	VCSN ≥ 2 V 0 V ≤ VSDO IN ≤ VDD	-10	-	10	µA
AC parameters						
f_{CLK}	Clock frequency	CSDO = 50 pF	-	-	6	MHz
t_{CLK}	Clock period	CSDO = 50 pF	166	-	-	ns
t_1 (1)	Clock high time		75	-	-	ns
t_2 (1)	Clock low time		75	-	-	ns
t_3 (1)	CLK low before CSN active		20	-	-	ns
t_4 (1)	CLK active after CSN active		100	-	-	ns
t_5 (1)	CLK passive before CSN passive		100	-	-	ns
t_6 (1)	SDI setup time		30	-	-	ns
t_7 (1)	SDI hold time		30	-	-	ns
t_8 (1)	SDO active after CSN active	CSDO = 50 pF	-	-	100	ns
t_9 (1)	SDO tristate after CSN passive	CSDO = 50 pF	-	-	100	ns
t_{10} (1)	SDO valid time	CSDO = 50 pF	-	-	70	ns
t_{11} (1)	SDO hold time	CSDO = 50 pF	10	-	-	ns
t_{12} (1)	SDO rise time	CSDO = 50 pF	-	-	50	ns
t_{13} (1)	SDO fall time	CSDO = 50 pF	-	-	50	ns
t_{14} (1)	CSN passive time to next frame		600	-	-	ns
t_{15} (1)	CLK passive time to next		100	-	-	ns
t_{16} (1)	SDI data of next frame		20	-	-	ns
t_{CSN_fail}	CSN low timeout	Tested by scan	20	35	50	ms
t_{START}	Time at the start up before a correct SPI frame can be received	Tested by scan	-	-	300	µs

1. *See the Figure 1.*

2.4.14 Indirect current sense output

V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, $V_{CP} > V_{DH}$ + 8.5 V, all voltages are referred to ground and currents are assumed positive when flow into the pin (unless otherwise specified).

Table 21. CSO parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$CSO_{xTOT\_error\_CHx\_50mV}$	Total error 50 mV	VDS HS or LS forces 50 mV, gain selected 10x1.5(1) validates also for gain 10x3	-4.6	-	4.6	mV
$CSO_{xTOT\_error\_CHx\_50mV}$	Total error 100 mV	VDS HS or LS forces 100 mV, gain selected 10x1.5(1) validates also for gain 10x3	-4.85	-	4.85	mV
$CSO_{xTOT\_error\_CHx\_150mV}$	Total error 150 mV	VDS HS or LS forces 150 mV, gain selected 2.5x3	-10.5	-	10.5	mV
$CSO_{xTOT\_error\_CHx\_450mV}$	Total error 450 mV	VDS HS or LS forces 450 mV, gain selected 2.5x3	-10.5	-	10.5	mV
CSO_{InR_A}	Indirect current sense input voltage Range A		10	-	140	mV
CSO_{InR_B}	Indirect current sense input voltage Range B		120	-	450	mV
CSO_{OutR_A}	Indirect current sense output voltage Range A	(1)	0.1	-	V_{DD} - 0.3	V
CSO_{OutR_B}	Indirect current sense output voltage Range B	(1)	0.3	-	V_{DD} - 0.3	V
$CSO_{Setting}$	Indirect current sense output setting time	Out from 0.1 V to 2 V (C = 1 nF)(1)	-	-	10	µs

1. *Not subject to production test, specified by design.*

3 Functional description

3.1 Power supply

The device has two supply input pins. VDH is the supply input of the charge pump for the MOSFET gate drivers. It must be connected to the battery through a reverse battery protection. VDD is the supply input of the internal voltage regulator for the logic, of the I/Os and of the current sense amplifiers output stage. This voltage has to be the same as the application microcontroller supply (for example, 3.3 V or 5 V). When both VDD and VDH are provided to the device, the power supply for the internal regulators for logic is taken from the VDD power pin. None of the supply input pins are internally protected against negative voltage. The VDD supply input can withstand a short to battery up to VDD absolute maximum rating. The decoupling capacitors on the VDD and VDH pins must be placed in the PCB as close as possible.

3.1.1 VDH overvoltage (VDHOV)

An overvoltage diagnostic is present in L99MH94 / L99MH92. The levels of the overvoltage diagnostic are described in the Supply, supply monitoring and current consumption. The overvoltage functionality is described in the Multi fail-safe mode.

3.1.2 VDH undervoltage (VDHUV)

When the VDH supply input voltage falls below the undervoltage protection threshold (V_{DHUV}) for a time longer than t_{UV_FILT}, then the corresponding undervoltage flag (VDHUV) is set, and (in order to protect the external power stage) the external MOSFETs are switched off. In particular, the LS MOSFETs gate drivers are forced to switch off actively the LS MOSFETs with the maximum available current, regardless of the programmed gate discharge current, whereas the HS MOSFETs gate drivers are forced, as long as $V_{CP} > V_{DH} + 3$ V, to switch off actively the HS MOSFETs with the maximum available current, after that the HS MOSFETs gate drivers will be disabled and the HS MOSFETs are passively switched off through the internal resistive connection between gate and source. The gate drivers come out of forced disabled mode, once the undervoltage flag VDHUV is cleared.

The undervoltage flag VDHUV can be cleared by an SPI “read and clear” command only if the V_{DH} undervoltage condition is no longer present, namely if $V_{DH} > V_{DHUV}$ for a time longer than the corresponding filtering time t_{ovuv_filt}.

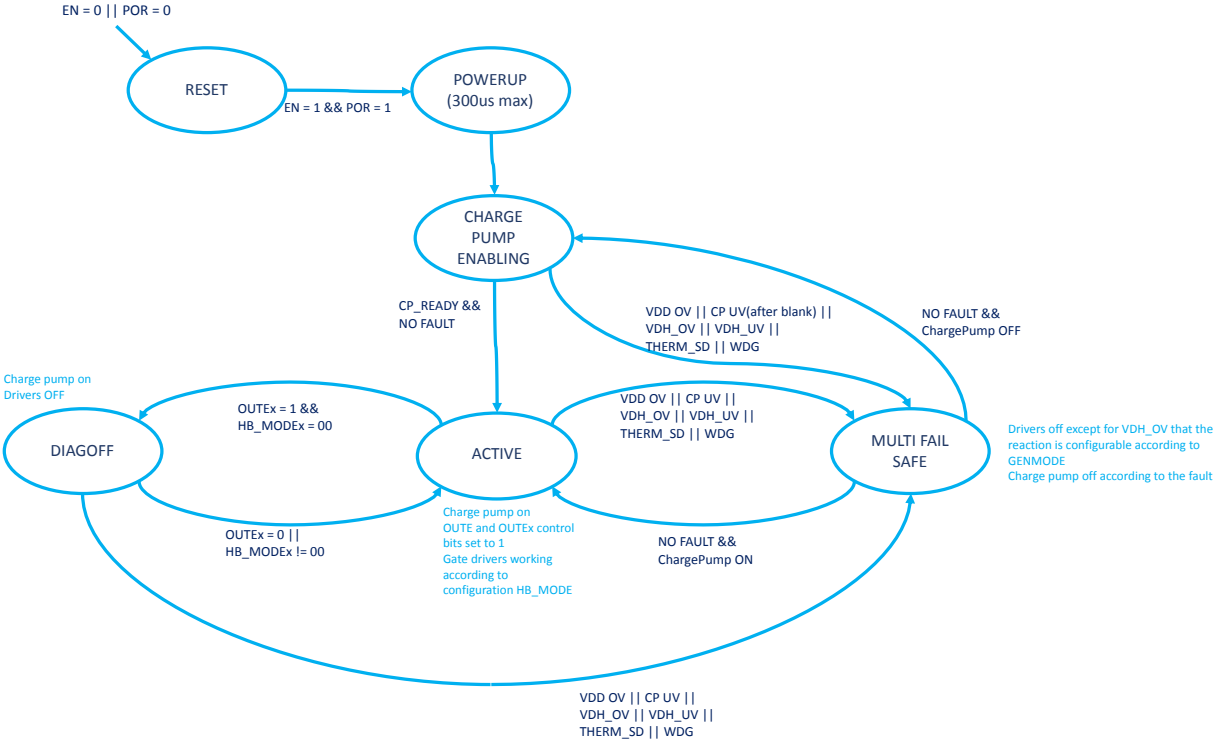
3.1.3 VDD overvoltage (VDDOV)

When the V_{DD} exceeds the V_{DDOV} threshold for a time longer than t_{OV_FILT}, then the corresponding overvoltage flag (VDDOV) is set, and (in order to protect the application) all the gate drivers are forced to switch off actively all the MOSFETs with the maximum available current, regardless of the programmed gate discharge current. The gate drivers come out of forced disabled mode, once the overvoltage flag VDDOV is cleared. The V_{DD} overvoltage protection aims at making the application robust against V_{DD} short to battery.

The overvoltage flag VDDOV can be cleared by an SPI “read and clear” command only if the V_{DD} overvoltage condition is no longer present, namely if $V_{DD} < V_{DDOV}$ for a time longer than the corresponding filtering time t_{OV_FILT}.

3.2 Operation modes

Figure 8. **Main operating modes**



3.2.1 Reset

The device gets out of reset mode to get into a power-up state as soon as the EN pin is high and the V_{DD} is above V_{DDPOR_OFF} (increasing phase). If either the V_{DD} falls below V_{DDPOR_ON} (decreasing phase) with the EN pin still high, the device experiences a power-on-reset and enters in reset mode.

Besides, the content of all the registers is reset to the default value. Once out of reset mode the global status RSTB bit will be set indicating that all the device registers have been reset to the default value. This bit will be automatically cleared by any valid SPI communication frame (after power-up state).

When the EN input pin is left floating, due of the internal pull-down resistor, the device enters (if not already done) in reset mode minimizing its current consumption. When the device is in reset mode, to have the minimum current drawn by V_{DH}, less than I_{DD_SDN} for CSN = high (SDO in tristate), the EN input pin must be low. In reset mode the gate drivers together with the charge pump are switched off, all the MOSFETs are passively switched off by the internal resistive link between gate and source present at each MOSFET and all the registers are reset to default values.

3.2.2 Power-up state and charge pump enabling

When L99MH94 / L99MH92 exits the reset state, before reaching the active state, the device passes through an intermediate state, called power-up state, with the aim of loading all the configurations necessary for the device to function. During this state it is not possible to guarantee the communication by SPI for a duration of t_{START}.

When the charge pump is out from the start up phase, the device will automatically exit from the charge pump enabling state to go to the active state. The start up phase duration is t_{CP_start}.

3.2.3 Active mode

In active mode the diagnostic device is available. In active mode, with no faults, the charge pump is enabled if VDH > VDHUV, the gate drivers are enabled if the OUTEx, x = 1...8, one for each half-bridge, control bits are set and the OUTE bit (one generic for all the gate drivers) is set. If the OUTEx control bits are reset, or the OUTE bit is reset, all the gate drivers are disabled and all the MOSFETs are switched off passively through the internal resistive connection between gate and source present at each MOSFET.

All the configurations shall be changed while the diagnosis/channel is not active to guarantee the correct value of the time selected and to apply the correct configuration. If the filter is changed during the actuation the value of the filter is not guaranteed.

3.2.4 Multi fail-safe mode

The L99MH94 / L99MH92 integrates a so called “multi fail-safe mode”, an automatic system that intervenes to switch off passively the gate driver/s to protect the device/application if a fault happens according to the registers settings.

In active mode, with no faults, the charge pump is enabled. The gate drivers outputs are driven according to the OUTEx control bit: when the OUTEx control bits are reset, all the gate drivers are low and the external MOSFETs are strongly shut off through the internal predriver pulldown. An additional passive pulldown connected between gate and GND and between source and GND of each MOSFET is present.

Once the OUTEx control bit is set, each HS and LS MOSFETs of the 4/2 half-bridges x, x = 1...4/2, can be:

- Deactivated
- Activated (statically, no PWM)
- Activated in PWM mode

The HB_MODEx registers are used to control the functionality of the single half-bridge. x indicates the number of the half-bridge to work on, x = 1 to 4/2. It is a 2-bit register, see the Table 22 and Table 24.

Table 22. HB_MODEx register functionality

HB_MODEx, x = 1...4/2	Setting
00	LS and HS of the half-bridge x are kept in DIAG OFF state (default)
01	LS of the half-bridge x is ON (static, no PWM), HS of the half-bridge x is OFF
10	HS of the half-bridge x is ON (static, no PWM), LS of the half-bridge x is OFF
11	LS or HS of the half-bridge x is ON according to the HB_PWMx, x=1…4/2, register

When a fault condition is detected, the behavior of the device is different depending on the cause of the fault itself.

When the VDH supply input voltage rises above the programmable overvoltage protection threshold (V_{DHOVT1} for OVTS = 0 or V_{DHOVT2} for OVTS = 1) for a time longer than t_{OV_FILT}, the corresponding overvoltage flag (VDHOV) is set to protect the application.

The overvoltage protection flag VDHOV can be cleared by an SPI “read and clear” command only if the VDH overvoltage condition is no longer present, namely if the foresaid condition that automatically enables the charge pump is fulfilled.

The following actions can be taken:

- The charge pump is left on. The external MOSFETs are switched off. In particular, the external HS and the LS MOSFETs are forced off actively with the maximum available current, regardless of the programmed gate discharge current. This working mode is obtained setting the GENMODEx = 0, x = 1...4/2
- In this second case, called GENERATOR MODE, the charge pump is left on. The HS external MOSFETs are switched off. The LS MOSFETs are switched on to lock the motor. This working mode is obtained setting the GENMODEx = 1, x = 1…4/2
- In this working mode the charge pump and the external MOSFETs are not switched off. L99MH94 / L99MH92 continues to work waiting for an interrupt from the microcontroller that will decide how to proceed. This working mode is obtained setting the GENMODEx = 2, x = 1...4/2

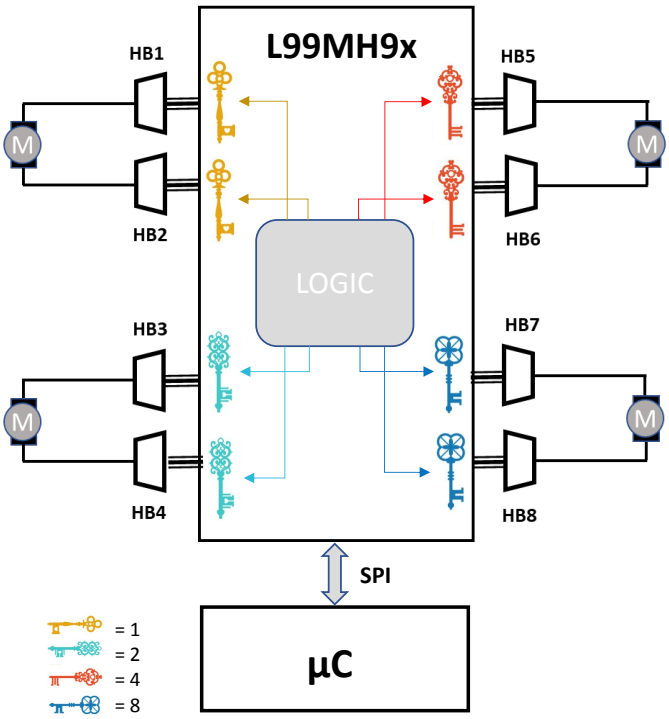
In the event of a fault due to V_{DD} overvoltage, thermal shutdown, watchdog event, the flag relating to the fault is set and the external MOSFETs, together with the charge pump are switched off to protect the device.

In case the VDD overvoltage condition is no longer present after the filtering time tOV_FLT, the charge pump is switched on again, while the other functions are kept off until the VDDOV flag is cleared.

When a V_{ds} monitoring failure event occurs, the half-bridge in which the V_{ds} monitoring failure occurred is switched off. In addition to the half-bridge in which the failure occurred, all half-bridges that are connected to the one that failed are also turned off. L99MH94 / L99MH92 is able to turn off only the half-bridges connected to each other in accordance with what is written in the HB_FAULTx, x = 1…4/2, register: at each half-bridge is assigned a key whose values can be 0, 1, 2, or 4, as shown in the Figure 9.

- 0 = the HBx is not connected to the other half-bridges;
- 1, 2, or 4 = the HBx relates to another HB with the same key.

Figure 9. Example of possible configuration to assign a key at each half-bridge

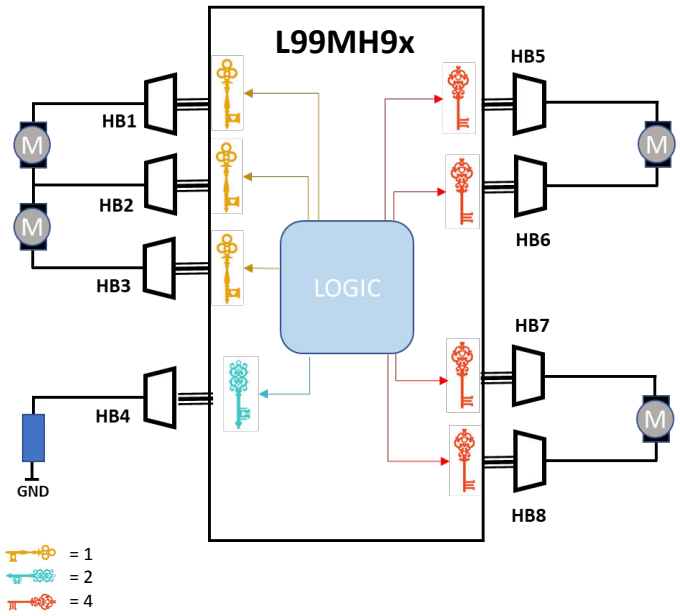


Note: The figure above relates to the L99MH98, L99MH94, and L99MH92 devices. The number of half-bridges available depends on the selected part number.

When a failure is detected in the half-bridge which has key x, all half-bridges that have key x will be turned off. All other half-bridges in which the failure is not detected, or which are connected to the half-bridge that fails, will remain switched on and will continue to work.

The Figure 10 shows an example of a possible configuration that associates different keys to different pairs of HB.

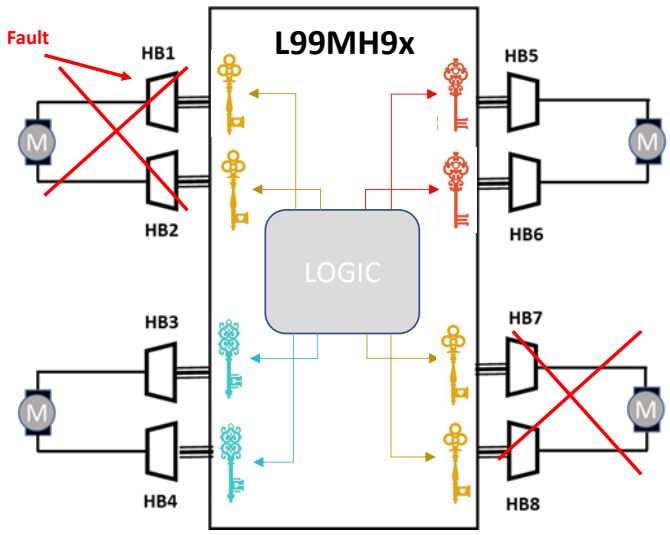
Figure 10. **Example of possible configuration where a key is associated to a different half-bridge**



Note: The figure above relates to the L99MH98, L99MH94, and L99MH92 devices. The number of half-bridges available depends on the selected part number.

The Figure 11 shows an example of a fault detected in HB1, connected with the same key to HB2, HB7 and HB8. The L99MH9x switches off HB1, HB2, HB7 and HB8 because linked with the same key.

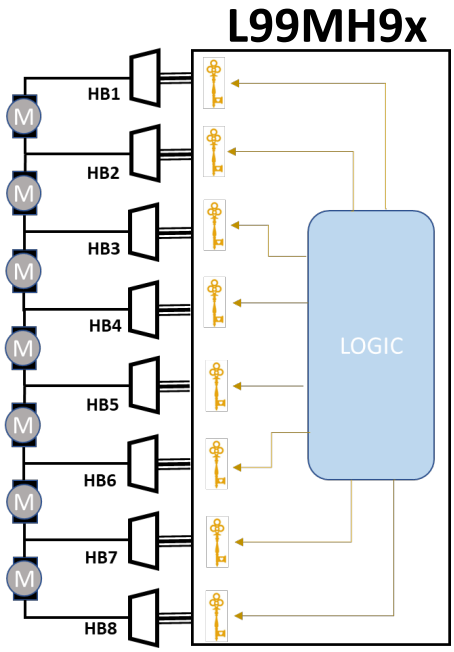
Figure 11. **Example of fault on HB1**



Note: The figure above relates to the L99MH98, L99MH94, and L99MH92 devices. The number of half-bridges available depends on the selected part number.

In case all HB are configured with the same key (see the Figure 12), if a fault occurs on one HB, all HBx are switched off.

Figure 12. **Example of HBs configured with the same key**



Note: The figure above relates to the L99MH98, L99MH94, and L99MH92 devices. The number of half-bridges available depends on the selected part number.

3.2.5 Operational matrix

The Table 23 summarizes which functions of L99MH94 / L99MH92 are turned off and which ones remain on as a function of the fault event that occurs.

Table 23. Reset matrix

Functions/ faults or input	Enable pin low	VDD under POR	VDD overvoltage	VDH overvoltage	VDH undervoltage	Thermal warning	Thermal shutdown	Charge pump over UV th at power-up (not ready)	Charge pump UV (CP UV FAULT)	Watchdog	VDSx monitoring	SPI error
SPI	X	X	X(1)	O	O	O	O	O	O	O	O	O
Watchdog	X	X	X(2)	O	O	O	O	O	O	O	O	O
Diagnostic logic	X	X	X	O	O	O	O	O	O	O	O	O
Register map	X	X	O	O	O	O	O	O	O	O(3)	O	O
PWM controller	X	X	X	X	X	O	X	X	X	X	X	O
DIAGN	X	X	A	A	A	A	A	A	A	A	A	A
Indirect current measurement system	X	X	X	X	X	O	X	X	X	X	O	O
Current generator and ADC for temperature measurement	X	X	X	X	X	O	X	X	X	X	O	O
Gate drivers	X	X	X	C	X	O	X	X	X	X	X(4)	O
Charge pump	X	X	X	O	O	O	X	X(5)	O	X	O	O

1. *SDO, DIAGN, and CSO1 outputs are low.*
2. *After a VDDOV event the watchdog restarts with a long open window and must be reprogrammed.*
3. *The OUTEx registers are reset.*
4. *The half bridge in which the failure occurred and all the half bridges that are connected to the one that failed are turned off.*
5. *In the case of a charge pump not ready the CP is in power-up phase.*

Note:

- *X = Power-off*
- *O = Normal operation*
- *A = Active*
- *C = All the MOSFETs are disabled if GENMODExx = 0*
  All the HS MOSFETs are disabled. LS MOSFETs are ON to lock the motor if GENMODExx = 1
  All the MOSFETs are ON. The microcontroller decides how to proceed if GENMODExx = 2

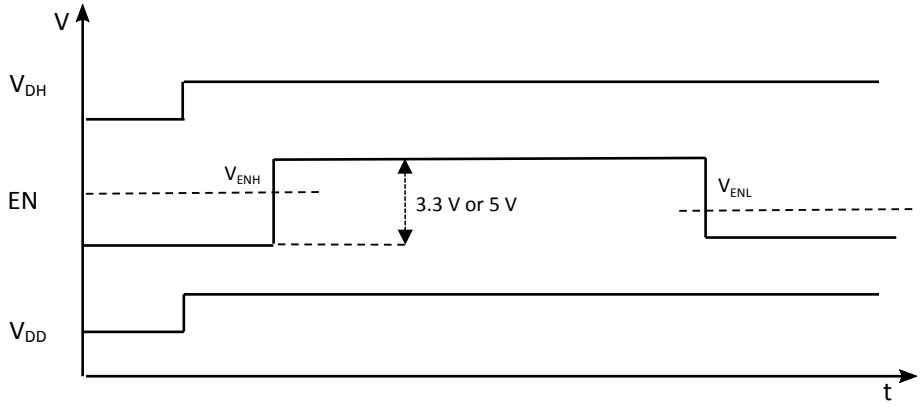
3.2.6 Power-up sequence

The power-up sequences that must be followed to turn on L99MH94 / L99MH92 are reported below.

The first case of a possible power-on sequence is shown in the Figure 13. In this case V_{DH} and V_{DD} are raised while the EN pin is kept low. After the V_{DH} and V_{DD} pins are high and stable, the EN pin is raised to turn on the device or lowered to turn it off. L99MH94 / L99MH92 turns on when the EN pin exceeds the rising V_{ENH} threshold and will turn off when it drops below the falling V_{ENL} threshold.

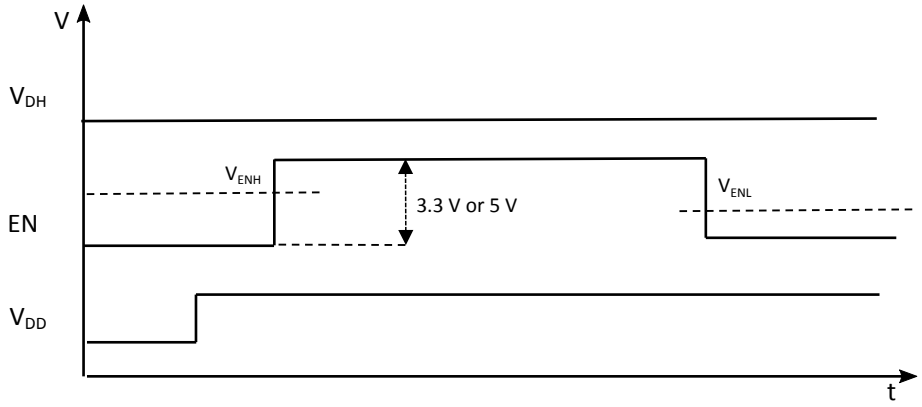
The fastest possible slew rate for V_{DD} is 100 µs at 3.3 V.

Figure 13. V_{DH} and V_{DD} high, EN pin goes high and low



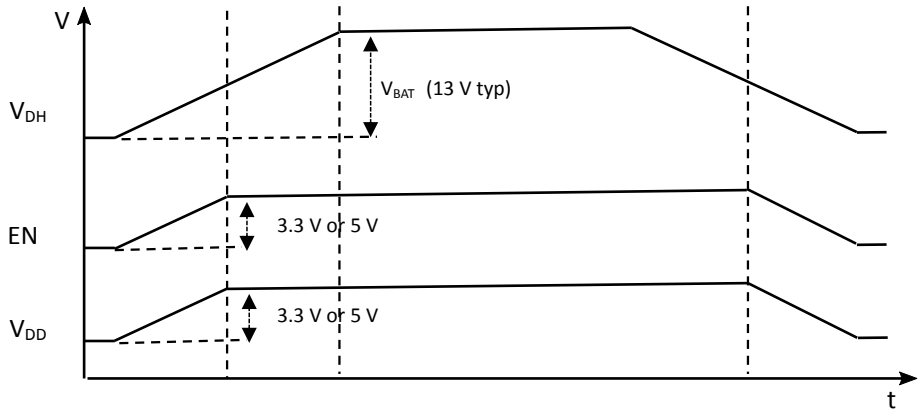
The second case of a possible power-on sequence is shown in the Figure 14. In this case the V_{DD} is raised while the V_{DH} and EN pins are kept low. After the V_{DD} pin is high and stable, the EN pin is raised to turn on the logic of the device or lowered to turn it off. L99MH94 / L99MH92 turns on when the EN pin exceeds the rising V_{ENH} threshold and will turn off when it drops below the falling V_{ENL} threshold.

Figure 14. V_{DH} low, V_{DD} high, EN pin goes high and low



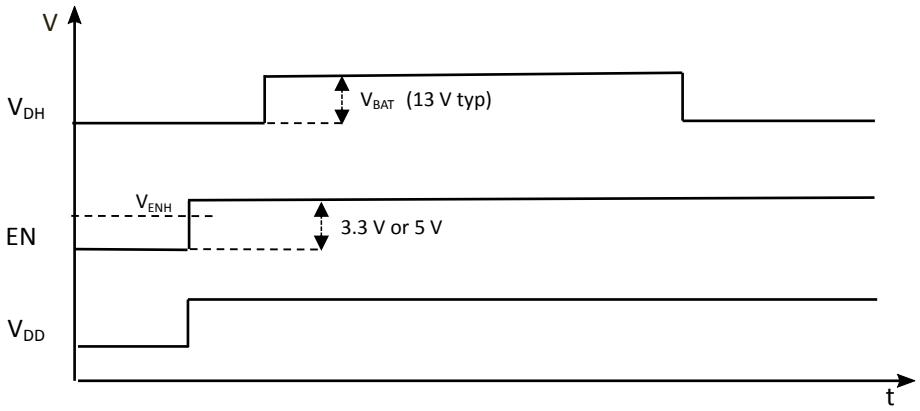
Another case of a possible power-on sequence of L99MH94 / L99MH92 is shown in the Figure 15. In this case V_{DD}, V_{DH} and EN pins are raised at the same time with the same slew rate.

Figure 15. V_{DH}, V_{DD} and EN pin goes high and low with the same slew rate



The last possible power-on sequence of L99MH94 / L99MH92 is shown in the Figure 16. It is possible to raise the V_{DD} and EN pins of L99MH94 / L99MH92 at the same time and with the same slope while keeping the V_{DH} pin low. With the V_{DD} and V_{DH} pins high it is possible to raise the V_{DH} pin to the battery and then lower it to the ground.

Figure 16. V_{DD} and EN goes high, V_{DH} goes high and low



3.3 Thermal warning and thermal shutdown (TW/TSD)

When the device junction temperature rises above the T_{jTW_ON} threshold for a time longer than $t_{fTjTW/TSD}$, the temperature warning flag TW is set and no action is taken. The TW flag can be cleared by an SPI “read and clear” command only if the thermal warning condition is no longer present for a time longer than the corresponding filtering time $t_{fTjTW/TSD}$. When the junction temperature rises above the T_{jSD_ON} threshold for a time longer than $t_{fTjTW/TSD}$, the thermal shutdown flag TSD is set and the external MOSFETs, together with the charge pump are switched off to protect the device. The LS gate drivers and the HS gate drivers remain disabled together with the charge pump until the TSD flag is cleared. The TSD flag can be cleared by an SPI “read and clear” command only if the thermal shut-down condition is no longer present, namely if $T_j < T_{jSD\_OFF}$ for a time longer than the corresponding filtering time $t_{fTjTW/TSD}$.

3.4 Charge pump

The dual stage charge pump uses two external flying capacitors, which are switched at the frequency f_{CP}, and one output capacitor connected between the CPOUT pin and the VDH pin. The output of the charge pump has a current limitation. After charge pump command enable, and after a filter time t_{CP_blank}, and without any fault, the charge pump is ready for gate driving functionality.

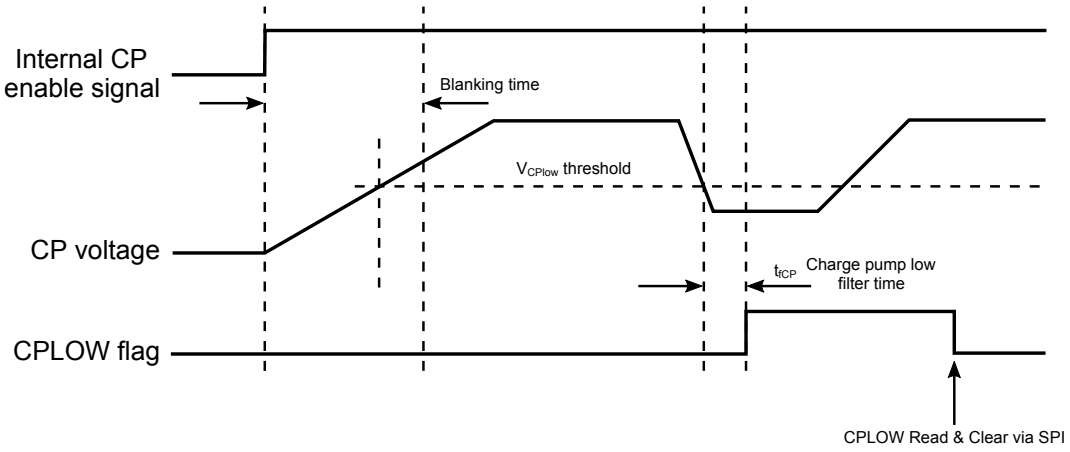
To enable the charge pump disabled by a thermal shut-down event detection, the TSD flag must be cleared.

After the charge pump start-up, after the initial blanking time, if the charge pump output voltage falls below the charge pump output voltage low threshold V_{CP_low} for a time longer than t_{CP}, the CPLOW flag is set and the external MOSFETs are switched off.

If the CP_LOW_CONFIG control bit is set to one, the CPLOW status flag becomes a status bit (set and reset automatically) and the gate drivers come out of forced disabled mode automatically upon recovery from the charge pump low voltage condition. In this case the status bit will be automatically cleared as soon as the charge pump output voltage is no longer below the low voltage threshold for a time longer than t_{CP}. If the CP_LOW_CONFIG control bit is set to zero, the gate drivers come out of forced disabled mode only once the charge pump low voltage flag CPLOW is cleared via SPI. The charge pump low voltage flag CPLOW can be cleared by a SPI “read and cear” command only if the charge pump low voltage condition is no longer present, namely if $V_{CP} > V_{CP\_LOW}$ for a time longer than t_{CP}.

To reduce electromagnetic emissions, the charge pump frequency dithering is enabled by default. However, the dithering can be disabled through the control bit CPFDD.

Figure 17. **CPLOW flag**



4 Gates driver

4.1 Outputs driving signals

To work with each half-bridge the following registers need:

1. HB_MODEx (half-bridge mode): this register is used to control the functionality of the single half-bridge. x indicates the number of the half-bridge to work on, x = 1 to 4/2. It is a 2-bit register (see the Table 24 and Table 25).
2. EN_PWMy (enable PWM): this 1-bit register is used to enable/disable the PWM signal, y indicates the PWM pins that must be enabled/disabled, y = 1...2 (see the Table 25).
3. HB_PWMx (Half bridge PWM): This 3-bit register is used to indicate which PWM signal is applied to the HS or LS of the x-th half-bridge, x = 1...4/2 (see the Table 25).

When a MOSFET of a half-bridge must be powered OFF or ON in the static mode the HB_MODEx register must be used. As an example, if the HS of the half-bridge 3 and the LS of the half-bridge 4 must be powered ON the following registers must be written:

- HB_MODE**3** = 10
- HB_MODE**4** = 01

A maximum of three PWM signals can be applied to the L99MH94 / L99MH92. Each PWM signal can be provided to each HS or LS of each half-bridge, using the correct programming of the registers HB_MODEx, EN_PWMy and HB_PWMx (see the Table 25).

As an example, an H-bridge is composed of half-bridge 2 and half-bridge 3, HS of 2 is always ON while PWM 2 is applied to the LS of half-bridge 3. In this case we have:

- HB_MODE**2** = 10 → HS of the half-bridge 2 is ON in states mode
- EN_PWM**2** = 1 → PWM2 signal is activated
- HB_PWM**2** = 001 → PWM2 signal is mapped on the LS of the half-bridge 3
- HB_MODE**3** = 11 → enable the HB3 to work in PWM mode

Configuration of the PWM map is shown in the table below:

Table 24. PWM signal application to the half-bridges

HB_PWMx	HB_MODEx	Setting
X	00	LS and HS of the half-bridge x are kept OFF (default).
X	01	LS of the half-bridge x is ON (static, no PWM), HS of the half-bridge x is OFF
X	10	HS of the half-bridge x is ON (static, no PWM), LS of the half-bridge x is OFF
000	11	Low-side of half-bridge x mapped on PWM1. EN_PWM1 must be set to 1
001	11	Low-side of half-bridge x mapped on PWM2. EN_PWM2 must be set to 1
010	11	No mapping
011	11	High-side of half-bridge x mapped on PWM1. EN_PWM1 must be set to 1
100	11	High-side of half-bridge x mapped on PWM2. EN_PWM2 must be set to 1
101	11	No mapping
110	XX	No mapping, if used the LS and HS of the half-bridge x are kept OFF
111	XX	No mapping, if used the LS and HS of the half-bridge x are kept OFF

The PWMx input pins have an internal pull-down current in order to put the outputs in a well-known condition in case any of the pins will no longer be driven by the microcontroller.

Four different free-wheeling strategies are available in the L99MH94 / L99MH92: active or passive freewheeling on either high-side or low-side MOSFETs. To choose the correct free-wheeling method the HB_WHEELx, x = 1...4/2, must be programmed according to the Table 25.

Table 25. **Free-wheeling mode**

HB_WHEELx, x=1...4/2	Setting
00	Passive free-wheeling
01	Active free-wheeling on HS of the half-bridge x
10	Active free-wheeling on LS of the half-bridge x
11	Passive free-wheeling

In the active free-wheeling case, the MOSFET is actively switched off by the pre-driver. In active free-wheeling the current is fixed. It is possible to configure two different currents according to the STRONG_ON_WHEELx, x = 1...8, bit: 4 mA if the bit is set to 0, 30 mA if the bit is set to 1.

If the microcontroller, in a not correct way, should program a PWM and an active free-wheeling in a MOSFET at the same time, L99MH94 / L99MH92 assigns the PWM to the selected MOSFET.

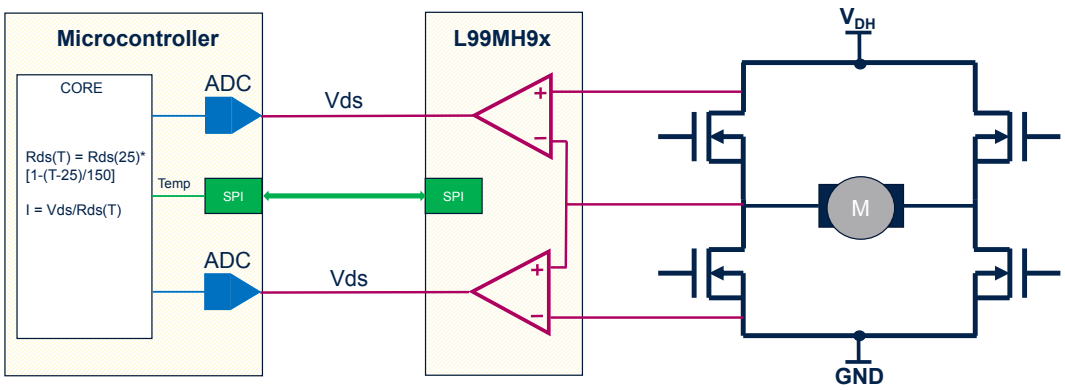
4.2 Indirect current measurement for external MOSFET

A new and innovative current sense method, different from the classical voltage drop on the shunt resistors, has been designed and here reported. The proposed method has the great advantage of not using external resistors, with the consequence of a lower cost of the application and no voltage drop on the sensing resistors.

The new current sense method is made up of 5 different phases:

1. CSO settings according to the used external MOSFETs;
2. Rds(on) and temperature calibration at application level;
3. Rds(on) prediction curve stored in the external µC;
4. Live temperature measurement for MOSFET Rds(on) prediction;
5. Real time V_{ds} measurement via CSO1 pin and external MOSFET current calculation (done at µC level).

Figure 18. **Overview of indirect current measurement**



4.2.1 Rds(on) calibration at application level

The first phase of current sensing is that of a correct measurement of the Rds(on) of each MOSFET of the 4 external H-bridges. This is because the Rds(on) of the MOSFETs have a large variability that can go up to ±25% of the typical value. Thus, to have a precise measurement of the current, a calibration must be performed during the manufacturing process. The Rds(on) calibration of each MOSFET must be done using the following strategy at room temperature:

1. Power on the MOSFET under measurement;
2. A fixed current, 1 A for instance, is sent in the drain pin. The V_{ds} is measured by L99MH94 / L99MH92;
3. The microcontroller calculates the Rds(on) = V_{ds}/1 A. This value is stored in the microcontroller memory. This value represents the Rds(on) of the MOSFET at room temperature;
4. The curve of the variation of the Rds(on) as function of the temperature is stored in the microcontroller memory.

4.2.2 V_{ds} measurement

The L99MH94 / L99MH92 is able to reflect the drain to source voltage across each of the external MOSFETs with some gain on one of the CSO1 pin. This is done for both the low and high side MOSFETs using an analog multiplexer. This allows the user, through SPI, to select and monitor the drain to source voltage on any MOSFET for the purpose of load current estimation. The selected drain source voltage is reflected on the CSO1 pin when the MOSFET is fully on. To do this, the CSO1 pin are tri-stated when the selected MOSFET is OFF and enabled, after some dead time, when the MOSFET is ON. This allows a small capacitor on the CSO1 pin to sustain the amplified drain to source voltage for reliable conversion by the ADC of the microcontroller.

The CSO1 output can be enabled/disabled by the CSOEN register. In case of disable the output is in high impedance.

The V_{ds} of all 8/4 MOSFETs connected to L99MH94 / L99MH92 can be measured. To map one of the V_{ds} to the CSO1, the two CSOSIG and CSO registers must be used (see the Table 26).

To read the V_{ds} voltage the device uses internal current sense amplifiers circuits. In this way, the L99MH94 / L99MH92 can reflect the drain to source voltage across each of the external MOSFETs, with a gain on one of the CSO1 pin. This is possible for both low and high side MOSFETs using an analog multiplexer. The error of the selected gain is included in the total error parameter.

The total gain of the CSO is composed by the contribution of two different stages:

- The gain of the first stage is related to the drain-source monitoring thresholds of the used MOSFET (VDS_CONFx bits). By setting the drain-source monitoring threshold to 75 mV (VDS_CONFx = 0000) or 150 mV (VDS_CONFx = 0001), the gain of the first stage will be set to 10 [V/V]. For drain-source monitoring thresholds from 200 mV (VDS_CONFx = 0010) to 400 mV (VDS_CONFx = 0101), however, the gain of the first stage is set to 2.5 V/V.
- The second stage gain, on the other hand, is controlled by a bit for each CSO channel, CSO_GAIN_SELx register. In this case the gain does not refer on how the single MOSFET is set, but it is a parameter related to the single CSO channel. When CSO_GAIN_SEL = 0 the gain set is 1.5 V/V, when CSO_GAIN_SEL = 1 is 3 V/V.

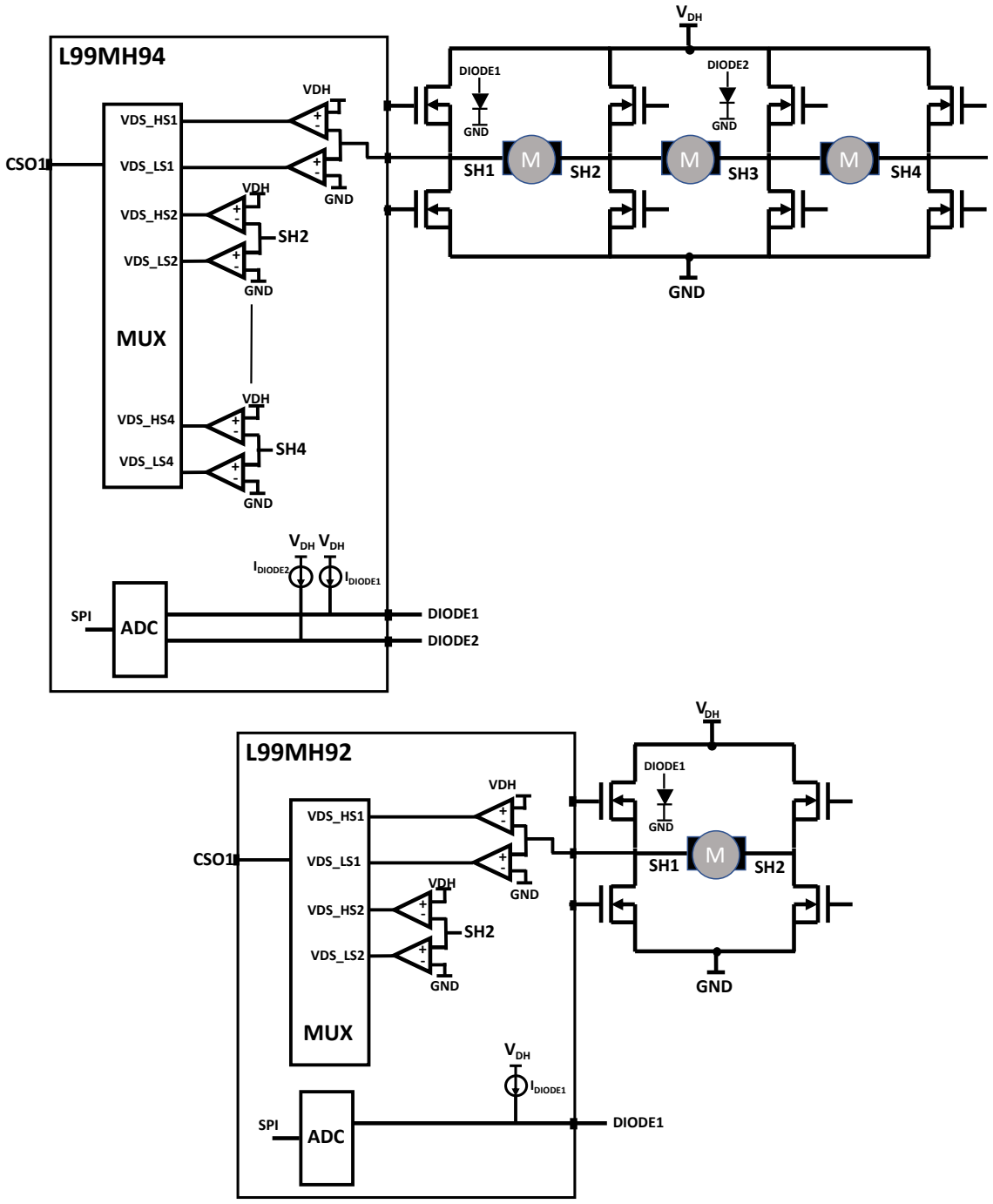
The total gain is, therefore, given by the product of the two selected gains.

The choice of the gains will be made according to the output voltage of the CSO. Since the validity of the output of the CSO is granted if its value is in the range between 0.1 V and VDD-0.3 V, the gains to choose must be set to obtain a compatible CSO output value (approximately in the middle of this range), starting from the considered input value of V_{ds}.

Table 26. V_{ds} mapping on CSO1

CSOSIG	CSOSH	Setting
0	00	V_{ds} of the HS1 mapped on the CSO1
0	01	V_{ds} of the HS2 mapped on the CSO1
0	10	L99MH94: V_{ds} of the HS3 mapped on the CSO1 L99MH92: No mapping
0	11	L99MH94: V_{ds} of the HS4 mapped on the CSO1 L99MH92: No mapping
1	00	V_{ds} of the LS1 mapped on the CSO1
1	01	V_{ds} of the LS2 mapped on the CSO1
1	10	L99MH94: V_{ds} of the LS3 mapped on the CSO1 L99MH92: No mapping
1	11	L99MH94: V_{ds} of the LS4 mapped on the CSO1 L99MH92: No mapping

Figure 19. V_{ds} measurement by CSO1



4.2.3 Temperature measurement for calibration and monitoring

To further improve indirect current measurement, a temperature control (via 4 external diodes/diode chain) is implemented inside the L99MH94 / L99MH92. Each diode/chain will be placed as close as possible to each H-bridge or to a relevant temperature hot-spot. The forward voltage, V_f, of the diode varies with temperature, therefore the diode's temperature coefficient is needed to get an accurate representation of the junction temperature. The control structure of the diodes is constituted by a current generator that injects a small current (programmable from 250 µA to 1 mA) in the anode of the diode while the cathode will be connected to the ground pin of the L99MH94 / L99MH92.

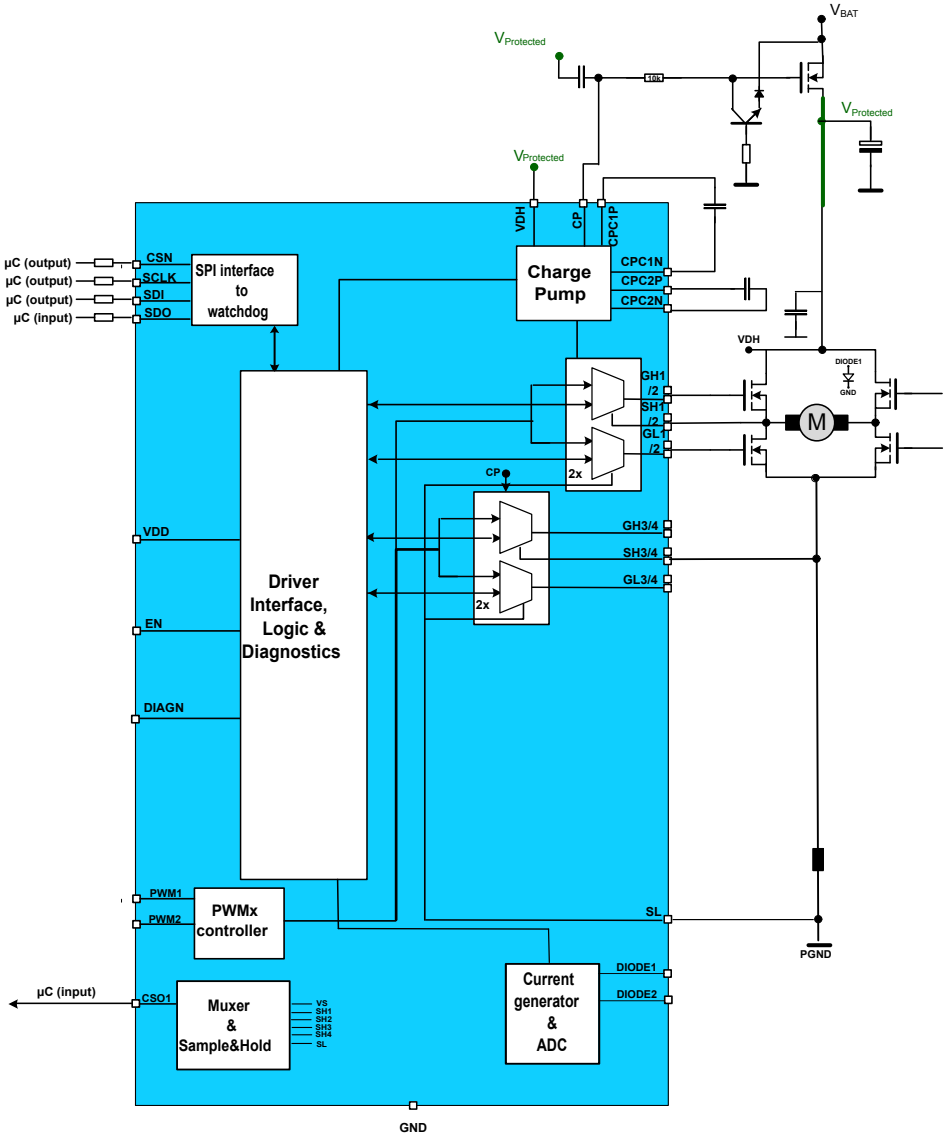
The voltage across the diode will then be measured by an internal ADC which will make the value available to the microcontroller: 4 dedicated registers, DIODEx_READ, x = 1...4, will report the read values to the microcontroller by SPI communication. The interval time between one temperature measurement and another is of 1 ms typ. If one or more diodes are not connected the information related to the connected diodes will always be available after 1 ms.

Reading the Vf(x°C) at an unknown temperature, knowing the V_f (25 °C) at 25 °C and knowing the temperature coefficient of the V_f, the microcontroller calculates the working temperature by applying the following formula:

$$T[C] = T[25\,^{\circ}C] + \left[V_f(x\,^{\circ}C) - V_f(25\,^{\circ}C)\right]/TenperatureCoefficient \quad (1)$$

V_f (25 °C) varies slightly from device to device: to overcome this behavior, a calibration data during the manufacturing process can be applied: in this case the V_f (25 °C) can be measured in the manufacturing process and the value can be stored in the microcontroller memory.

Figure 20. L99MH94 application diagram for temperature measurement



If a more precise temperature measurement is required, two heat map methods can be adopted:

1. The first way is to measure the temperature difference between the H-bridge MOSFET and the point where the diode(s) is soldered through the thermal map of the application board. The temperature difference between the two points is then saved in the memory of the microcontroller as a corrective factor: each time the microcontroller carries out the temperature measurement through the diode it applies the previously stored correction factor to obtain a temperature measurement of the MOSFET closest to reality.
2. The second solution is to foresee places in the PCB where the diode(s) can be soldered in order to find the best spot to sense the temperature. By making a heat map of the application board the user will be able to discover the most suitable place where to put the thermal sensor. In this way the measurement made by the diode will be the closest to real MOSFET temperature. In any case, a corrective factor, as foreseen in point 1, can be considered. The thermal sensor(s) can also be used in the normal working mode for controlling the maximum PCB temperature.

The monitor of the external 4 diodes/chains allows to detect steady, not fast, temperature raising of specific PCB areas; a temperature control of the module can be also implemented via the external diodes.

4.2.4 H-bridge current calculation

After having known the temperature at which the H-bridge is working and having measured the V_{ds}, the microcontroller will be able to evaluate the working current. To do this, the microcontroller must follow two simple calculations:

- Calculate Rds(on) at working temperature. The microcontroller has in its memory the trend of the variation curve of the Rds(on) in temperature: knowing the temperature, it can estimate the value of the Rds(on) at the temperature in which the H bridge is working.
- Calculate the current. At this point the microcontroller has calculated the value of the Rds(on) and has acquired the measured value of the V_{ds}: the current flowing in the bridge H is easily calculated as the ratio between V_{ds}/Rds(on).

4.3 Power ON/OFF

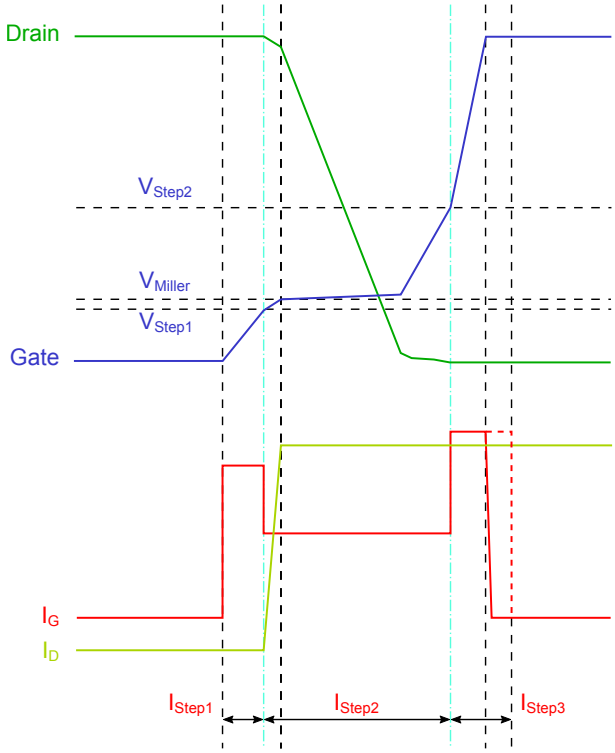
4.3.1 Three stages gate current

A tailored gate current strategy for the $T_{on/off}$ of the external MOSFETs, called “three stages gate current”, has been implemented in the L99MH94 / L99MH92. Behavior is showed in the Figure 21.

The new gate current strategy is implemented in the following three stages:

- **Stage 1**
  The first stage occurs when $V_{GS} < V_{step1xl}$, x = 1...4 for L99MH94 and x = 1, 2 for L99MH92, in case of switch ON of the external MOSFETs or $V_{GS} < V_{step1xh}$, x = 1...4 / x = 1, 2, in case of switch OFF of the external MOSFETs. In the first stage the gate drive current will be I_{onx} (ISTEP1_CONFx, x = 1...4 / x = 1, 2 register), x = 1...4 / x = 1, 2, in cases of switch ON and I_{offx} (ISTEP1_CONFx, x = 1...4 / x = 1, 2, register), x = 1...4 / x = 1, 2, in case of switch OFF of the external MOSFETs.
- **Stage 2**
  The second stage occurs when $V_{step1xh} < V_{GS} < V_{step2xh}$, x = 1...4 / x = 1, 2, in case of switch OFF of the external MOSFETs or $V_{step1xl} < V_{GS} < V_{step2xl}$, x = 1...4 / x = 1, 2, in case of switch ON of the external MOSFETs. In this second stage the gate drive current can be programmed differently in the switch ON and switch OFF phases. In case of switch ON, the I_{onx}, x = 1...4 / x = 1, 2, is set programming the ISTEP2_CONFx, x = 1...4 / x = 1, 2, register. In case of switch OFF, the I_{offx}, x = 1...4 / x = 1, 2, is set programming the ISTEP2_OFF_CONFx, x = 1...4 / x = 1, 2, register.
- **Stage 3**
  The third stage occurs when $V_{GS} > V_{step2xl}$, x = 1...4 / x = 1, 2, in case of switch ON of the external MOSFETs or $V_{GS} > V_{step2xh}$, x = 1...4 / x = 1, 2, in case of switch OFF of the external MOSFETs. In the third stage the gate drive current will be I_{onx} (ISTEP3_CONFx, x = 1...4 / x = 1, 2 register), x = 1...4 / x = 1, 2, in cases of switch ON and I_{offx} (ISTEP3_CONFx, x = 1...4 / x = 1, 2 register), x = 1...4 / x = 1, 2, in case of switch OFF of the external MOSFETs.

Figure 21. **Power ON/OFF steps for gate drivers**



5 Protections and diagnostics

5.1 Reverse polarity protection

The output of the charge pump (CPOUT pin) can be used to supply an external n-channel MOSFET, building an active reverse polarity protection (refer to the Figure 22).

5.2 Programmable cross current protection time (DT)

In any input mode (quad/dual half-bridge mode or full-bridge mode), the device adds the configured dead-time between the turn-off of a MOSFET and the turn-on of the complementary one (that is, the other MOSFET of the same leg) to avoid cross-conduction in any of the half-bridges. Two different methods have been implemented to choose the starting point of the cross-current protection time according to the DTP_REF bit. If the DTP_REF = 0, the cross-current protection time is calculated starting from the command to switch off a MOSFET and switch on the complementary. If the DTP_REF = 1, the cross current protection time is calculated starting from the instant in which the V_{gs} of the MOSFET being switched off has reached the value set in the V_{STEP1x}. In quad/dual half-bridge mode each half-bridge dead-time t_{DTxxx} is independently configurable by control bits DTx[2:0], x = 1...4/2.

5.3 Short circuit detection/drain source monitoring (DSHS/DSLS)

The voltage-drop over each MOSFET is sensed and compared to a programmable threshold to detect an overcurrent condition. This monitoring is activated only on the external MOSFETs of the half bridges driven to be ON. In the L99MH94 / L99MH92 each half-bridge has its own programmable threshold (VDS_CONFx[3:0], x = 1...4/2), blanking time (VDS_BLANKx[3:0], x = 1...4/2) and filtering time (VDS_FILTx[2:0], x = 1...4/2).

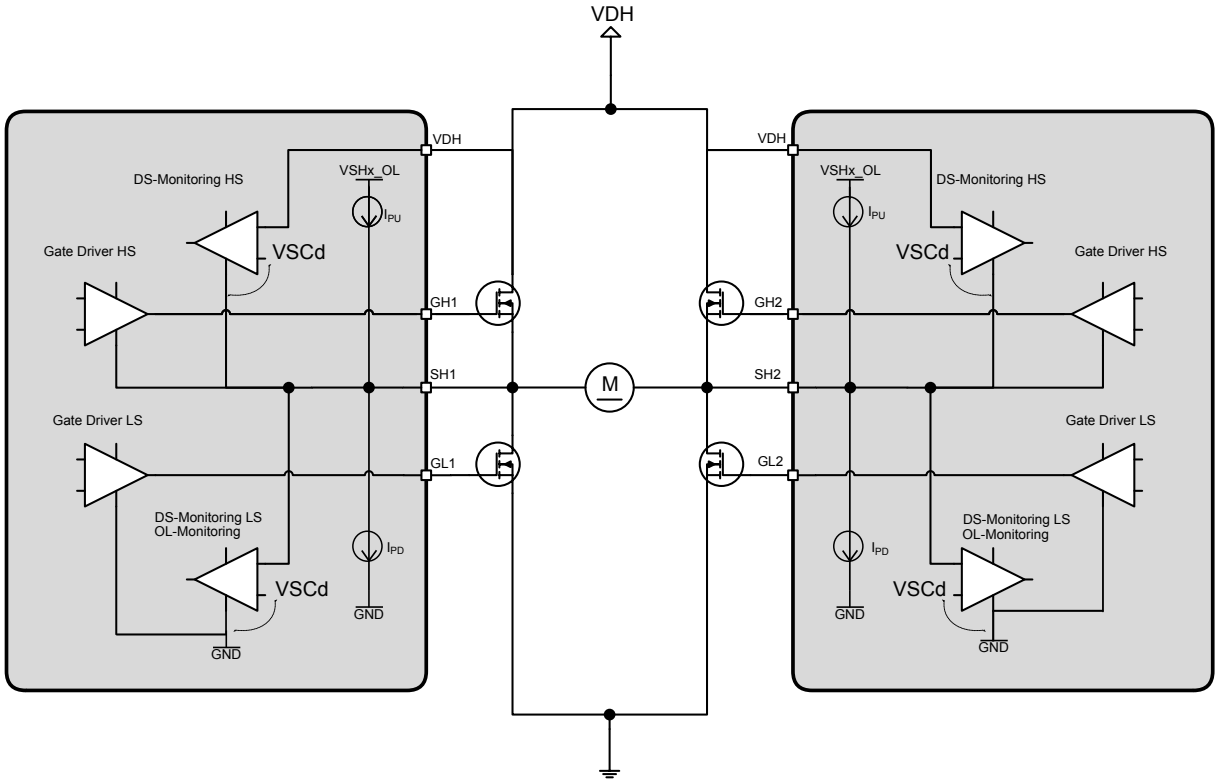
As soon as the gate driver starts to turn ON a MOSFET, the corresponding drain source monitoring comparator output is masked for the programmed blanking time to give time to the MOSFET to turn on. After the blanking time is expired, a filtering time is applied to filter noise. Both values must be chosen depending on the application.

If the voltage-drop over the driven MOSFET exceeds the programmed threshold voltage V_{SCdx} (VDS_CONFx[3:0], x = 1...4/2) for a time longer than the programmed filtering time (and the programmed blanking time, where applicable), either the gate drivers belonging to the faulty leg are forced to switch off actively the half-bridge MOSFETs with the maximum available current, regardless of the programmed gate discharge current bits.

In any case the drain source monitoring flag VDSHSx, x = 1…4/2, or VDSLSx, x = 1...4/2, of the MOSFET detecting the fault is set. The drain source monitoring flags must be cleared through SPI to reactivate the affected half-bridge/full-bridge gate drivers that are forced in disabled mode. The drain source monitoring flag VDSHSx/ VDSLSx can be cleared by an SPI “read and clear” command only if the fault condition is no longer present.

If the voltage-drop over the driven MOSFET still exceeds the programmed threshold voltage V_{SCdx} (VDS_CONFx[3:0], x = 1...4/2) for a time longer than the programmed filtering time (and the programmed blanking time, where applicable) after the SPI “read and clear” command, the drain source monitoring flag VDSHSx, x = 1...4/2, or VDSLSx, x = 1...4/2 will be set again. It is up to the microcontroller to decide how many attempts to make before finally turning off the half-bridges where the over current is present.

Figure 22. **Full-bridge drain source monitoring diagnosis**



5.4 Diagnostic in off-mode

5.4.1 Off-state diagnostic introduction

The off-state diagnostic features (that is, the MOSFETs are off while the diagnostic is performed) offer several advantages:

- Diagnostic checks can be performed for loads that are infrequently activated.
- MOSFET short circuit conditions are detected without the stress inherent to on-state diagnostic mode. For example, the microcontroller can perform an off-state diagnostic right before the activation request of the load. Upon the fault condition, the application software can report the failure and inhibits the load activation, avoiding any stress to the MOSFETs.

To perform the off-state diagnostic the following suggestions must be taken:

- The half-bridge drivers must be in active mode: EN = High, OUTEx = 1, x = 1...4/2
- The corresponding MOSFETs are off: HB_MODEx = 00, x = 1...4/2
- The device is operating in normal mode:
  - V_{DH} and V_{DD} are in the normal operating range
  - No watchdog failure

Note: It is highly recommended to restore the setting of V_{SCdx} once the off-state diagnostic is performed for an appropriate MOSFET protection in on-state.

The L99MH94 / L99MH92 enables the detection of the following fault conditions while the MOSFETs are deactivated:

- SHx is shorted to V_{DH}
- SHx is shorted to GND
- Open load

The Figure 23 shows the block diagram of the off-state diagnostic functionality integrated into the L99MH94 / L99MH92.

The following integrated components are used to perform the off-state diagnostic:

- Pull-up diagnostic current (I_{shx_PU})
- Pull-down diagnostic current (I_{shx_PD})
- Comparator for the high-side (HS) and low-side (LS) drain-source voltage monitoring
- The checked node can go up or down and it is not bounded to the pull-up value of the off state

I_{shx_PU} and I_{shx_PD} can be activated for each half-bridge only if the bridge driver is in active mode as set by the control bits OUTEx, x = 1…4/2. Also I_{shx_PU} and I_{shx_PD} can be activated only when the off-state diagnostic is enabled by the microcontroller.

The V_{ds} comparators change their state after a filter time called tDIAG. The faults in the DSRx are not latched and the configurations placed in the registers are bypassed during diag off.

The I_{shx_PU} ,and I_{shx_PD} values can be selected by using the DIAGOFF_CURR_SEL register.

The L99MH94 / L99MH92 determines the voltage at SHx, using the drain-source overvoltage comparators of the high-side or low-side MOSFETs. The microcontroller can read the status bit VDS_HSx_DIAG, x = 1...4/2, or the status bit VDS_LSx_DIAG, x = 1...4/2 to determine if V_{SHx} is high or low.

The diagnostic process is controlled by the microcontroller, whose task is:

- To activate and deactivate I_{shx_PU} and I_{shx_PD}, controlled by the HB_IDIAGx registers
- To read and interpret the status bits VDS_LSx_DIAG and VDS_HSx_DIAG

The following conditions are equivalent in the rest of this document:

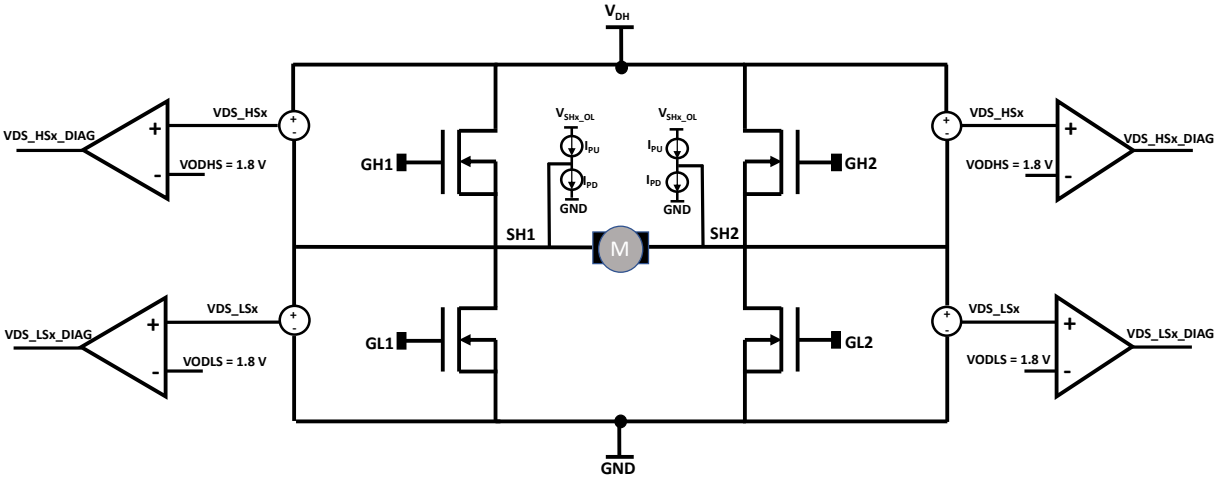
- VDS_HSx_DIAG = VDS_LSx_DIAG = 0: SHx is low
- VDS_HSx_DIAG = VDS_LSx_DIAG = 1: SHx is high

5.4.2 Example with a DC motor controlled by two half-bridges

This section gives an example of an off-state diagnostic with one DC motor controlled by the half-bridges 1 and 2. The voltages at SH1/SH2 (noted V_{SH1}/V_{SH2}) are analyzed in the following test configurations:

- **Configuration 1**
  I_{shx_PU} HB1 OFF, I_{shx_PU} HB2 OFF, I_{shx_PD} HB1 ON, I_{shx_PD} HB2 ON
- **Configuration 2**
  I_{shx_PU} HB1 ON, I_{shx_PU} HB2 OFF, I_{shx_PD} HB1 OFF, I_{shx_PD} HB2 ON
- **Configuration 3**
  I_{shx_PU} HB1 OFF, I_{shx_PU} HB2 ON, I_{shx_PD} HB1 ON, I_{shx_PD} HB2 OFF

Figure 23. Simplified block diagram with one DC motor controlled by two half-bridges



5.4.3 Normal load conditions

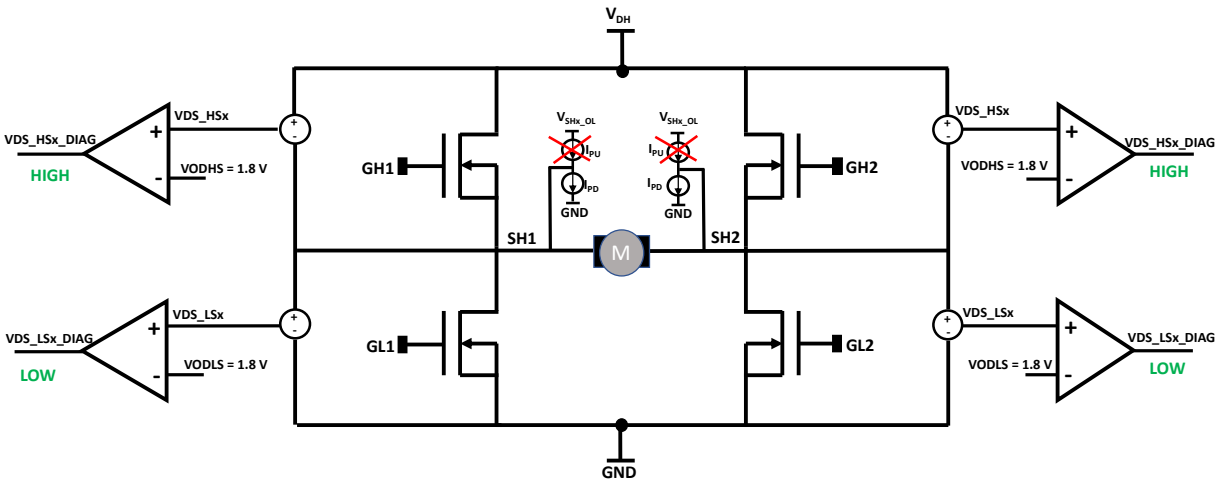
Configuration 1

- I_{shx_PU} HB1 OFF, I_{shx_PD} HB1 ON
- I_{shx_PU} HB2 OFF, I_{shx_PD} HB2 ON

In normal conditions, the motor is connected between SH1 and SH2 without any short circuit.

If I_{shx_PU} of HB1 and HB2 are off, the SH1 and SH2 are pulled down by I_{shx_PD} of HB1 and HB2 (see the Figure 24), so VDS_LS1 = VDS_LS2 = LOW and VDS_HS1 = VDS_HS2 = HIGH.

Figure 24. One motor in normal conditions, I_{shx_PU} HB1/HB2 OFF with normal load

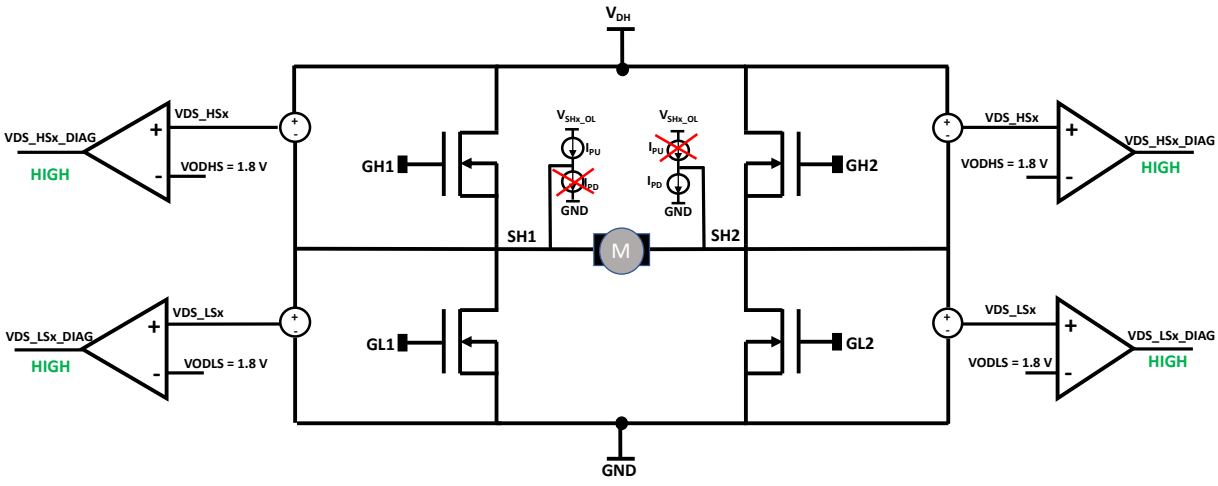


Configuration 2

- I_{shx_PU} HB1 ON, I_{shx_PD} HB1 OFF
- I_{shx_PU} HB2 OFF, I_{shx_PD} HB2 ON

With I_{shx_PU} HB1 ON the SH1 is pulled to V_{SHx_OL}, so VDS_LS1 and VDS_HS1 go HIGH (see the Figure 25). SH2 is also pulled to V_{SHx_OL} by I_{shx_PU} of HB1 via the motor, so also VDS_LS2 and VDS_HS2 go HIGH VDS_LS2.

Figure 25. One motor in normal conditions with one pull-up diagnostic current on - Configuration 2



Configuration 3

- I_{shx_PU} HB1 OFF, I_{shx_PD} HB1 ON
- I_{shx_PU} HB2 ON, I_{shx_PD} HB2 OFF

This configuration is equivalent to the configuration 2, with HB2 pull-up activated instead of HB1.

With I_{shx_PU} HB2 ON the SH2 is pulled to V_{SHx_OL}, so VDS_LS2 and VDS_HS2 go HIGH (see the Figure 25). SH1 is also pulled to V_{SHx_OL} by I_{shx_PU} of HB2 via the motor, so also VDS_LS1 and VDS_HS1 go HIGH.

The Table 27 summarizes the results obtained in normal conditions.

Figure 26. **One motor in normal conditions with one pull-up diagnostic current on - Configuration 3**

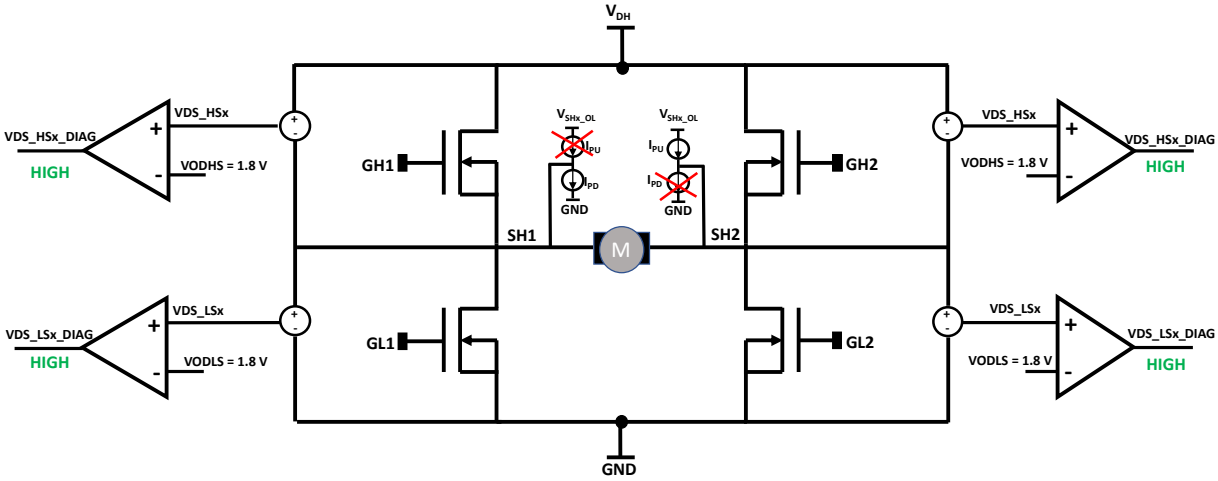


Table 27. **Truth table with normal load conditions**

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
2	ON	OFF	OFF	ON	HIGH	HIGH	HIGH	HIGH
3	OFF	ON	ON	OFF	HIGH	HIGH	HIGH	HIGH

5.4.4 Short circuit to V_{DH}

A short circuit between SH1 and V_{DH} results in VDS_HS1 = LOW and VDS_LS1 = HIGH when I_{shx_PD} HB1 and I_{shx_PD} HB2 are activated.

SH2 is also pulled up by the short circuit via the motor, so VDS_HS2 = LOW and VDS_LS2 = HIGH.

Similarly, a short circuit of SH2 to V_{DH} results in VDS_HS1/2 = LOW and VDS_LS1/2 = HIGH.

The Figure 27 and Table 28 summarize the results obtained with a short circuit of one output to V_{DH}.

Figure 27. **Short circuit to V_{DH}**

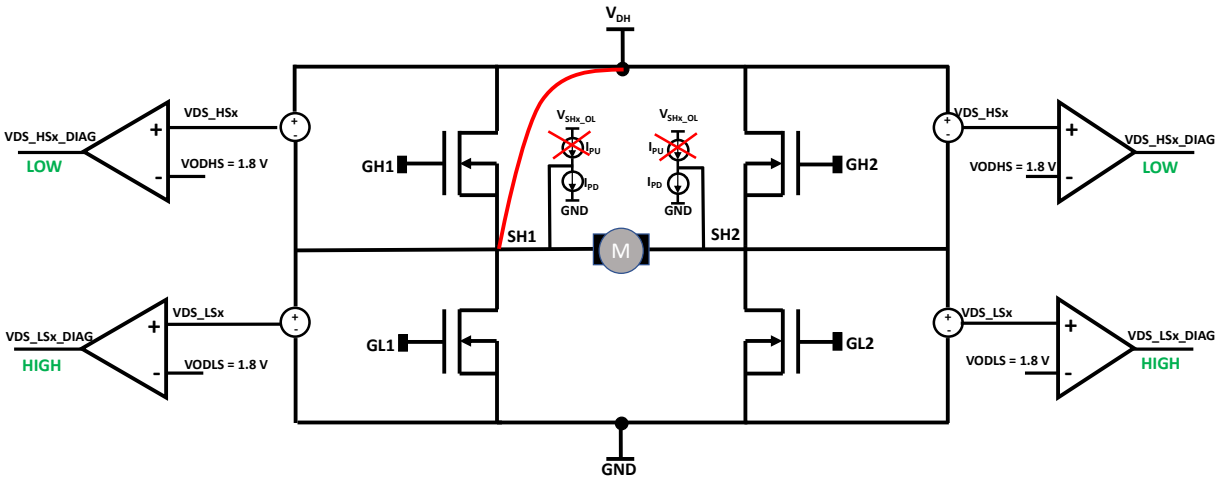


Table 28. **Truth table with a short circuit to V_{DH}**

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
1	OFF	OFF	ON	ON	HIGH	HIGH	LOW	LOW

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
2	ON	OFF	OFF	ON	HIGH	HIGH	LOW	LOW
3	OFF	ON	ON	OFF	HIGH	HIGH	LOW	LOW

5.4.5 Short circuit to GND

A short circuit between SH1 and GND results in VDS_HS1 = HIGH and VDS_LS1 = LOW even if I_{shx_PU} are activated. SH2 is pulled down by the short circuit via the motor winding, so VDS_HS2 = HIGH and VDS_LS2 = LOW.

Similarly, a short circuit of SH2 to GND results in VDS_HS1/2 = HIGH and VDS_LS1/2 = LOW, independently from the state of I_{shx_PU}.

The Figure 28 and Table 29 summarize the results obtained with a short circuit of one output to GND.

Figure 28. Short circuit to GND

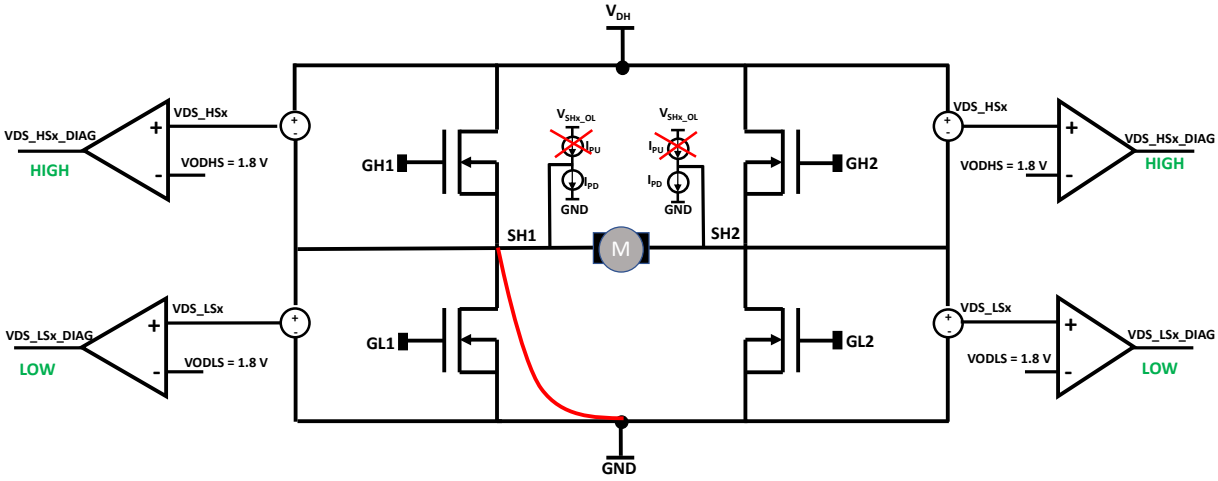


Table 29. Truth table with a short circuit to GND

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
2	ON	OFF	OFF	ON	LOW	LOW	HIGH	HIGH
3	OFF	ON	ON	OFF	LOW	LOW	HIGH	HIGH

5.4.6 Open load - SH1 disconnected

Configuration 1

- I_{shx_PU} HB1 OFF, I_{shx_PD} HB1 ON
- I_{shx_PU} HB2 OFF, I_{shx_PD} HB2 ON

SH1 and SH2 are pulled down by their respective pull-down diagnostic current, so VDS_LS1 = VDS_LS2 = LOW. VDS_HS1 and VDS_HS2, instead, are HIGH

Configuration 2

- I_{shx_PU} HB1 ON, I_{shx_PD} HB1 OFF
- I_{shx_PU} HB2 OFF, I_{shx_PD} HB2 ON

SH1 is pulled up by I_{shx_PU} HB1, so VDS_LS1 = HIGH and VDS1_HS1 = HIGH. Due to the motor disconnection at SH1, SH2 is pulled down by I_{shx_PD} HB2, so VDS_LS2 = LOW and VDS_HS2 = HIGH

Configuration 3

- I_{shx_PU} HB1 OFF, I_{shx_PD} HB1 ON
- I_{shx_PU} HB2 ON, I_{shx_PD} HB2 OFF

SH1 is pulled down by I_{shx_PD} HB1, so VDS_LS1 = LOW and VDS_HS1 = HIGH. Instead, SH2 is pulled up by I_{shx_PU} HB2: VDS_LS2 = HIGH and VDS_HS2 = HIGH.

The Figure 29 and Table 30 summarize the results obtained with an open load at SH1.

Figure 29. One motor - Diagnostic results with an open load at SH1

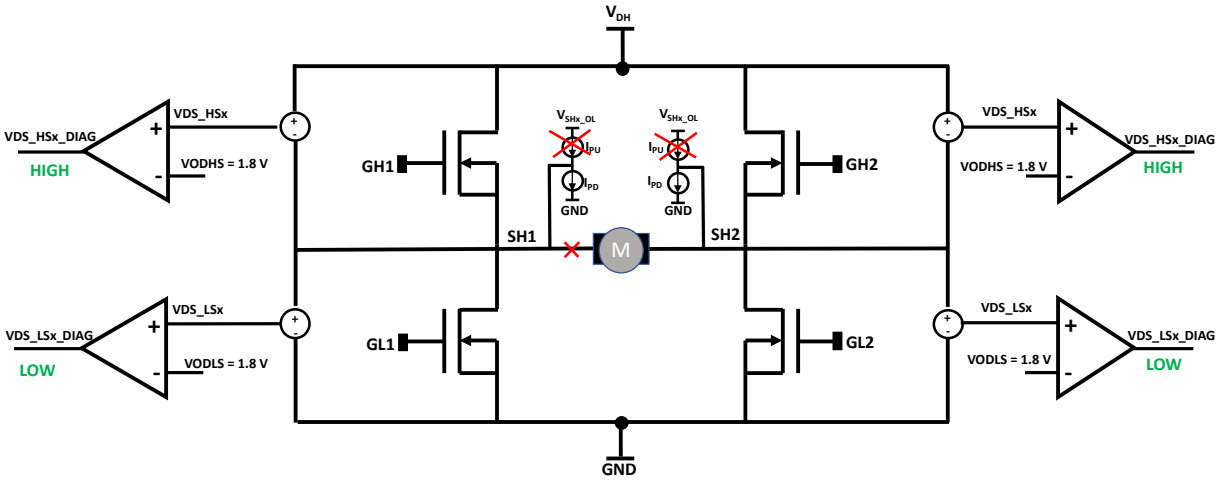


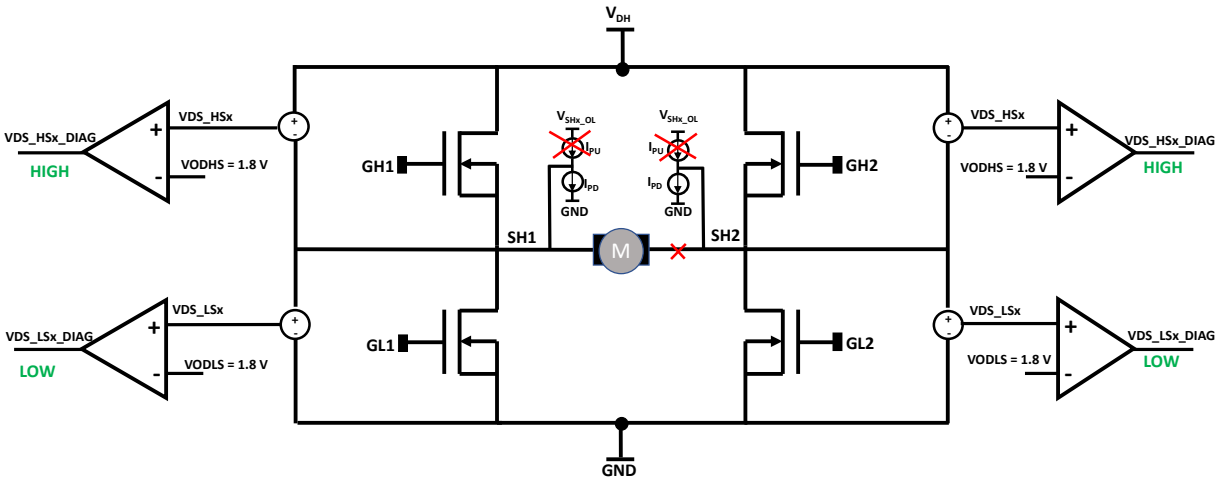
Table 30. Truth table open load - SH1 disconnected

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
2	ON	OFF	OFF	ON	HIGH	LOW	HIGH	HIGH
3	OFF	ON	ON	OFF	LOW	HIGH	HIGH	HIGH

5.4.7 Open load - SH2 is disconnected

Similarly, a motor disconnection at SH2 shows the same result as for a motor disconnection at SH1 (see the Figure 30). Therefore, the Table 30 is valid for an open load, independently from the location of the disconnection.

Figure 30. One motor - Diagnostic results with an open load at SH2



5.5 Summary of the off-state diagnostic

When compiling the results from the Table 27, Table 28, Table 29 and Table 30, we see that the test configuration 1 and the test configuration 2 (or test configuration 1 and the test configuration 3) are sufficient to detect and distinguish between a normal load condition, a short circuit to V_{DH}/GND, and an open load.

The normal condition is described in the Table 31 first line.

Short to VDH condition is described in the Table 31 second line.

Short to GND condition is described in the Table 31 third line.

Open load condition is described in the Table 31 fourth line. The pull-up and pull-down can be selected by using the register HB_IDIAGx for each half-bridge.

The available configuration is reported below:

- 00: pull-up OFF, pull-down OFF
- 01: pull-up OFF, pull-down ON
- 10: pull-up ON, pull-down OFF
- 11: pull-up OFF pull-down OFF

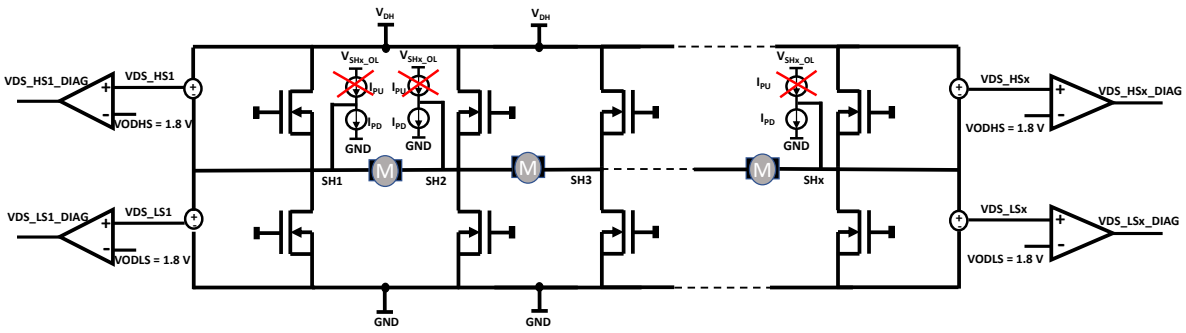
Table 31. Differentiation between normal condition, short to V_{DH}, short to GND and open load with one motor

Load conditions	Configuration	I_{PU} HBx	I_{PU} HBy	I_{PD} HBx	I_{PD} HBy	VDS_LSx	VDS_LSy	VDS_HSx	VDS_HSy
Normal condition	1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
	2	ON	OFF	OFF	ON	HIGH	HIGH	HIGH	HIGH
	3	OFF	ON	ON	OFF	HIGH	HIGH	HIGH	HIGH
Short to V_{DH}	1	OFF	OFF	ON	ON	HIGH	HIGH	LOW	LOW
	2	ON	OFF	OFF	ON	HIGH	HIGH	LOW	LOW
	3	OFF	ON	ON	OFF	HIGH	HIGH	LOW	LOW
Short to GND	1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
	2	ON	OFF	OFF	ON	LOW	LOW	HIGH	HIGH
	3	OFF	ON	ON	OFF	LOW	LOW	HIGH	HIGH
Open load	1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
	2	ON	OFF	OFF	ON	HIGH	LOW	HIGH	HIGH
	3	OFF	ON	ON	OFF	LOW	HIGH	HIGH	HIGH

5.6 Off-state diagnostic with more cascaded motors

The L99MH94 / L99MH92 allows to connect and drive up to four motors sequentially (see the Figure 31). This chapter provides hints about the off-state diagnostic with two cascaded motors controlled by three half-bridges (see the Figure 32). The same logic can be used to perform off-state diagnostics when more than two motors are connected in a sequential configuration

Figure 31. Four cascaded DC motors summary of the off-state diagnostic



The proposed principle for the off-state diagnostic consists of analyzing VDS_LS1/2/3 and VDS_HS1/2/3 when all pull-up diagnostic currents are deactivated, and when two out of three pull-up diagnostic currents are activated. The results are summarized in the Table 32.

Figure 32. **Two cascaded DC motors summary of the off-state diagnostic**

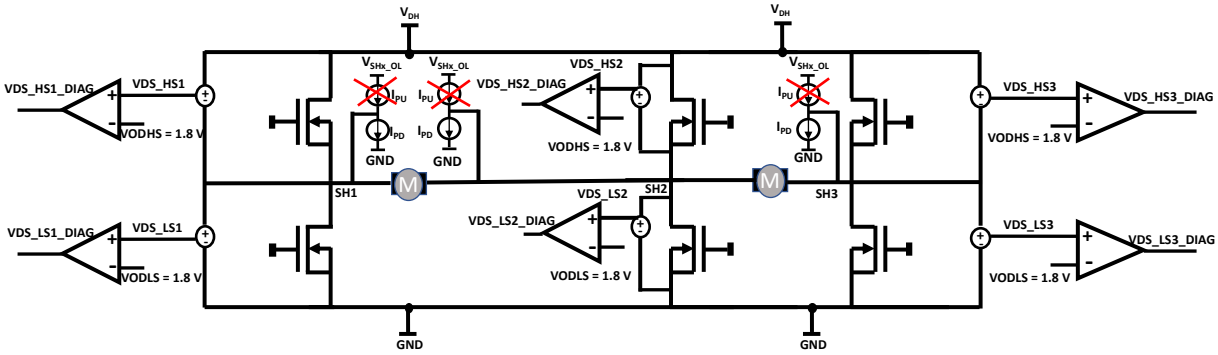


Table 32. **Differentiation between normal condition, short to V_{DH}, short to GND and open load with two motors**

Load conditions	Configuration	I_{PU} HB1	I_{PU} HB2	I_{PU} HB3	I_{PD} HB1	I_{PD} HB2	I_{PD} HB3	VDS_LS1	VDS_LS2	VDS_LS3	VDS_HS1	VDS_HS2	VDS_HS3
Normal condition	1	OFF	OFF	OFF	ON	ON	ON	LOW	LOW	LOW	HIGH	HIGH	HIGH
	2	ON	ON	OFF	OFF	OFF	ON	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
	3	OFF	ON	ON	ON	OFF	OFF	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
	4	ON	OFF	ON	OFF	ON	OFF	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
Short to V_{DH}	1	OFF	OFF	OFF	ON	ON	ON	HIGH	HIGH	HIGH	LOW	LOW	LOW
	2	ON	ON	OFF	OFF	OFF	ON	HIGH	HIGH	HIGH	LOW	LOW	LOW
	3	OFF	ON	ON	ON	OFF	OFF	HIGH	HIGH	HIGH	LOW	LOW	LOW
	4	ON	OFF	ON	OFF	ON	OFF	HIGH	HIGH	HIGH	LOW	LOW	LOW
Short to GND	1	OFF	OFF	OFF	ON	ON	ON	LOW	LOW	LOW	HIGH	HIGH	HIGH
	2	ON	ON	OFF	OFF	OFF	ON	LOW	LOW	LOW	HIGH	HIGH	HIGH
	3	OFF	ON	ON	ON	OFF	OFF	LOW	LOW	LOW	HIGH	HIGH	HIGH
	4	ON	OFF	ON	OFF	ON	OFF	LOW	LOW	LOW	HIGH	HIGH	HIGH
Open load motor 1	1	OFF	OFF	OFF	ON	ON	ON	LOW	LOW	LOW	HIGH	HIGH	HIGH
	2	ON	ON	OFF	OFF	OFF	ON	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
	3	OFF	ON	ON	ON	OFF	OFF	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
	4	ON	OFF	ON	OFF	ON	OFF	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
Open load motor 2	1	OFF	OFF	OFF	ON	ON	ON	LOW	LOW	LOW	HIGH	HIGH	HIGH
	2	ON	ON	OFF	OFF	OFF	ON	HIGH	HIGH	LOW	HIGH	HIGH	HIGH
	3	OFF	ON	ON	ON	OFF	OFF	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
	4	ON	OFF	ON	OFF	ON	OFF	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
Open load motor 1 and motor 2	1	OFF	OFF	OFF	ON	ON	ON	LOW	LOW	LOW	HIGH	HIGH	HIGH
	2	ON	ON	OFF	OFF	OFF	ON	HIGH	HIGH	LOW	HIGH	HIGH	HIGH
	3	OFF	ON	ON	ON	OFF	OFF	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
	4	ON	OFF	ON	OFF	ON	OFF	HIGH	LOW	HIGH	HIGH	HIGH	HIGH

The test configurations 1, 2, 3 are sufficient to differentiate a normal load condition from all the fault conditions.

5.7 Diagnostic not output (DIAGN)

The microcontroller can use the DIAGN pin for diagnostic.

DIAGN pin is used to detect a device fault, including a SPI error, watchdog error or a device power-on-reset event: the purpose of the DIAGN output pin is to warn immediately the microcontroller that a new fault, which the microcontroller was not yet aware of, has been detected by the device, without the need of periodic SPI transfers.

The logic level signal at the pin is the logical NOR combination of all the status flags and status bits linked to the pin through the DIAGCR1 and DIAGCR2 control registers, together with the global status byte RSTB bit.

Once the device comes out of reset mode, the DIAGN pin is pulled low because of the global status byte RSTB bit. In case that just the global status byte RSTB bit is set, any valid SPI communication frame clears the RSTB bit pulling up the DIAGN pin. Any read access to the DSR1 and DSR2 registers reset this signal to a high level, until an error coming from a new source occurs again by pulling the pin low.

DIAGN pin is active low as default, but it is possible to change its functionality by the DIAGN_ACTIVE_LEVEL bit: setting this bit to one the DIAGN pin will be active high.

If a fault coming from a new error source occurs during the read access to the DSR1 and DSR2 registers, the DIAGN output pin remains low (this avoids any loss of information since the new error source status flag/bit will not be reported by the concomitant read access, but a new read access would be required).

Even if a read operation of the status register should always come before a “read and clear” operation: any “read and clear” operation of status registers DSR1 and DSR2 will pull the DIAGN pin high.

5.8 Configurable window watchdog

Out of reset mode, the L99MH94 / L99MH92 watchdog monitors the microcontroller status within a periodic window. By default, as soon as the device finishes the powerup phase, the watchdog is enabled and starts running with a long open window. The long open window provides more time to the microcontroller for the L99MH94 / L99MH92 initialization and allows the watchdog disabling procedure to be run when no watchdog is required by the application.

To trigger the watchdog for the first time during a LOW (long open window), the microcontroller must write 5555h to the watchdog trigger/disable register (WDGTRDIS) before the end of the long open window.

After the first valid watchdog trigger, the watchdog will enter in window mode. In window mode the microcontroller has to serve the watchdog by alternating the watchdog trigger bits (that is, 2AAAh,5555h,…) of the watchdog trigger/disable register (WDGTRDIS) within the watchdog open window. Any correct watchdog trigger SPI frame will immediately start a new window.

In case of a watchdog failure, because of any watchdog trigger outside the open window, invalid or unexpected watchdog trigger bits value, any watchdog timeout, any disabling procedure out of the LOW or any wrong disabling procedure during the LOW will set the WDG_ERROR flag, stop the watchdog and put the device in fail-safe mode. In fail-safe mode the OUTEx control bits are reset, and the gate drivers are forced to switch off actively all the MOSFETs with the maximum available current, regardless of the programmed gate discharge current. To reactivate the gate drivers that are forced in disabled mode, the WDG_ERROR flag must be cleared via SPI (clearing the WDG_ERROR flag makes the device come out of the fail-safe mode and makes the watchdog start again with a long open window) and then the OUTEx control bits must be set to one via SPI. As long as the device is in fail-safe mode (WDG_ERROR = 1), the OUTEx control bits are reset and cannot be set via SPI.

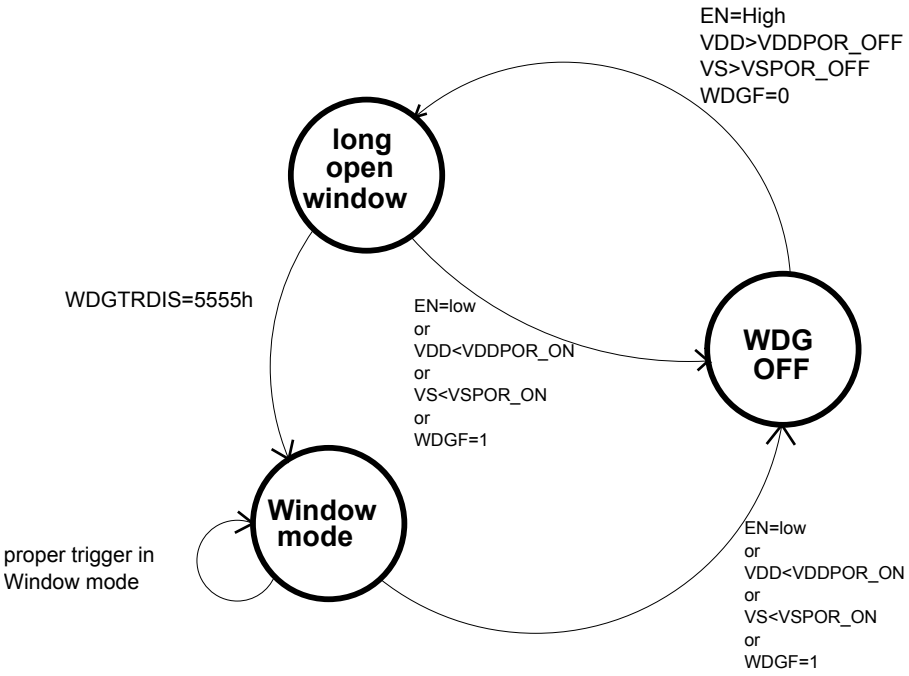
Once the watchdog starts running again with a long open window after coming out of the fail-safe mode, to enter in window mode the microcontroller must write 5555h to the watchdog trigger/disable register (WDGTRDIS).

To disable the watchdog, the microcontroller must write a specific key, consisting in two consecutive valid SPI frames to be sent in the right order (2F6Bh first key word, 1097h second key word), to control register WDGTRDIS, within a window ($t_{timeout}$). To enable the watchdog, the microcontroller must write a specific key, consisting in two consecutive valid SPI frames to be sent in the right order (5C99h first key word, 4360h second key word), to control register WDGTRDIST, within a window ($t_{timeout}$).

Any other SPI transfer between the two SPI frames carrying the key, including an invalid SPI transfer, will abort the disabled process and generate a watchdog fault (WDG_ERROR). Besides, the keys sent in the wrong order will not disable the watchdog and generate a watchdog fault as well.

Any read access to the WDGTRDIS register provides information concerning the watchdog disabling procedure result together with the three least significant bits of the latest write operation performed on the same register.

Figure 33. **Watchdog state diagram**



6 Serial peripheral interface (SPI)

A 24-bit SPI is used for bidirectional communication with the microcontroller.

The microcontroller SPI peripheral must run in the following configuration:

- CPOL = 0
- CPHA = 1

In this configuration the input data from the SDI pin is sampled by the high to low transition of the serial clock CLK, and the output data is changed by the low to high transition of the serial clock CLK.

The correct reception of any SPI frame is not guaranteed during a t_{START} time after the enable pin goes high with the VDD supply already ON.

The SPI protocol implemented in L99MH94 / L99MH92 is an out-of-frame: the IC provides on the frame n+1 the content of the reading request on the frame n.

Note: The SPI bus can be used in a parallel configuration by controlling the CSN signal of the connected IC's.

It is advisable to read the global status SPI registers after the power-up in order to clear the diagnostic.

Chip select not (CSN)

The CSN input pin is used to address the SPI communication with the device. When CSN is high, the output pin (SDO) is in high impedance. When CSN is low, the output pin (SDO) driver is enabled, and a serial communication can start. The information transferred during CSN = 0 is called a communication frame. When CSN = high for t > t_9 the SDO output is switched into high impedance to allow SPI communications with other SPI nodes.

Serial data in (SDI)

The SDI input pin is used to transfer data into the device. The data applied to the SDI will be sampled on the falling edge of the serial CLK signal and shifted into an internal 24-bit shift register. At the rising edge of the CSN signal the content of the shift register will be transferred to the data input register. The writing to the selected data input register is enabled only if exactly 24 bits are transmitted within one communication frame (that is, CSN low). Instead, the writing to the selected data input register is not enabled if one of the following cases happens:

- More or less than 24 clock pulses are counted within one frame
- During the falling and rising edge of CSN the level of SCLK is not low
- All bits of a command received at SDI are logic 0 or logic 1
- The number of CKL rising edges in a frame is not 24
- The address field is unknown
- The parity check fails

This safety function is implemented to avoid an activation of the output stages by any wrong communication frame.

Serial data out (SDO)

The SDO output driver is activated by a logical low level at the CSN input and will go from high impedance to low or high level depending on the global error flag value (GSBN bit). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the "SPI error or RESET" bit and, immediately after, the global status byte bit out. Each subsequent rising edge of the CLK shifts the following bits out.

Serial clock (CLK)

The CLK input pin is used to synchronize the input and output serial bit streams. The data input (SDI) is sampled on the falling edge of the CLK and the data output (SDO) will change on the rising edge of the CLK. The SPI can work with a CLK frequency up to 6 MHz.

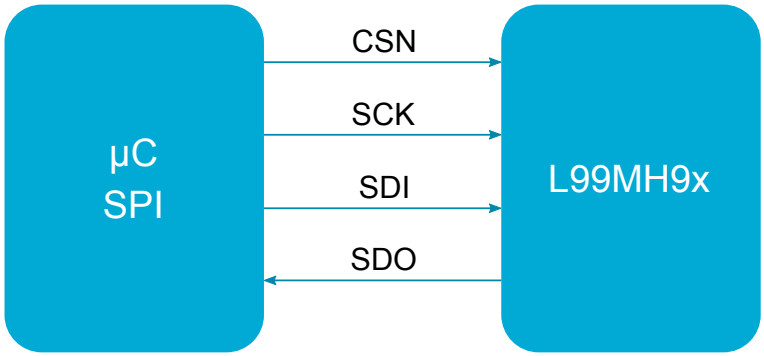
6.1 Physical layer

This chapter describes the SPI protocol configuration. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, fail-safe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

The SPI connection between the microcontroller and the L99MH94 / L99MH92 is shown in the Figure 34.

Figure 34. **SPI connection**



6.2 Clock and data characteristics

The L99MH94 / L99MH92 SPI can be driven by a microcontroller with its SPI peripheral.

Any communication frame starts with the falling edge of the CSN (communication start). CLK must be low.

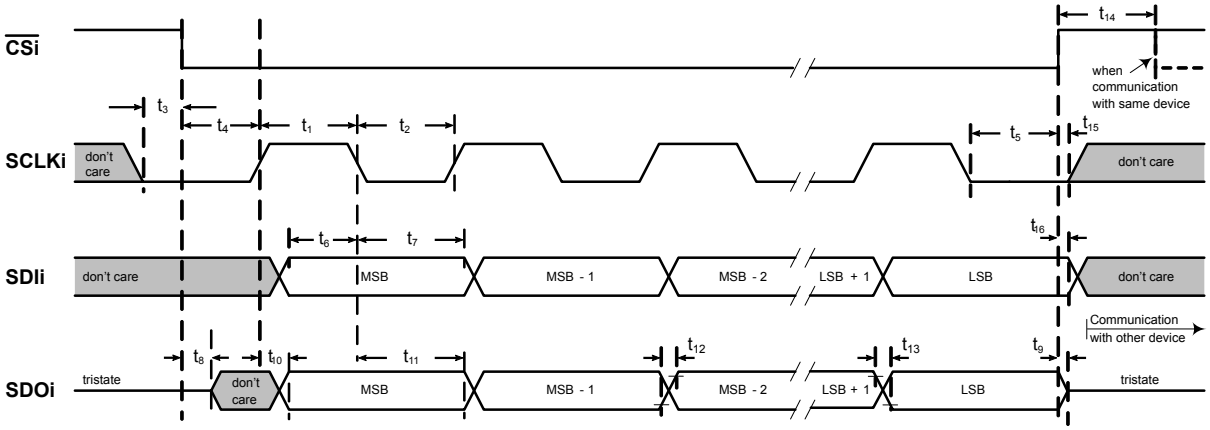
The SDI data is then latched at all following rising CLK edges into the internal shift registers.

After communication start the SDO leaves 3-state mode and presents the MSB of the data shifted out to SDO. At all following falling CLK edges data is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication took place (for example, correct number of CLK cycles, access to a valid address, no parity error), the requested operation according to the operating code will be performed (write or clear operation).

The SPI signal description is shown in the Figure 35.

Figure 35. **SPI signal description**



6.3 Communication protocol

6.3.1 SDI frame

The device data-in frame consists of 24 bits (OpCode (1 bit) + Reserved (1 bit) + Address (6 bits) + Data Byte 2 (8 bits) + Data Byte 1 (7 bits) + Parity bit (1 bit)):

- **OpCode** = The first transmitted bit (MSB) contains the operation code, which represents the command/ instruction that will be performed
- **Reserved** = Not used in the SDI frame (MSB-1)
- **Address** = The following 6 bits (MSB-2 to MSB-7) represent the register address on which the command/ operation will be performed
- **Data Bytes** = The subsequent 15 bits (MSB-8 to MSB-22) contain the payload to write
- **Parity bit** = Last bit (MSB-23) contains the parity bit for the integrity check

6.3.1.1 *OpCode*

The operating code is used to distinguish between different commands/operations on registers of the receiver device.

Table 33. OpCode

MSB	Description
0	Read command
1	Write command

A Write command (with no parity error, no wrong address and no CLK count error) will modify the content of the addressed control register with the payload at the next communication start. Besides this a shift out of the content (data present at communication start) of the addressed register is performed.

With the Read command two different events can be performed

- A Read event shifts out in the frame n+1 the data's addressed in the frame n. In this case all the bits of the payload data sent in the frame n is set to 0, and the data of the addressed register will not be modified.
- A Clear on Read event shifts out in the frame n+1 the data's addressed in the frame n, but with some bits that are cleared. In this case all the bits of the payload data sent that must be cleared will be set to 1, the bits that must not be cleared will be put to 0.

6.3.1.2 *Address*

The Address bits are used to indicate the register on which the command/operation will be performed:

- In case of read command (frame n) on the OpCode bit, the Address bits indicate the register you want to read. The contents of the register to be read will be put in the next frame (n+1) sent by the SDO pin.
- In case of write command on the OpCode bit, the Address bits indicate the register where the data bytes must be written.

6.3.1.3 *Data word*

The payload (Data Byte 2 to Data Byte 1) is the data transferred to the device with every SPI communication. The payload always follows the Address bits.

- For a Write access the payload represents the new data written to the addressed register.
- For a Read operation the payload is not used. The payload will be all set to '0'.
- For a Clear on Read operation the payload is used. All the bits that must be cleared will be set to '1', all the others will be set to '0'.

6.3.1.4 *Parity bit*

A parity bit is a bit added at the end of the 24 bits of each frame as an error detection code.

An odd parity bit for each communication must be calculated considering the entire 24-bit frame. The frame is considered valid only if the result of the Parity check is valid, which means an odd number of '1' is present in the SDI frame, if not the frame will be ignored and an SPI_ERROR event will be triggered.

6.3.2 SDO frame

The Data-Out frame consists of 24 bits (SPI ERROR (1 bit) + GSBN (1 bit) + Address (6 bits) + Data Byte 2 (8 bits) + Data Byte 1 (7 bits) + Parity bit (1 bit)).

- **SPI ERROR** = The first transmitted bit (MSB) contains the information about a SPI error or RESET
- **GSBN** = Global Status bit, used only in the SDO frame (MSB-1)
- **Address** = The following 6 bits (MSB-2 to MSB-7) represent the register address on which the command/operation will be performed
- **Data Bytes** = The subsequent 15 bits (MSB-8 to MSB-22) contain the payload
- **Parity bit** = Last bit (MSB-23) contains the parity bit for the integrity check

6.3.2.1 *SPI ERROR bit*

The SPI ERROR bit contains the information about a SPI error or a RESET event according to the Table 34:

Table 34. **SPI ERROR bit**

MSB	Description
0	No SPI error in previous access and no RESET event before this access
1	SPI error in previous access or RESET event before this access

6.3.2.2 *Global Status Bit (GSBN)*

The GSBN is a logically NOR combination of DSR1 and DSR2 registers + SPI error bit + RSTB bit + WDG error bit. GSBN bit is directly related to the DIAGN pin.

- GSBN = 1 (no error), DSR1 bits + DSR2 bits + SPI error bit + RSBT bit all set to 0
- GSBN = 0 (error), one or more bit/s of DSR1 or DSR2 or SPI error or RSBT is/are set to 1

6.3.2.3 *Address*

The Address bits are used to indicate the register on which the operation has been performed:

- In case of SPI error or reset or first access, address field contains the address of the DRS0 register
- In other cases, both for read and write, Address field contains the address selected in the previous frame

6.3.2.4 *Data word*

The payload (Data Byte 2 to Data Byte 1) is the data transferred to the device with every SPI communication, and always follows the Address bits indicating:

- In case of SPI error or reset or first access, data field contains the DRS0 register data saved at CS falling
- In other cases, both for read and write, data field contains the data value of the register at the address selected saved at CS falling

6.3.3 Protocol failure detection

To achieve a communication protocol that covers certain fail-safe requirements a basic set of SPI communication failure detection mechanisms are implemented.

6.3.3.1 *Clock count*

During communication (CSN low) a clock monitor counts the valid CLK clock edges. The number of rising edges of a valid communication command must be 24. If the number of rising edges is not 24 the SPI write command will be ignored and the SPI error bit will be set in the response of the next SPI command.

6.3.3.2 *CLK polarity (CPOL) check*

During the falling and rising edge of CS the level of SCLK must be low. If SCLK is not low during the falling or the rising edge of CS, the SPI write command will be ignored and the SPI error bit will be set in the response of the next SPI command.

6.3.3.3 *CSN timeout*

By pulling CSN low the SDO is set active and leaves its tristate condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck at low a CSN timeout is implemented. By pulling CSN low an internal timer is started. When the timer reaches its end, the ongoing command is rejected, the SPIE is set (and it will be visible at the next communication) and the SDO is set in tristate condition.

6.3.3.4 *SDI stuck at LOW*

As a communication with data all ‘0’ and OpCode ‘0’ on address b’000000’ cannot be distinguished between a valid command and a SDI stuck at LOW, this communication is not allowed. Nevertheless, in case a stuck at LOW is detected the command will be rejected and the SPIE will be set and it will be visible at the next communication.

6.3.3.5 *SDI stuck at HIGH*

As a communication with data all ‘1’ and OpCode ‘1’ on address b’111111’ cannot be distinguished between a valid command and a SDI stuck at HIGH, this communication is not allowed. In case a stuck at HIGH is detected the command will be rejected and the SPIE will be set and it will be visible at the next communication.

6.4 SPI communication scenarios

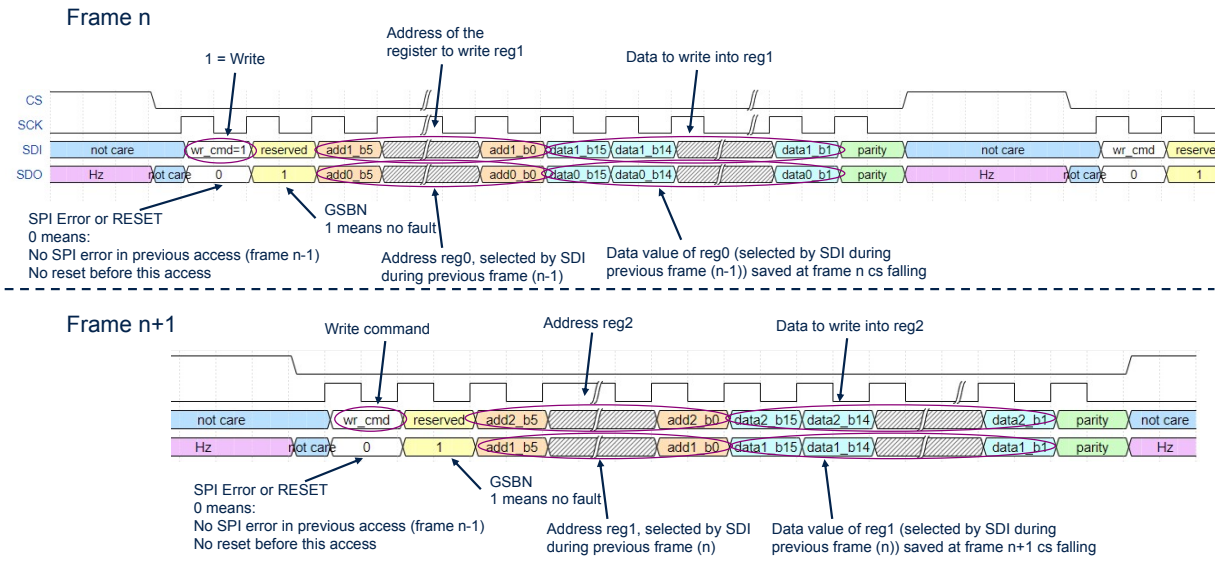
Some SPI communication scenarios are shown in the following sections.

6.4.1 Write access scenario

When a write communication must be performed the following steps must be considered:

- Frame n
  - SDI:
    - Bit 23 = 1 (write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n)
    - Bit 0 = Parity bit

Figure 36. Write access scenario

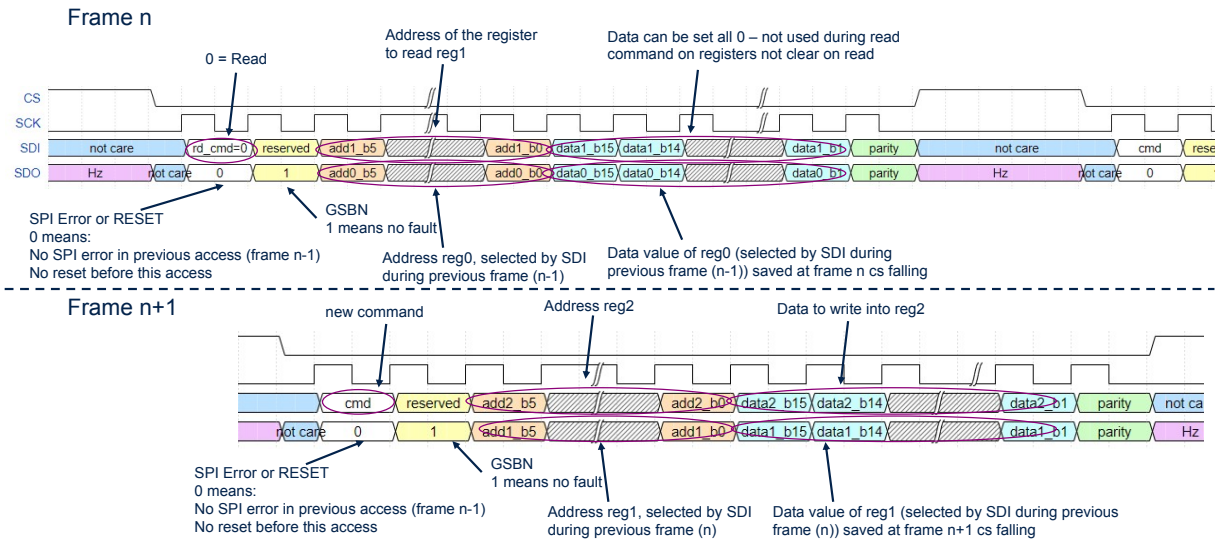


6.4.2 Read access scenario

When a read communication must be performed the following steps must be considered:

- Frame n
  - SDI:
    - Bit 23 = 0 (read command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read
    - Bits 15 to 1 = Data can be set to '0'
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n)
    - Bit 0 = Parity bit

Figure 37. Read access scenario

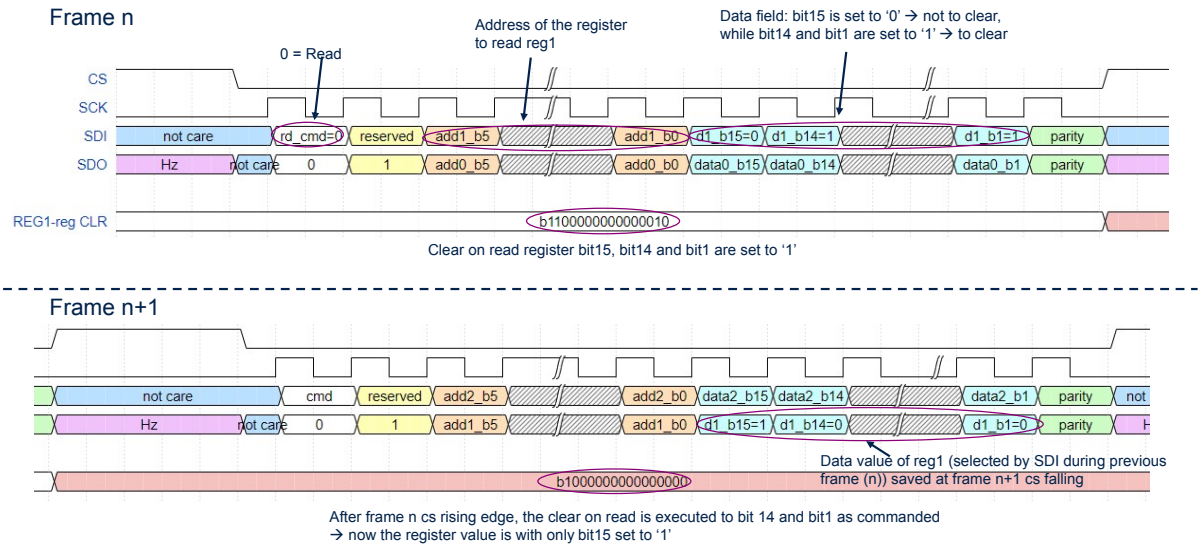


6.4.3 Clear on read scenario

When a clear on read communication must be performed the following steps must be considered:

- Frame n
  - SDI:
    - Bit 23 = 0 (read command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read
    - Bits 15 to 1 = Set to 0 the bits “not to clear”, set to 1 the bits “to clear”
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n) with the bits cleared
    - Bit 0 = Parity bit

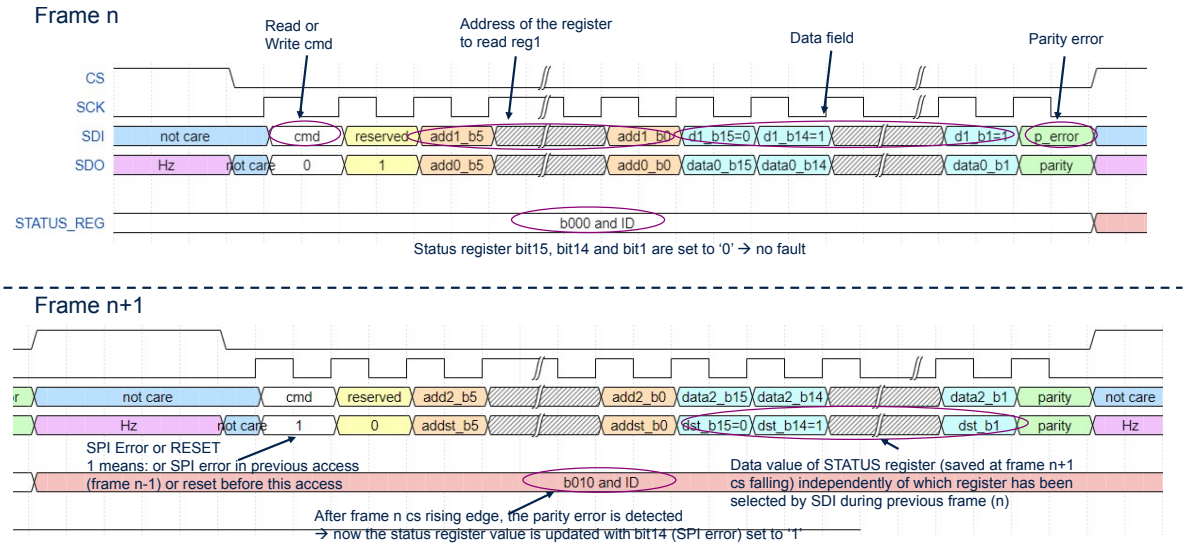
Figure 38. Clear on Read scenario



6.4.4 Write or read with SPI error scenario

- Frame n
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 1 (SPI error or RESET detected in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the STATUS register independently of which register has been selected by SDI during previous frame (n)
    - Bit 0 = Parity bit

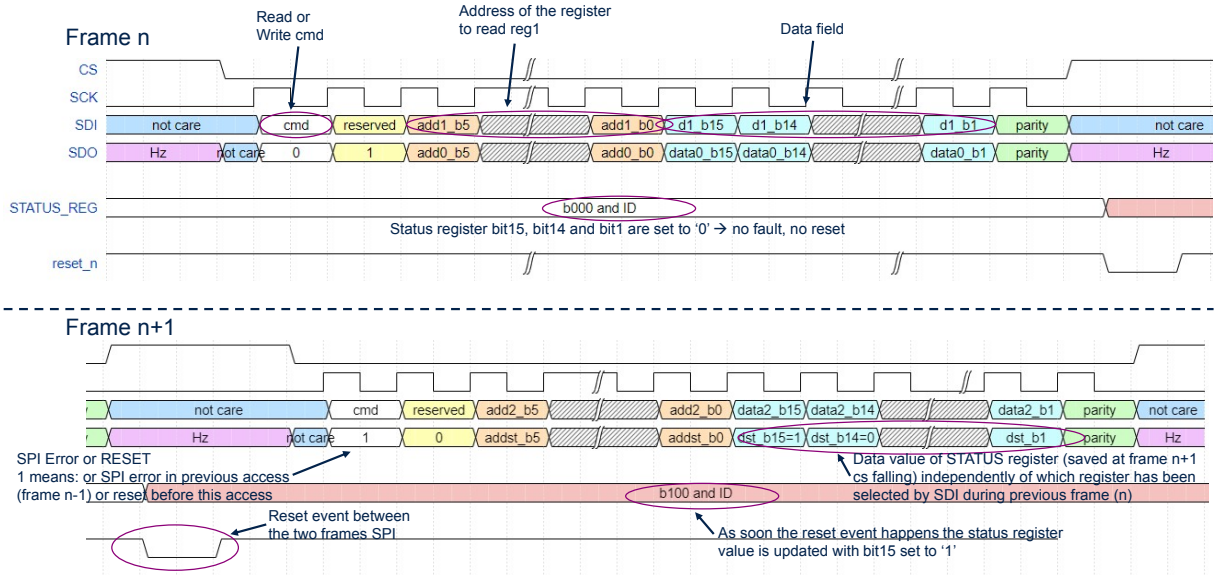
Figure 39. Write or read with SPI error scenario



6.4.5 Access after RESET scenario

- Frame n
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 1 (SPI error or RESET event in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the STATUS register
    - Bits 15 to 1 = Data value of the STATUS register
    - Bit 0 = Parity bit

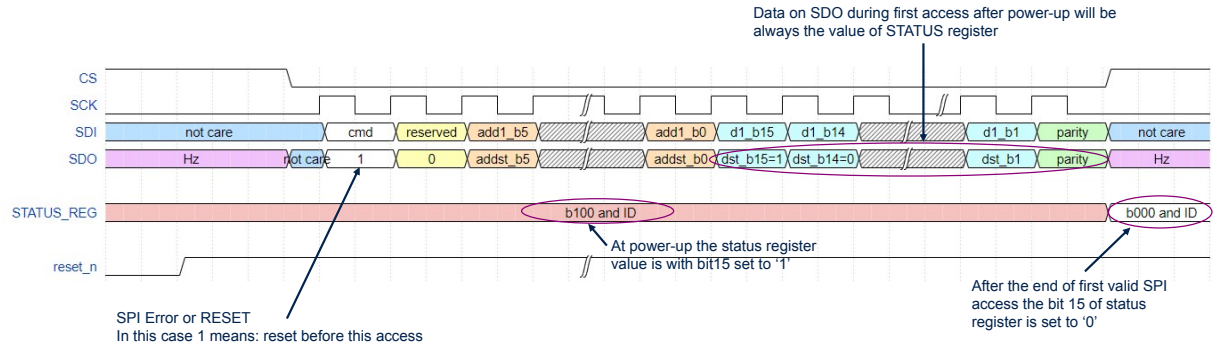
Figure 40. Access after RESET scenario



6.4.6 First SPI access at power-up scenario

- Frame 1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 1 (SPI error or RESET event in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the STATUS register
    - Bits 15 to 1 = Data value of the STATUS register
    - Bit 0 = Parity bit

Figure 41. First SPI access at power-up scenario

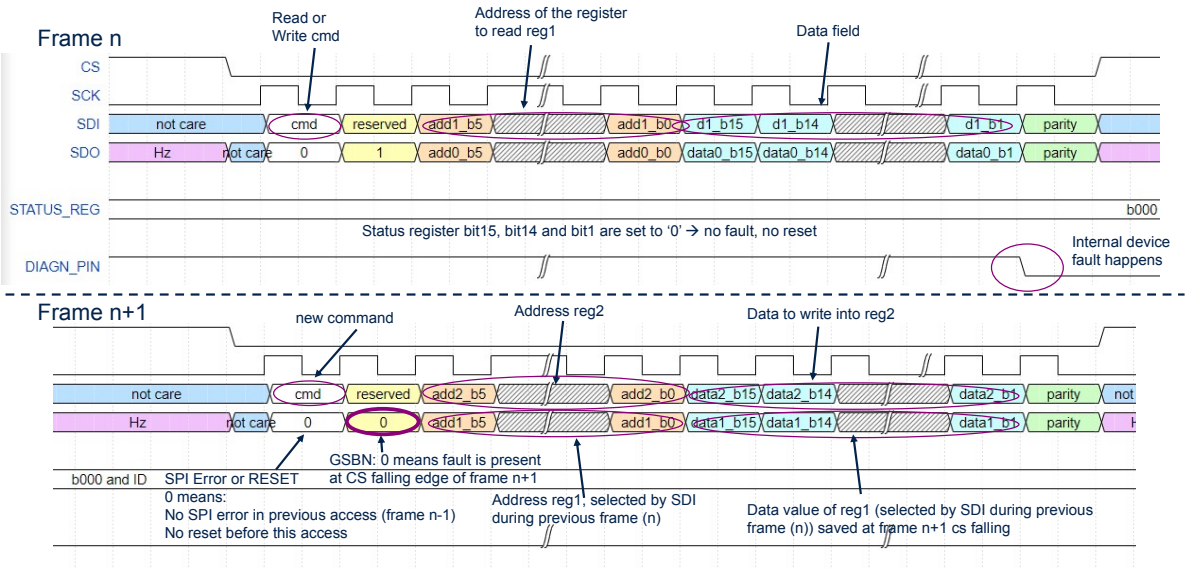


6.4.7 Access while an internal fault happens scenario

- Frame n
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit

- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (0 = Fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n)
    - Bit 0 = Parity bit

Figure 42. Access while an internal fault happens scenario



7 SPI Registers

7.1 Register map overview

Table 35. Register map overview

Addr.	Name	Bits	15	14	13	12	11	10	9	8	Mode
			7	6	5	4	3	2	1	0	
0x01	DSR0	MSB	-	RSTB	SPI_ERROR	WDG_ERROR	REVISION_ID[7]	REVISION_ID[6]	REVISION_ID[5]	REVISION_ID[4]	RO/CR
		LSB	REVISION_ID[3]	REVISION_ID[2]	REVISION_ID[1]	REVISION_ID[0]	DEVICE_ID[3]	DEVICE_ID[2]	DEVICE_ID[1]	DEVICE_ID[0]	
0x02	DSR1	MSB	-	RES	VDHOV	VDHUV	VDDOV	TW	TSD	DIAGCR	RO/CR
		LSB	RES	RES	RES	RES	VDSHS4	VDSHS3	VDSHS2	VDSHS1	
0X03	DSR2	MSB	-	RES	RES	RES	RES	RES	RES	RES	RO/CR
		LSB	RES	RES	RES	VDSLS4	VDSLS3	VDSLS2	VDSLS1	CPLOW	
0X04	GLOBAL_CFG	MSB	-	RES	RES	RES	OSC_SS_DIS	DIAGN_ ACTIVE_ LEVEL	DIAGOFF_ CURR_SEL	VDS_OFFSET_ ENABLE	RO/RW
		LSB	DTP_REF	OVTS	OUTE	CP_LOW_ CONFIG	CPFDD	EN_PWM1	EN_PWM2	RES	
0X05	CSO_CFG	MSB	-	SPARE0	RES	RES	RES	CSO_GAIN_SEL1	RES	CSOSIG1	RW
		LSB	RES	CSOEN1	RES	RES	RES	RES	CSOSH1[1]	CSOSH1[0]	
0X06	DIODE_CFG	MSB	-	RES	RES	RES	RES	RES	RES	RES	RW
		LSB	RES	RES	RES	RES	IDIODE_CONF2 [1]	IDIODE_CONF2 [0]	IDIODE_CONF1 [1]	IDIODE_CONF1 [0]	
0X07	DIODE1_READ	MSB	-	RES	RES	RES	RES	DIODE1_READ [10]	DIODE1_READ [9]	DIODE1_READ [8]	RO
		LSB	DIODE1_READ [7]	DIODE1_READ [6]	DIODE1_READ [5]	DIODE1_READ [4]	DIODE1_READ [3]	DIODE1_READ [2]	DIODE1_READ [1]	DIODE1_READ [0]	
0X08	DIODE2_READ	MSB	-	RES	RES	RES	RES	DIODE2_READ [10]	DIODE2_READ [9]	DIODE2_READ [8]	RO
		LSB	DIODE2_READ [7]	DIODE2_READ [6]	DIODE2_READ [5]	DIODE2_READ [4]	DIODE2_READ [3]	DIODE2_READ [2]	DIODE2_READ [1]	DIODE2_READ [0]	
0X09	DIODE3_READ (1)	RESERVED									RO
0X0A	DIODE4_READ (1)	RESERVED									RO
0X0B	DIAG_OFF_HS	MSB	-	RES	RES	RES	RES	RES	RES	RES	RO
		LSB	RES	RES	RES	RES	VDS_HS4_DIAG	VDS_HS3_DIAG	VDS_HS2_DIAG	VDS_HS1_DIAG	
0X0C	DIAG_OFF_LS	MSB	-	RES	RES	RES	RES	RES	RES	RES	RO
		LSB	RES	RES	RES	RES	VDS_LS4_DIAG	VDS_LS3_DIAG	VDS_LS2_DIAG	VDS_LS1_DIAG	
0X0D	DIAGCR1	MSB	-	DGWG	DGSPIERR	DGVDHOV	DGVDHUV	DGTW	DGTSD	DGCPLOW	RW
		LSB	RES	RES	RES	RES	DGVDSHS4	DGVDSHS3	DGVDSHS2	DGVDSHS1	
0X0E	DIAGCR2	MSB	-	RES	RES	RES	RES	DGVDSLS4	DGVDSLS3	DGVDSLS2	RW
		LSB	DGVDSLS1	RES	RES	RES	RES	RES	RES	RES	
0X0F	WDGTRDIS	MSB	-	WDGTRDIS [14]	WDGTRDIS [13]	WDGTRDIS [12]	WDGTRDIS [11]	WDGTRDIS [10]	WDGTRDIS [9]	WDGTRDIS [8]	WO
		LSB	WDGTRDIS [7]	WDGTRDIS [6]	WDGTRDIS [5]	WDGTRDIS [4]	WDGTRDIS [3]	WDGTRDIS [2]	WDGTRDIS [1]	WDGTRDIS [0]	
0X0F	WDGTRDIS	MSB	-	RES	RES	RES	RES	RES	RES	RES	RO
		LSB	RES	RES	RES	RES	WDGSTATUS	WDGINF [2]	WDGINF [1]	WDGINF [0]	
0X10	HB1_MODE_ CFG	MSB	-	RES	HB1_SPARE	DT1 [2]	DT1 [1]	DT1 [0]	STRONG_ON_ WHEEL1	HB_IDIAG1 [1]	RW
		LSB	HB_IDIAG1 [0]	HB_PWM1 [2]	HB_PWM1 [1]	HB_PWM1 [0]	HB_MODE1 [1]	HB_MODE1 [0]	HB_WHEEL1 [1]	HB_WHEEL1 [0]	
0X11	HB1_DRIVER_ CFG	MSB	-	RES	VSTEP2_CONF1 [1]	VSTEP2_CONF1 [0]	ISTEP3_CONF1 [3]	ISTEP3_CONF1 [2]	ISTEP3_CONF1 [1]	ISTEP3_CONF1 [0]	RW
		LSB	ISTEP2_CONF1 [3]	ISTEP2_CONF1 [2]	ISTEP2_CONF1 [1]	ISTEP2_CONF1 [0]	ISTEP1_CONF1 [3]	ISTEP1_CONF1 [2]	ISTEP1_CONF1 [1]	ISTEP1_CONF1 [0]	
0X12	HB1_DIAG_CFGLSB	MSB	-	RES	RES	RES	RES	VDS_CONF1 [3]	VDS_CONF1 [2]	VDS_CONF1 [1]	RW
		LSB	VDS_CONF1 [0]	VDS_BLANK1 [3]	VDS_BLANK1 [2]	VDS_BLANK1 [1]	VDS_BLANK1 [0]	VDS_FILT1 [2]	VDS_FILT1 [1]	VDS_FILT1 [0]	
0x13	HB1_TURN_OFF_CFG	MSB	-	RES	RES	RES	RES	RES	GENMODE1 [1]	GENMODE1 [0]	RW
		LSB	RES	RES	HB_FAULT1 [1]	HB_FAULT1 [0]	ISTEP2_OFF_ CONF1 [3]	ISTEP2_OFF_ CONF1 [2]	ISTEP2_OFF_ CONF1 [1]	ISTEP2_OFF_ CONF1 [0]	
0X14	HB2_MODE_ CFG	MSB	-	RES	HB2_SPARE	DT2 [2]	DT2 [1]	DT2 [0]	STRONG_ON_ WHEEL2	HB_IDIAG2 [1]	RW
		LSB	HB_IDIAG2 [0]	HB_PWM2 [2]	HB_PWM2 [1]	HB_PWM2 [0]	HB_MODE2 [1]	HB_MODE2 [0]	HB_WHEEL2 [1]	HB_WHEEL2 [0]	
0X15	HB2_DRIVER_ CFG	MSB	-	RES	VSTEP2_CONF2 [1]	VSTEP2_CONF2 [0]	ISTEP3_CONF2 [3]	ISTEP3_CONF2 [2]	ISTEP3_CONF2 [1]	ISTEP3_CONF2 [0]	RW

Addr.	Name	Bits	15	14	13	12	11	10	9	8	Mode
			7	6	5	4	3	2	1	0	
0X15	HB2_DRIVER_ CFG	LSB	ISTEP2_CONF2 [3]	ISTEP2_CONF2 [2]	ISTEP2_CONF2 [1]	ISTEP2_CONF2 [0]	ISTEP1_CONF2 [3]	ISTEP1_CONF2 [2]	ISTEP1_CONF2 [1]	ISTEP1_CONF2 [0]	RW
0X16	HB2_DIAG_CFG	MSB	-	RES	RES	RES	RES	VDS_CONF2 [3]	VDS_CONF2 [2]	VDS_CONF2 [1]	RW
		LSB	VDS_CONF2 [0]	VDS_BLANK2 [3]	VDS_BLANK2 [2]	VDS_BLANK2 [1]	VDS_BLANK2 [0]	VDS_FILT2 [2]	VDS_FILT2 [1]	VDS_FILT2 [0]	
0x17	HB2_TURN_OFF_CFG	MSB	-	RES	RES	RES	RES	RES	GENMODE2 [1]	GENMODE2 [0]	RW
		LSB	RES	RES	HB_FAULT2 [1]	HB_FAULT2 [0]	ISTEP2_OFF_ CONF2 [3]	ISTEP2_OFF_ CONF2 [2]	ISTEP2_OFF_ CONF2 [1]	ISTEP2_OFF_ CONF2 [0]	
0X18	HB3_MODE_ CFG	MSB	-	RES	HB3_SPARE	DT3 [2]	DT3 [1]	DT3 [0]	STRONG_ON_ WHEEL3	HB_IDIAG3 [1]	RW
		LSB	HB_IDIAG3 [0]	HB_PWM3 [2]	HB_PWM3 [1]	HB_PWM3 [0]	HB_MODE3 [1]	HB_MODE3 0]	HB_WHEEL3 [1]	HB_WHEEL3 [0]	
0X19	HB3_DRIVER_ CFG	MSB	-	RES	VSTEP2_CONF3 [1]	VSTEP2_CONF3 [0]	ISTEP3_CONF3 [3]	ISTEP3_CONF3 [2]	ISTEP3_CONF3 [1]	ISTEP3_CONF3 [0]	RW
		LSB	ISTEP2_CONF3 [3]	ISTEP2_CONF3 [2]	ISTEP2_CONF3 [1]	ISTEP2_CONF3 [0]	ISTEP1_CONF3 [3]	ISTEP1_CONF3 [2]	ISTEP1_CONF3 [1]	ISTEP1_CONF3 [0]	
0X1A	HB3_DIAG_CFG	MSB	-	RES	RES	RES	RES	VDS_CONF3 [3]	VDS_CONF3 [2]	VDS_CONF3 [1]	RW
		LSB	VDS_CONF3 [0]	VDS_BLANK3 [3]	VDS_BLANK3 [2]	VDS_BLANK3 [1]	VDS_BLANK3 [0]	VDS_FILT3 [2]	VDS_FILT3 [1]	VDS_FILT3 [0]	
0x1B	HB3_TURN_OFF_CFG	MSB	-	RES	RES	RES	RES	RES	GENMODE3 [1]	GENMODE3 [0]	RW
		LSB	RES	RES	HB_FAULT3 [1]	HB_FAULT3 [0]	ISTEP2_OFF_ CONF3 [3]	ISTEP2_OFF_ CONF3 [2]	ISTEP2_OFF_ CONF3 [1]	ISTEP2_OFF_ CONF3 [0]	
0X1C	HB4_MODE_ CFG	MSB	-	RES	HB4_SPARE	DT4 [2]	DT4 [1]	DT4 [0]	STRONG_ON_ WHEEL4	HB_IDIAG4 [1]	RW
		LSB	HB_IDIAG4 [0]	HB_PWM4 [2]	HB_PWM4 [1]	HB_PWM4 [0]	HB_MODE4 [1]	HB_MODE4 [0]	HB_WHEEL4 [1]	HB_WHEEL4 [0]	
0X1D	HB4_DRIVER_ CFG	MSB	-	RES	VSTEP2_CONF4 [1]	VSTEP2_CONF4 [0]	ISTEP3_CONF4 [3]	ISTEP3_CONF4 [2]	ISTEP3_CONF4 [1]	ISTEP3_CONF4 [0]	RW
		LSB	ISTEP2_CONF4 [3]	ISTEP2_CONF4 [2]	ISTEP2_CONF4 [1]	ISTEP2_CONF4 [0]	ISTEP1_CONF4 [3]	ISTEP1_CONF4 [2]	ISTEP1_CONF4 [1]	ISTEP1_CONF4 [0]	
0X1E	HB4_DIAG_CFG	MSB	-	RES	RES	RES	RES	VDS_CONF4 [3]	VDS_CONF4 [2]	VDS_CONF4 [1]	RW
		LSB	VDS_CONF4 [0]	VDS_BLANK4 [3]	VDS_BLANK4 [2]	VDS_BLANK4 [1]	VDS_BLANK4 [0]	VDS_FILT4 [2]	VDS_FILT4 [1]	VDS_FILT4 [0]	
0x1F	HB4_TURN_OFF_CFG	MSB	-	RES	RES	RES	RES	RES	GENMODE4 [1]	GENMODE4 [0]	RW
		LSB	RES	RES	HB_FAULT4 [1]	HB_FAULT4 [0]	ISTEP2_OFF_ CONF4 [3]	ISTEP2_OFF_ CONF4 [2]	ISTEP2_OFF_ CONF4 [1]	ISTEP2_OFF_ CONF4 [0]	
0X20	HB5_MODE_ CFG (1)	RESERVED									RW
0X21	HB5_DRIVER_ CFG (1)	RESERVED									RW
0X22	HB5_DIAG_CFG (1)	RESERVED									RW
0x23	HB5_TURN_OFF_CFG (1)	RESERVED									RW
0X24	HB6_MODE_ CFG (1)	RESERVED									RW
0X25	HB6_DRIVER_ CFG (1)	RESERVED									RW
0X26	HB6_DIAG_CFG (1)	RESERVED									RW
0x27	HB6_TURN_OFF_CFG (1)	RESERVED									RW
0X28	HB7_MODE_ CFG (1)	RESERVED									RW
0X29	HB7_DRIVER_ CFG (1)	RESERVED									RW
0X2A	HB7_DIAG_CFG (1)	RESERVED									RW
0x2B	HB7_TURN_OFF_CFG (1)	RESERVED									RW
0X2C	HB8_MODE_ CFG (1)	RESERVED									RW
0X2D	HB8_DRIVER_ CFG (1)	RESERVED									RW
0X2E	HB8_DIAG_CFG (1)	RESERVED									RW
0x2F	HB8_TURN_OFF_CFG (1)	RESERVED									RW
0x30	OUT_ENABLE	MSB	-	RES	RES	RES	RES	RES	RES	RES	RW
		LSB	RES	RES	RES	RES	OUT4	OUT3	OUT2	OUT1	

1. *"Address Error" when accessing this register, only for L99MH94Q7*

7.2 Status registers

Table 36. **DSR0 (0x01) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (CRF)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RSTB	SPI_ERROR	WDG_ERROR	REVISION_ID [7]	REVISION_ID [6]	REVISION_ID [5]	REVISION_ID [4]
Reset bit flag	SPI fault flag	Watchdog fault flag	Revision ID flag [7]	Revision ID flag [6]	Revision ID flag [5]	Revision ID flag [4]

Table 37. **DSR0 (0x01) MSB description**

Bit	Name	Description
14	RSTB	RESET bit flag 1: Device coming out from the POR. This indicates that all the device registers have been reset. 0: Device is not coming out from POR Automatically cleared at first valid SPI communication frame has been received after the reset
13	SPI_ERROR	SPI fault flag 0: No SPI failure detected 1: SPI failure detected Automatically cleared at first valid SPI communication frame
12	WDG_ERROR	Watchdog fault flag 0: No WDG failure detected 1: WDG failure detected
11	REVISION_ID [7]	Revision ID bit [7] Version ID to identify the silicon version
10	REVISION_ID [6]	Revision ID bit [6] Version ID to identify the silicon version
9	REVISION_ID [5]	Revision ID bit [5] Version ID to identify the silicon version
8	REVISION_ID [4]	Revision ID bit [4] Version ID to identify the silicon version

Table 38. **DSR0 (0x01) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
REVISION_ID [3]	REVISION_ID [2]	REVISION_ID [1]	REVISION_ID [0]	DEVICE_ID [3]	DEVICE_ID [2]	DEVICE_ID [1]	DEVICE_ID [0]
Revision ID flag [3]	Revision ID flag [2]	Revision ID flag [1]	Revision ID flag [0]	Device ID flag [3]	Device ID flag [2]	Device ID flag [1]	Device ID flag [0]

Table 39. **DSR0 (0x01) LSB description**

Bit	Name	Description
7	REVISION_ID [3]	Revision ID bit [3] Version ID to identify the silicon version
6	REVISION_ID [2]	Revision ID bit [2]

Bit	Name	Description
		Version ID to identify the silicon version
5	REVISION_ID [1]	Revision ID bit [1] Version ID to identify the silicon version
4	REVISION_ID [0]	Revision ID bit [0] Version ID to identify the silicon version
3	DEVICE_ID [3]	Device ID bit [3] Device ID to identify the L99MH94 / L99MH92 device
2	DEVICE_ID [2]	Device ID bit [2] Device ID to identify the L99MH94 / L99MH92 device
1	DEVICE_ID [1]	Device ID bit [1] Device ID to identify the L99MH94 / L99MH92 device
0	DEVICE_ID [0]	Device ID bit [0] Device ID to identify the L99MH94 / L99MH92 device

Table 40. DSR1 (0x02) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (CRF)	0 (CRF)	0 (CRF)	0 (CRF)	0 (CRF)	0 (RO)
RES	VDHOV	VDHUV	VDDOV	TW	TSD	DIAGCR
Reserved	VDH overvoltage flag	VUH overvoltage flag	VDD overvoltage flag	Thermal warning flag	Thermal shutdown flag	DIAGN flag

Table 41. DSR1 (0x02) MSB description

Bit	Name	Description
14	RES	Reserved
13	VDHOV	VDH overvoltage flag This flag is set and latched as soon as an overvoltage is detected on VDH supply. It can be cleared by SPI only if the source of the fault is no longer present. Automatically cleared at first valid SPI communication frame
12	VDHUV	VDH undervoltage flag This flag is set and latched as soon as an undervoltage is detected on VDH supply. It can be cleared by SPI only if the source of the fault is no longer present. Automatically cleared at first valid SPI communication frame
11	VDDOV	VDD overvoltage fault flag This flag is set and latched as soon as an overvoltage is detected on VDD supply. It can be cleared by SPI only if the source of the fault is no longer present. Automatically cleared at first valid SPI communication frame
10	TW	Thermal warning flag This flag is set and latched as soon as device junction temperature exceeds TW threshold for a time longer than the corresponding filter time. It can be cleared by SPI only if the source of the fault is no longer present. Automatically cleared at first valid SPI communication frame
9	TSD	Thermal shutdown flag This flag is set and latched as soon as device junction temperature exceeds TSD threshold for a time longer than the corresponding filter time. It can be cleared by SPI only if the source of the fault is no longer present. Automatically cleared at first valid SPI communication frame
8	DIAGCR	DIAGN flag This flag is set as soon as the DIAGN pin is activated. It is automatically cleared as soon as the DIAGN is de-activated

Table 42. **DSR1 (0x02) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (CR)	0 (CR)	0 (CR)	0 (CR)	0 (CRF)	0 (CRF)	0 (CRF)	0 (CRF)
RES	RES	RES	RES	VDSHS4	VDSHS3	VDSHS2	VDSHS1
Reserved	Reserved	Reserved	Reserved	VDS monitoring HS4	VDS monitoring HS3	VDS monitoring HS2	VDS monitoring HS1

Table 43. **DSR1 (0x02) LSB description**

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	RES	
4	RES	
3	VDSHS4	VDS monitoring flags, only for L99MH94.
2	VDSHS3	Flag VDSHSx (x = 1...4) is set and latched as soon as the VDS of the corresponding HS MOSFET exceeds the relative threshold (set by VDS_CONFx, x = 1...4) for a time longer than the corresponding filtering time or blanking filtering time, where the blanking time is applicable. It can be cleared by SPI only if the source of the fault is no longer present.
1	VDSHS2	VDS monitoring flags
0	VDSHS1	Flag VDSHSx (x = 1...4 for L99MH94, x = 1, 2 for L99MH92) is set and latched as soon as the VDS of the corresponding HS MOSFET exceeds the relative threshold (set by VDS_CONFx, x = 1...4 for L99MH94, x = 1, 2 for L99MH92) for a time longer than the corresponding filtering time or blanking filtering time, where the blanking time is applicable. It can be cleared by SPI only if the source of the fault is no longer present.

Table 44. **DSR2 (0x03) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (CR)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 45. **DSR2 (0x03) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (CR)	0 (CR)	0 (CR)	0 (CR)	0 (CR)	0 (CR)	0 (CR)	0 (CR)
RES	RES	RES	VDSLS4	VDSLS3	VDSLS2	VDSLS1	CPLOW
Reserved	Reserved	Reserved	Reserved	VDS monitoring HS4	VDS monitoring HS3	VDS monitoring HS2	CP LOW flag

Table 46. **DSR2 (0x03) LSB description**

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	RES	
4	VDSLS4	VDS monitoring flags, only for L99MH94.
3	VDSLS3	

Bit	Name	Description
		Flag VDSLSx (x = 1...4) is set and latched as soon as the VDS of the corresponding LS MOSFET exceeds the relative threshold (set by VDS_CONFx, x = 1...4) for a time longer than the corresponding filtering time or blanking filtering time, where the blanking time is applicable. It can be cleared by SPI only if the source of the fault is no longer present.
2	VDSLS2	VDS monitoring flags. Flag VDSLSx (x = 1...4 for L99MH94, x = 1, 2 for L99MH92) is set and latched as soon as the VDS of the corresponding LS MOSFET exceeds the relative threshold (set by VDS_CONFx, x = 1...4 for L99MH94, x = 1, 2 for L99MH92) for a time longer than the corresponding filtering time or blanking filtering time, where the blanking time is applicable. It can be cleared by SPI only if the source of the fault is no longer present.
1	VDSLS1	
0	CPLOW	CP low flag If the CP_LOW_CONFIG control bit is set to one, the CPLOW status flag becomes a status bit (set and reset automatically) and the gate drivers come out of forced disabled mode automatically upon recovery from the charge pump low voltage condition. In this case the status bit will be automatically cleared as soon as the charge pump output voltage is no longer below the low voltage threshold for a time longer than t_{CP} If the CP_LOW_CONFIG control bit is set to zero, the gate drivers come out of forced disabled mode only once the charge pump low-voltage flag CPLOW is cleared via SPI. The charge pump low voltage flag CPLOW can be cleared by a SPI “read and clear” command only if the charge pump low-voltage condition is no longer present, namely if $V_{CP} > V_{CP\_LOW}$ for a time longer than t_{CP}.

7.3 Control Registers

Table 47. GLOBAL_CFG (0x04) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	OSC_SS_DIS	DIAGN_ACTIVE_ LEVEL	DIAGOFF_CURR_ SEL	VDS_OFFSET_ ENABLE
Reserved	Reserved	Reserved	Spread spectrum enable	DIAGN pin active level	DIAGOFF current selection	VDS offset enable

Table 48. GLOBAL_CFG (0x04) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	OSC_SS_DIS	Spread spectrum enable 0: Spread spectrum enabled 1 : Spread spectrum disabled
10	DIAGN_ACTIVE_ LEVEL	DIAGN pin active level 0: DIAGN pin active low 1: DIAGN pin active high
9	DIAGOFF_CURR_ SEL	DIAGOFF current selection 0 ⇒ 1 mA 1 ⇒ 2 mA
8	VDS_OFFSET_ ENABLE	Offset of 6 mV on the V_{ds} measurements. To be inserted in case of short circuit to be measured 0: No offset inserted 1: Offset inserted

Table 49. **GLOBAL_CFG (0x04) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	1 (RW)	0 (RW)	0 (RW)	0 (RW)
DTP_REF	OVTS	OUTE	CP_LOW_CONFIG	CPFDD	EN_PWM1	EN_PWM2	RES
Cross current protection time reference	V_{DH} over voltage protection threshold	Outputs enable	CP low configuration	CP frequency enable dithering	PWM1 enable	PWM2 enable	Reserved

Table 50. **GLOBAL_CFG (0x04) LSB description**

Bit	Name	Description
7	DTP_REF	Cross current protection time reference 0: the cross current protection time is calculated starting from the command to switch off a MOSFET and switch on the complementary 1: the cross current protection time is calculated starting from the instant in which the V_{gs} of the MOSFET being switched off has reached the value set in the VSTEP1x
6	OVTS	VDH over voltage protection threshold 0: V_{DH} over-voltage threshold 1 (V_{DHOVT1}) selected 1: V_{DH} over-voltage threshold 2 (V_{DHOVT2}) selected
5	OUTE	Outputs enable 0: all the gate drivers are OFF independently from OUTEx bits setting 1: the gate drivers can be put OFF or ON according to the OUTEx bits setting
4	CP_LOW_CONFIG	CP low configuration 0: the gate drivers come out of forced disabled mode only once the charge pump low voltage flag CPLOW is cleared via SPI 1: CPLOW status flag becomes a status bit (set and reset automatically) and the gate drivers come out of forced disabled mode automatically upon recovery from the charge pump low voltage condition
3	CPFDD	Charge pump frequency dithering 0: charge pump dithering doesn't enable 1: charge pump dithering enabled
2	EN_PWM1	PWM1 enable 0: PWM1 disabled 1: PWM1 enabled
1	EN_PWM2	PWM2 enable 0: PWM2 disabled 1: PWM2 enabled
0	RES	Reserved bit

Table 51. **CSO_CFG (0x05) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	CSO_GAIN_SEL1	RES	CSOSIG1
Reserved	Reserved	Reserved	Reserved	CSO1 gain selection	Reserved	CSO1 Vds mapping

Table 52. **CSO_CFG (0x05) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	CSO_GAIN_SEL1	CSO1 gain selection 0: gain sets to 1.5 1: gain sets to 3
9	RES	Reserved
8	CSOSIG1	CSO1 V_{ds} mapping 0: V_{ds} of the HSx mapped on CSO1 (to use in combination with CSOSHx) 1: V_{ds} of the LSx mapped on CSO1 (to use in combination with CSOSHx)

Table 53. **CSO_CFG (0x05) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RO)	0 (RW)	0 (RW)
RES	CSOEN1	RES	RES	RES	RES	CSOSH1 [1]	CSOSH1 [0]
Reserved	CSO1 enable	Reserved	Reserved	Reserved	Reserved	HSx mapping on CSO1 [1]	HSx mapping on CSO1 [0]

Table 54. **CSO_CFG (0x05) LSB description**

Bit	Name	Description
7	RES	Reserved bit
6	CSOEN1	CSO1 enable 0: CSO1 output disabled 1: CSO1 output enabled
5	RES	Reserved bits
4	RES	
3	RES	
2	RES	
1	CSOSH1 [1]	V_{ds} of HSx mapping on CSO1, CSOSH1 [1] not writable for L99MH92.
0	CSOSH1 [0]	00: V_{ds} of HS1 mapped on CSO1 01: V_{ds} of HS2 mapped on CSO1 10: V_{ds} of HS3 mapped on CSO1 (only for L99MH94) 11: V_{ds} of HS4 mapped on CSO1 (only for L99MH94)

Table 55. **DIODE_CFG (0x06) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 56. **DIODE_CFG (0x06) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	1 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	IDIODE_ CONF2 [1]	IDIODE_ CONF2 [0]	IDIODE_ CONF1 [1]	IDIODE_ CONF1 [0]
Reserved	Reserved	Reserved	Reserved	Idiode2 configuration [1]	Idiode2 configuration [0]	Idiode1 configuration [1]	Idiode1 configuration [0]

Table 57. **DIODE_CFG (0x06) LSB description**

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	RES	
4	RES	
3	IDIODE_CONF2 [1]	Configuration of the current of the diode 2
2	IDIODE_CONF2 [0]	00 ⇒ 250 µA 01 ⇒ 500 µA 10 ⇒ 750 µA 11 ⇒ 1000 µA
1	IDIODE_CONF1 [1]	Configuration of the current of the diode 1
0	IDIODE_CONF1 [0]	00 ⇒ 250 µA 01 ⇒ 500 µA 10 ⇒ 750 µA 11 ⇒ 1000 µA

Table 58. **DIODE1_READ (0x07) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	DIODE1_READ [10]	DIODE1_READ [9]	DIODE1_READ [8]
Reserved	Reserved	Reserved	Reserved	Diode1 read bit [10]	Diode1 read bit [9]	Diode1 read bit [8]

Table 59. **DIODE1_READ (0x07) MSB description**

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	DIODE1_READ [10]	ADC output bits for the diode 1
9	DIODE1_READ [9]	
8	DIODE1_READ [8]	

Table 60. **DIODE1_READ (0x07) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
DIODE1_ READ [7]	DIODE1_ READ [6]	DIODE1_ READ [5]	DIODE1_ READ [4]	DIODE1_ READ [3]	DIODE1_ READ [2]	DIODE1_ READ [1]	DIODE1_ READ [0]
Diode1 read bit [7]	Diode1 read bit [6]	Diode1 read bit [5]	Diode1 read bit [4]	Diode1 read bit [3]	Diode1 read bit [2]	Diode1 read bit [1]	Diode1 read bit [0]

Table 61. **DIODE1_READ (0x07) LSB description**

Bit	Name	Description
7	DIODE1_READ [7]	ADC output bits for the diode 1
6	DIODE1_READ [6]	
5	DIODE1_READ [5]	
4	DIODE1_READ [4]	
3	DIODE1_READ [3]	
2	DIODE1_READ [2]	
1	DIODE1_READ [1]	
0	DIODE1_READ [0]	

Table 62. **DIODE2_READ (0x08) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	DIODE2_READ [10]	DIODE2_READ [9]	DIODE2_READ [8]
Reserved	Reserved	Reserved	Reserved	Diode2 read bit [10]	Diode2 read bit [9]	Diode2 read bit [8]

Table 63. **DIODE2_READ (0x08) MSB description**

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	DIODE2_READ [10]	ADC output bits for the diode 2
9	DIODE2_READ [9]	
8	DIODE2_READ [8]	

Table 64. **DIODE2_READ (0x08) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
DIODE2_ READ [7]	DIODE2_ READ [6]	DIODE2_ READ [5]	DIODE2_ READ [4]	DIODE2_ READ [3]	DIODE2_ READ [2]	DIODE2_ READ [1]	DIODE2_ READ [0]
Diode2 read bit [7]	Diode2 read bit [6]	Diode2 read bit [5]	Diode2 read bit [4]	Diode2 read bit [3]	Diode2 read bit [2]	Diode2 read bit [1]	Diode2 read bit [0]

Table 65. DIODE2_READ (0x08) LSB description

Bit	Name	Description
7	DIODE2_READ [7]	ADC output bits for the diode 2
6	DIODE2_READ [6]	
5	DIODE2_READ [5]	
4	DIODE2_READ [4]	
3	DIODE2_READ [3]	
2	DIODE2_READ [2]	
1	DIODE2_READ [1]	
0	DIODE2_READ [0]	

Table 66. DIODE3_READ (0x09) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 67. DIODE3_READ (0x09) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 68. DIODE4_READ (0x0A) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 69. DIODE4_READ (0x0A) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 70. DIAG_OFF_HS (0x0B) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 71. DIAG_OFF_HS (0x0B) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	VDS_HS4_DIAG	VDS_HS3_DIAG	VDS_HS2_DIAG	VDS_HS1_DIAG
Reserved	Reserved	Reserved	Reserved	VDS HS4 bit	VDS HS3 bit	VDS HS2 bit	VDS HS1 bit

Table 72. DIAG_OFF_HS (0x0B) LSB description

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	RES	
4	RES	
3	VDS_HS4_DIAG	Only for L99MH94.
2	VDS_HS3_DIAG	Status of the HSx comparator during diag off, with a symmetric filter of 200 µs 0: LOW 1: HIGH
1	VDS_HS2_DIAG	Status of the HSx comparator (x = 1...4 for L99MH94, x = 1, 2 for L99MH92) during diag off, with a symmetric filter of 200 µs 0: LOW 1: HIGH
0	VDS_HS1_DIAG	

Table 73. DIAG_OFF_LS (0x0C) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 74. DIAG_OFF_LS (0x0C) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)
RES	RES	RES	RES	VDS_LS4_DIAG	VDS_LS3_DIAG	VDS_LS2_DIAG	VDS_LS1_DIAG
Reserved	Reserved	Reserved	Reserved	VDS LS4 bit	VDS LS3 bit	VDS LS2 bit	VDS LS1 bit

Table 75. DIAG_OFF_LS (0x0C) LSB description

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	RES	
4	RES	

Bit	Name	Description
3	VDS_LS4_DIAG	Only for L99MH94.
2	VDS_LS3_DIAG	Status of the LSx comparator during diag off, with a symmetric filter of 200 µs 0: LOW 1: HIGH
1	VDS_LS2_DIAG	Status of the LSx comparator (x = 1...4 for L99MH94, x = 1, 2 for L99MH92) during diag off, with a symmetric filter of 200 µs 0: LOW 1: HIGH
0	VDS_LS1_DIAG	

Table 76. DIAGCR1 (0x0D) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)
DGWDG	DGSPIERR	DGVDHOV	DGVDHUV	DGTW	DGTSD	DGCPLOW
Diagnostic WDG_ERR enable bit	Diagnostic SPI_ERR enable bit	Diagnostic VDHOV enable bit	Diagnostic VDHUV enable bit	Diagnostic TW enable bit	Diagnostic TSD enable bit	Diagnostic CPLOW enable bit

Table 77. DIAGCR1 (0x0D) MSB description

Bit	Name	Description
14	DGWDG	Diagnostic WDG ERROR enable control bit Setting this bit enables WDG_ERR status flag to be mapped on diagnostic output pin (DIAGN) 0: WDG_ERR no mapped on DIAGN pin 1: WDG_ERR mapped on DIAGN pin
13	DGSPIERR	Diagnostic SPI ERROR enable control bit Setting this bit enables SPI_ERR status flag to be mapped on diagnostic output pin (DIAGN) 0: SPI_ERR no mapped on DIAGN pin 1: SPI_ERR mapped on DIAGN pin
12	DGVDHOV	Diagnostic VDHOV enable control bit Setting this bit enables VDHOV status flag to be mapped on diagnostic output pin (DIAGN) 0: VDHOV no mapped on DIAGN pin 1: VDHOV mapped on DIAGN pin
11	DGVDHUV	Diagnostic VDHUV enable control bit Setting this bit enables VDHUV status flag to be mapped on diagnostic output pin (DIAGN) 0: VDHUV no mapped on DIAGN pin 1: VDHUV mapped on DIAGN pin
10	DGTW	Diagnostic TW enable control bit Setting this bit enables TW status flag to be mapped on diagnostic output pin (DIAGN) 0: TW no mapped on DIAGN pin 1: TW mapped on DIAGN pin
9	DGTSD	Diagnostic TSD enable control bit Setting this bit enables TSD status flag to be mapped on diagnostic output pin (DIAGN) 0: TSD no mapped on DIAGN pin 1: TSD mapped on DIAGN pin
8	DGCPLOW	Diagnostic CPLOW enable control bit

Bit	Name	Description
		Setting this bit enables CPLOW status flag to be mapped on diagnostic output pin (DIAGN) 0: CPLOW no mapped on DIAGN pin 1: CPLOW mapped on DIAGN pin

Table 78. DIAGCR1 (0x0D) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)
RES	RES	RES	RES	DGVDSHS4	DGVDSHS3	DGVDSHS2	DGVDSHS1
Reserved	Reserved	Reserved	Reserved	Diagnostic enable VDS_HS4 bit	Diagnostic enable VDS_HS3 bit	Diagnostic enable VDS_HS2 bit	Diagnostic enable VDS_HS1 bit

Table 79. DIAGCR1 (0x0D) LSB description

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	RES	
4	RES	
3	DGVDSHS4	Diagnostic VDS_HS4 enable control bit, only for L99MH94. Setting this bit enables VDS_HS4 status flag to be mapped on diagnostic output pin (DIAGN) 0: VDS_HS4 no mapped on DIAGN pin 1: VDS_HS4 mapped on DIAGN pin
2	DGVDSHS3	Diagnostic VDS_HS3 enable control bit, only for L99MH94. Setting this bit enables VDS_HS3 status flag to be mapped on diagnostic output pin (DIAGN) 0: VDS_HS3 no mapped on DIAGN pin 1: VDS_HS3 mapped on DIAGN pin
1	DGVDSHS2	Diagnostic VDS_HS2 enable control bit Setting this bit enables VDS_HS2 status flag to be mapped on diagnostic output pin (DIAGN) 0: VDS_HS2 no mapped on DIAGN pin 1: VDS_HS2 mapped on DIAGN pin
0	DGVDSHS1	Diagnostic VDS_HS1 enable control bit Setting this bit enables VDS_HS1 status flag to be mapped on diagnostic output pin (DIAGN) 0: VDS_HS1 no mapped on DIAGN pin 1: VDS_HS1 mapped on DIAGN pin

Table 80. DIAGCR2 (0x0E) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)
RES	RES	RES	RES	DGVDSLS4	DGVDSLS3	DGVDSLS2
Reserved	Reserved	Reserved	Reserved	Diagnostic enable VDS_LS4 bit	Diagnostic enable VDS_LS3 bit	Diagnostic enable VDS_LS2 bit

Table 81. **DIAGCR2 (0x0E) MSB description**

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	DGVDSLS4	Diagnostic VDS_LS4 enable control bit, only for L99MH94. Setting this bit enables VDS_LS4 status flag to be mapped on diagnostic output pin (DIAGN) 0: VDS_LS4 no mapped on DIAGN pin 1: VDS_LS4 mapped on DIAGN pin
9	DGVDSLS3	Diagnostic VDS_LS3 enable control bit, only for L99MH94. Setting this bit enables VDS_LS3 status flag to be mapped on diagnostic output pin (DIAGN) 0: VDS_LS3 no mapped on DIAGN pin 1: VDS_LS3 mapped on DIAGN pin
8	DGVDSLS2	Diagnostic VDS_LS2 enable control bit Setting this bit enables VDS_LS2 status flag to be mapped on diagnostic output pin (DIAGN) 0: VDS_LS2 no mapped on DIAGN pin 1: VDS_LS2 mapped on DIAGN pin

Table 82. **DIAGCR2 (0x0E) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
DGVDSLS1	RES	RES	RES	RES	RES	RES	RES
Diagnostic enable VDS_LS1 bit	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 83. **DIAGCR2 (0x0E) LSB description**

Bit	Name	Description
7	DGVDSLS1	Diagnostic VDS_LS1 enable control bit Setting this bit enables VDS_LS1 status flag to be mapped on diagnostic output pin (DIAGN) 0: VDS_LS1 no mapped on DIAGN pin 1: VDS_LS1 mapped on DIAGN pin
6	RES	Reserved bits
5	RES	
4	RES	
3	RES	
2	RES	
1	RES	
0	RES	

Table 84. **WDGTRDIS (0x0F) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
WDGTRDIS [14]	WDGTRDIS [13]	WDGTRDIS [12]	WDGTRDIS [11]	WDGTRDIS [10]	WDGTRDIS [9]	WDGTRDIS [8]
Watchdog trigger [14]	Watchdog trigger [13]	Watchdog trigger [12]	Watchdog trigger [11]	Watchdog trigger [10]	Watchdog trigger [9]	Watchdog trigger [8]

Table 85. WDGTRDIS (0x0F) MSB description

Bit	Name	Description
14	WDGTRDIS [14]	Watchdog trigger ⇒ the device must receive alternatively 5555h and 2AAAh. The first word must be 5555h Watchdog disable ⇒ the device must receive in the right order 2F6Bh (first key word) and 1097h (second key word) Watchdog enable ⇒ the device must receive in the right order 5C99h (first key word) and 4360h (second key word)
13	WDGTRDIS [13]	
12	WDGTRDIS [12]	
11	WDGTRDIS [11]	
10	WDGTRDIS [10]	
9	WDGTRDIS [9]	
8	WDGTRDIS [8]	

Table 86. WDGTRDIS (0x0F) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
WDGTRDIS [7]	WDGTRDIS [6]	WDGTRDIS [5]	WDGTRDIS [4]	WDGTRDIS [3]	WDGTRDIS [2]	WDGTRDIS [1]	WDGTRDIS [0]
Watchdog trigger [7]	Watchdog trigger [6]	Watchdog trigger [5]	Watchdog trigger [4]	Watchdog trigger [3]	Watchdog trigger [2]	Watchdog trigger [1]	Watchdog trigger [0]

Table 87. WDGTRDIS (0x0F) LSB description

Bit	Name	Description
7	WDGTRDIS [7]	Watchdog trigger ⇒ the device must receive alternatively 5555h and 2AAAh. The first word must be 5555h Watchdog disable ⇒ the device must receive in the right order 2F6Bh (first key word) and 1097h (second key word) Watchdog enable ⇒ the device must receive in the right order 5C99h (first key word) and 4360h (second key word)
6	WDGTRDIS [6]	
5	WDGTRDIS [5]	
4	WDGTRDIS [4]	
3	WDGTRDIS [3]	
2	WDGTRDIS [2]	
1	WDGTRDIS [1]	
0	WDGTRDIS [0]	

Table 88. WDGTRDIS (0x0F) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 89. **WDGTRDIS (0x0F) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	WDGSTATUS	WDGINF [2]	WDGINF [1]	WDGINF [0]
Reserved	Reserved	Reserved	Reserved	Watchdog status	Watchdog inf [2]	Watchdog inf [1]	Watchdog inf [0]

Table 90. **WDGTRDIS (0x0F) LSB description**

Bit	Name	Description
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	WDGSTATUS	Watchdog status This bit is enabled if the watchdog has been successfully disabled
2	WDGINF [2]	Watchdog info These bits represent the three least significant bits of the latest write command performed on the same register
1	WDGINF [1]	
0	WDGINF [0]	

Table 91. **HB1_MODE_CFG (0x10) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	DT1 [2]	DT1 [1]	DT1 [0]	STRONG_ON _WHEEL1	HB_IDIAG1 [1]
Reserved	Reserved	Dead Time 1 [2]	Dead Time 1 [1]	Dead Time 1 [0]	Free-wheeling strong on HB1	HB1 diagnostic current

Table 92. **HB1_MODE_CFG (0x10) MSB description**

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	DT1 [2]	Dead time of the HB1 000 ⇒ 0.5 µs 001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 16 µs
11	DT1 [1]	
10	DT1 [0]	
9	STRONG_ON_ WHEEL1	Free-wheeling strong ON of the HB1 0: Strong on disabled, free-wheeling gate current set to 4 mA 1: Strong on enabled, free-wheeling gate current set to 30 mA
8	HB_IDIAG1 [1]	Half bridge 1 diagnostic currents setting 00: pull-up and pull-down currents off

Bit	Name	Description
		01: pull-up current off and pull-down current on 10: pull-up current on and pull-down current off 11: pull-up and pull-down currents off

Table 93. HB1_MODE_CFG (0x10) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
HB_IDIAG1 [1]	HB_PWM1 [2]	HB_PWM1 [1]	HB_PWM1 [0]	HB_MODE1 [1]	HB_MODE1 [0]	HB_WHEEL1 [1]	HB_WHEEL1 [0]
HB1 diagnostic current	HB1 PWM mapping [2]	HB1 PWM mapping [1]	HB1 PWM mapping [0]	HB1 mode [1]	HB1 mode [0]	HB1 free-wheeling [1]	HB1 free-wheeling [0]

Table 94. HB1_MODE_CFG (0x10) LSB description

Bit	Name	Description
7	HB_IDIAG1 [0]	Half bridge 1 diagnostic currents setting 00: pull-up and pull-down currents off 01: pull-up current off and pull-down current on 10: pull-up current on and pull-down current off 11: pull-up and pull-down currents off
6	HB_PWM1 [2]	PWM mapping on HB1 This 3 bits register is used to indicate which PWM signal is applied to the HS or LS of the half-bridge 1 000 ⇒ LS of HB mapped on PWM1 001 ⇒ LS of HB mapped on PWM2 011 ⇒ HS of HB mapped on PWM1 100 ⇒ HS of HB mapped on PWM2 010 = 101 = 110 = 111 ⇒ No Mapped
5	HB_PWM1 [1]	
4	HB_PWM1 [0]	
3	HB_MODE1 [1]	HB1 functionality mode 00 ⇒ LS and HS of the HB1 are kept off 01 ⇒ LS of the HB1 is ON (static, no PWM), HS of the HB1 is OFF 10 ⇒ HS of the half bridge 1 is ON (static, no PWM), LS of the half bridge is OFF 11 ⇒ LS or HS of the half-bridge is ON according to the HB_PWM1 register
2	HB_MODE1 [0]	
1	HB_WHEEL1 [1]	HB1 free-wheeling mode 00 = 11 ⇒ No mapping 01 ⇒ Active free-wheeling on HS of the HB 10 ⇒ Active free-wheeling on LS of the HB
0	HB_WHEEL1 [0]	

Table 95. HB1_DRIVER_CFG (0x11) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	VSTEP2_CONF1 [1]	VSTEP2_CONF1 [0]	ISTEP3_CONF1 [3]	ISTEP3_CONF1 [2]	ISTEP3_CONF1 [1]	ISTEP3_CONF1 [0]
Reserved	HB1 Vstep1 and Vstep2 conf [1]	HB1 Vstep1 and Vstep2 conf [0]	HB1 Istep3 conf [3]	HB1 Istep3 conf [2]	HB1 Istep3 conf [1]	HB1 Istep3 conf [0]

Table 96. HB1_DRIVER_CFG (0x11) MSB description

Bit	Name	Description
14	RES	Reserved bit
13	VSTEP2_CONF1 [1]	Vstep1 and Vstep2 thresholds configuration of the HB1
12	VSTEP2_CONF1 [0]	These two bits set the Vstep1 and Vstep2 thresholds of the HB1 00: Vstep1 = 1.1 V, Vstep2 = 2.67 V for the switch ON 00: Vstep1 = 1.3 V, Vstep2 = 3.33 V for the switch OFF 01: Vstep1 = 1.1 V, Vstep2 = 3.56 V for the switch ON 01: Vstep1 = 1.3 V, Vstep2 = 4.44 V for the switch OFF 10: Vstep1 = 2.2 V, Vstep2 = 4.45 V for the switch ON 10: Vstep1 = 2.6 V, Vstep2 = 5.55 V for the switch OFF 11: Vstep1 = 2.2 V, Vstep2 = 5.34 V for the switch ON 11: Vstep1 = 2.6 V, Vstep2 = 6.66 V for the switch OFF
11	ISTEP3_CONF1 [3]	Istep3 configuration of the HB1
10	ISTEP3_CONF1 [2]	0000 ⇒ 2 mA
9	ISTEP3_CONF1 [1]	0001 ⇒ 4 mA
8	ISTEP3_CONF1 [0]	0010 ⇒ 8 mA 0011 ⇒ 12 mA 0100 ⇒ 20 mA 0101 ⇒ 28 mA 0110 ⇒ 36 mA 0111 ⇒ 44 mA 1000 ⇒ 52 mA 1001 ⇒ 60 mA 1010 ⇒ 68 mA 1011 ⇒ 76 mA 1100 ⇒ 84 mA 1101 ⇒ 92 mA 1110 ⇒ 104 mA 1111 ⇒ 120 mA

Table 97. HB1_DRIVER_CFG (0x11) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF1 [3]	ISTEP2_CONF1 [2]	ISTEP2_CONF1 [1]	ISTEP2_CONF1 [0]	ISTEP1_CONF1 [3]	ISTEP1_CONF1 [2]	ISTEP1_CONF1 [1]	ISTEP1_CONF1 [0]
HB1 Istep3 conf [3]	HB1 Istep3 conf [2]	HB1 Istep3 conf [1]	HB1 Istep3 conf [0]	HB1 Istep3 conf [3]	HB1 Istep3 conf [2]	HB1 Istep3 conf [1]	HB1 Istep3 conf [0]

Table 98. HB1_DRIVER_CFG (0x11) LSB description

Bit	Name	Description
7	ISTEP2_CONF1 [3]	Istep2 configuration of the HB1 for the low to high transition
6	ISTEP2_CONF1 [2]	0000 ⇒ 1 mA
5	ISTEP2_CONF1 [1]	0001 ⇒ 2 mA
4	ISTEP2_CONF1 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA

Bit	Name	Description
		0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
3	ISTEP1_CONF1 [3]	Istep1 configuration of the HB1 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
2	ISTEP1_CONF1 [2]	
1	ISTEP1_CONF1 [1]	
0	ISTEP1_CONF1 [0]	

Table 99. HB1_DIAG_CFG (0x12) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	Bit 12	Bit 11	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	VDS_CONF1 [3]	VDS_CONF1 [2]	VDS_CONF1 [1]
Reserved	Reserved	Reserved	Reserved	VDS conf of the HB1 [3]	VDS conf of the HB1 [2]	VDS conf of the HB1 [1]

Table 100. HB1_DIAG_CFG (0x12) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	VDS_CONF1 [3]	V_{ds} monitor threshold configuration of the HB1 0000 ⇒ 75 mV
9	VDS_CONF1 [2]	

Bit	Name	Description
8	VDS_CONF1 [1]	0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V

Table 101. HB1_DIAG_CFG (0x12) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
VDS_CONF1 [0]	VDS_BLANK1 [3]	VDS_BLANK1 [2]	VDS_BLANK1 [1]	VDS_BLANK1 [0]	VDS_FILT1 [2]	VDS_FILT1 [2]	VDS_FILT1 [2]
VDS conf of the HB1 [0]	VDS blanking time conf [3]	VDS blanking time conf [2]	VDS blanking time conf [1]	VDS blanking time conf [0]	VDS filter time conf [2]	VDS filter time conf [1]	VDS filter time conf [0]

Table 102. HB1_DIAG_CFG (0x12) LSB description

Bit	Name	Description
7	VDS_CONF1 [0]	V_{ds} monitor threshold configuration of the HB1 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
6	VDS_BLANK1 [3]	V_{ds} blanking time configuration of the HB1 0000 ⇒ 0.625 µs 0001 ⇒ 1 µs 0010 ⇒ 1.25 µs 0011 ⇒ 1.5 µs 0100 ⇒ 2 µs 0101 ⇒ 3 µs 0110 ⇒ 4 µs 0111 ⇒ 5 µs 1000 ⇒ 6 µs 1001 ⇒ 7 µs 1010 ⇒ 8 µs 1x11 ⇒ 0.625 µs
5	VDS_BLANK1 [2]	
4	VDS_BLANK1 [1]	
3	VDS_BLANK1 [0]	
2	VDS_FILT1 [2]	V_{ds} filtering time configuration 000 ⇒ 0.5 µs
1	VDS_FILT1 [1]	

Bit	Name	Description
0	VDS_FILT1 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 0.5 µs

Table 103. HB1_TURN_OFF_CFG (0x13) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	GENMODE1 [1]	GENMODE1 [0]
Reserved	Reserved	Reserved	Reserved	Reserved	GENMODE bit conf [1]	GENMODE bit conf [0]

Table 104. HB1_TURN_OFF_CFG (0x13) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	RES	
9	GENMODE1 [1]	HB1 Gate driver actions when a VDH overvoltage is detected: 00 ⇒ Gate driver off 01 ⇒ HS off, LS on to lock the motor 10 ⇒ Flag only 11 ⇒ Gate driver off
8	GENMODE1 [0]	

Table 105. HB1_TURN_OFF_CFG (0x13) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	HB_FAULT1 [1]	HB_FAULT1 [0]	ISTEP2_OFF_ CONF1 [3]	ISTEP2_OFF_ CONF1 [2]	ISTEP2_OFF_ CONF1 [1]	ISTEP2_OFF_ CONF1 [0]
Reserved	Reserved	HB1 fault key [1]	HB1 fault key [0]	HB1 Istep2 conf [3]	HB1 Istep2 conf [2]	HB1 Istep2 conf [1]	HB1 Istep2 conf [0]

Table 106. HB1_TURN_OFF_CFG (0x13) LSB description

Bit	Name	Description
7	HB_FAULT1 [3]	Reserved bits
6	HB_FAULT1 [2]	
5	HB_FAULT1 [1]	HB1 fault key 00 ⇒ No key 01 ⇒ key 1 10 ⇒ key 2 (only for L99MH94)
4	HB_FAULT1 [0]	

Bit	Name	Description
		11 ⇒ key 1 + key 2 (only key 1 in L99MH92 because MSB not writable)
3	ISTEP2_OFF_CONF1 [3]	Istep2 configuration of the HB1 in case of the switch OFF of the external MOSFET
2	ISTEP2_OFF_CONF1 [2]	0000 ⇒ 1 mA
1	ISTEP2_OFF_CONF1 [1]	0001 ⇒ 2 mA
0	ISTEP2_OFF_CONF1 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA

Table 107. HB2_MODE_CFG (0x14) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	DT2 [2]	DT2 [1]	DT2 [0]	STRONG_ON _WHEEL2	HB_IDIAG2 [1]
Reserved	Reserved	Dead Time 2 [2]	Dead Time 2 [1]	Dead Time 2 [0]	Free-wheeling strong on HB2	HB2 diagnostic current

Table 108. HB2_MODE_CFG (0x14) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	DT2 [2]	Dead time of the HB2
11	DT2 [1]	000 ⇒ 0.5 µs
10	DT2 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 16 µs
9	STRONG_ON_ WHEEL2	Free-wheeling strong ON of the HB2 0: strong on disabled, free-wheeling gate current set to 4 mA 1: strong on enabled, free-wheeling gate current set to 30 mA
8	HB_IDIAG2 [1]	HB2 diagnostic currents setting 00: pull-up and pull-down currents off

Bit	Name	Description
		01: pull-up current off and pull-down current on 10: pull-up current on and pull-down current off 11: pull-up and pull-down currents off

Table 109. HB2_MODE_CFG (0x14) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
HB_IDIAG2 [1]	HB_PWM2 [2]	HB_PWM2 [1]	HB_PWM2 [0]	HB_MODE2 [1]	HB_MODE2 [0]	HB_WHEEL2 [1]	HB_WHEEL2 [0]
HB2 diagnostic current	HB2 PWM mapping [2]	HB2 PWM mapping [1]	HB2 PWM mapping [0]	HB2 mode [1]	HB2 mode [0]	HB2 free-wheeling [1]	HB2 free-wheeling [0]

Table 110. HB2_MODE_CFG (0x14) LSB description

Bit	Name	Description
7	HB_IDIAG2 [0]	Half-bridge 2 diagnostic currents setting 00: pull-up and pull-down currents off 01: pull-up current off and pull-down current on 10: pull-up current on and pull-down current off 11: pull-up and pull-down currents off
6	HB_PWM2 [2]	PWM mapping on HB2
5	HB_PWM2 [1]	This 3 bits register is used to indicate which PWM signal is applied to the HS or LS of the half-bridge 2
4	HB_PWM2 [0]	000 ⇒ LS of HB mapped on PWM1 001 ⇒ LS of HB mapped on PWM2 011 ⇒ HS of HB mapped on PWM1 100 ⇒ HS of HB mapped on PWM2 010 = 101 = 110 = 111 ⇒ No Mapped
3	HB_MODE2 [1]	HB2 functionality mode
2	HB_MODE2 [0]	00 ⇒ LS and HS of the HB2 are kept off 01 ⇒ LS of the HB2 is ON (static, no PWM), HS of the HB2 is OFF 10 ⇒ HS of the HB2 is ON (static, no PWM), LS of the HB2 is OFF 11 ⇒ LS or HS of the HB2 are ON according to the HB_PWM2 register
1	HB_WHEEL2 [1]	HB2 free-wheeling mode
0	HB_WHEEL2 [0]	00 = 11 ⇒ No mapping 01 ⇒ Active free-wheeling on HS of the HB 10 ⇒ Active free-wheeling on LS of the HB

Table 111. HB2_DRIVER_CFG (0x15) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	VSTEP2_CONF2 [1]	VSTEP2_CONF2 [0]	ISTEP3_CONF2 [3]	ISTEP3_CONF2 [2]	ISTEP3_CONF2 [1]	ISTEP3_CONF2 [0]
Reserved	HB2 Vstep1 and Vstep2 conf [1]	HB2 Vstep1 and Vstep2 conf [0]	HB2 Istep3 conf [3]	HB2 Istep3 conf [2]	HB2 Istep3 conf [1]	HB2 Istep3 conf [0]

Table 112. HB2_DRIVER_CFG (0x15) MSB description

Bit	Name	Description
14	RES	Reserved bit
13	VSTEP2_CONF2 [1]	Vstep1 and Vstep2 thresholds configuration of the HB2
12	VSTEP2_CONF2 [0]	These two bits set the Vstep1 and Vstep2 thresholds of the HB2 00: Vstep1 = 1.1 V, Vstep2 = 2.67 V for the switch ON 00: Vstep1 = 1.3 V, Vstep2 = 3.33 V for the switch OFF 01: Vstep1 = 1.1 V, Vstep2 = 3.56 V for the switch ON 01: Vstep1 = 1.3 V, Vstep2 = 4.44 V for the switch OFF 10 = Vstep1 = 2.2 V, Vstep2 = 4.45 V for the switch ON 10: Vstep1 = 2.6 V, Vstep2 = 5.55 V for the switch OFF 11: Vstep1 = 2.2 V, Vstep2 = 5.34 V for the switch ON 11: Vstep1 = 2.6 V, Vstep2 = 6.66 V for the switch OFF
11	ISTEP3_CONF2 [3]	Istep3 configuration of the HB2
10	ISTEP3_CONF2 [2]	0000 ⇒ 2 mA
9	ISTEP3_CONF2 [1]	0001 ⇒ 4 mA
8	ISTEP3_CONF2 [0]	0010 ⇒ 8 mA 0011 ⇒ 12 mA 0100 ⇒ 20 mA 0101 ⇒ 28 mA 0110 ⇒ 36 mA 0111 ⇒ 44 mA 1000 ⇒ 52 mA 1001 ⇒ 60 mA 1010 ⇒ 68 mA 1011 ⇒ 76 mA 1100 ⇒ 84 mA 1101 ⇒ 92 mA 1110 ⇒ 104 mA 1111 ⇒ 120 mA

Table 113. HB2_DRIVER_CFG (0x15) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF2 [3]	ISTEP2_CONF2 [2]	ISTEP2_CONF2 [1]	ISTEP2_CONF2 [0]	ISTEP1_CONF2 [3]	ISTEP1_CONF2 [2]	ISTEP1_CONF2 [1]	ISTEP1_CONF2 [0]
HB2 Istep3 conf [3]	HB2 Istep3 conf [2]	HB2 Istep3 conf [1]	HB2 Istep3 conf [0]	HB2 Istep3 conf [3]	HB2 Istep3 conf [2]	HB2 Istep3 conf [1]	HB2 Istep3 conf [0]

Table 114. HB2_DRIVER_CFG (0x15) LSB description

Bit	Name	Description
7	ISTEP2_CONF2 [3]	Istep2 configuration of the HB2 for the low to high transition
6	ISTEP2_CONF2 [2]	0000 ⇒ 1 mA
5	ISTEP2_CONF2 [1]	0001 ⇒ 2 mA
4	ISTEP2_CONF2 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA

Bit	Name	Description
		0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
3	ISTEP1_CONF2 [3]	Istep1 configuration of the HB2 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
2	ISTEP1_CONF2 [2]	
1	ISTEP1_CONF2 [1]	
0	ISTEP1_CONF2 [0]	

Table 115. HB2_DIAG_CFG (0x16) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	VDS_CONF2 [3]	VDS_CONF2 [2]	VDS_CONF2 [1]
Reserved	Reserved	Reserved	Reserved	VDS conf of the HB2 [3]	VDS conf of the HB2 [2]	VDS conf of the HB2 [1]

Table 116. HB2_DIAG_CFG (0x16) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	VDS_CONF2 [3]	V_{ds} monitor threshold configuration of the HB2 0000 ⇒ 75 mV
9	VDS_CONF2 [2]	

Bit	Name	Description
8	VDS_CONF2 [1]	0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V

Table 117. HB2_DIAG_CFG (0x16) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
VDS_CONF2 [0]	VDS_BLANK2 [3]	VDS_BLANK2 [2]	VDS_BLANK2 [1]	VDS_BLANK2 [0]	VDS_FILT2 [2]	VDS_FILT2 [2]	VDS_FILT2 [2]
VDS conf of the HB2 [0]	VDS blanking time conf [3]	VDS blanking time conf [2]	VDS blanking time conf [1]	VDS blanking time conf [0]	VDS filter time conf [2]	VDS filter time conf [1]	VDS filter time conf [0]

Table 118. HB2_DIAG_CFG (0x16) LSB description

Bit	Name	Description
7	VDS_CONF2 [0]	V_{ds} monitor threshold configuration of the HB2 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
6	VDS_BLANK2 [3]	V_{ds} blanking time configuration of the HB2 0000 ⇒ 0.625 µs 0001 ⇒ 1 µs 0010 ⇒ 1.25 µs 0011 ⇒ 1.5 µs 0100 ⇒ 2 µs 0101 ⇒ 3 µs 0110 ⇒ 4 µs 0111 ⇒ 5 µs 1000 ⇒ 6 µs 1001 ⇒ 7 µs 1010 ⇒ 8 µs 1x11 ⇒ 0.625 µs
5	VDS_BLANK2 [2]	
4	VDS_BLANK2 [1]	
3	VDS_BLANK2 [0]	
2	VDS_FILT2 [2]	V_{ds} filtering time configuration of the HB2 000 ⇒ 0.5 µs
1	VDS_FILT2 [1]	

Bit	Name	Description
0	VDS_FILT2 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 0.5 µs

Table 119. HB2_TURN_OFF_CFG (0x17) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	GENMODE2 [1]	GENMODE2 [0]
Reserved	Reserved	Reserved	Reserved	Reserved	GENMODE bit conf [1]	GENMODE bit conf [0]

Table 120. HB2_TURN_OFF_CFG (0x17) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	RES	
9	GENMODE2 [1]	HB2 Gate driver actions when a VDH overvoltage is detected: 00: Gate driver off 01: HS off, LS on to lock the motor 10: Flag only 11: Gate driver off
8	GENMODE2 [0]	

Table 121. HB2_TURN_OFF_CFG (0x17) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	HB_FAULT2 [1]	HB_FAULT2 [0]	ISTEP2_OFF_ CONF2 [3]	ISTEP2_OFF_ CONF2 [2]	ISTEP2_OFF_ CONF2 [1]	ISTEP2_OFF_ CONF2 [0]
Reserved	Reserved	HB2 fault key [1]	HB2 fault key [0]	HB2 Istep2 conf [3]	HB2 Istep2 conf [2]	HB2 Istep2 conf [1]	HB2 Istep2 conf [0]

Table 122. HB2_TURN_OFF_CFG (0x17) LSB description

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	HB_FAULT2 [1]	HB2 fault key 00 ⇒ No key 01 ⇒ key 1 10 ⇒ key 2 (only for L99MH94)
4	HB_FAULT2 [0]	

Bit	Name	Description
		11 ⇒ key 1 + key 2 (only key 1 in L99MH92 because MSB not writable)
3	ISTEP2_OFF_CONF2 [3]	Istep2 configuration of the HB2 in case of the switch OFF of the external MOSFET
2	ISTEP2_OFF_CONF2 [2]	0000 ⇒ 1 mA
1	ISTEP2_OFF_CONF2 [1]	0001 ⇒ 2 mA
0	ISTEP2_OFF_CONF2 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA

Table 123. HB3_MODE_CFG (0x18) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	DT3 [2]	DT3 [1]	DT3 [0]	STRONG_ON _WHEEL3	HB_IDIAG3 [1]
Reserved	Reserved	Dead Time 3 [2]	Dead Time 3 [1]	Dead Time 3 [0]	Free-wheeling strong on HB3	HB3 diagnostic current

Table 124. HB3_MODE_CFG (0x18) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	DT3 [2]	Dead time of the HB3
11	DT3 [1]	000 ⇒ 0.5 µs
10	DT3 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 16 µs
9	STRONG_ON_ WHEEL3	Free-wheeling strong ON of the HB3 0: strong on disabled, free-wheeling gate current set to 4 mA 1: strong on enabled, free-wheeling gate current set to 30 mA
8	HB_IDIAG3 [1]	Half-bridge 3 diagnostic currents setting 00: pull-up and pull-down currents off

Bit	Name	Description
		01: pull-up current off and pull-down current on 10: pull-up current on and pull-down current off 11: pull-up and pull-down currents off

Table 125. HB3_MODE_CFG (0x18) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
HB_IDIAG3 [1]	HB_PWM3 [2]	HB_PWM3 [1]	HB_PWM3 [0]	HB_MODE3 [1]	HB_MODE3 [0]	HB_WHEEL3 [1]	HB_WHEEL3 [0]
HB3 diagnostic current	HB3 PWM mapping [2]	HB3 PWM mapping [1]	HB3 PWM mapping [0]	HB3 mode [1]	HB3 mode [0]	HB3 free-wheeling [1]	HB3 free-wheeling [0]

Table 126. HB3_MODE_CFG (0x18) LSB description

Bit	Name	Description
7	HB_IDIAG3 [0]	HB3 diagnostic currents setting 00: pull-up and pull-down currents off 01: pull-up current off and pull-down current on 10: pull-up current on and pull-down current off 11: pull-up and pull-down currents off
6	HB_PWM3 [2]	PWM mapping on HB3 (only for L99MH94)
5	HB_PWM3 [1]	This 3 bits register is used to indicate which PWM signal is applied to the HS or LS of the half-bridge 3
4	HB_PWM3 [0]	000 ⇒ LS of HB mapped on PWM1 001 ⇒ LS of HB mapped on PWM2 011 ⇒ HS of HB mapped on PWM1 100 ⇒ HS of HB mapped on PWM2 010 = 101 = 110 = 111 ⇒ No Mapped
3	HB_MODE3 [1]	HB3 functionality mode (only for L99MH94)
2	HB_MODE3 [0]	00 ⇒ LS and HS of the HB3 are kept off 01 ⇒ LS of the HB3 is ON (static, no PWM), HS of the HB3 is OFF 10 ⇒ HS of the HB3 is ON (static, no PWM), LS of the HB3 is OFF 11 ⇒ LS or HS of the HB3 is ON in according to the HB_PWM1 register
1	HB_WHEEL3 [1]	HB3 free-wheeling mode (only for L99MH94)
0	HB_WHEEL3 [0]	00 = 11 ⇒ No mapping 01 ⇒ Active free-wheeling on HS of the HB 10 ⇒ Active free-wheeling on LS of the HB

Table 127. HB3_DRIVER_CFG (0x19) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	VSTEP2_CONF3 [1]	VSTEP2_CONF3 [0]	ISTEP3_CONF3 [3]	ISTEP3_CONF3 [2]	ISTEP3_CONF3 [1]	ISTEP3_CONF3 [0]
Reserved	HB3 Vstep1 and Vstep2 conf [1]	HB3 Vstep1 and Vstep2 conf [0]	HB3 Istep3 conf [3]	HB3 Istep3 conf [2]	HB3 Istep3 conf [1]	HB3 Istep3 conf [0]

Table 128. HB3_DRIVER_CFG (0x19) MSB description

Bit	Name	Description
14	RES	Reserved bit
13	VSTEP2_CONF3 [1]	Vstep1 and Vstep2 thresholds configuration of the HB3 (only for L99MH94)
12	VSTEP2_CONF3 [0]	These two bits set the Vstep1 and Vstep2 thresholds of the HB3 00: Vstep1 = 1.1 V, Vstep2 = 2.67 V for the switch ON 00: Vstep1 = 1.3 V, Vstep2 = 3.33 V for the switch OFF 01: Vstep1 = 1.1 V, Vstep2 = 3.56 V for the switch ON 01: Vstep1 = 1.3 V, Vstep2 = 4.44 V for the switch OFF 10: Vstep1 = 2.2 V, Vstep2 = 4.45 V for the switch ON 10: Vstep1 = 2.6 V, Vstep2 = 5.55 V for the switch OFF 11: Vstep1 = 2.2 V, Vstep2 = 5.34 V for the switch ON 11: Vstep1 = 2.6 V, Vstep2 = 6.66 V for the switch OFF
11	ISTEP3_CONF3 [3]	Istep3 configuration of the HB3 (only for L99MH94)
10	ISTEP3_CONF3 [2]	0000 ⇒ 2 mA
9	ISTEP3_CONF3 [1]	0001 ⇒ 4 mA
8	ISTEP3_CONF3 [0]	0010 ⇒ 8 mA 0011 ⇒ 12 mA 0100 ⇒ 20 mA 0101 ⇒ 28 mA 0110 ⇒ 36 mA 0111 ⇒ 44 mA 1000 ⇒ 52 mA 1001 ⇒ 60 mA 1010 ⇒ 68 mA 1011 ⇒ 76 mA 1100 ⇒ 84 mA 1101 ⇒ 92 mA 1110 ⇒ 104 mA 1111 ⇒ 120 mA

Table 129. HB3_DRIVER_CFG (0x19) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF3 [3]	ISTEP2_CONF3 [2]	ISTEP2_CONF3 [1]	ISTEP2_CONF3 [0]	ISTEP1_CONF3 [3]	ISTEP1_CONF3 [2]	ISTEP1_CONF3 [1]	ISTEP1_CONF3 [0]
HB3 Istep3 conf [3]	HB3 Istep3 conf [2]	HB3 Istep3 conf [1]	HB3 Istep3 conf [0]	HB3 Istep3 conf [3]	HB3 Istep3 conf [2]	HB3 Istep3 conf [1]	HB3 Istep3 conf [0]

Table 130. HB3_DRIVER_CFG (0x19) LSB description

Bit	Name	Description
7	ISTEP2_CONF3 [3]	Istep2 configuration of the HB3 for the low to high transition (only for L99MH94)
6	ISTEP2_CONF3 [2]	0000 ⇒ 1 mA
5	ISTEP2_CONF3 [1]	0001 ⇒ 2 mA
4	ISTEP2_CONF3 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA

Bit	Name	Description
		0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
3	ISTEP1_CONF3 [3]	Istep1 configuration of the HB3 (only for L99MH94) 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
2	ISTEP1_CONF3 [2]	
1	ISTEP1_CONF3 [1]	
0	ISTEP1_CONF3 [0]	

Table 131. HB3_DIAG_CFG (0x1A) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	VDS_CONF3 [3]	VDS_CONF3 [2]	VDS_CONF3 [1]
Reserved	Reserved	Reserved	Reserved	VDS conf of the HB3 [3]	VDS conf of the HB3 [2]	VDS conf of the HB3 [1]

Table 132. HB3_DIAG_CFG (0x1A) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	VDS_CONF3 [3]	V_{ds} monitor threshold configuration of the HB3 (only for L99MH94) 0000 ⇒ 75 mV
9	VDS_CONF3 [2]	

Bit	Name	Description
8	VDS_CONF3 [1]	0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V

Table 133. HB3_DIAG_CFG (0x1A) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
VDS_CONF3 [0]	VDS_BLANK3 [3]	VDS_BLANK3 [2]	VDS_BLANK3 [1]	VDS_BLANK3 [0]	VDS_FILT3 [2]	VDS_FILT3 [2]	VDS_FILT3 [2]
VDS conf of the HB3 [0]	VDS blanking time conf [3]	VDS blanking time conf [2]	VDS blanking time conf [1]	VDS blanking time conf [0]	VDS filter time conf [2]	VDS filter time conf [1]	VDS filter time conf [0]

Table 134. HB3_DIAG_CFG (0x1A) LSB description

Bit	Name	Description
7	VDS_CONF3 [0]	V_{ds} monitor threshold configuration of the HB3 (only for L99MH94) 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
6	VDS_BLANK3 [3]	V_{ds} blanking time configuration of the HB3 (only for L99MH94) 0000 ⇒ 0.625 µs 0001 ⇒ 1 µs 0010 ⇒ 1.25 µs 0011 ⇒ 1.5 µs 0100 ⇒ 2 µs 0101 ⇒ 3 µs 0110 ⇒ 4 µs 0111 ⇒ 5 µs 1000 ⇒ 6 µs 1001 ⇒ 7 µs 1010 ⇒ 8 µs 1x11 ⇒ 0.625 µs
5	VDS_BLANK3 [2]	
4	VDS_BLANK3 [1]	
3	VDS_BLANK3 [0]	
2	VDS_FILT3 [2]	V_{ds} filtering time configuration of the HB3 (only for L99MH94) 000 ⇒ 0.5 µs
1	VDS_FILT3 [1]	

Bit	Name	Description
0	VDS_FILT3 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 0.5 µs

Table 135. HB3_TURN_OFF_CFG (0x1B) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	GENMODE3 [1]	GENMODE3 [0]
Reserved	Reserved	Reserved	Reserved	Reserved	GENMODE bit conf [1]	GENMODE bit conf [0]

Table 136. HB3_TURN_OFF_CFG (0x1B) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	RES	
9	GENMODE3 [1]	HB3 Gate driver actions when a VDH overvoltage is detected (only for L99MH94): 00: Gate driver off 01: HS off, LS on to lock the motor 10: Flag only 11: Gate driver off
8	GENMODE3 [0]	

Table 137. HB3_TURN_OFF_CFG (0x1B) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	HB_FAULT3 [1]	HB_FAULT3 [0]	ISTEP2_OFF_ CONF3 [3]	ISTEP2_OFF_ CONF3 [2]	ISTEP2_OFF_ CONF3 [1]	ISTEP2_OFF_ CONF3 [0]
Reserved	Reserved	HB3 fault key [1]	HB3 fault key [0]	HB3 Istep2 conf [3]	HB3 Istep2 conf [2]	HB3 Istep2 conf [1]	HB3 Istep2 conf [0]

Table 138. HB3_TURN_OFF_CFG (0x1B) LSB description

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	HB_FAULT3 [1]	HB3 fault key (only for L99MH94)
4	HB_FAULT3 [0]	00 ⇒ No key 01 ⇒ key 1 10 ⇒ key 2 (not writable in L99MH92)

Bit	Name	Description
		11 ⇒ key 1 + key 2 (only key 1 in L99MH92 because MSB not writable)
3	ISTEP2_OFF_CONF3 [3]	Istep2 configuration of the HB3 in case of the switch OFF of the external MOSFET (only for L99MH94) 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
2	ISTEP2_OFF_CONF3 [2]	
1	ISTEP2_OFF_CONF3 [1]	
0	ISTEP2_OFF_CONF3 [0]	

Table 139. HB3_MODE_CFG (0x1C) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	DT4 [2]	DT4 [1]	DT4 [0]	STRONG_ON _WHEEL4	HB_IDIAG4 [1]
Reserved	Reserved	Dead Time 4 [2]	Dead Time 4 [1]	Dead Time 4 [0]	Free-wheeling strong on HB4	HB4 diagnostic current

Table 140. HB3_MODE_CFG (0x1C) MSB description

Bit	Name	Description
14	RES	Reserved bit
13	RES	Reserved bit
12	DT4 [2]	Dead time of the HB4 (only for L99MH94) 000 ⇒ 0.5 µs 001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 16 µs
11	DT4 [1]	
10	DT4 [0]	
9	STRONG_ON_ WHEEL4	Free-wheeling strong ON of the HB4 (only for L99MH94) 0: strong on disabled, free-wheeling gate current set to 4 mA 1: strong on enabled, free-wheeling gate current set to 30 mA
8	HB_IDIAG4 [1]	HB4 diagnostic currents setting (only for L99MH94)

Bit	Name	Description
		00: pull-up and pull-down currents off 01: pull-up current off and pull-down current on 10: pull-up current on and pull-down current off 11: pull-up and pull-down currents off

Table 141. HB3_MODE_CFG (0x1C) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
HB_IDIAG4 [1]	HB_PWM4 [2]	HB_PWM4 [1]	HB_PWM4 [0]	HB_MODE4 [1]	HB_MODE4 [0]	HB_WHEEL4 [1]	HB_WHEEL4 [0]
HB4 diagnostic current	HB4 PWM mapping [2]	HB4 PWM mapping [1]	HB4 PWM mapping [0]	HB4 mode [1]	HB4 mode [0]	HB4 free-wheeling [1]	HB4 free-wheeling [0]

Table 142. HB3_MODE_CFG (0x1C) LSB description

Bit	Name	Description
7	HB_IDIAG4 [0]	HB4 diagnostic currents setting (only for L99MH94) 00: pull-up and pull-down currents off 01: pull-up current off and pull-down current on 10: pull-up current on and pull-down current off 11: pull-up and pull-down currents off
6	HB_PWM4 [2]	PWM mapping on HB4 (only for L99MH94) This 3 bits register is used to indicate which PWM signal is applied to the HS or LS of the half-bridge 4 000 ⇒ LS of HB mapped on PWM1 001 ⇒ LS of HB mapped on PWM2 011 ⇒ HS of HB mapped on PWM1 100 ⇒ HS of HB mapped on PWM2 010 = 101 = 110 = 111 ⇒ No Mapped
5	HB_PWM4 [1]	
4	HB_PWM4 [0]	
3	HB_MODE4 [1]	HB4 functionality mode (only for L99MH94) 00 ⇒ LS and HS of the HB1 are kept off 01 ⇒ LS of the HB1 is ON (static, no PWM), HS of the HB1 is OFF 10 ⇒ HS of the half bridge 1 is ON (static, no PWM), LS of the half bridge is OFF 11 ⇒ LS or HS of the half-bridge is ON according to the HB_PWM1 register
2	HB_MODE4 [0]	
1	HB_WHEEL4 [1]	HB4 free-wheeling mode (only for L99MH94) 00 = 11 ⇒ No mapping 01 ⇒ Active free-wheeling on HS of the HB 10 ⇒ Active free-wheeling on LS of the HB
0	HB_WHEEL4 [0]	

Table 143. HB4_DRIVER_CFG (0x1D) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	VSTEP2_CONF4 [1]	VSTEP2_CONF4 [0]	ISTEP3_CONF4 [3]	ISTEP3_CONF4 [2]	ISTEP3_CONF4 [1]	ISTEP3_CONF4 [0]

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved	HB4 Vstep1 and Vstep2 conf [1]	HB4 Vstep1 and Vstep2 conf [0]	HB4 Istep3 conf [3]	HB4 Istep3 conf [2]	HB4 Istep3 conf [1]	HB4 Istep3 conf [0]

Table 144. HB4_DRIVER_CFG (0x1D) MSB description

Bit	Name	Description
14	RES	Reserved bit
13	VSTEP2_CONF4 [1]	Vstep1 and Vstep2 thresholds configuration of the HB4 (only for L99MH94)
12	VSTEP2_CONF4 [0]	These two bits set the Vstep1 and Vstep2 thresholds of the HB4 00: Vstep1 = 1.1 V, Vstep2 = 2.67 V for the switch ON 00: Vstep1 = 1.3 V, Vstep2 = 3.33 V for the switch OFF 01: Vstep1 = 1.1 V, Vstep2 = 3.56 V for the switch ON 01: Vstep1 = 1.3 V, Vstep2 = 4.44 V for the switch OFF 10: Vstep1 = 2.2 V, Vstep2 = 4.45 V for the switch ON 10: Vstep1 = 2.6 V, Vstep2 = 5.55 V for the switch OFF 11: Vstep1 = 2.2 V, Vstep2 = 5.34 V for the switch ON 11: Vstep1 = 2.6 V, Vstep2 = 6.66 V for the switch OFF
11	ISTEP3_CONF4 [3]	Istep3 configuration of the HB4 (only for L99MH94)
10	ISTEP3_CONF4 [2]	0000 ⇒ 2 mA
9	ISTEP3_CONF4 [1]	0001 ⇒ 4 mA
8	ISTEP3_CONF4 [0]	0010 ⇒ 8 mA 0011 ⇒ 12 mA 0100 ⇒ 20 mA 0101 ⇒ 28 mA 0110 ⇒ 36 mA 0111 ⇒ 44 mA 1000 ⇒ 52 mA 1001 ⇒ 60 mA 1010 ⇒ 68 mA 1011 ⇒ 76 mA 1100 ⇒ 84 mA 1101 ⇒ 92 mA 1110 ⇒ 104 mA 1111 ⇒ 120 mA

Table 145. HB4_DRIVER_CFG (0x1D) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF4 [3]	ISTEP2_CONF4 [2]	ISTEP2_CONF4 [1]	ISTEP2_CONF4 [0]	ISTEP1_CONF4 [3]	ISTEP1_CONF4 [2]	ISTEP1_CONF4 [1]	ISTEP1_CONF4 [0]
HB4 Istep3 conf [3]	HB4 Istep3 conf [2]	HB4 Istep3 conf [1]	HB4 Istep3 conf [0]	HB4 Istep3 conf [3]	HB4 Istep3 conf [2]	HB4 Istep3 conf [1]	HB4 Istep3 conf [0]

Table 146. HB4_DRIVER_CFG (0x1D) LSB description

Bit	Name	Description
7	ISTEP2_CONF4 [3]	Istep2 configuration of the HB4 for the low to high transition (only for L99MH94)
6	ISTEP2_CONF4 [2]	0000 ⇒ 1 mA

Bit	Name	Description
5	ISTEP2_CONF4 [1]	0001 ⇒ 2 mA
4	ISTEP2_CONF4 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
3	ISTEP1_CONF4 [3]	Istep1 configuration of the HB4 (only for L99MH94)
2	ISTEP1_CONF4 [2]	0000 ⇒ 1 mA
1	ISTEP1_CONF4 [1]	0001 ⇒ 2 mA
0	ISTEP1_CONF4 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA

Table 147. HB4_DIAG_CFG (0x1E) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	VDS_CONF4 [3]	VDS_CONF4 [2]	VDS_CONF4 [1]
Reserved	Reserved	Reserved	Reserved	VDS conf of the HB4 [3]	VDS conf of the HB4 [2]	VDS conf of the HB4 [1]

Table 148. HB4_DIAG_CFG (0x1E) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	

Bit	Name	Description
12	RES	Reserved bits
11	RES	
10	VDS_CONF4 [3]	V_{ds} monitor threshold configuration of the HB4 (only for L99MH94)
9	VDS_CONF4 [2]	0000 ⇒ 75 mV
8	VDS_CONF4 [1]	0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V

Table 149. HB4_DIAG_CFG (0x1E) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
VDS_CONF4 [0]	VDS_BLANK4 [3]	VDS_BLANK4 [2]	VDS_BLANK4 [1]	VDS_BLANK4 [0]	VDS_FILT4 [2]	VDS_FILT4 [2]	VDS_FILT4 [2]
VDS conf of the HB4 [0]	VDS blanking time conf [3]	VDS blanking time conf [2]	VDS blanking time conf [1]	VDS blanking time conf [0]	VDS filter time conf [2]	VDS filter time conf [1]	VDS filter time conf [0]

Table 150. HB4_DIAG_CFG (0x1E) LSB description

Bit	Name	Description
7	VDS_CONF4 [0]	V_{ds} monitor threshold configuration of the HB4 (only for L99MH94) 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
6	VDS_BLANK4 [3]	V_{ds} blanking time configuration of the HB4 (only for L99MH94)
5	VDS_BLANK4 [2]	0000 ⇒ 0.625 µs
4	VDS_BLANK4 [1]	0001 ⇒ 1 µs
3	VDS_BLANK4 [0]	0010 ⇒ 1.25 µs 0011 ⇒ 1.5 µs 0100 ⇒ 2 µs 0101 ⇒ 3 µs 0110 ⇒ 4 µs 0111 ⇒ 5 µs 1000 ⇒ 6 µs 1001 ⇒ 7 µs

Bit	Name	Description
		1010 ⇒ 8 µs 1x11 ⇒ No mapped
2	VDS_FILT4 [2]	V_{ds} filtering time configuration of the HB4 (only for L99MH94)
1	VDS_FILT4 [1]	000 ⇒ 0.5 µs
0	VDS_FILT4 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ No mapped

Table 151. HB4_TURN_OFF_CFG (0x1F) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	GENMODE4 [1]	GENMODE4 [0]
Reserved	Reserved	Reserved	Reserved	Reserved	GENMODE bit conf [1]	GENMODE bit conf [0]

Table 152. HB4_TURN_OFF_CFG (0x1F) MSB description

Bit	Name	Description
14	RES	Reserved bits
13	RES	
12	RES	
11	RES	
10	RES	
9	GENMODE4 [1]	HB4 Gate driver actions when a VDH overvoltage is detected (only for L99MH94):
8	GENMODE4 [0]	00: Gate driver off 01: HS off, LS on to lock the motor 10: Flag only 11: Gate driver off

Table 153. HB4_TURN_OFF_CFG (0x1F) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	HB_FAULT4 [1]	HB_FAULT4 [0]	ISTEP2_OFF_ CONF4 [3]	ISTEP2_OFF_ CONF4 [2]	ISTEP2_OFF_ CONF4 [1]	ISTEP2_OFF_ CONF4 [0]
Reserved	Reserved	HB4 fault key [1]	HB4 fault key [0]	HB4 Istep2 conf [3]	HB4 Istep2 conf [2]	HB4 Istep2 conf [1]	HB4 Istep2 conf [0]

Table 154. HB4_TURN_OFF_CFG (0x1F) LSB description

Bit	Name	Description
7	RES	Reserve bits

Bit	Name	Description
6	RES	Reserve bits
5	HB_FAULT4 [1]	HB4 fault key (only for L99MH94)
4	HB_FAULT4 [0]	00 ⇒ No key 01 ⇒ key 1 10 ⇒ key 2 (not writable in L99MH92) 11 ⇒ key 1 + key 2 (only key 1 in L99MH92 because MSB not writable)
3	ISTEP2_OFF_CONF4 [3]	Istep2 configuration of the HB4 in case of the switch OFF of the external MOSFET (only for L99MH94)
2	ISTEP2_OFF_CONF4 [2]	0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
1	ISTEP2_OFF_CONF4 [1]	
0	ISTEP2_OFF_CONF4 [0]	

Table 155. HB5_MODE_CONFIG (0x20) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 156. HB5_MODE_CONFIG (0x20) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 157. HB5_DRIVER_CFG (0x21) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 158. HB5_DRIVER_CFG (0x21) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 159. HB5_DIAG_CFG (0x22) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 160. HB5_DIAG_CFG (0x22) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 161. HB5_TURN_OFF_CFG (0x23) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 162. HB5_TURN_OFF_CFG (0x23) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 163. HB6_MODE_CONFIG (0x24) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 164. HB6_MODE_CONFIG (0x24) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 165. HB6_DRIVER_CFG (0x25) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 166. HB6_DRIVER_CFG (0x25) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 167. HB6_DIAG_CFG (0x26) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 168. HB6_DIAG_CFG (0x26) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 169. HB6_TURN_OFF_CFG (0x27) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 170. HB6_TURN_OFF_CFG (0x27) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 171. HB7_MODE_CONFIG (0x28) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 172. HB7_MODE_CONFIG (0x28) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 173. HB7_DRIVER_CFG (0x29) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 174. HB7_DRIVER_CFG (0x29) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF7 [3]	RES	RES	RES	RES	RES	RES	RES
HB7 Istep3 conf [3]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 175. HB7_DIAG_CFG (0x2A) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 176. HB7_DIAG_CFG (0x2A) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 177. HB7_TURN_OFF_CFG (0x2B) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 178. HB7_TURN_OFF_CFG (0x2B) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 179. HB8_MODE_CONFIG (0x2C) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 180. HB8_MODE_CONFIG (0x2C) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 181. HB8_DRIVER_CFG (0x2D) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 182. HB8_DRIVER_CFG (0x2D) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 183. HB8_DIAG_CFG (0x2E) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 184. HB8_DIAG_CFG (0x2E) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 185. HB8_TURN_OFF_CFG (0x2F) MSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 186. HB8_TURN_OFF_CFG (0x2F) LSB

"Address Error" when accessing this register, only for L99MH94Q7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 187. OUT_ENABLE (0x30) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 188. **OUT_ENABLE (0x30) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	OUT4	OUT3	OUT2	OUT1
Reserved	Reserved	Reserved	Reserved	Out enable HB4	Out enable HB3	Out enable HB2	Out enable HB1

Table 189. **OUT_ENABLE (0x30) LSB description**

Bit	Name	Description
7	RES	Reserved bits
6	RES	
5	RES	
4	RES	
3	OUT4	Gate driver enables bit to control HB4 (only for L99MH94). This bit is reset if a watchdog error is detected
2	OUT3	Gate driver enables bit to control HB3 (only for L99MH94). This bit is reset if a watchdog error is detected
1	OUT2	Gate driver enables bit to control HB2. This bit is reset if a watchdog error is detected
0	OUT1	Gate driver enables bit to control HB1. This bit is reset if a watchdog error is detected

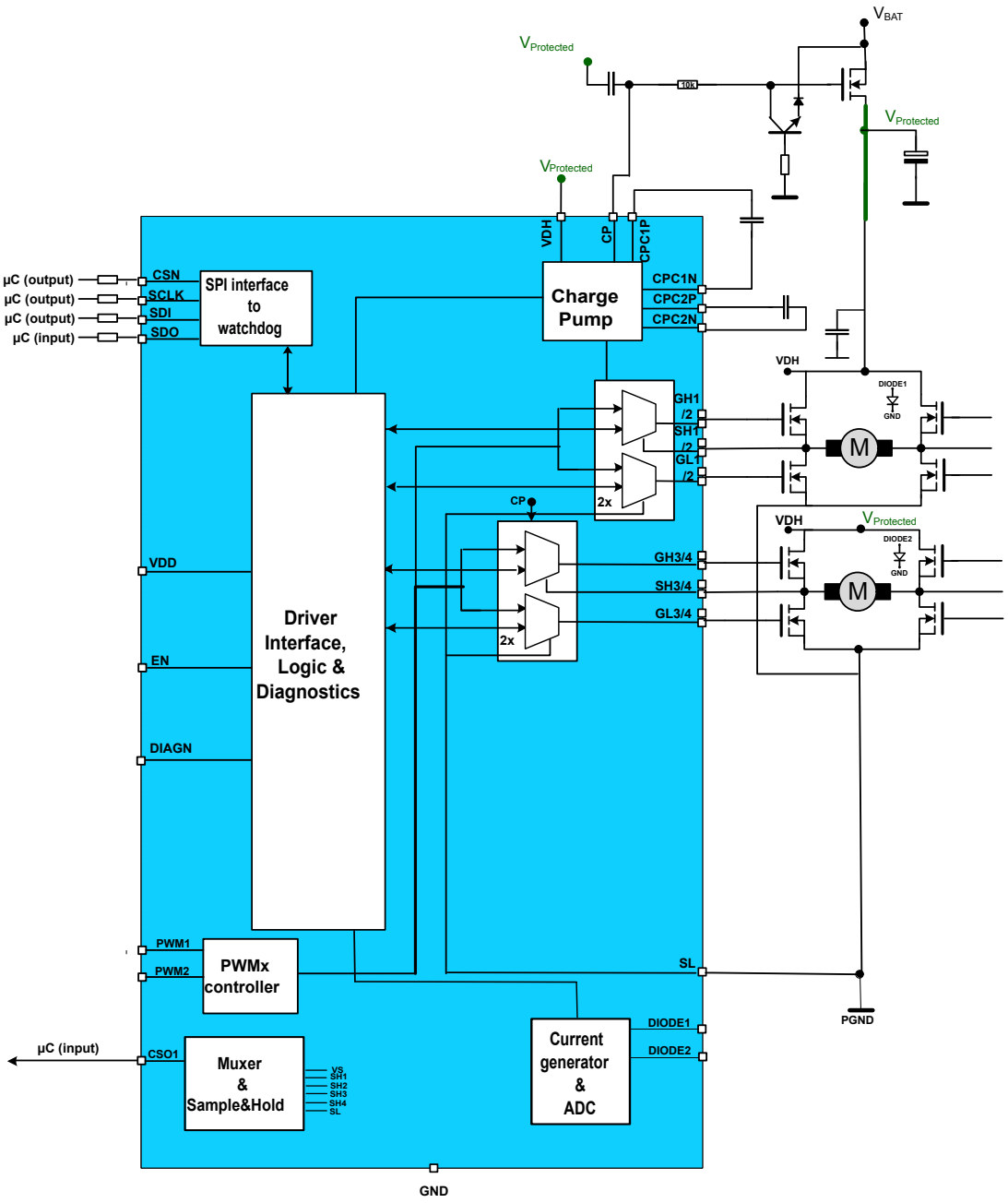
8 Application examples

The L99MH94 / L99MH92 is a device that integrates the control of 4 / 2 external half-bridges in a completely independent and configurable way. This allows the device to be used in multiple application scenarios.

To show the potential of L99MH94 / L99MH92 some of the possible application scenarios are shown here.

A classic configuration where 2 motors are controlled simultaneously is shown in the Figure 43: 2 different H-bridges are controlled simultaneously from L99MH94 / L99MH92.

Figure 43. Driving 2 DC motors simultaneously



The Figure 44 shows an application scenario where 2 resistive loads (heater, fan etc.) are driven by a high side and a low side and 2 motors are controlled by 2 H-bridges.

Figure 44. L99MH94 driving 1 DC motors + 1 additional independent loads simultaneously

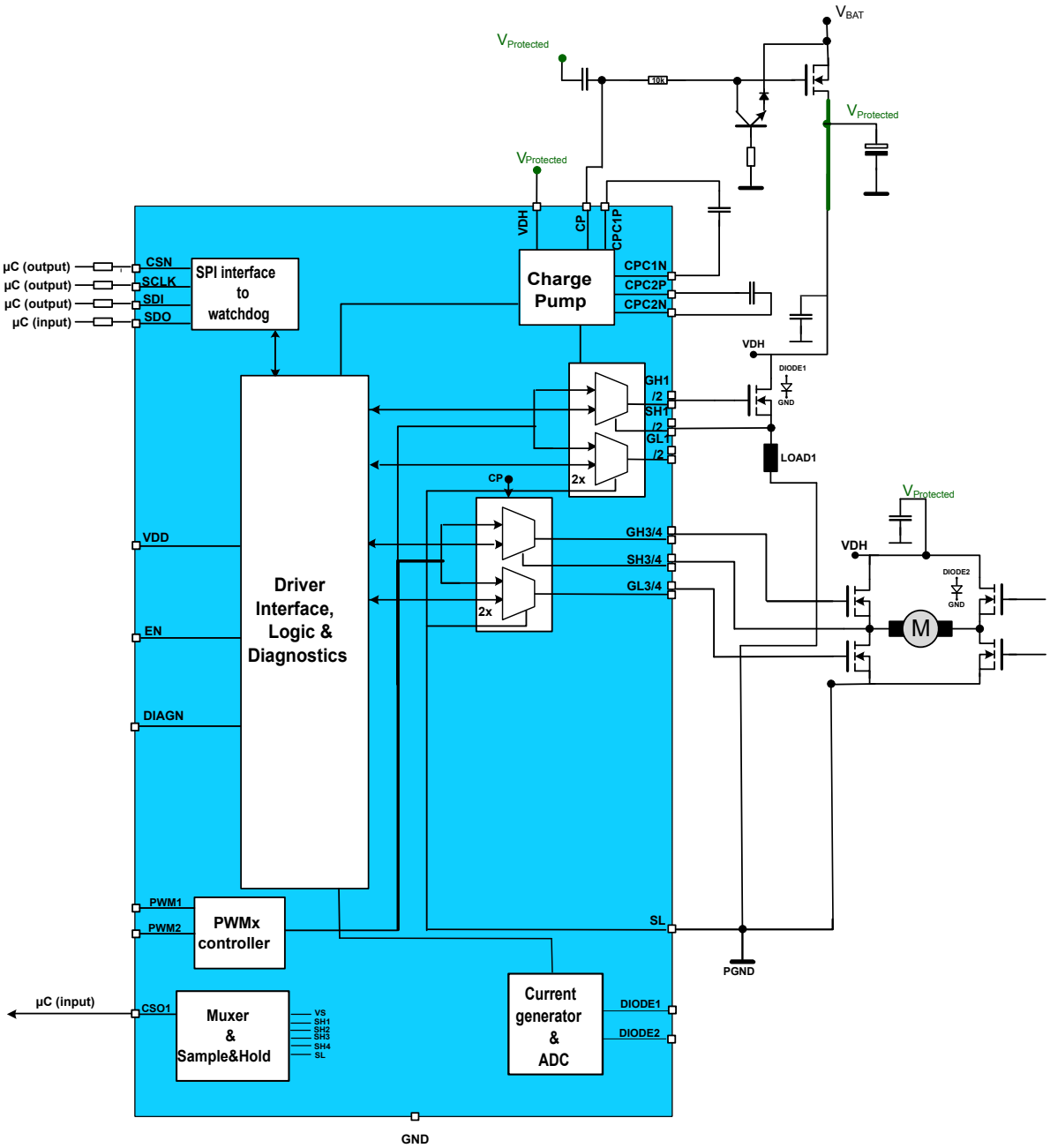
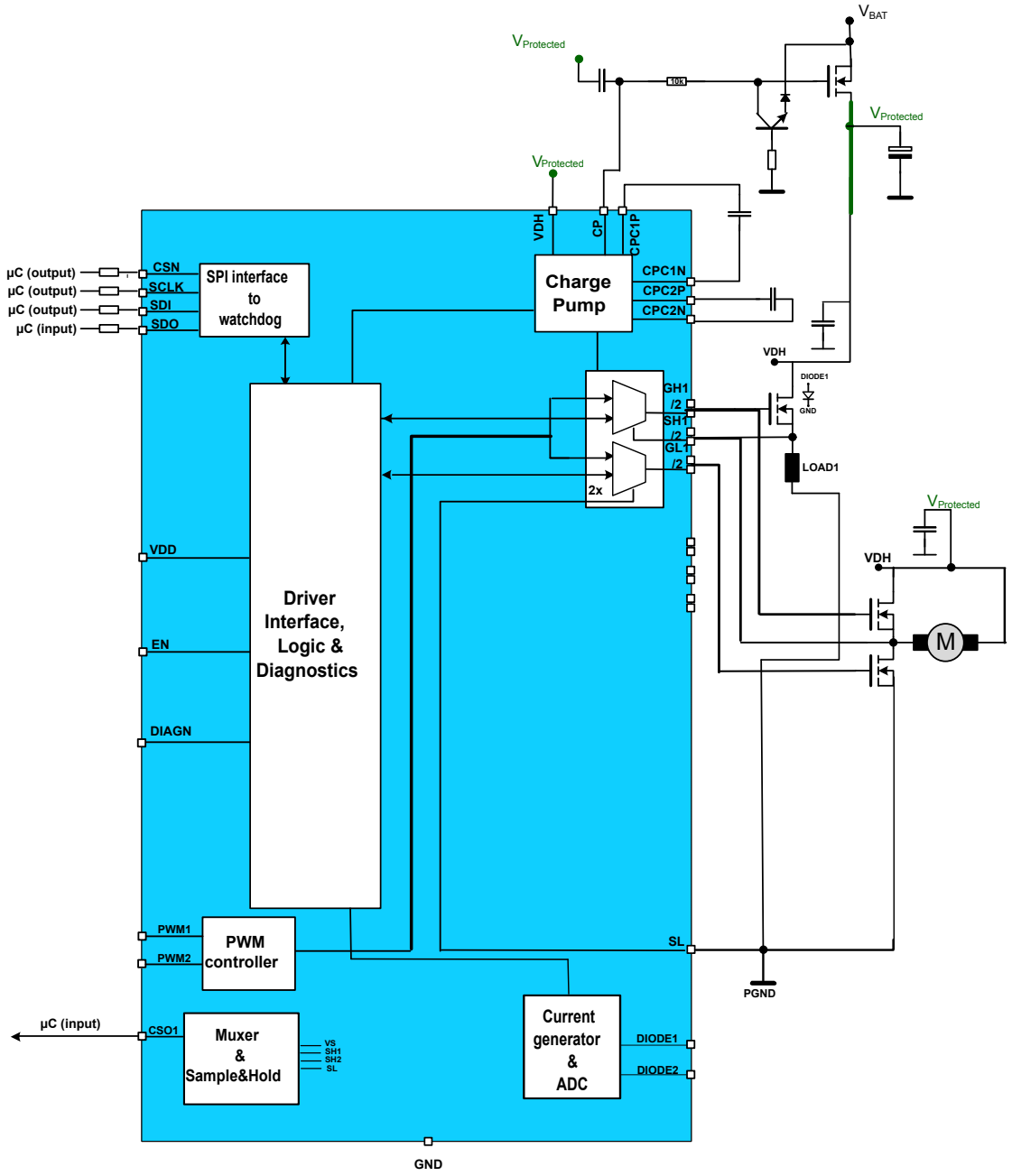
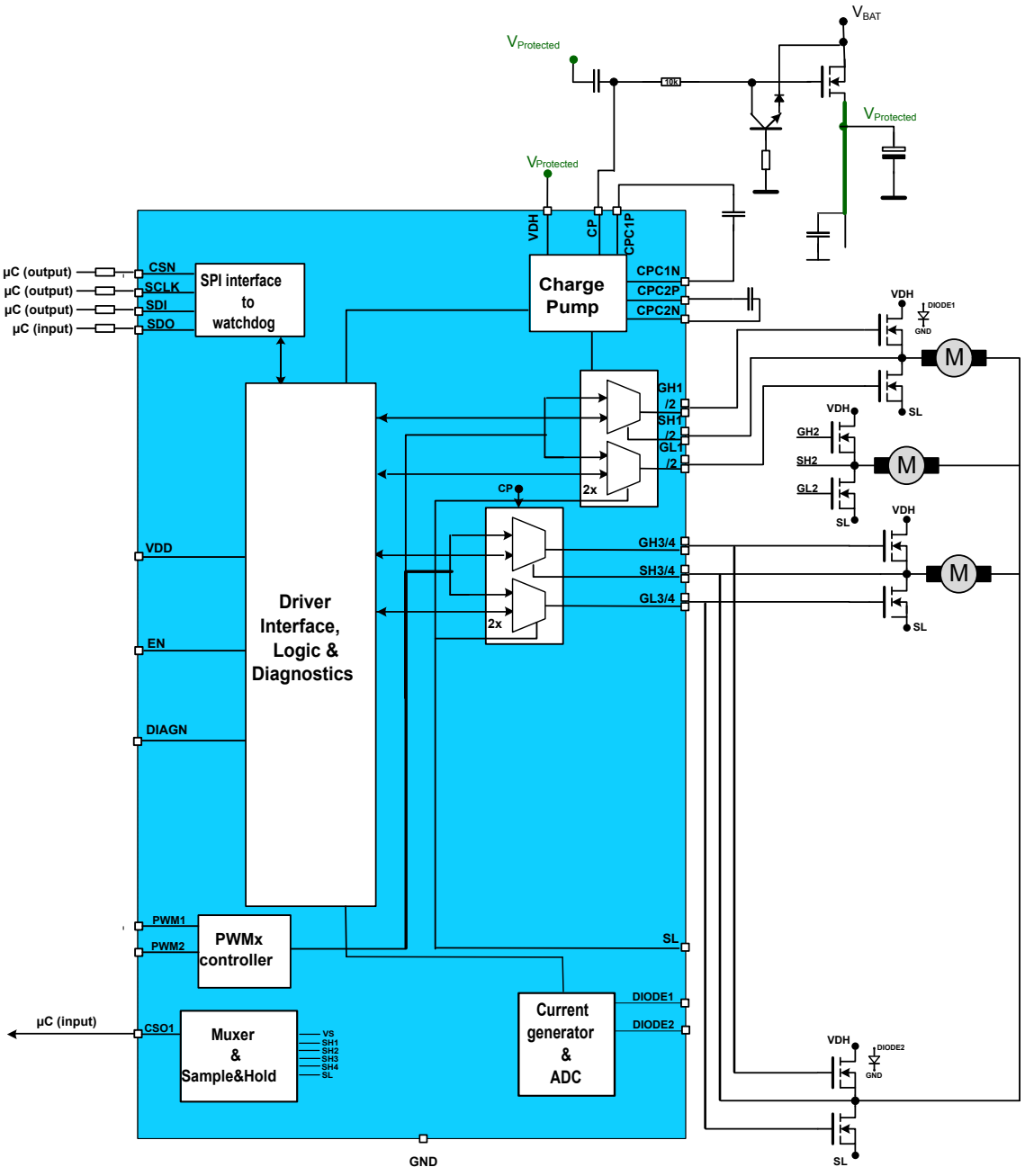


Figure 45. **L99MH92 driving 1 DC motors + 1 additional independent loads simultaneously**



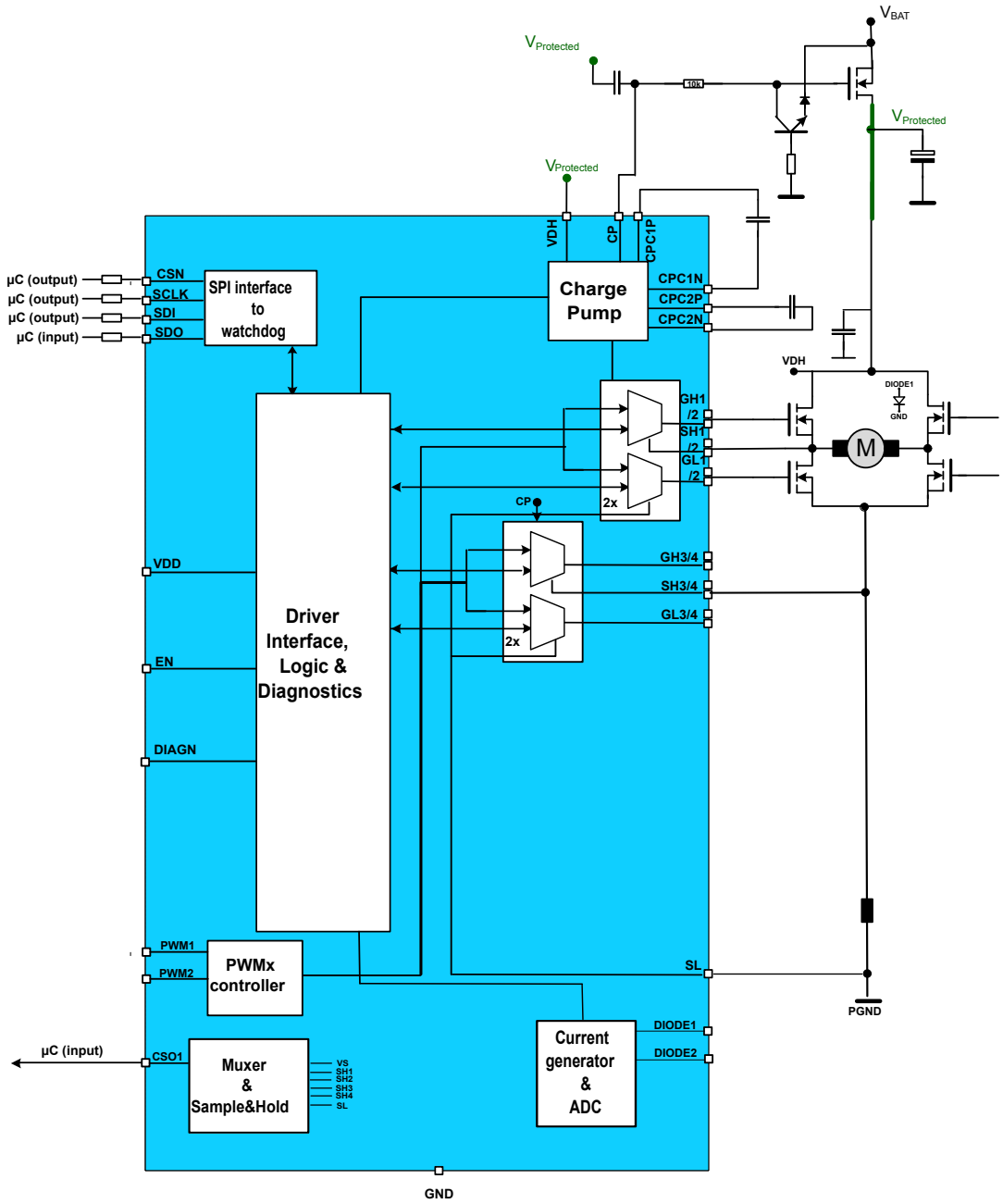
The Figure 46 shows an application scenario where 3 motors are controlled by 4 half bridges.

Figure 46. L99MH94 driving 3 motors sequentially



The L99MH94 / L99MH92 also allows the classic current measurement system through a sensing resistor connected to the low side sources of an H-bridge. In this case, one of the pins of the resistor, the one connected to the low side sources, must be connected to the SHx pin of one of the other half bridges and the second pin of the resistor to the SL pin of L99MH94 / L99MH92 (see the Figure 47).

Figure 47. L99MH94 driving 1 DC motor with classical current measurement via shunt resistor



The L99MH94 / L99MH92 logic also allows any connection between the half bridges of the device, GHx/SHx/GLx can be associated with any GHy/SHy/GLy (see the Figure 48).

Figure 48. L99MH94 driving DC motors simultaneously with not sequentially gate drivers

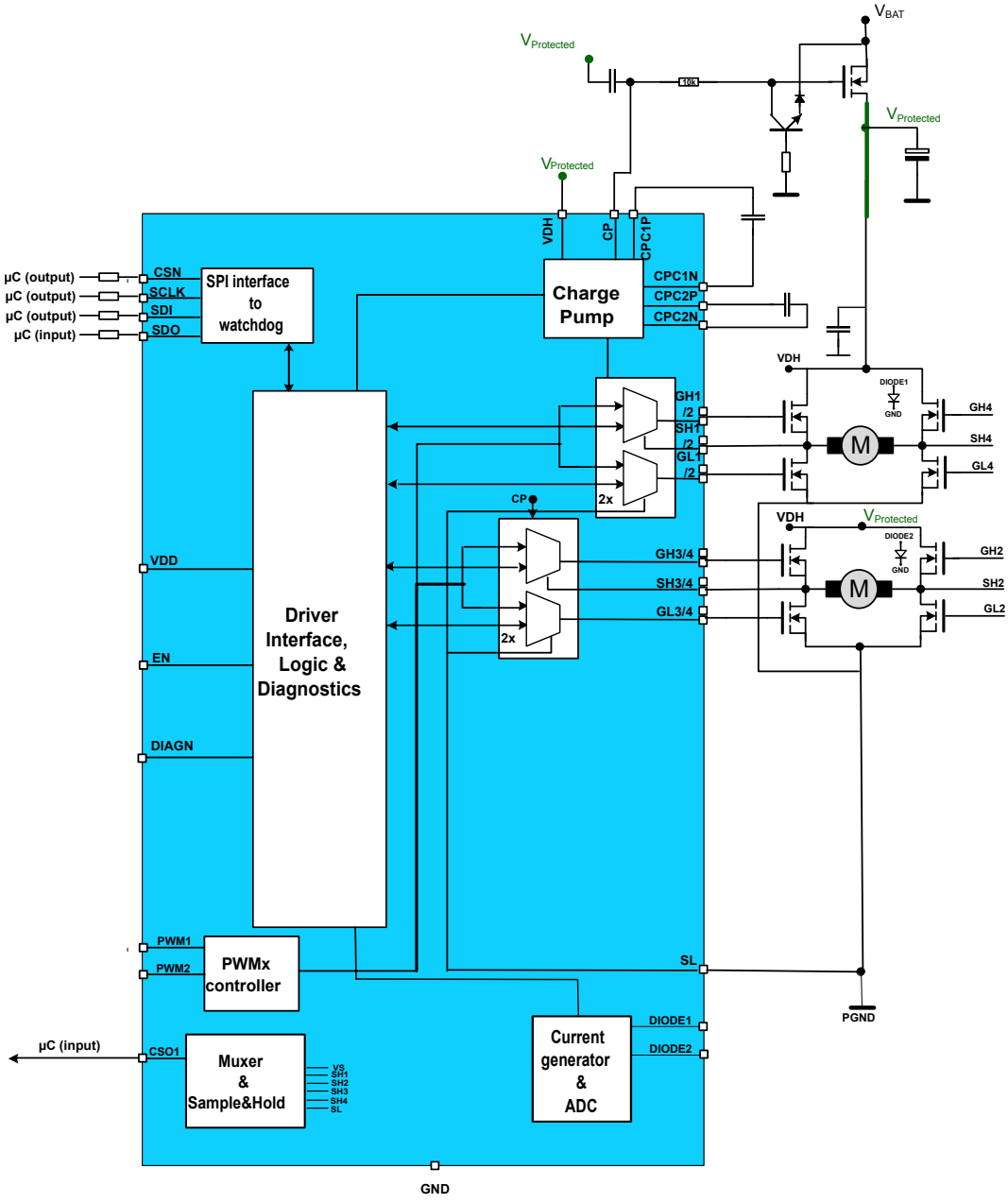
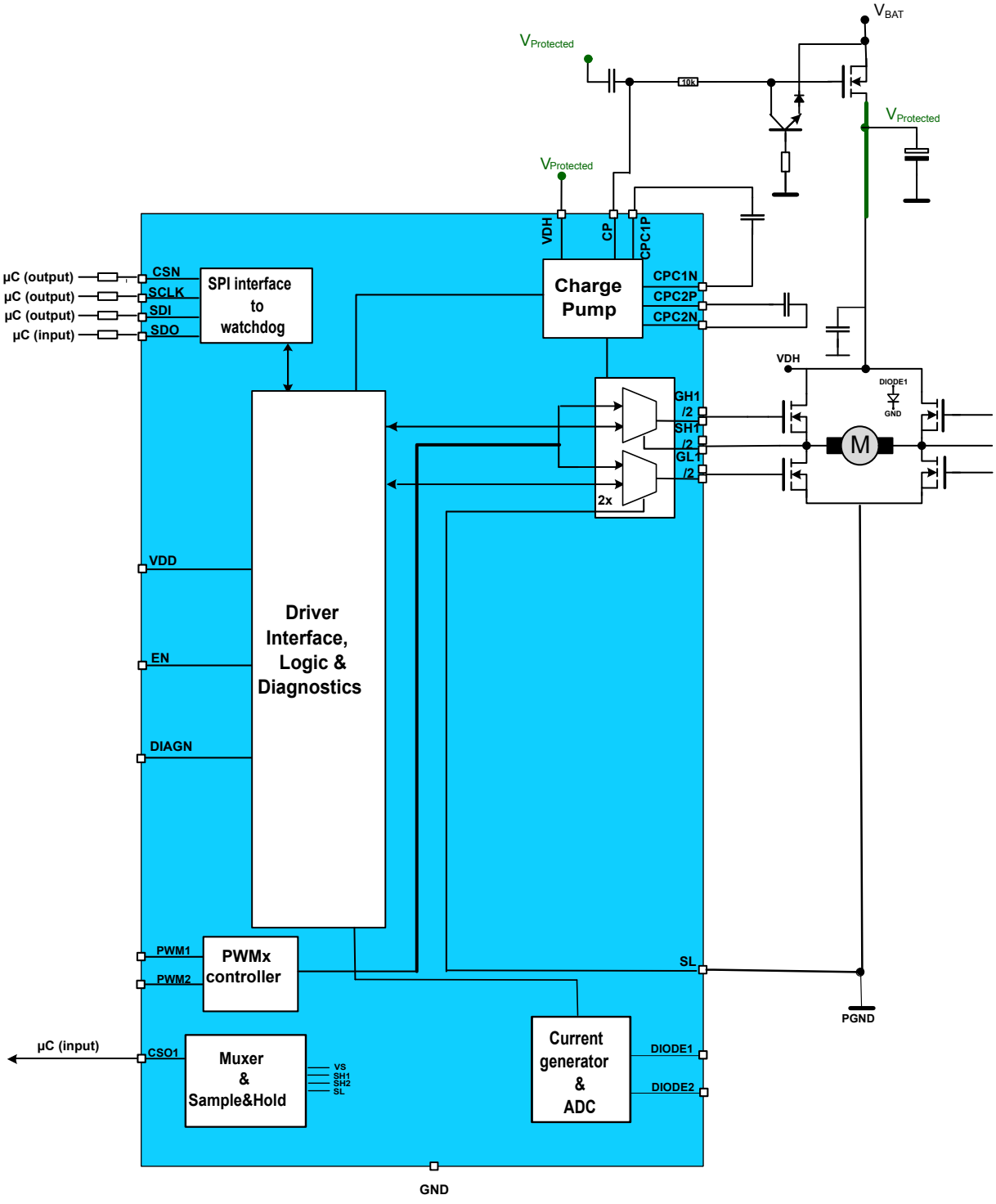


Figure 49. **L99MH92 driving DC motors simultaneously with not sequentially gate drivers**



9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 VFQFN32L (5x6x0.9 mm exp. pad down) package information

Figure 50. VFQFN32L (5x6x0.9 mm exp. pad down) package outline

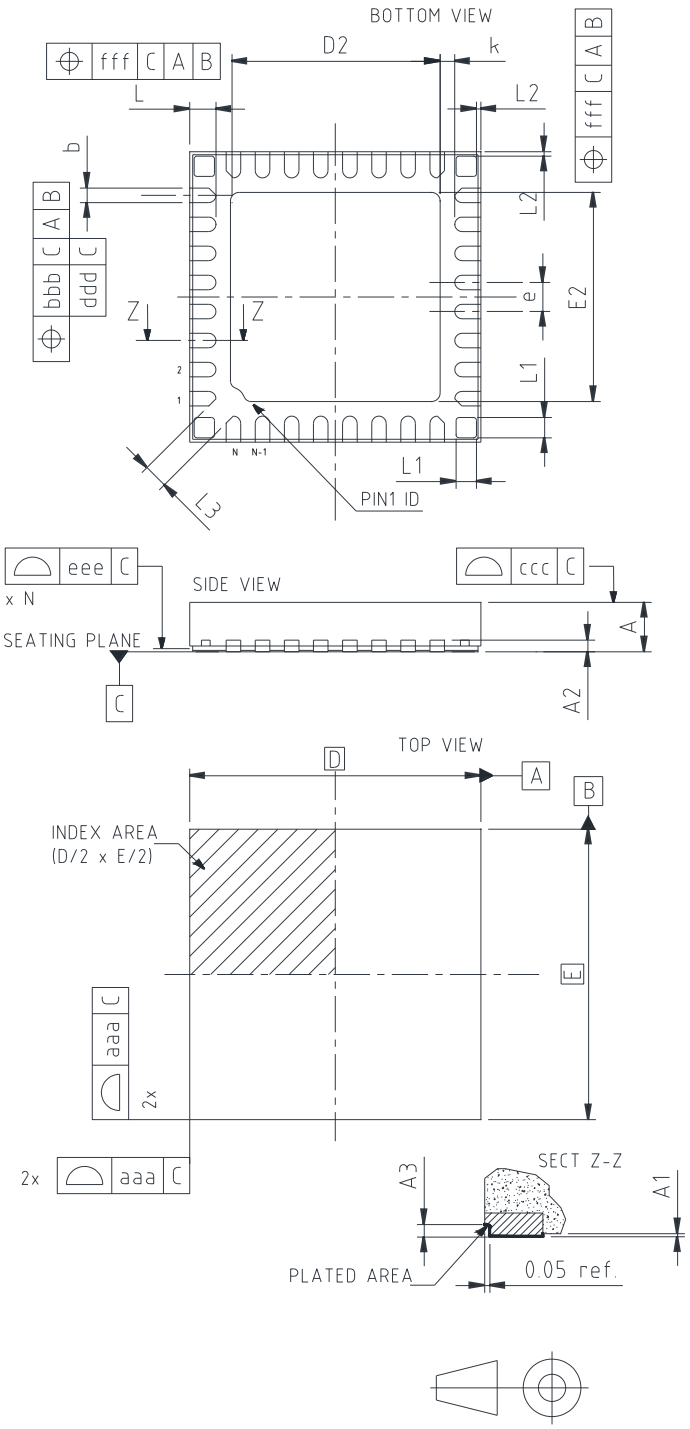


Table 190. **VFQFN32L (5x5x0.9 mm exp. pad down) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.2 REF	
A3	0.10	-	-
b	0.20	0.25	0.30
D	-	5.00	-
e	-	0.5	-
E	-	5.00	-
L	0.35	0.45	0.55
L1	-	0.35	-
L2	-	0.075	-
L3	-	0.42	-
k	0.20	-	-
N		32+4	
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

9.2 VFQFN48L (7x7x0.9 mm exp. pad down) package information

Figure 51. **VFQFN48L (7x7x0.9 mm exp. pad down) package outline**

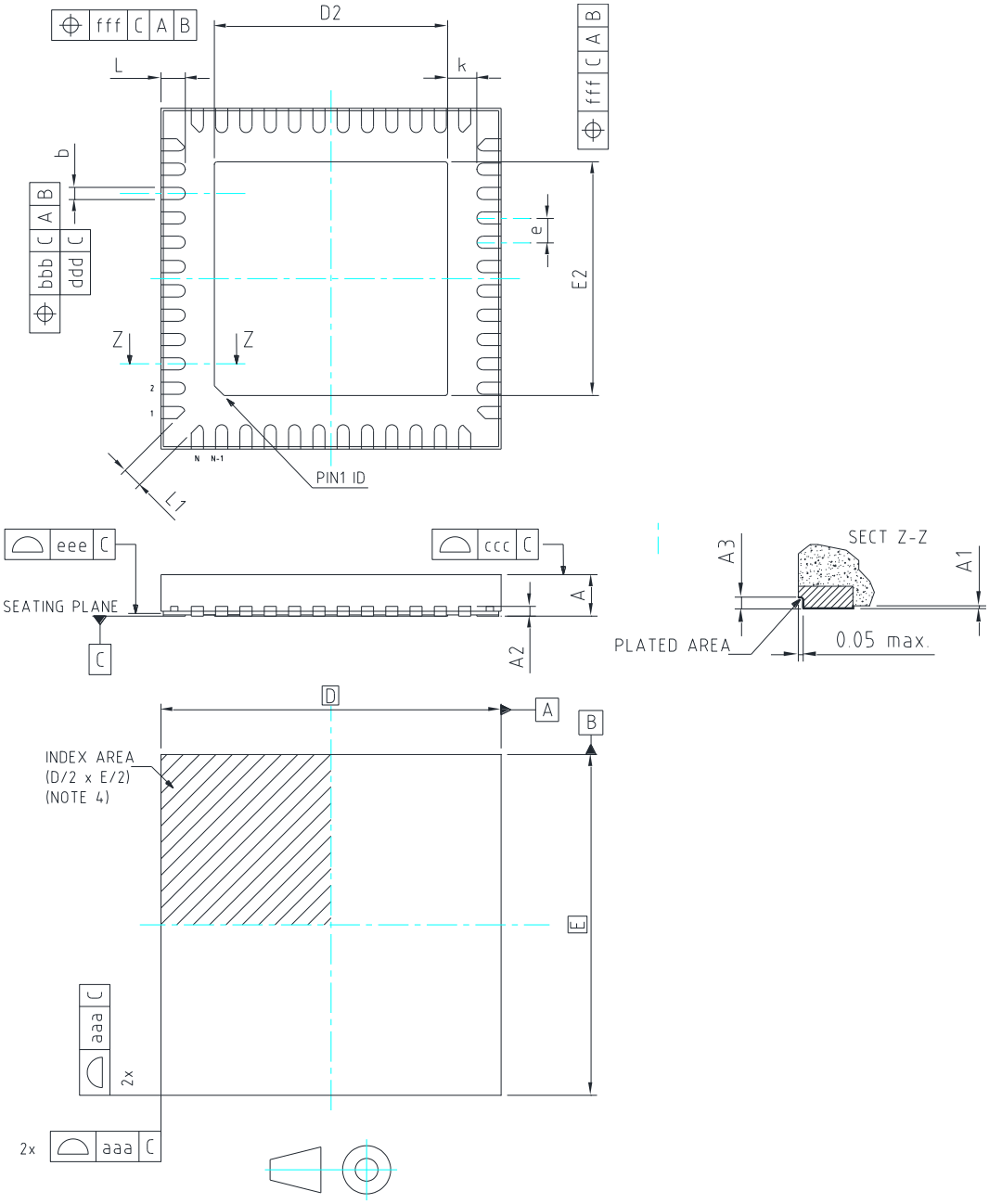


Table 191. **VFQFN48L (7x7x0.9 mm exp. pad down) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.2 REF	
A3	0.10	-	-
b	0.20	0.25	0.30
D	-	7.00	-
D2	5.30	5.40	5.50
e	-	0.5	-
E	-	7.00	-
E2	5.30	5.40	5.50
L	0.45	0.50	0.55
L1	0.35	-	-
k	0.25	-	-
N		48	
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.05	
eee		0.10	
fff		0.10	
REF		-	

10 Ordering information

Table 192. **Order code**

Order code	Package	Packing
L99MH92Q5-TR	VFQFN32+4L WF 5x5x0.9 mm	Tape and reel
L99MH94Q5-TR	VFQFN32+4L WF 5x5x0.9 mm	Tape and reel
L99MH94Q7-TR	VFQFN48L WF 7x7x0.9 mm	Tape and reel

Revision history

Table 193. **Document revision history**

Date	Version	Changes
07-Nov-2025	1	Initial release.

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