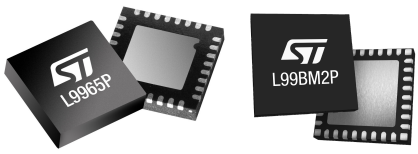
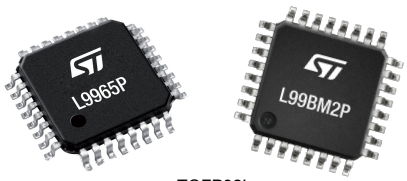
L9965P, L9965P

Datasheet

Single channel pyro-fuse driver



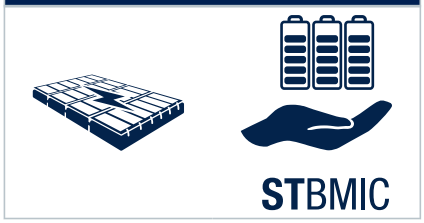
VFQFN32+4L
5x5x0.9 mm



TQFP32L
7x7x1 mm

Product summary		
Order code	**FuSa**	**Qualification**
L9965P-FN	Full ISO26262 compliant ASIL-D systems ready	AEC-Q100 grade 1 qualified
L9965P-FN-TR		
L99BM2P-FN-TR	-	-
L9965P-FP	Full ISO26262 compliant ASIL-D systems ready	AEC-Q100 grade 1 qualified
L9965P-FP-TR		
L99BM2P-FP-TR	-	-

Product labels



Features

- Very low power consumption:
  - Less than 10 µA in deep-sleep mode (only trigger detection enabled)
  - Less than 4 mA in low-power mode (trigger detection enabled, ER boost recharge active, cyclic diagnostics every 100 ms)
- Boost regulator to charge Energy Reserve (ER) with bang-bang control to reduce consumption
- FENH/FENL digital input triggers, compatible to level or PWM signals (16 kHz and 125 kHz), with line integrity check feature
- Autonomous cyclic diagnostic routine to ensure detection of all failures which may prevent safe deployment and/or cause inadvertent deployment
- Programmable deployment profile: current value and time duration can be adapted to different pyro-fuse igniters
- Firing strategy supporting multiple retry attempts based on user-selectable FIRE_GOOD signal
- Embedded NVM for configuration parameters storage and runtime configuration integrity check
- Easy integration with L9965C/L99BM2C companion CSA, implementing many of the safety mechanisms needed to achieve safety targets, thus allowing easy L9965P/L99BM2P plug and play in the system
- Pyro-fuse deployment available down to a minimum operating battery voltage of 6 V
- 24-bit peripheral SPI for direct MCU/L9965C/L99BM2C interface
- Compatible with pyro-fuses certified according LV-16 and USCAR-28

Application

- High voltage battery packs for BEVs and PHEVs
- Backup energy storage systems and UPS

Description

L9965P/L99BM2P is a single channel pyro-fuse driver capable to break high voltage battery busbar quickly and reliably in case of short circuit or car crash.

To accomplish this function, the device features a dual FET output stage made of a HS and a LS powerMOS. The stage is equipped with a closed loop current feedback and can be configured to deliver controlled firing profiles programming both current value and time duration.

Moreover, the power stage is able to perform a defined number of auto-retry attempts based on the success or not of the deployment.

The device embeds a programmable firing logic allowing to generate the trigger signal from two SPI commands or from two digital inputs (FENH/FENL).

The digital input triggers are compatible with both level and PWM encoding, supporting 16 kHz and 125 kHz encoded signals.

Product labels

The device supports the charging of an external capacitor to be used as tank capacitor or as energy reserve (ER) in case of battery loss. An internal boost regulator can be used to control the ER cap voltage around a programmable setpoint. Boosting the input battery voltage allows using smaller ER capacitor values to store the energy needed for firing, even in case of ECU battery loss.

The device has been designed to deliver maximum safety and performance while still being energy efficient. A low-power operation strategy allows minimizing the idle consumption, keeping the device in an ultra low power state while still performing all the diagnostic sweeps needed for achieving the safety targets. The periodicity of the diagnostic sweeps can be programmed in order to comply with any FTTI. During such ultra low power state, the device is still sensitive to wake-up/trigger sources in order to be ready to fire.

Operation in conjunction with L9965C/L99BM2C companion chip allows simplifying the software development, as many safety mechanisms are already implemented by L9965C/L99BM2C.

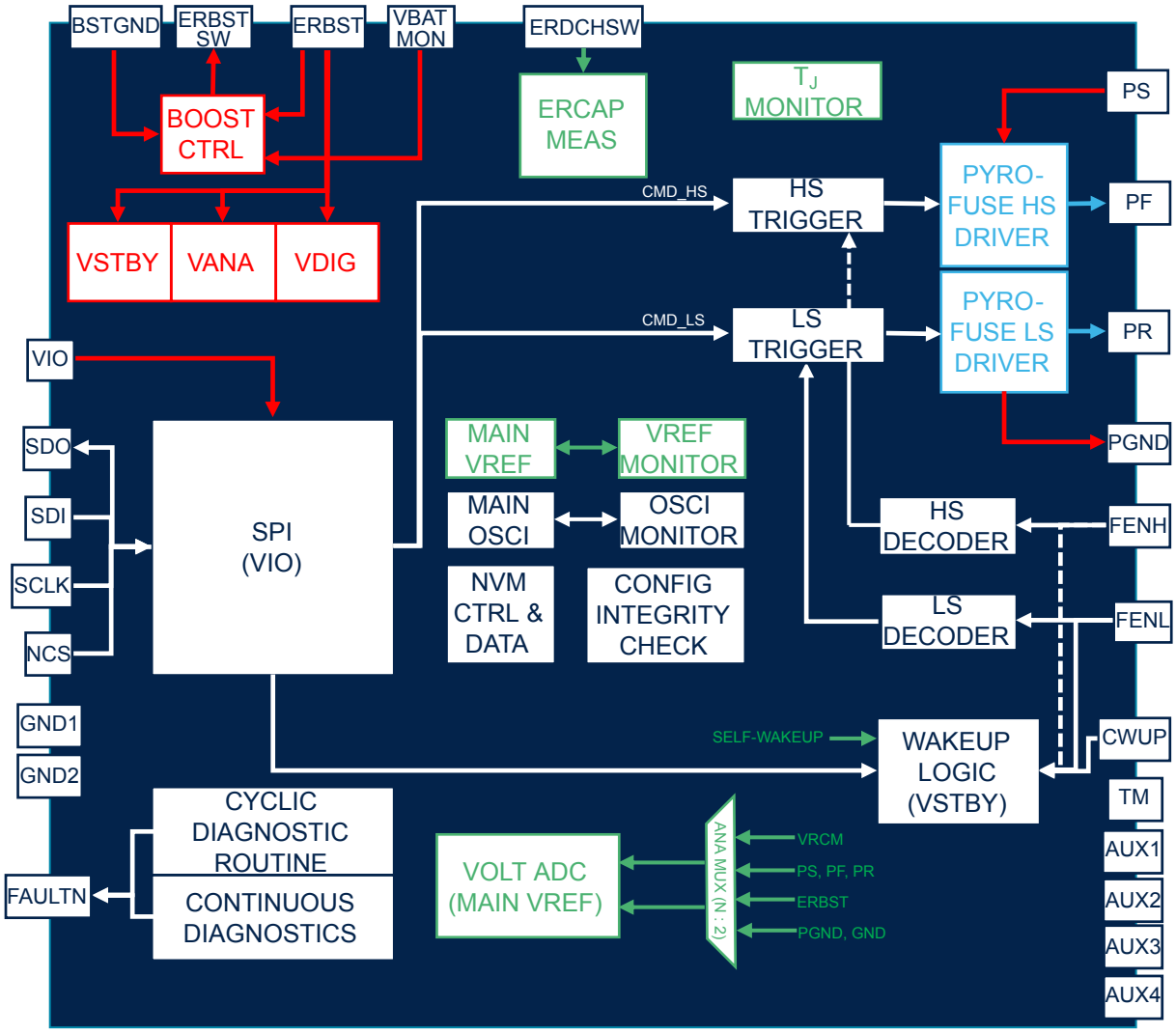
Product summary

Order code	Package	Packing	FuSa	Qualification
L9965P-FN	VFQFN32	Tray	Full ISO26262 compliant ASIL-D systems ready	AEC-Q100 grade 1 qualified
L9965P-FN-TR		Tape and reel		
L99BM2P-FN-TR	VFQFN32	Tape and reel	-	-
L9965P-FP	TQFP32L	Tray	Full ISO26262 compliant ASIL-D systems ready	AEC-Q100 grade 1 qualified
L9965P-FP-TR		Tape and reel		
L99BM2P-FP-TR	TQFP32L	Tape and reel	-	-

1 Block diagram and pin description

1.1 Block diagram

Figure 1. **Block diagram**



1.2 Pin description

Figure 2. Pinout (top view)

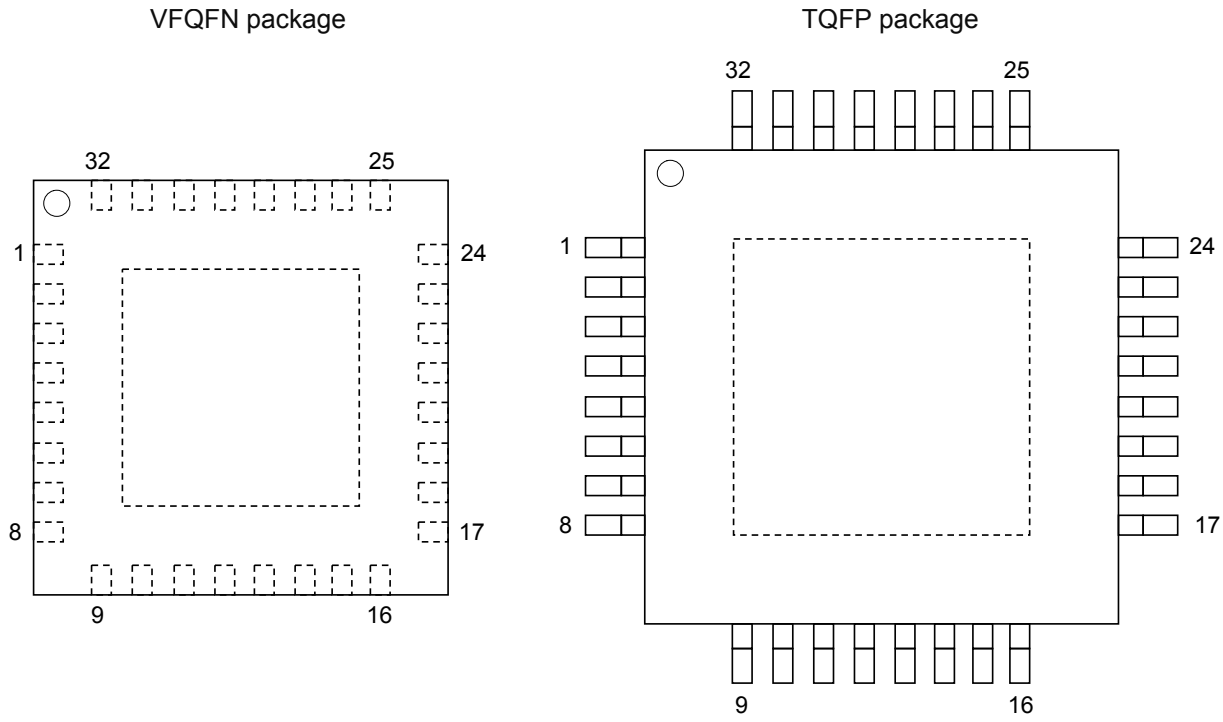


Table 1. Pin function

#	Name	Function	Internal PU/PD	Type
1	CWUP	Cyclic wake-up input	PD	Local
2	GND2	Ground pin	-	Global
3	FAULTN	Open-drain fault output pin	-	Local
4	AUX1	Short to ground in application	-	Local
5	NCS	SPI chip select	PU	Local
6	SCLK	SPI clock	PD	Local
7	SDI	SPI data in (MOSI)	PD	Local
8	SDO	SPI data out (MISO)	-	Local
9	VIO	Digital output buffer supply input	-	Local
10	AUX2	Short to ground in application	-	Local
11	TM	ST test mode pin, short to ground in application	PD	Local
12	GND1	Ground pin	-	Global
13	AUX3	Open in application	PD	Local
14	FENH	Fire enable high-side	PU/PD (configurable)	Local
15	AUX4	Open in application	PD	Local
16	FENL	Fire enable low-side	PU/PD (configurable)	Local
17	PGND	Pyro-fuse driver low-side ground	-	Local
18	NC	No connection	-	Local
19	PR	Pyro-fuse driver low-side output	-	Global
20	NC	No connection	-	Local
21	PF	Pyro-fuse driver high-side output	-	Global
22	NC	No connection	-	Local
23	PS	Pyro-fuse driver high-side supply	-	Global
24	NC	No connection	-	Local
25	ERDCHSW	Energy reserve discharge switch	-	Local
26	NC	No connection	-	Local
27	ERBST	Main supply/energy reserve boost output	-	Global
28	NC	No connection	-	Local
29	BSTGND	Energy reserve boost ground	-	Local
30	ERBSTSW	Energy reserve boost switching node	-	Local
31	NC	No connection	-	Local
32	VBATMON	Input battery monitor pin	-	Global
33	EP	Exposed pad: connect to GND	-	-

2 Product ratings

2.1 Thermal ratings

Table 2. Thermal ratings

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
T_{AMB}	Operating and testing temperature		-40	-	125	°C
T_J	Junction temperature for all parameters		-40	-	150	°C
T_{STG}	Storage temperature		-40	-	150	°C
$R_{TH\_ja,TQFP}$	Junction to ambient thermal resistance, TQFP32 package	According JEDEC standard on 2s2p PCB	-	29.4	-	°C/W
$R_{TH\_ja,QFN}$	Junction to ambient thermal resistance, VFQFN32 package	According JEDEC standard on 2s2p PCB	-	35	-	°C/W

2.2 Electrical ratings

The following section describes the different operational ranges.

For each device pin:

- **Operating range (OR)**: within this range functions operate as specified and without parameter deviations. All the device electrical parameters are tested and guaranteed in this range and are valid in the whole T_J operating range, unless otherwise specified.
- **Absolute maximum rating range (AMR)**: within this range functions may not operate properly. However, the IC will not be damaged. Exposure to AMR conditions for extended periods may affect device reliability. Exceeding any AMR may cause permanent damage to the integrated circuit.

Note:

- *Currents are noted with a positive sign when flowing into a pin.*
- *Integrated protections and diagnostics are designed to prevent device destruction under the fault conditions described in the specification. Fault conditions are considered to be out of normal operating range. Protection functions are not designed for continuous repetitive operation.*

Table 3. Pin electrical ratings

Parameter	Description	Test condition	AMR_{MIN}	OR_{MIN}	OR_{MAX}	AMR_{MAX}	Unit	Note
Power supply								
V_{VIO}	VIO: voltage range	vs. GNDx	-0.3	3	5.5	20	V	-
V_{ERBST}	ERBST: voltage range	vs. GNDx	-0.3	6	26	40	V	-
$V_{ERBSTSW}$	ERBSTSW: voltage range	vs. GNDx	-0.3	0	$V_{ERBST\_110}+V_{DFW}$	40	V	Only if ERBST used
$V_{ERDCHSW}$	ERDCHSW: voltage range	vs. GNDx	-0.3	6	V_{ERBST}	40	V	-
V_{PS}	PS: voltage range	vs. GNDx	-0.3	6	26	40	V	-
$V_{VBATMON}$	VBATMON: voltage range	vs. GNDx	-0.3	6	26	40	V	-
Ground								
V_{BSTGND}	BSTGND: voltage range	vs. GNDx	-0.3	-0.1	0.1	0.6	V	-
V_{PGND}	PGND: voltage range	vs. GNDx	-0.3	-0.1	0.1	0.6	V	-
SPI								
V_{NCS}	NCS: voltage range	vs. GNDx	-0.3	0	V_{VIO}	20	V	-
V_{SCLK}	SCLK: voltage range	vs. GNDx	-0.3	0	V_{VIO}	20	V	-
V_{SDI}	SDI: voltage range	vs. GNDx	-0.3	0	V_{VIO}	20	V	-
V_{SDO}	SDO: voltage range	vs. GNDx	-0.3	0	V_{VIO}	$V_{VIO}+0.3$	V	-
Pyro-fuse								
V_{FENx}	FENH,FENL: voltage range	vs. GNDx	-0.3	0	V_{VIO}	20	V	-
V_{PF}	PF: voltage range	vs. GNDx	-1	0	V_{PS}	$V_{PS}+0.3$	V	-
V_{PR}	PR: voltage range	vs. GNDx	-0.3	0	V_{PS}	35	V	-
Wake-up								
V_{CWUP}	CWUP: voltage range	vs. GNDx	-0.3	0	V_{VIO}	20	V	-
Fault								
V_{FAULTN}	FAULTN: voltage range	vs. GNDx	-0.3	0	V_{VIO}	20	V	-

2.2.1 Absolute maximum ratings

Table 4. **Absolute maximum ratings**

Symbol	Test condition	Min	Typ	Max	Unit
CWUP		-0.3	-	20	V
GND2	GND1, GND2 and EP in short to substrate	-	0	-	V
FAULTN		-0.3	-	20	V
AUX1		-0.3	-	20	V
NCS		-0.3	-	20	V
SCLK		-0.3	-	20	V
SDI		-0.3	-	20	V
SDO		-0.3	-	V_{VIO}+0.3	V
VIO		-0.3	-	20	V
AUX2		-0.3	-	20	V
TM		-0.3	-	20	V
GND1	GND1, GND2 and EP in short to substrate	-	0	-	V
AUX3		-0.3	-	20	V
FENH		-0.3	-	20	V
AUX4		-0.3	-	20	V
FENL		-0.3	-	20	V
PGND		-0.3	-	0.6	V
NC		-	-	-	
PR		-0.3	-	35	V
PF		-1	-	V_{PS}+0.3	V
PS		-0.3	-	40	V
ERDCHSW		-0.3	-	40	V
ERBST		-0.3	-	40	V
BSTGND		-0.3	-	0.6	V
ERBSTSW		-0.3	-	40	V
VBATMON		-0.3	-	40	V
EP	GND1, GND2 and EP in short to substrate	-	0	-	V

2.3 ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{ESD\_HBM\_GLOBAL}$	Human body model	Global pins are connected at ground_all except global pin under test (ground_all = all ground pins connected together).	-4	-	4	kV	-
$V_{ESD\_HBM\_LOCAL}$	Human body model	Local pins, test done according to AEC-Q100-002.	-2	-	2	kV	Class C2
$V_{ESD\_CDM\_LATERAL}$	Charged device model	Test done according to AEC-Q100-011	-500	-	500	V	Class C3
$V_{ESD\_CDM\_CORNER}$	Charged device model for corner pins	Test done according to AEC-Q100-011	-750	-	750	V	Class C4
I_{LATCH_UP}	Latch up current test	Test done according to AEC-Q100-004	-100	-	100	mA	-

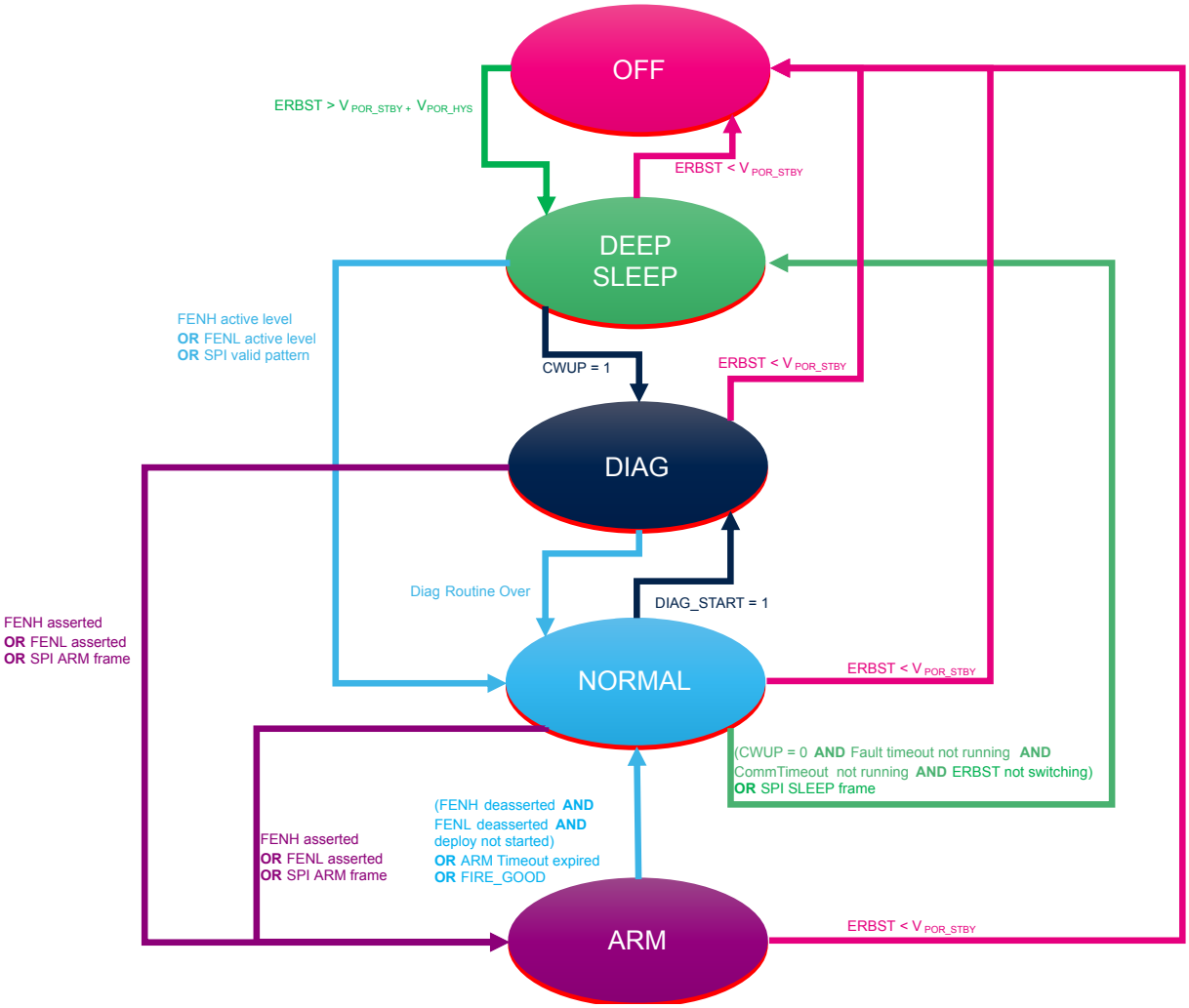
3 Functional description

In the following paragraphs all the bits in ***bold*** are located in the NVM and are protected by lock to avoid unwanted modification (see the Section 3.15: Configuration Lock).

3.1 Device functional states (FSM)

The L9965P/L99BM2P operates according to the FSM shown in the Figure 3.

Figure 3. Device FSM



The Table 6 summarizes the FSM behavior, describing the transitions and the resources active in each operating state.

Table 6. Device FSM

State	Purpose	Reached from	Condition	Active resources
OFF	Device OFF	Any state	When the ERBST voltage falls below the V_{POR_TH} threshold	None
DEEP-SLEEP	Ultralow power state for managing long inactivity periods or implementing low-power strategies	NORMAL	When CWUP is low, fault timeout ($t_{FAULT\_HANDLING\_TIMEOUT}$) is expired, the SPI communication timeout ($t_{SPI\_COMM\_TIMEOUT}$) is expired and ERBST is not working (ER CAP charged) **OR** SPI SLEEP frames	Wake-up from cyclic wake-up pin (CWUP) Wake-up via peripheral SPI Wake-up from fire enable inputs (FENH/FENL)
		OFF	When ERBST voltage rises above the V_{POR_TH} threshold	Wake-up from cyclic wake-up pin (CWUP) Wake-up via peripheral SPI
DIAG	Diagnostic state	DEEP-SLEEP	When CWUP is asserted	All resources are active in NORMALAdditionally, all the resources needed to perform the diagnostic routine
		NORMAL	When commanded via SPI	
NORMAL	Normal operating state	DEEP-SLEEP	Wake-up from any of the enabled sources (FENH or FENL or SPI valid pattern)	All resources are active, except the ones needed to perform the diagnostic routine
		ARM	All the enabled deploy conditions (FENH and FENL) are deasserted **OR** Arming timeout (corresponding to deployment time) expired **OR** FIRE_GOOD	
		DIAG	Diagnostic routine over	
ARM	Prepare to deploy	NORMAL or DIAG	At least one deploy condition asserted between FENH, FENL or SPI ARM frame	All resources active in NORMAL, except the ones needed to perform the diagnostic routine

3.1.1 SPI SLEEP commands

To force the device to go in a DEEP-SLEEP state, the following procedure shall be implemented:

1. MCU writes 0x77 into the SPECIAL_KEY register to enter partial go-to-sleep;
2. MCU writes 0xCC into the SPECIAL_KEY register to confirm go-to-sleep.

3.1.2 Diagnostics summary

This section describes in detail the enable/masking of all the diagnostic features implemented in the device, according to the functional state.

Note: Many diagnostics may be subject to user-defined configurations and/or enable. The following table assumes that all diagnostics have been enabled in the device configuration.

Table 7. Diagnostics summary

State	ERBST OV	PS UV/OV	FENx decoder diag	Deployment autoretry	Diag routine	Oscillator monitor	Reference monitor	GND loss	Config integrity check
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DEEP-SLEEP	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DIAG	AON	AON	AON	OFF	OD/CYC	AON	AON	AON	AON
NORMAL	AON	AON	AON	OFF	OFF	AON	AON	AON	AON
ARM	AON	AON	AON	AON	OFF	AON	AON	AON	AON

Note:

- *AON → Diagnostic always-on and running*
- *OD → Diagnostic available on-demand*
- *CYC → Diagnostic cyclically activated by internal timer*
- *OFF → Diagnostic disabled/masked*

3.2 Power management

The IC is supplied by ERBST pin, which is then used to generate all the internal regulated supplies.

The IC is usually supplied by an isolated DC/DC converter feeding from the 12 V LV supply (reinforced isolation); alternatively by an isolated DC/DC converter from the HV battery pack.

3.2.1 Power management electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 8. Device current consumption

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{POR_TH}	POR threshold (sensed on ERBST pin)		-	-	4.7	V
I_{BASE_SLP0}	Base current consumption of the device in DEEP-SLEEP state (from VBATMON, ERBSTSW, ERBST, ERDCHSW and PS)	-40 °C ≤ T_{amb} ≤ +85 °C DEEP-SLEEP	-	-	10	µA
I_{BASE_SLP1}	Base current consumption of the device in DEEP-SLEEP state (from VBATMON, ERBSTSW, ERBST, ERDCHSW and PS)	+85 °C ≤ T_{amb} ≤ +125 °C +85 °C ≤ T_J ≤ +125 °C DEEP-SLEEP	-	-	15	µA
I_{BASE_NORM}	Base current consumption of the device in NORMAL state with all resources enabled (from VBATMON, ERBSTSW, ERBST, ERDCHSW and PS)	NORMAL	-	-	2.4	mA
I_{BASE_DIAG}	Base current consumption of the device in DIAG state with all resources enabled (from VBATMON, ERBSTSW, ERBST, ERDCHSW and PS)	DIAG with no diagnostics active	-	-	2.4	mA
I_{DELTA_BOOST}	Delta current when the boost controller is in the duty-phase	NORMAL, DIAG, ARM, boost charging the ER cap (excluding boost charging current)	-	-	7.5	mA
I_{DELTA_ADC}	Delta current when the voltage ADC is enabled and continuously converting	NORMAL, ADC continuously converting for on-demand conversions	-	-	3.5	mA
$I_{DELTA\_ACT\_PD\_PR}$	Delta current when the PR active pull-down is enabled	NORMAL, PR pull-down enabled	-	-	0.2	mA
I_{DELTA_SS}	Delta current when the spread spectrum is enabled	NORMAL, spread spectrum enabled	-	-	0.06	mA
I_{DELTA_NVM}	Delta current when the NVM is downloaded	NORMAL, NVM download	-	-	1	mA
I_{DELTA_ABIST}	Delta current when the ABIST is running	DIAG, ABIST continuously running	-	-	0.6	mA
I_{DELTA_HWSC}	Delta current from ERBST when the HWSC is running	DIAG, HSWC continuously running	-	-	3.5	mA
$I_{DELTA\_VRCM\_CHECK}$	Delta current when the VRCM check is running	DIAG, VRCM check continuously running (excluding diagnostic currents)	-	-	4.2	mA
$I_{DELTA\_PYRO\_LEAK\_TEST}$	Delta current when the pyro outputs leakage test is running	DIAG, pyro outputs leakage test continuously running	-	-	3.5	mA
$I_{DELTA\_RES\_MEAS}$	Delta current when the pyro igniter resistance measurement is running	DIAG, Pyro igniter resistance measurement continuously running (excluding diagnostic currents)	-	-	4.5	mA
$I_{DELTA\_FET\_TEST}$	Delta current when the FETs test is running	DIAG, Pyro deployment FETs test continuously running (excluding diagnostic currents)	-	-	3.5	mA
$I_{DELTA\_ER\_CAP\_DIAG}$	Delta current when the ER capacitor diagnostic is running	DIAG, ER capacitor diagnostic continuously running (excluding diagnostic current sunk from ERDCHSW)	-	-	2.5	mA
I_{VIO_BASE}	Base current consumption from VIO pin	DEEP-SLEEP, SDO in HiZ	-	-	1	µA
I_{VIO_DELTA}	Delta current consumption from VIO pin with activity on FAULTN and SDO	NORMAL, DIAG, ARM	-	-	500	µA

3.3 Power supply section

3.3.1 Main supply (ERBST)

The ERBST pin is the main supply. This line:

- Feeds the internal VANA LDO used for biasing the analog circuitry.
- Feeds the internal VDIG LDO used for biasing the digital circuitry.
- Feeds the internal VSTBY LDO used for biasing the circuitry in DEEP-SLEEP.

The boost regulator is disabled by default and can be enabled via NVM setting the ***ERBST_EN*** bit to 1. Once the boost regulator is enabled via NVM, it can be turned-off via the ERBST_DIS bit.

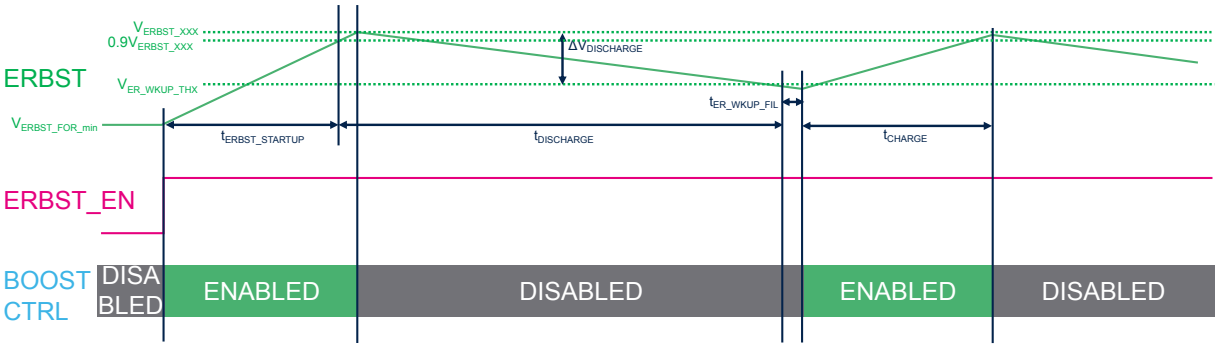
Once $V_{ERBST} > V_{VBATMON} - V_{ERBST\_DIS}$ for $t > t_{ERBST\_READY\_FLT}$, the initial charge phase is over, the ERBST_RDY bit in the ERBOOST register is set to 1 and the switching operation starts. This ensures the presence of the external diode between VBATMON pin and ERBST pin. If $V_{ERBST} < V_{VBATMON} - V_{ERBST\_DIS}$ after $t_{ERBST\_READY\_FLT}$, the ERBST regulator is turned-off and the ERBST_RDY bit is set to 0.

Once started, the boost operates according to a bang-bang strategy, as shown in the Figure 4:

- The controller is enabled and boosts the battery voltage whenever V_{ERBST} falls below the $V_{ER\_WKUP\_THX}$ voltage programmed in the ***VER_WKUP_TH*** bit field for an interval longer than $t_{ER\_WKUP\_FLT}$. While in the duty phase, the IC is kept in NORMAL and any transition to DEEP-SLEEP is delayed until the setpoint has been reached.
- The controller is disabled whenever V_{ERBST} reaches the target V_{ERBST_XXX} setpoint.

This strategy guarantees high energy efficiency meantime the ER cap voltage is always charged for firing the pyro-fuse. In fact, considering the typical range for C_{ERBST} capacitor, the boost controller spends most of the time in the disabled state.

Figure 4. ERBST controller working principle



To allow quick charging of the ER cap at every system startup, the boost controller has been designed to guarantee a maximum $t_{ERBST\_STARTUP}$ startup time in the worst-case application scenario.

Moreover, the controller has been designed to limit the maximum power consumption to P_{IN_ERBST}. It is possible to enable this function through the ***PIN_LIMIT*** bit in NVM.

Note: In applications where the power limitation is required, to limit the initial inrush current it is possible to mount the resistor R_{CHG} between the VBATMON pin and the ERBST inductor L_{ERBST}. Once the initial charge phase has finished ($V_{ERBST} > V_{VBATMON} - V_{ERBST\_DIS}$), the ERBST_RDY bit is set to 1. The MCU can read this flag and drive a GPIO to short the resistor R_{CHG}.

It is possible to kept disabled the ERBST regulator setting ERBST_DIS=1 in the ERBOOST register.

3.3.1.1 ERBST diagnostics

Table 9. ERBST diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
ERBST UV	If the V_{ERBST} voltage falls below $V_{ERBST\_UV\_TH}$ for an interval longer than $t_{ERBST\_UV\_FLT}$ the ERBST UV fault is acknowledged	The ERBST_UV flag is set FAULTN line is asserted The “fire inhibit” signal is set	If the V_{ERBST} voltage rises above $V_{ERBST\_UV\_TH}$ + $V_{ERBST\_UV\_HYS}$, the fault flag can be cleared by MCU	FAULTN line is released Pyro-fuse fire is possible again	Non-maskable
ERBST OV	If the V_{ERBST} voltage rises above $V_{ERBST\_OV\_TH}$ for an interval longer than $t_{ERBST\_OV\_FLT}$ the ERBST OV fault is acknowledged	The ERBST_OV flag is set FAULTN line is asserted The ERBST is turned OFF The “fire inhibit” signal is set	If the V_{ERBST} voltage drops below $V_{ERBST\_OV\_TH}$ - $V_{ERBST\_OV\_HYS}$, the fault flag can be cleared by MCU	FAULTN line is released Pyro-fuse fire is possible again	***ERBST_OV_FAULTN_MSK*** masks fault redirection on FAULTN pin ***ERBST_OV_FIRE_MSK*** masks the inhibition of pyro-fuse fire commands
ERBSTSW OC	If the ERBSTSW current raises above I_{ERBST_OC} for $N_{ERBST\_OC\_COUNT}$ times the ERBST OC fault is acknowledged	The ERBST_OC flag is set FAULTN line is asserted The ERBST is turned OFF	Power cycle (CWUP toggle) is needed to restart again	None	***ERBSTSW_OC_FAULTN_MSK*** masks fault redirection on FAULTN pin
ERBSTSW OT	If the ERSBSTW driver temperature exceeds $T_{ERBSTSW\_SD}$ for an interval longer than $t_{ERBSTSW\_SD\_FLT}$ the ERBST OT fault is acknowledged	The ERBST_OT flag is set FAULTN line is asserted The ERBST is turned OFF	If the ERBSTSW driver temperature drops below $T_{ERBSTSW\_SD}$ - $T_{ERBSTSW\_SD\_HYS}$, the fault flag can be cleared by MCU	ERBST re-enabled FAULTN line is released	***ERBSTSW_OT_FAULTN_MSK*** masks fault redirection on FAULTN pin
ERBST diode loss	If $V_{ERBSTSW}$-V_{ERBST} voltage rises above the $V_{ERBST\_DLOSS\_TH}$ threshold for $N_{ERBST\_DLOSS\_COUNT}$ times, the external diode loss failure is acknowledged	The ERBST_DLOSS flag is set FAULTN line is asserted The ERBST is turned OFF The ERBSTSW clamping voltage is activated, limiting the voltage value to $V_{ERBSTSW\_CLAMP}$	Power cycle (CWUP toggle) is needed to restart again	None	***ERBST_DLOSS_FAULTN_MSK*** masks fault redirection on FAULTN pin
BSTGND loss	See the Section 3.13: Ground loss monitor (GNDMON)	See the Section 3.13: Ground loss monitor (GNDMON)	See the Section 3.13: Ground loss monitor (GNDMON)	See the Section 3.13: Ground loss monitor (GNDMON)	See the Section 3.13: Ground loss monitor (GNDMON)

3.3.1.2 ERBST electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 10. ERBST supply electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$V_{ERBST\_UV\_TH}$	ERBST undervoltage threshold	Max slew rate = 2.3 V/ms	4.7	-	5.3	V	ERBST
$V_{ERBST\_UV\_HYS}$	ERBST undervoltage hysteresis	Max slew rate = 2.3 V/ms	50	-	150	mV	ERBST
$t_{ERBST\_UV\_FLT}$	ERBST undervoltage filter time	Tested by SCAN	7	9	11	us	ERBST
$V_{ERBST\_OV\_TH}$	ERBST overvoltage threshold	Considering max nom value of 26 V + 5%, max slew rate = 2.3 V/ms	27.4	-	31.1	V	ERBST

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$V_{ERBST\_OV\_HYS}$	ERBST overvoltage hysteresis	Max slew rate = 2.3 V/ms	150	-	250	mV	ERBST
$t_{ERBST\_OV\_FLT}$	ERBST overvoltage filter time	Tested by SCAN	17	20	21	us	ERBST
V_{ERBST_000}	ERBST regulated voltage	***ERBST_SET*** = 000 All operating lines and loads	16.92	18	19.08	V	ERBST
V_{ERBST_001}		***ERBST_SET*** = 001 All operating lines and loads	17.86	19	20.14	V	ERBST
V_{ERBST_010}		***ERBST_SET*** = 010 All operating lines and loads	18.80	20	21.20	V	ERBST
V_{ERBST_011}		***ERBST_SET*** = 011 All operating lines and loads	19.74	21	22.26	V	ERBST
V_{ERBST_100}		***ERBST_SET*** = 100 All operating lines and loads	20.68	22	23.32	V	ERBST
V_{ERBST_101}		***ERBST_SET*** = 101 All operating lines and loads	21.62	23	24.38	V	ERBST
V_{ERBST_110}		***ERBST_SET*** = 110 All operating lines and loads	22.56	24	25.44	V	ERBST
V_{ERBST_111}		***ERBST_SET*** = 111 All operating lines and loads	NA	NA	NA	V	ERBST
$V_{ER\_WKUP\_TH0}$	ERBST cap discharge threshold (in tracking with V_{ERBST_XXX} setpoint)	***VER_WKUP_TH*** = 000	15.04	16	16.96	V	ERBST
$V_{ER\_WKUP\_TH1}$		***VER_WKUP_TH*** = 001	15.98	17	18.02	V	ERBST
$V_{ER\_WKUP\_TH2}$		***VER_WKUP_TH*** = 010	16.92	18	19.08	V	ERBST
$V_{ER\_WKUP\_TH3}$		***VER_WKUP_TH*** = 011	17.86	19	20.14	V	ERBST
$V_{ER\_WKUP\_TH4}$		***VER_WKUP_TH*** = 100	18.80	20	21.20	V	ERBST
$V_{ER\_WKUP\_TH5}$		***VER_WKUP_TH*** = 101	19.74	21	22.26	V	ERBST
$V_{ER\_WKUP\_TH6}$		***VER_WKUP_TH*** = 110	20.68	22	23.32	V	ERBST
$V_{ER\_WKUP\_TH7}$		***VER_WKUP_TH*** = 111	NA	NA	NA	V	ERBST
$t_{ERBST\_WKUP\_FLT}$	ERBST discharge comparator deglitch	Guaranteed by SCAN	17	20	21	µs	ERBST
P_{IN_ERBST}	Boost input peak power	Input power limitation to guarantee $t_{ERBST\_STARTUP}$ in V_{IN} = 6 V to 18 V range	1.8	-	2.6	W	ERBST
η_{ERBST}	Boost efficiency	$P_{IN\_ERBST} = P_{IN\_ERBSTmax}$ V_{IN} = 6 V Guaranteed by design	0.6	-	-	W/W	ERBST, ERBSTSW
f_{ERBST}	Switching frequency	Design info, taking in consideration temperature and external competent variations	1.6	-	2.4	MHz	ERBST
$t_{ERBST\_ON\_MIN}$	Minimum ON-time	Design info		80	-	ns	ERBSTSW
C_{ERBST}	External output capacitor	Application info, including component tolerance	0.1	-	1.2	mF	ERBST
C_{ERBST_ESR}	External output capacitor ESR	Application info, including component tolerance	100	-	500	mΩ	ERBST

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
L_{ERBST}	External output inductor	I_{SAT} >> $I_{ERBST\_PEAK\_LIM}$ Application info	-20%	33	+20%	µH	ERBST
L_{ERBST_DCR}	External inductor DCR	Application info		-	1.5	Ω	ERBST
V_{DFW}	External diode forward voltage	Application info		-	1.2	V	ERBST
V_{ERBST_DIS}	ERBST disable threshold during power-up	Voltage difference between VBATMON pin and ERBST pin	1.5	2.2	2.7	V	VBATMON, ERBST
$t_{ERBST\_READY\_FLT}$	ERBST ready filter time	Tested by SCAN	10	20	25	µs	VBATMON, ERBST
$t_{ERBST\_STARTUP}$	ERBST startup time	From V_{ERBST} = 5.3 V to 90% of V_{ERBST_110} C_{ERBST} = $C_{ERBSTmax}$ V_{IN} = 6 V		-	220	ms	ERBST
$T_{ERBSTSW\_SD}$	Thermal shutdown threshold	Guaranteed by design	150	-	190	°C	ERBST
$T_{ERBSTSW\_SD\_HYS}$	Thermal shutdown threshold hysteresis	Guaranteed by design	5	-	15	°C	ERBST
$t_{ERBST\_SD\_FLT}$	Thermal shutdown filter time	Guaranteed by design	7	8.5	10	µs	ERBST
$I_{ERBST\_PEAK\_LIM\_0}$	ERBSTSW peak current limitation	***PIN_LIMIT*** = 0	330	-	480	mA	ERBSTSW
$I_{ERBST\_PEAK\_LIM\_1}$	ERBSTSW peak current limitation	***PIN_LIMIT*** = 1 V_{IN} = 6 V	300	-	440	mA	ERBSTSW
I_{ERBST_OC}	ERBSTSW overcurrent threshold		460	-	700	mA	ERBSTSW
$N_{ERBST\_OC\_COUNT}$	Number of counts before turn-off	Overcurrent events	-	5	-	#	ERBSTSW
$R_{DSON\_ERBSTSW}$	Boost switch ON resistance		-	-	1	Ω	ERBSTSW
$V_{ERBST\_DLOSS\_TH}$	ERBST diode loss detection threshold	Voltage difference between ERBSTSW pin and ERBST pin	2.3	3.3	4.0	V	ERBST, ERBSTSW
$V_{ERBSTSW\_CLAMP}$	ERBSTSW pin clamping voltage	Diode loss	33	-	40	V	ERBSTSW
$N_{ERBST\_DLOSS\_COUNT}$	Number of counts before turn-off	Diode loss clamping events	-	3	-	#	ERBSTSW
$t_{RISE\_ERBSTSW}$	ERBSTSW rise time	From 10% to 90% of $V_{ERBSTSW\_max}$ Min $I_{ERDCHSW}$ peak current Application info	-	-	15	ns	ERBSTSW
$t_{FALL\_ERBSTSW}$	ERBSTSW fall time	From 90% to 10% of $V_{ERBSTSW\_max}$ Max $I_{ERDCHSW}$ peak current Application info	-	-	20	ns	ERBSTSW

3.3.2 Power stage supply (PS)

The PS pin is the power stage supply input. This line:

- Feeds the level shifters between the **signal stage** and the **power stage**.
- Feeds the HS circuitry of the **power stage**.

3.3.2.1 PS diagnostics

Table 11. PS diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
PS UV	If the V_{PS} voltage falls below $V_{PS\_UV\_TH}$, the PS_UV fault is acknowledged	The PS_UV flag is set FAULTN line is asserted The “fire inhibit” signal is set	If the V_{PS} voltage rises above $V_{PS\_UV\_TH}$ + $V_{PS\_UV\_HYS}$, the PS_UV flag can be cleared by MCU	FAULTN line is released Pyro-fuse fire is possible again	Non-maskable
PS OV	If the V_{PS} voltage rises above $V_{PS\_OV\_TH}$, the PS_OV fault is acknowledged	The PS_OV flag is set FAULTN line is asserted The “fire inhibit” signal is set	If the V_{PS} voltage drops below $V_{PS\_OV\_TH}$ - $V_{PS\_OV\_HYS}$, the PS_OV flag can be cleared by MCU	FAULTN line is released Pyro-fuse fire is possible again	***PS_OV_FAULTN_MSK*** masks fault redirection on FAULTN pin PS_OV_FIRE_MSK masks the inhibition of pyro-fuse fire commands

3.3.2.2 PS electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 12. PS supply electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$V_{PS\_UV\_TH}$	PS undervoltage threshold	Max slew rate = 2.3 V/ms	4.7	-	5.3	V	PS
$V_{PS\_UV\_HYS}$	PS undervoltage hysteresis	Max slew rate = 2.3 V/ms	150	-	250	mV	PS
$t_{PS\_UV\_FLT}$	PS undervoltage filter time	Tested by SCAN	17	20	21	µs	PS
$V_{PS\_OV\_TH}$	PS overvoltage threshold	Considering max nom value of 26 V + 5% Max slew rate = 2.3 V/ms	27.4	-	31.1	V	PS
$V_{PS\_OV\_HYS}$	PS overvoltage hysteresis	Max slew rate = 2.3 V/ms	150	-	250	mV	PS
$t_{PS\_OV\_FLT}$	PS overvoltage filter time	Tested by SCAN	17	20	21	µs	PS

3.3.3 IO output buffer supply (VIO)

The VIO pin is the digital output buffer supply. This line feeds the SDO output buffer. It is suggested to add a bypass ceramic capacitor near the VIO pin.

The VIO shall be supplied externally and it enables compatibility with both 3.3 V and 5 V controllers.

There is no diagnostic on the VIO supply.

3.4 Wake-up sources

The following section lists the available wake-up sources and their behavior.

Whenever a wake-up source is validated, the wake-up sequence is initiated and shall successfully end within $t_{WAKEUP\_TIMEOUT}$. Otherwise, the IC returns to the previously held low power state.

Table 13. Wake-up sources electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$t_{WAKEUP\_TIMEOUT}$	Timeout for completing the wake-up sequence	Tested by SCAN	20	-	25	ms	CWUP, FENH, FENL, SPI

3.4.1 Wake-up from cyclic wake-up pin (CWUP)

The CWUP pin can be used by the host controller for the following purposes:

- Triggering cyclic wakeups and diagnostics in low-power strategies.
- Keep the device constantly in NORMAL state in full-power strategies.

When the CWUP pin is set high for longer than $t_{CWUP\_POWERUP\_PULSE}$ (t_{CWUP_FLT} filter time is applied), a wake-up condition is acknowledged and latched in the CWUP_WAKEUP bit in INTERNAL_STATUS register. The IC completes the power-up phase after $t_{CWUP\_POWERUP\_TIME}$ since the CWUP signal is set high.

This wake-up source is always available.

3.4.1.1 CWUP electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 14. CWUP electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
t_{CWUP_FLT}	CWUP filter time	Input filter time, guaranteed by design	250	-	800	ns	CWUP
$t_{CWUP\_POWERUP\_PULSE}$	CWUP min input pulse to start power-up	Minimum time to guarantee a correct power-up (starting from the CWUP low to high transition)	100	-	-	µs	CWUP
$t_{CWUP\_POWERUP\_TIME}$	IC wake-up latency	From the CWUP low to high transition to the IC in DIAG (full download of NVM)	-	-	1	ms	CWUP

3.4.2 Wake-up from fire enable inputs (FENH/FENL)

In DEEP-SLEEP state the IC is still responsive to FENH/FENL inputs in order to quickly wake-up and be ready to fire when required.

When either FENH/FENL pin holds the active level for longer than t_{FENx_FLT}, a wake-up condition is acknowledged and latched in the FENX_WAKEUP bit in the INTERNAL_STATUS register.

If active level of FENH and FENL pins disappears after wake-up trigger, the IC remains in NORMAL state for $t_{FENx\_WAKEUP\_WAIT}$ before returning in DEEP-SLEEP state.

These wake-up sources can be enabled setting ***FENH_EN*** = 1 and ***FENL_EN*** = 1 in NVM.

The active levels can also be programmed through ***FENH_LEVEL*** and ***FENL_LEVEL***.

Note: In order to speed up the wake-up procedure, when the device is awakened by FENH/FENL pin, NVM operations are locked (neither download nor upload). A transition to DEEP-SLEEP is needed to unlock NVM.

3.4.2.1 FENH/FENL wake-up electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 15. Wake-up sources electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
t_{FENx_FLT}	FENH, FENL input filter	Analog filter, guaranteed by design	250	-	800	ns	FENH, FENL
$t_{FENx\_WAKEUP\_TIME}$	IC wake-up latency	From the FENH/FENL assertion to the IC in ARM state (no NVM download)	-	-	400	µs	FENH, FENL
$t_{FENx\_WAKEUP\_WAIT}$	IC wake-up wait	From the FENH/FENL assertion to the IC return in DEEP-SLEEP state	1.8	2	2.1	ms	FENH, FENL

3.4.3 Wake-up via peripheral SPI

The IC can be woken up by any valid SPI frame. A wake-up condition is acknowledged when the following pattern is received:

1. A NCS high to low transition
2. 24 SCK pulses
3. A NCS low to high transition

To prevent the logic being stuck in the wake-up detection state upon incomplete patterns, the $t_{SPI\_WAKEUP\_TIMEOUT}$ is started upon every NCS assertion, and the wake-up pattern shall end before timeout expiration, otherwise it is discarded.

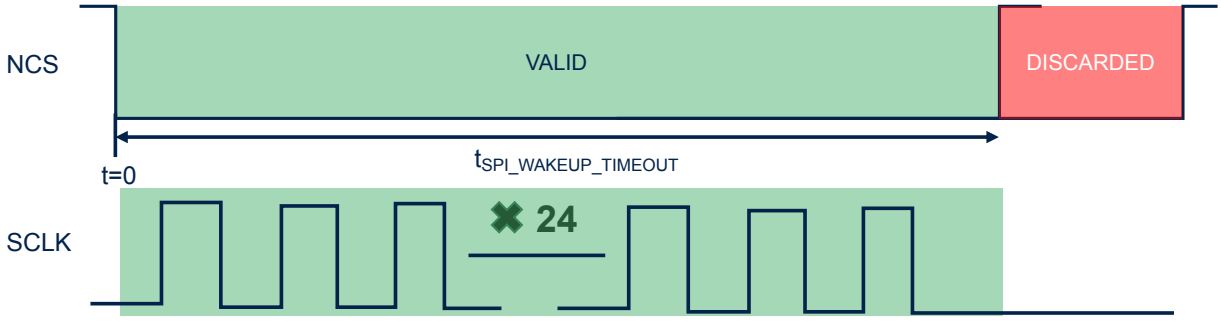
Wake-up frames are not decoded, so their content may be arbitrary.

Note: It is strongly recommended to send READ commands to avoid inadvertent write operations in case the device is already awake.

When a correct wake-up sequence is acknowledged, the event is latched in the SPI_WAKEUP bit located in the INTERNAL_STATUS register. The latch-set pulse also triggers the start of the $t_{SPI\_COMM\_TIMEOUT}$ communication timeout. Such a timer is intended to avoid the IC being left unintendedly in a high consumption power state in case the controller is unresponsive:

- The $t_{SPI\_COMM\_TIMEOUT}$ is reset and restarted in case a valid frame is received (no CRC error and correct number of SCK pulses).
- The $t_{SPI\_COMM\_TIMEOUT}$ is reset and stopped in case a high level is detected on CWUP. From that moment on, moving the device to a low power state requires setting CWUP low.

Figure 5. Wake-up condition by peripheral SPI



3.4.3.1 *SPI wake-up electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 16. SPI electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$t_{SPI\_WAKEUP\_TIMEOUT}$	Timeout for receive of wake-up frame	Guaranteed by SCAN	0.4	-	2	ms	NCS, SDI, SDO, SCLK
$t_{SPI\_COMM\_TIMEOUT}$	Communication timeout started in case of wake-up via peripheral SPI	Guaranteed by SCAN	-	2	-	s	NCS, SDI, SDO, SCLK
$t_{SPI\_WAKEUP\_TIME}$	IC wake-up latency	From the NCS low to high transition to the IC in NORMAL (full NVM download)	-	-	1	ms	NCS, SDI, SDO, SCLK

3.5 Fault notification (FAULTN)

Detected faults are reported via SPI by the FAULTN_ECHO bit of the GSW. The FAULTN_ECHO bit being set to '1' indicates the IC has not detected a failure.

Additionally, the fault status can also be reported by the FAULTN output, which can be disabled by setting ***FAULTN_DIS*** = 1 in NVM.

Whenever a fault condition is detected, the open-drain FAULTN output is asserted low. The output is released when every latched fault has been cleared.

Depending on the IC configuration, some diagnostics can be masked and their redirection onto FAULTN line can also be masked. Refer to the diagnostic tables for the specific masking conditions.

Whenever a fault is asserted and the CWUP input level is low, the $t_{FAULT\_HANDLING\_TIMEOUT}$ is released and runs in background. The timeout is reset by the CWUP high level: if the host controller does not raise CWUP before the timeout expires, the IC moves back to DEEP-SLEEP. If a fault occurs when the CWUP input level is high and it is still present when the CWUP input level is set low, the $t_{FAULT\_HANDLING\_TIMEOUT}$ does not start.

3.5.1 FAULTN integrity check

To enable reaching the safety targets at system level, the IC provides a means to periodically verify the integrity of the FAULTN line. Depending on the power management strategy, different configurations may apply, as reported in the Table 17.

Table 17. FAULTN configuration according to different power management strategies

Power management strategy	L9965C/ L99BM2C state	L9965P/ L99BM2P state	CWUP	FAULTN	Configuration	Note
Full power	NORMAL	NORMAL	Static high	Pulse generation every t_{FAULTN_PERIOD}	***FAULTN_DIS*** = 0 FAULTN_CYCLIC_PULSE = 1	The FAULTN path is continuously checked, allowing quick detection of line stuck failures
Full power	NORMAL	NORMAL	Static high	Level mode	***FAULTN_DIS*** = 0 FAULTN_CYCLIC_PULSE = 0	The FAULTN output integrity can only be verified manually using the FAULTN_FORCE command
Low power	NORMAL	CYCLIC WAKEUP (alternation between DEEP-SLEEP and DIAG)	Cyclic high pulse generated by L9965C/ L99BM2C or MCU	Pulse generation every t_{CWUP_PERIOD}	***FAULTN_DIS*** = 0 FAULTN_CYCLIC_PULSE = 0	The FAULTN path is checked at each cyclic wake-up event: FAULTN low pulses are synchronized to received CWUP pulses

FAULTN_FORCE should be used only with FAULTN_CYCLIC_PULSE = 0. If used with FAULTN_CYCLIC_PULSE = 1, it is a fault injection.

When enabled, the integrity check can be executed:

- Continuously in full power mode (refer to the Figure 6)
  - This diagnostic requires FAULTN_CYCLIC_PULSE = 1. Pulse generation starts t_{FAULTN_PERIOD} after such a bit is written high (see the Figure 7).
  - If a failure occurs and FAULTN is held active low for fault signaling, the t_{FAULTN_PERIOD} timer is kept under reset. It restarts once all faults have been cleared and FAULTN returns to its inactive high state.
- Manually
  - Setting FAULTN_FORCE = 1 forces the FAULTN output low, instead setting FAULTN_FORCE = 0 releases the output. The FAULTN_FORCE command overrides any other FAULTN output buffer driving signal.
  - This strategy is recommended when multiple L9965P/L99BM2P are present in the system and their FAULTN outputs are connected in wired-OR.

- Once per cycle in low power mode (refer to the Figure 8 and Figure 9)
  - At each CWUP rising edge, the L9965P/L99BM2P starts its cyclic wake-up.
  - Once awake, the L9965P/L99BM2P generates a negative pulse lasting t_{FAULTN_PULSE} on the FAULTN output line.
  - This diagnostic does not require the use of the FAULTN_CYCLIC_PULSE bit since the FAULTN pin is automatically checked at each wake-up cycle.

Figure 6. FAULTN integrity check in full power mode

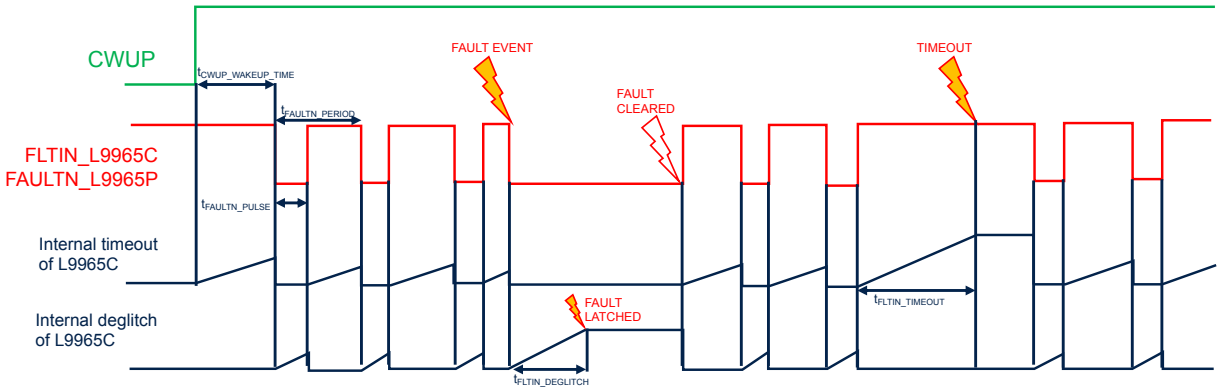


Figure 7. FAULTN cyclic pulse generation start

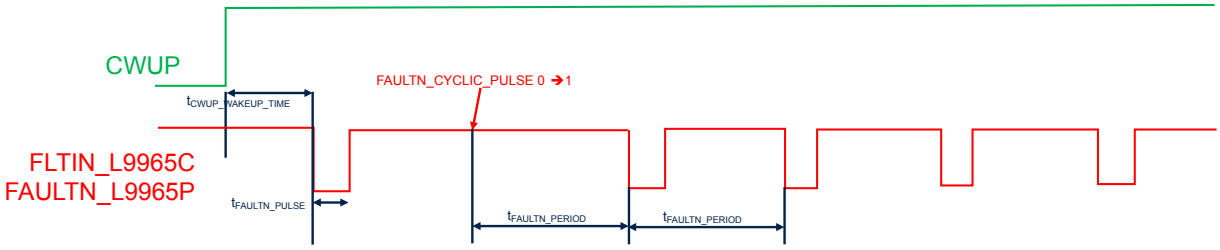


Figure 8. FAULTN integrity check in low power mode (example of timeout detected by L9965C/L99BM2C)

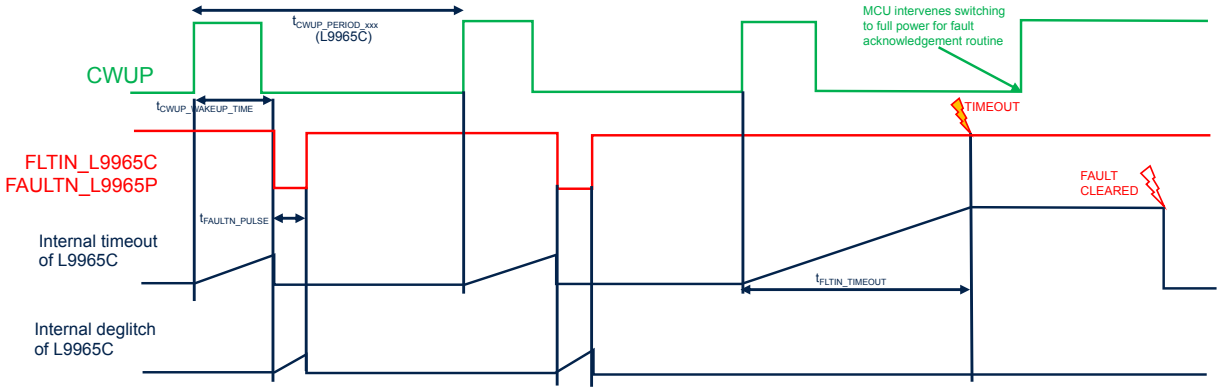
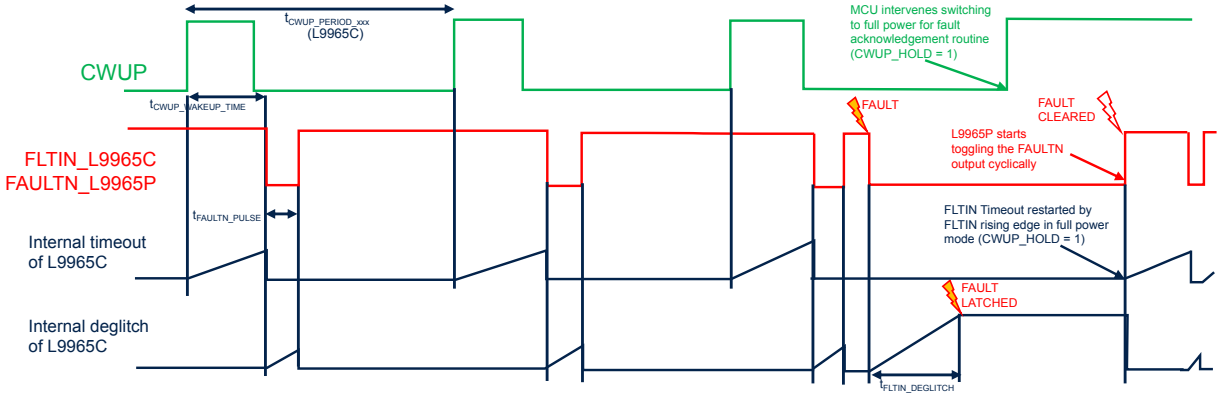


Figure 9. FAULTN integrity check in low power mode (example of fault detected by L9965P/L99BM2P)



3.5.2 FAULTN electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

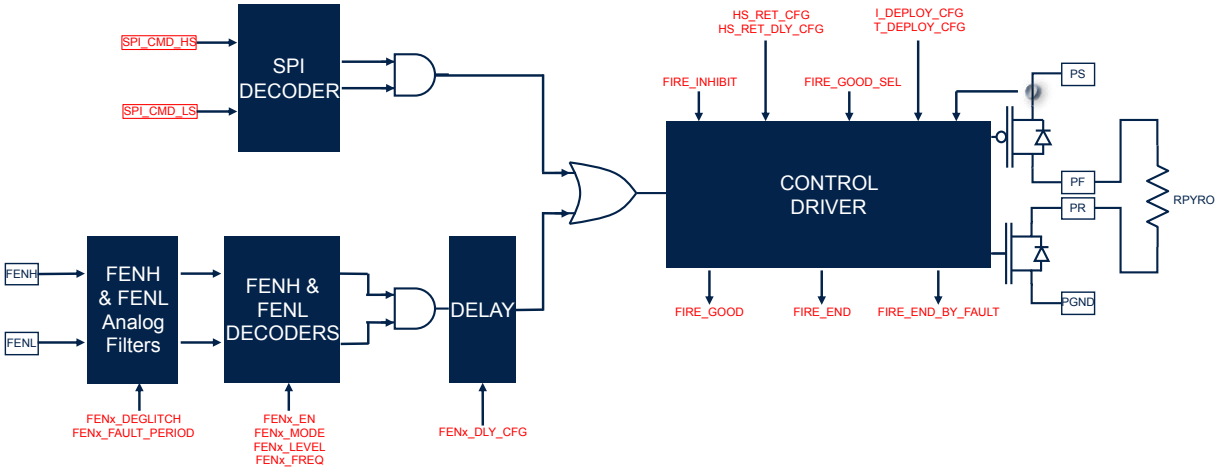
Table 18. FAULTN electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
t_{FAULTN_PERIOD}	FAULTN line integrity pulse period	Guaranteed by SCAN	5.5	-	14.5	ms	FAULTN
t_{FAULTN_PULSE}	FAULTN line integrity pulse duration	Guaranteed by SCAN	-	10	-	µs	FAULTN
$t_{FAULT\_HANDLING\_TIMEOUT}$	Fault handling timeout	Guaranteed by SCAN	1.8	2	2.1	s	FAULTN

3.6 Pyro-fuse deployment stage

The Figure 10 shows the pyro-fuse deployment stage architecture.

Figure 10. Pyro-fuse deployment stage architecture



Two independent paths are implemented to drive the HS and LS output switches:

- One via hardware through FENH and FENL pins.
- One via software through two SPI commands.

Three substages are present:

- Signal stage
  - The FENH and FENL signals decoders are configured via SPI registers and their configuration is stored into NVM.
  - A delay stage on the FENx path enables fine-tuning of the trigger output propagation delay for applications where several L9965P/L99BM2P pyro-fuse drivers need to be phase-shifted.
  - A parallel decoder stage for SPI arming commands is available.
- Control driver
  - The control driver translates the signal stage outputs into suitable commands for the power-stage output domain.
- Power stage
  - The LS and HS are turned on by a latch whose reset occurs whenever the fire attempt ends successfully or the deploy timer expires.
  - A HS current sensing is implemented to deploy the pyro-fuse with the programmed current profile and manage the deployment autoretry.
  - The power stage is inhibited by a “fire inhibit” signal in case a fault occurs.

3.6.1 Signal stage (FENH/FENL/SPI)

The IC has two digital inputs, FENH and FENL, whose signals are treated by two different decoders to generate the driving stimulus for the HS and LS switches.

Additionally, the switches can be triggered by dedicated SPI commands.

The FENH/FENL/SPI decoders are only available in DIAG, NORMAL and ARM states, while in DEEP-SLEEP they are disabled, since FENH/FENL/SPI may only be used as wake-up sources.

3.6.1.1 FENH/FENL decoders configuration

The two decoders can be individually enabled by setting ***FENH_EN*** = 1 and ***FENL_EN*** = 1. When disabled, their output is always in the inactive state (no trigger).

Before being input to the digital decoders, the FENH/FENL inputs are always pre-filtered by an analog stage (t_{FENx_FLT}) to prevent noise from altering the decoding process.

Each decoder can be configured in different modes:

- FENH_MODE/FENL_MODE = 0 sets the level-based decoding
  - A programmable deglitch filter $t_{FENx\_DEGLITCH}$ helps to filter out unwanted spikes on the trigger inputs. The deglitch value is valid for both FENH and FENL inputs.
  - When the FENL/FENH deglitched signal holds the active level, an arming condition is acknowledged on the corresponding branch.
- FENH_MODE/FENL_MODE = 1 sets the PWM-based decoding. The PWM-based encoding allows the L9965P/L99BM2P continuously monitoring the status of the trigger lines, being capable of detecting frequency drifts and stuck-at faults in real-time, as described in the Section 3.6.1.2.
  The decoder frequency can be selected between two options:
  - ***FENH_FREQ/FENL_FREQ*** = 0 sets the 125 kHz option
  - ***FENH_FREQ/FENL_FREQ*** = 1 sets the 16 kHz option

  The programmable $N_{FENx\_FAULT\_PERIOD}$ up/down counter is used to deglitch the PWM periods. The counter value is valid for both FENH and FENL inputs. The counter output behaves as follows:
  - In case it reaches the programmed threshold, it saturates and an arming condition is acknowledged on the corresponding branch.
  - In case the output value is less than the programmed threshold, the arming is released.

The FENH/FENL active state is configured through ***FENH_LEVEL/FENL_LEVEL*** bits:

- ***FENH_LEVEL*** = ***FENL_LEVEL*** = 0 sets the active state to:
  - Low level in case of level-based decoding (FENx_MODE = 0)
  - $t_{ON\_FAULT\_0L}$ low on-time in case of PWM-based decoding (FENx_MODE = 1) and high frequency selected (FENx_FREQ = 0)
  - $t_{ON\_FAULT\_1L}$ low on-time in case of PWM-based decoding (FENx_MODE = 1) and low frequency selected (FENx_FREQ = 1)
- ***FENH_LEVEL*** = ***FENL_LEVEL*** = 1 sets the active state to:
  - High level in case of level-based decoding (FENx_MODE = 0)
  - $t_{ON\_FAULT\_0H}$ high on-time in case of PWM-based decoding (FENx_MODE = 1) and high frequency selected (FENx_FREQ = 0)
  - $t_{ON\_FAULT\_1H}$ high on-time in case of PWM-based (FENx_MODE = 1) decoding and low frequency selected (FENx_FREQ = 1)

Note: To be robust against common cause failures, it is recommended to apply complementary active states to FENH and FENL.

Having selected the active states, the FENH/FENL internal pull-up/pull-down resistors can be programmed accordingly to manage the Hi-Z input condition:

- ***FENH_PU_PD***/***FENL_PU_PD*** = 0 enables the internal pull-up to the 3.3 V internal regulator.
- ***FENH_PU_PD***/***FENL_PU_PD*** = 1 enables the internal pull-down to GND.

Note: To prevent inadvertent trigger generation in case of pin loss, it is recommended to select the internal pull-up/pull-down configuration which leads the input signal to the inactive state in case of FENH/FENL pin loss.

The decoder output normally holds the inactive level. The block generates an active output level (delayed if delay is set) whenever the switches need to be turned ON in response to a valid trigger detected on FENH/FENL.

Whenever one of the two signals FENH/FENL is detected as valid, the FSM moves to ARM state. If both FENH and FENL are detected as valid, the deployment takes place as both HS and LS switches are closed.

It is possible to check the arming condition set by FENH and FENL reading the dedicated bits, respectively FENH_ARM and FENL_ARM.

The deployment condition is latched: to ensure reliable deployment delivering a suitable amount of energy to the igniter, an ongoing deployment (FIRE_RUNNING bit set to 1) cannot be interrupted even if the trigger conditions disappear.

After the deployment is complete, whatever the outcome is (FIRE_END bit set to 1 if no faults occur, FIRE_END_BY_FAULT bit se to 1 if a PS_OV or PGND_LOSS fault occurs), the device returns to NORMAL state.

The Table 19 summarizes FENH/FENL decoder output according to the different configurations:

Table 19. FENx decoder output behavior

FENx_EN	FENx_MODE	FENx_LEVEL	FENx input (deglitched)	Decoder output
0	X	X	X	Low
1	0	0	0	High
1	0	0	1	Low
1	0	1	0	Low
1	0	1	1	High
1	1	0	25% duty	High
1	1	0	75% duty	Low
1	1	1	25% duty	Low
1	1	1	75% duty	High

3.6.1.2 *FENH/FENL integrity check*

The IC provides diagnostics embedded in the decoder stage aimed at verifying the integrity of the trigger input signals. Their behavior depends on the corresponding signaling mode and configuration:

- In PWM mode (FENx_MODE = 1), the signal integrity is continuously monitored by an internal timer measuring the time interval between rising edges
  - Signals whose frequency lies within $f_{FENx\_PWM\_FREQ\_TH\_xL}$/$f_{FENx\_PWM\_FREQ\_TH\_xH}$ limits are considered ***valid*** and their duty-cycle is furtherly evaluated by the decoder to determine whether the pulse corresponds to a ***fire***/***no-fire***/***invalid*** command (see the Figure 11).
  - Signals whose frequency is higher than $f_{FENx\_PWM\_FREQ\_TH\_xH}$ are considered ***invalid*** and the corresponding FENH_HIGH_FREQ / FENL_HIGH_FREQ latch in FENX_INTEGRITY_STATUS register is set (see the Figure 12).
  - Signals whose frequency is lower than $f_{FENx\_PWM\_FREQ\_TH\_xL}$ but still higher than $f_{FENx\_PWM\_FREQ\_TH\_xT}$ are considered ***invalid*** and the corresponding FENH_LOW_FREQ / FENL_LOW_FREQ latch in FENX_INTEGRITY_STATUS register is set (see the Figure 12).
  - If the signals frequency drops below $f_{FENx\_PWM\_FREQ\_TH\_xT}$, a ***timeout*** condition is acknowledged and the corresponding FENH_PWM_TIMEOUT / FENL_PWM_TIMEOUT latch in FENX_INTEGRITY_STATUS register is set (see the Figure 11).
  - The above requirements on frequency can be seen also as requirements on times, as shown in the Figure 13.
  - The internal timeout to check the PWM frequency starts as soon as the FENx_MODE bit is set to 1 and is reset on each rising edge (see the Figure 11 and Figure 12).
  - ***"No-fire"*** and ***"invalid"*** signals decrement the $N_{FENx\_FAULT\_PERIOD}$ fault counter by 1, while ***"fire"*** signals increment the $N_{FENx\_FAULT\_PERIOD}$ by 1. In case of ***"timeout"***, the $N_{FENx\_FAULT\_PERIOD}$ counter is reset and restarts from 0.
- When in level mode (FENx_MODE = 0), the signal integrity check can be enabled by setting FENH_INT_CHECK_EN = 1/FENL_INT_CHECK_EN = 1
  - In this scenario, the IC locks to the FAULTN signal to perform the FENH/FENL integrity check. An internal $t_{FENx\_TIMEOUT}$ is started upon FAULTN rising edge and reset after two consecutive edges on the corresponding FENx line.
  - If the timeout expires, the corresponding FENH_LEV_TIMEOUT/FENL_LEV_TIMEOUT latch in the FENX_INTEGRITY_STATUS register is set (see the Figure 14). Once latched, the fault is cleared, and the correspondent timeout is reset, when the FENH_LEV_TIMEOUT/FENL_LEV_TIMEOUT bit is read.
  - When the low power strategy is implemented, to detect a possible fault due to timeout expiration, the IC shall be kept awake for a time greater than $t_{FENx\_TIMEOUT}$. This could be done simply by keeping the CWUP pin high for more than $t_{FENx\_TIMEOUT}$, and/or enabling *VRCM check* and *pyro outputs leakage test*.
- Alternatively, a manual integrity check can be performed by the MCU, toggling the FENH and FENL input signals and looking at the FENH_ECHO and FENL_ECHO status bits in the FENX_INTEGRITY_STATUS register.

Figure 11. FENx line integrity check in PWM mode (example of timeout detection)

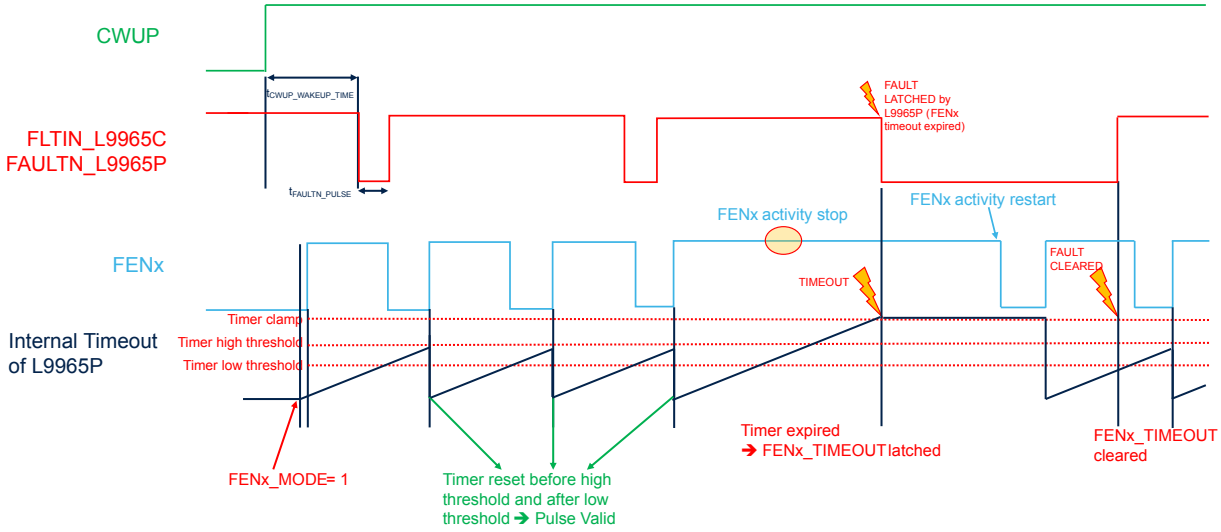


Figure 12. FENx line integrity check in PWM mode (example of frequency out of range)

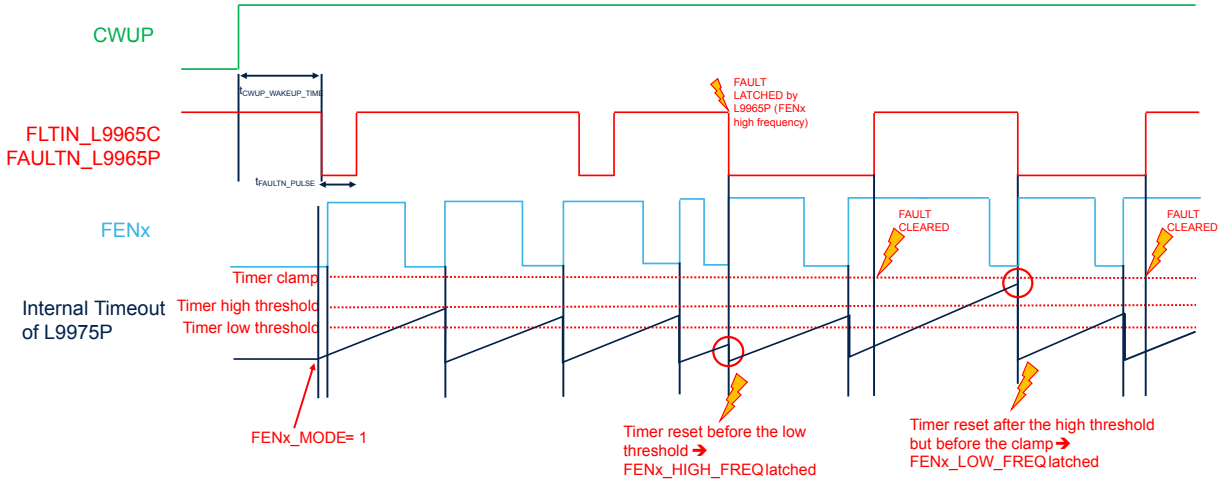


Figure 13. FENx decoder times in PWM mode

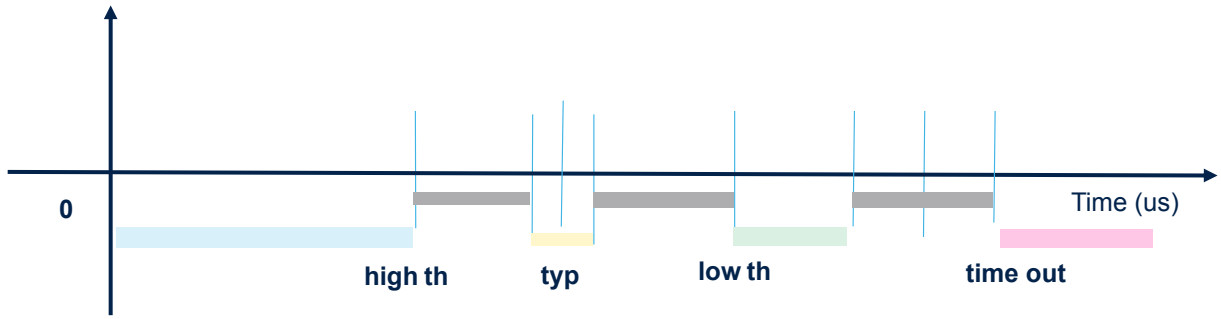
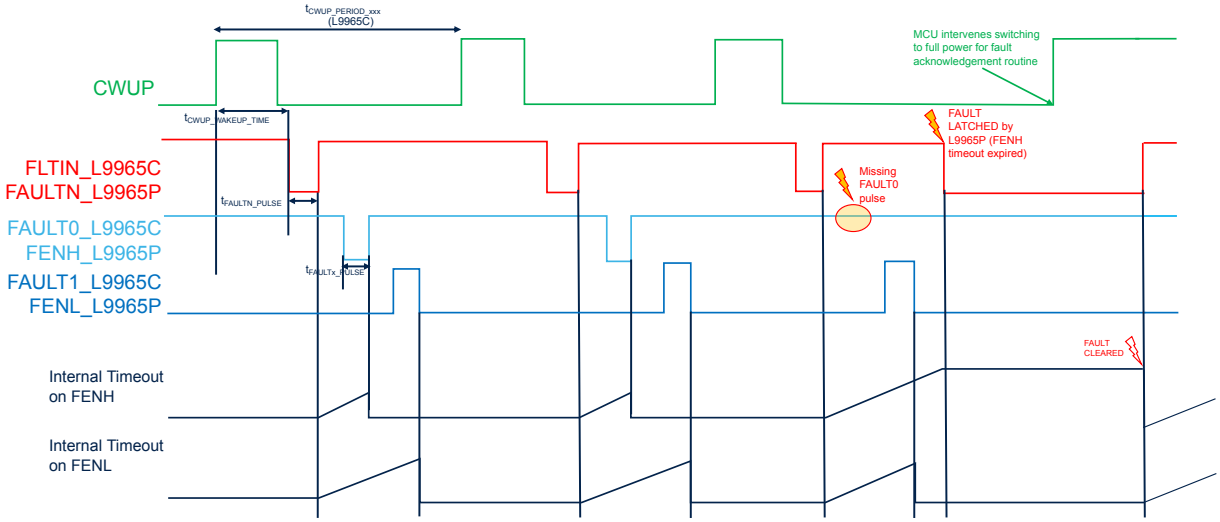


Figure 14. FENx line integrity check in level mode (example of timeout on FENH)



3.6.1.3 *Programmable delay*

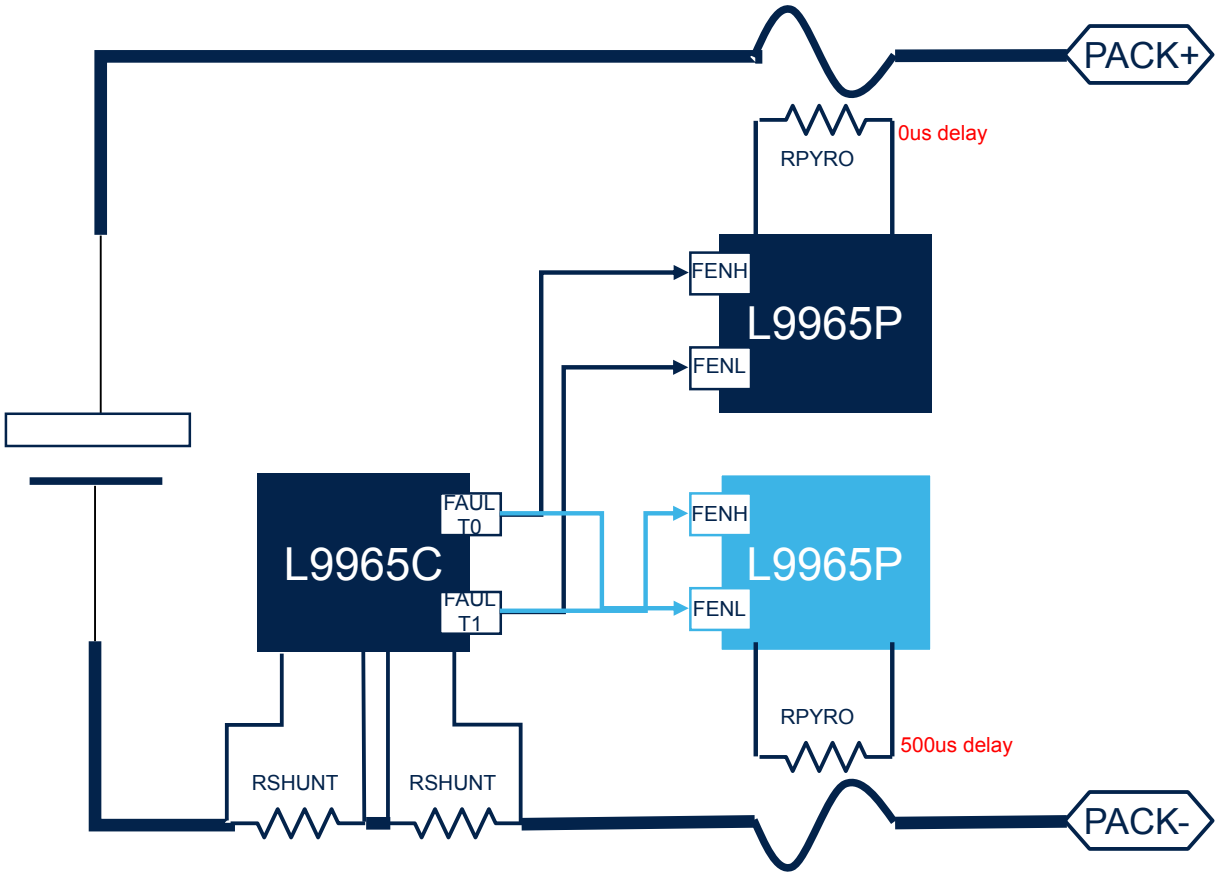
In systems where multiple L9965P/L99BM2P ICs are used, it may be required to apply a phase shift between pyro-fuses deployment (see example in the Figure 15).

In such case, the deploy control stage can be configured to apply a t_{DEPLOY_DELAY} shift to the start of the deployment procedure (when both arming conditions are set).

The delay is programmed through the ***FENx_DLY_CFG*** bit.

The delay insertion is only available in case of deployment triggered via FENH/FENL signals, while it shall be managed by MCU timers in case of deployment triggered via SPI.

Figure 15. Example of two pyro-drivers in a system



3.6.1.4 *Pyro-fuse trigger via SPI*

The output switches can be triggered also by SPI commands:

- Writing the 0x155 command in the HS_CMD register
- Writing the 0x2AA command in the LS_CMD register

HS_CMD and LS_CMD are located at different addresses of the SPI register map so that a sequence of two commands is needed to perform a deployment. The two commands are intentionally different to prevent inadvertent deployment.

3.6.1.5 FENH/FENL diagnostics

Table 20. FENH/FENL diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
FENx high frequency	When in PWM mode (FENx_MODE = 1) if the input signal period becomes lower than high threshold the high frequency fault is acknowledged	The FENx_HIGH_FREQ flag is set FAULTN line is asserted $N_{FENx\_FAULT\_PERIOD}$ counter is decremented by 1	If the input signal period becomes lower than high threshold the fault flag can be cleared by MCU	FAULTN line is released	FENx_MODE = 0 masks diagnostic execution. When disabled, the FENx_HIGH_FREQ flag can always be cleared by the MCU. ***FENX_HIGH_FREQ_FAULTN_MSK*** masks fault redirection on FAULTN pin
FENx low frequency	When in PWM mode (FENx_MODE = 1) if the input signal period is between low and timeout thresholds the low frequency fault is acknowledged	The FENx_LOW_FREQ flag is set FAULTN line is asserted $N_{FENx\_FAULT\_PERIOD}$ counter is decremented by 1	If the input signal period becomes higher than low threshold the fault flag can be cleared by MCU	FAULTN line is released	FENx_MODE = 0 masks diagnostic execution. When disabled, the FENx_LOW_FREQ flag can always be cleared by the MCU. ***FENX_LOW_FREQ_FAULTN_MSK*** masks fault redirection on FAULTN pin
FENx timeout in PWM mode	When in PWM mode (FENx_MODE = 1) if the input signal period becomes lower than timeout threshold the PWM timeout fault is acknowledged	The FENx_PWM_TIMEOUT flag is set FAULTN line is asserted $N_{FENx\_FAULT\_PERIOD}$ counter is reset (but not stopped)	If the input signal period becomes higher than timeout threshold the fault flag can be cleared by MCU	FAULTN line is released	FENx_MODE = 0 masks diagnostic execution. When disabled, the FENx_PWM_TIMEOUT flag can always be cleared by MCU. ***FENX_TIMEOUT_FAULTN_MSK*** masks fault redirection on FAULTN pin
FENx timeout in level mode	When in Level mode (FENx_MODE = 0), following a FAULTN pulse, the FENx input signal is expected to exhibit two edges within $t_{FENx\_TIMEOUT}$. If this does not happen, the level timeout fault is acknowledged	The FENx_LEV_TIMEOUT flag is set FAULTN line is asserted	The fault flag can always be cleared by the MCU	FAULTN line is released	FENx_MODE = 1 masks diagnostic execution. When disabled, the FENx_LEV_TIMEOUT flag can always be cleared by MCU. FENx_INT_CHECK_EN = 0 masks diagnostic execution. When disabled, the FENx_LEV_TIMEOUT flag can always be cleared by MCU. ***FENX_TIMEOUT_FAULTN_MSK*** masks fault redirection on FAULTN pin

3.6.1.6 *FENH/FENL electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 21. FENH/FENL decoder electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$t_{FENX\_DEGLITCH\_00}$	FENH/FENL input level deglitch filter	***FENX_DEGLITCH*** = 00	-	20	-	µs	FENH, FENL
$t_{FENX\_DEGLITCH\_01}$		***FENX_DEGLITCH*** = 01	-	80	-	µs	FENH, FENL
$t_{FENX\_DEGLITCH\_10}$		***FENX_DEGLITCH*** = 10	-	320	-	µs	FENH, FENL
$t_{FENX\_DEGLITCH\_11}$		***FENX_DEGLITCH*** = 11	-	1280	-	µs	FENH, FENL
$N_{FENX\_FAULT\_PERIOD\_00}$	FENH/FENL PWM periods deglitch filter	***FENX_FAULT_PERIOD*** = 00	-	2	-	periods	FENH, FENL
$N_{FENX\_FAULT\_PERIOD\_01}$		***FENX_FAULT_PERIOD*** = 01	-	8	-	periods	FENH, FENL
$N_{FENX\_FAULT\_PERIOD\_10}$		***FENX_FAULT_PERIOD*** = 10	-	32	-	periods	FENH, FENL
$N_{FENX\_FAULT\_PERIOD\_11}$		***FENX_FAULT_PERIOD*** = 11	-	128	-	periods	FENH, FENL
$f_{FENx\_PWM\_FREQ\_0}$	FENH/FENL decoder frequency in PWM mode	***FENx_FREQ*** = 0	-	125	-	kHz	FENH, FENL
$f_{FENx\_PWM\_FREQ\_1}$		***FENx_FREQ*** = 1	-	16	-	kHz	FENH, FENL
$t_{FENx\_PWM\_PERIOD\_0}$	FENH/FENL decoder period in PWM mode	***FENx_FREQ*** = 0	-	8	-	µs	FENH, FENL
$t_{FENx\_PWM\_PERIOD\_1}$		***FENx_FREQ*** = 1	-	62.5	-	µs	FENH, FENL
$t_{FENx\_PWM\_PERIOD\_TH\_0L}$	FENH/FENL period monitor low threshold (PWM low frequency)	***FENx_FREQ*** = 0	13	-	-	µs	FENH, FENL
$t_{FENx\_PWM\_PERIOD\_TH\_1L}$		***FENx_FREQ*** = 1	99	-	-	µs	FENH, FENL
$t_{FENx\_PWM\_PERIOD\_TH\_0H}$	FENH/FENL period monitor high threshold (PWM high frequency)	***FENx_FREQ*** = 0	-	-	4	µs	FENH, FENL
$t_{FENx\_PWM\_PERIOD\_TH\_1H}$		***FENx_FREQ*** = 1	-	-	38	µs	FENH, FENL
$t_{FENx\_PWM\_PERIOD\_TH\_0T}$	FENH/FENL period monitor timeout threshold (in tracking with low threshold)	***FENx_FREQ*** = 0	20	-	-	µs	FENH, FENL
$t_{FENx\_PWM\_PERIOD\_TH\_1T}$		***FENx_FREQ*** = 1	159	-	-	µs	FENH, FENL
$t_{ON\_FAULT\_0L}$	FENH/FENL valid on-time range for low signal at high PWM	FENx_MODE = 1, ***FENx_FREQ*** = 0 and ***FENx_LEVEL*** = 0	1.5	2.0	3.9	µs	FENH, FENL
$t_{ON\_FAULT\_0H}$	FENH/FENL valid on-time range for high signal at high PWM	FENx_MODE = 1, ***FENx_FREQ*** = 0 and ***FENx_LEVEL*** = 1	4.7	6.0	8.2	µs	FENH, FENL
$t_{ON\_FAULT\_1L}$	FENH/FENL valid on-time range for low signal at low PWM	FENx_MODE = 1, ***FENx_FREQ*** = 1 and ***FENx_LEVEL*** = 0	11.4	15.6	30.6	µs	FENH, FENL

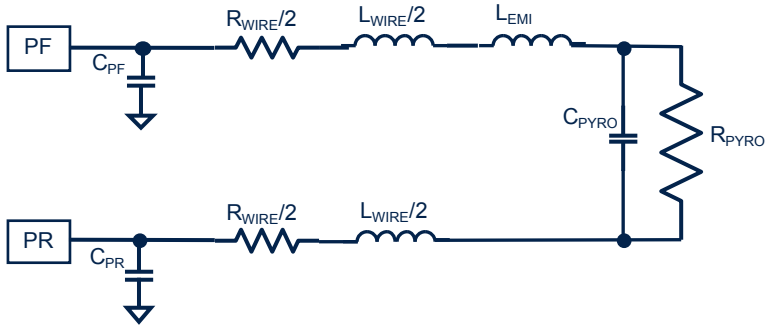
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$t_{ON\_FAULT\_1H}$	FENH/FENL valid on-time range for high signal at low PWM	FENx_MODE = 1, ***FENx_FREQ*** = 1 and ***FENx_LEVEL*** = 1	34.3	46.9	64.7	µs	FENH, FENL
$t_{FENx\_TIMEOUT}$	FENH/FENL timeout for integrity check in level mode	FENx_MODE = 0	1.75	2	2.25	ms	FENH, FENL
$t_{DEPLOY\_DELAY\_00}$	FENH/FENL deploy trigger delay	***FENX_DLY_CFG*** = 00	-	0	-	ms	FENH, FENL
$t_{DEPLOY\_DELAY\_01}$		***FENX_DLY_CFG*** = 01	1.8	2	2.2	ms	FENH, FENL
$t_{DEPLOY\_DELAY\_10}$		***FENX_DLY_CFG*** = 10	3.6	4	4.4	ms	FENH, FENL
$t_{DEPLOY\_DELAY\_11}$		***FENX_DLY_CFG*** = 11	7.2	8	8.8	ms	FENH, FENL

3.6.2 Power stage (PS/PF/PR/PGND)

The power stage is made of two power switches whose actuation is triggered by two independent paths, as shown in the Figure 10.

The Figure 16 shows the equivalent load model of a pyro-fuse igniter input. The following circuit have been considered when performing power stage diagnostics and deployment simulations.

Figure 16. Pyro-fuse input model



3.6.2.1 *Active pull-down on LS*

A pull-down current generator ($I_{ACT\_PD\_PR}$) is present on PR pin to have a minimum current-limited pull-down path to PR and PF pin. The circuit is connected between PR pin force pad and GND pin. As a diagnostic resource is enabled, the pull-down generator is automatically disabled. It is possible to force the disable state of the pull-down generator using the PR_PD_DIS bit located in the INTERNAL_CFG register.

3.6.2.2 *LS driver deactivation delay*

A delay $t_{LS\_OFF\_DEACT}$ is implemented in the LS driver deactivation with respect to HS driver to:

- Limit the LS recirculation energy after fire to E_{LS_CLAMP};
- Protect the device pins against voltage spikes at the end of a deployment event, clamping the voltage to V_{LS_CLAMP}.

No equivalent delay is applied at deployment event start.

3.6.2.3 *Pyro-fuse deployment profile*

The HS power-stage features a current controlled powerMOS supporting flexible deployment profiles. It is possible to configure both the current level and the duration:

- The ***I_DEPLOY_CFG*** field selects the target deploy current level;
- The ***T_DEPLOY_CFG*** field selects the target deploy time.

The HS switch has been designed to withstand a maximum deployment energy of $E_{HS\_DEPLOY\_x}$ starting from the maximum operating T_J.

3.6.2.4 *Deployment routine*

As soon as the IC enters the ARM state, any ongoing diagnostic is interrupted.

Once in ARM state, if a valid trigger command is received, the t_{DEPLOY} deployment timer starts. The current flowing in the HS is monitored by a dedicated current comparator, whose threshold is $I_{DEP\_MON\_TH}$ and is proportional to the programmed deployment current value I_{DEPLOY_xx}.

One digital current counter is present to count how much time the deployment current stays above $I_{DEP\_MON\_TH}$. It is initialized to 0 upon system power-on and reset. The value is stored in the DEP_CURR_MON bit field located in the DEPLOY_CURRENT_MONITOR register. The counter is reset when the device goes in ARM state and a new valid deployment command sequence is received. The value of this counter is then compared with the digital value of $t_{DEP\_MON\_TH}$ threshold.

The deployment current monitor timer threshold $t_{DEP\_MON\_TH}$ can be calculated as follows:

$$t_{DEP\_MON\_TH} = \boldsymbol{DEP\_MON\_THR} \times t_{DEP\_MON\_TH\_RES} \quad (1)$$

After a deployment event, a pyro igniter resistance measurement can be performed and the result, saved in the RES_MEAS_POST register, is compared with the $R_{PYRO\_POST\_TH}$ threshold selected through ***VRES_POST_TH*** bit in NVM.

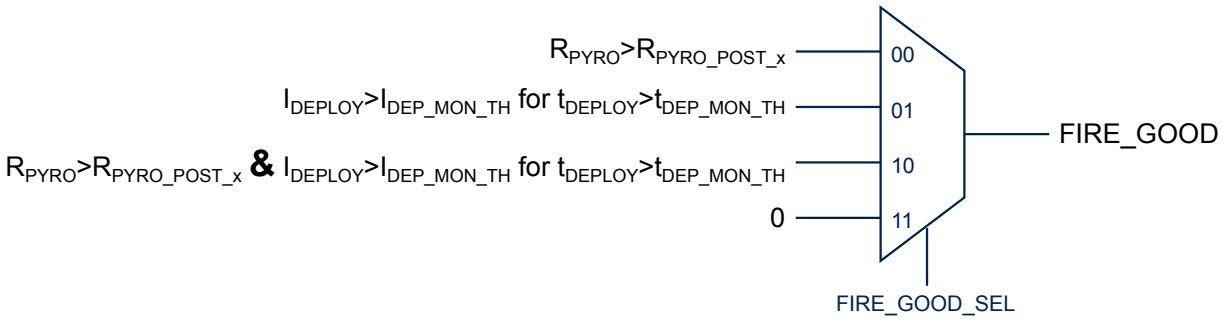
Note: If a deployment attempt ends successfully, the pyro-fuse resistance increases to values greater than 100 Ω. Hence, if further deployments are attempted, almost the entire PS voltage would fall on the initiator resistance, which in turn would result in the PF-PR voltage measurement close to saturation. This can be seen as a further confirmation of the fire outcome (FIRE_GOOD bit set).

The deployment routine ends when the FIRE_GOOD signal is set to 1. In this case the deployment info is saved and then the device returns in NORMAL state.

Through the ***FIRE_GOOD_SEL*** bit field, it is possible to select when the fire good signal is set (Figure 17):

- Measured resistance value above resistance threshold (***FIRE_GOOD_SEL*** = 00)
- Deployment current value above the current monitor threshold for the selected deployment current duration (***FIRE_GOOD_SEL*** = 01)
- Measured resistance value above resistance threshold AND deployment current value above current monitor threshold for the selected deployment current duration (***FIRE_GOOD_SEL*** = 10)
- Fire good signal is never set (***FIRE_GOOD_SEL*** = 11)

Figure 17. Fire good signal selection



The “fire inhibit” signal inhibits the deployment of the pyro-fuse, sets the FIRE_INHIBIT latch and asserts the FAULTN line. Any further deployment is not possible until latched bit is read (clear-on-read bit).

3.6.2.5 *Safe operating area*

There is no constraint on the selection between different I_{DEPLOY_XX} and t_{DEPLOY}, so it is under user's responsibility to prevent excessive thermal heating in the squib driver section by setting the deploy parameters carefully.

The power stage has been sized according to the following recommended combinations:

- I_{DEPLOY_00} and t_{DEPLOY} = 1050 µs
  Profile valid for 8.4 V ≤ V_{PS} ≤ 27.3 V ($V_{PS,min}$ = 8.4 V considering max resistance contribute)
- I_{DEPLOY_01} and t_{DEPLOY} = 750 µs
  Profile valid for 9.8 V ≤ V_{PS} ≤ 27.3 V ($V_{PS,min}$ = 9.8 V considering max resistance contribute)
- I_{DEPLOY_10} and t_{DEPLOY} = 550 µs
  Profile valid for 11.2 V ≤ V_{PS} ≤ 27.3 V ($V_{PS,min}$ = 11.2 V considering max resistance contribute)
- I_{DEPLOY_11} and t_{DEPLOY} = 250 µs
  Profile valid for 19.6 V ≤ V_{PS} ≤ 27.3 V ($V_{PS,min}$ = 19.6 V considering max resistance contribute)

The power stage is not sized to stand a deployment event with PF pin shorted to ground. So, if this scenario is expected, the maximum operating voltage on PS pin should be reduced accordingly to chosen deployment profile:

- I_{DEPLOY_00} and t_{DEPLOY} = 1050 µs
  This profile is valid for 6 V ≤ V_{PS} ≤ 23 V
- I_{DEPLOY_01} and t_{DEPLOY} = 750 µs
  This profile is valid for 6 V ≤ V_{PS} ≤ 23 V
- I_{DEPLOY_10} and t_{DEPLOY} = 550 µs
  This profile is valid for 6 V ≤ V_{PS} ≤ 22 V
- I_{DEPLOY_11} and t_{DEPLOY} = 250 µs
  Not tolerated

The effective deployment time t_{DEP_EFF} (time interval in which the deployment current value is above 90% of the programmed target value I_{DEPLOY_xx}) can be calculated as follows:

$$t_{DEP\_EFF} = t_{DEPLOY} - t_{DEP\_DLY} = \text{DEP\_TIME\_x} \times t_{DEPLOY\_RES} - t_{DEP\_DLY} \quad (2)$$

Where:

- DEP_TIME_x * t_{DEPLOY_RES} is the equivalent time of the programmed deployment duration counter value.
- t_{DEP_DLY} is the delay time between the actual receiving of the deployment start signal (SPI CS rising edge or FENH and FENL acknowledge) and the rising deployment current value reaching 90% of the programmed target value.

3.6.2.6 *Deployment auto-retry*

The IC offers the possibility of performing multiple fire attempts in case the first one fails:

- The ***HS_RET_CFG*** bit field configures the maximum number of deployment attempts.
- The ***HS_RET_DLY_CFG*** bit field configures the interval between consecutive retry attempts.

If one of the following conditions occurs, the auto-retry is stopped:

- FIRE_GOOD is set following a successful deployment.
- The maximum number of attempts (configured by ***HS_RET_CFG*** bit field) is exceeded without a successful deployment.

The ***FIRE_GOOD_SEL*** = 11 case is useful in test case scenario where the Pyro igniter is replaced by a dummy load: multiple deployments are performed and their number is limited by the configured maximum number of retries.

*Note: The time between two retries is the bigger between the resistance measurement time and the interval time defined by **HS_RET_DLY_CFG** bit field in NVM.*

If, once reached the maximum number of attempts, the deployment condition is still present (FENH and FENL signals still in active state), another retry routine is performed after a minimum delay time of $t_{RET\_ROUTINE\_DLY}$.

The number of performed deployments is readable in the DEPLOY_CNT bit field in the DEPLOY_STATUS register.

3.6.2.7 *Deployment electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 22. Deployment electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_{DEPLOY_00}	Pyro-fuse deployment current	***I_DEPLOY_CFG*** = 00	1.50	-	1.91	A	PR, PGND
I_{DEPLOY_01}		***I_DEPLOY_CFG*** = 01	1.75	-	2.23	A	PR, PGND
I_{DEPLOY_10}		***I_DEPLOY_CFG*** = 10	2.00	-	2.55	A	PR, PGND
I_{DEPLOY_11}		***I_DEPLOY_CFG*** = 11	3.50	-	4.46	A	PR, PGND
t_{DEPLOY_RES}	Deployment timer resolution		14.7	16	17.3	µs	PS, PF
N_{DEPLOY}	Deployment timer bits number	***T_DEPLOY_CFG***	-	7	-	Bits	PS, PF
t_{DEPLOY}	Deployment timer	t_{DEPLOY_RES} * ***T_DEPLOY_CFG***	-	-	2032	µs	PS, PF
$t_{LS\_OFF\_DEACT}$	Delay between HS turn-off and LS turn-off		50	-	-	µs	PR, PGND
E_{LS_CLAMP}	Low side recirculation energy after fire	Considering L_{WIRE} + L_{EMI} $T_{J,START}$ = 135 °C	-	-	300	µJ	PR, PGND
V_{LS_CLAMP}	LS voltage clamp		35	-	40	V	PR
$t_{DEP\_CUR\_RISE}$	From 10% to 90% of the I_{DEPLOY_XX}	Including R_{PYRO}, L_{WIRE}, C_{WIRE}, L_{EMI}, C_{PYRO}	-	-	32	µs	PF, PR
t_{DEP_DLY}	From deployment start signal (SPI CS rising edge or FENH/FENL acknowledge) to 90% of the I_{DEPLOY_XX}	Including R_{PYRO}, L_{WIRE}, C_{WIRE}, L_{EMI}, C_{PYRO}	-	-	50	µs	PF, PR
$t_{DEP\_CUR\_FALL}$	From 90% to 10% of the I_{DEPLOY_XX}	Including R_{PYRO}, L_{WIRE}, C_{WIRE}, L_{EMI}, C_{PYRO}	-	-	32	µs	PF, PR
$t_{DEP\_CUR\_MON}$	Deployment current monitor resolution	***DEP_CURR_MON***	-	8	-	µs	PS, PF
$I_{DEP\_MON\_TH}$	Deployment current monitor threshold		90%*I_{DEPLOY_xx}	-	-	A	PS, PF
$t_{DEP\_MON\_TH\_RES}$	Deployment current monitor timer threshold resolution		-	32	-	µs	PS, PF
$N_{DEP\_MON\_TH}$	Deployment current monitor timer threshold bits number	***DEP_MON_THR***	-	5	-	Bits	PS, PF
$t_{DEP\_MON\_TH}$	Deployment current monitor timer threshold	$t_{DEP\_MON\_TH\_RES}$ * ***DEP_MON_THR***	-	-	992	µs	PS, PF
$E_{HS\_DEPLOY\_1}$	High side switch deployment energy capability	Single event, V_{PS} = 27.3 V I_{DEP} = 1.91 A, t_{ON} = 1191 µs R_{dsON_LS} = 0 Ω, R_{WIRE} = 0.1 Ω R_{PYRO} = 1.7 Ω, $T_{J,START}$ = 135 °C	-	-	54.4	mJ	PS, PF

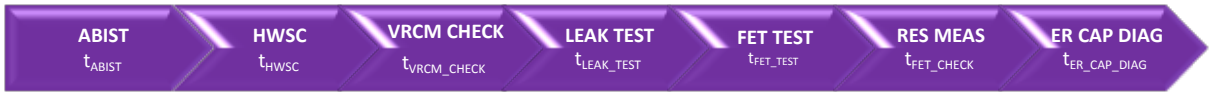
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$E_{HS\_DEPLOY\_2}$	High side switch deployment energy capability	Single event, V_{PS} = 27.3 V I_{DEP} = 2.23 A, t_{ON} = 851 µs R_{dsON_LS} = 0 Ω, R_{WIRE} = 0.1 Ω R_{PYRO} = 1.7 Ω, $T_{J,START}$ = 135 °C	-	-	44.2	mJ	PS, PF
$E_{HS\_DEPLOY\_3}$		Single event, V_{PS} = 27.3 V I_{DEP} = 2.55 A, t_{ON} = 630 µs R_{dsON_LS} = 0 Ω, R_{WIRE} = 0.1 Ω R_{PYRO} = 1.7 Ω, $T_{J,START}$ = 135 °C	-	-	36.5	mJ	PS, PF
$E_{HS\_DEPLOY\_4}$		Single event, V_{PS} = 27.3 V I_{DEP} = 4.46 A, t_{ON} = 289 µs R_{dsON_LS} = 0 Ω, R_{WIRE} = 0.1 Ω R_{PYRO} = 1.7 Ω, $T_{J,START}$ = 135 °C	-	-	24.9	mJ	PS, PF
R_{dsON_HS}	HS switch ON resistance	I_{SINK} = 100 mA	-	-	1	Ω	PS, PF
R_{dsON_LS}	LS switch ON resistance	I_{SOURCE} = 100 mA	-	-	1	Ω	PR, PGND
L_{WIRE}	Pyro-fuse wire load inductance	Application information	-	-	36	µH	PF, PR
L_{EMI}	Pyro-fuse input EMI filter	Application information	-	-	7.7	µH	PF, PR
R_{WIRE}	Pyro-fuse wire load resistance	Application information	-	-	1.1	Ω	PF, PR
C_{PYRO}	Pyro-fuse differential capacitance between input contacts	Application information	-	-	100	nF	PF, PR
R_{PYRO}	Pyro-fuse igniter resistance	Application information	1.7	-	2.5	Ω	PF, PR
$R_{PYRO\_POST\_0}$	Pyro-fuse igniter resistance threshold post deployment	***VRES_POST_TH*** = 0	-	99	-	Ω	PF, PR
$R_{PYRO\_POST\_1}$		***VRES_POST_TH*** = 1	-	49	-	Ω	PF, PR
C_{ESD}	PF/PR PCB connector input capacitance for ESD/EMI	Application information	13	22	138	nF	PF, PR
$N_{HS\_RET\_00}$	HS deployment attempts	***HS_RET_CFG*** = 00	-	1	-	times	PR, PGND
$N_{HS\_RET\_01}$		***HS_RET_CFG*** = 01	-	2	-	times	PR, PGND
$N_{HS\_RET\_10}$		***HS_RET_CFG*** = 10	-	3	-	times	PR, PGND
$N_{HS\_RET\_11}$		***HS_RET_CFG*** = 11	-	4	-	times	PR, PGND
$t_{HS\_RET\_00}$	HS delay between retry attempts	***HS_RET_DLY_CFG*** = 00	0.46	0.5	0.54	ms	PR, PGND
$t_{HS\_RET\_01}$		***HS_RET_DLY_CFG*** = 01	0.92	1	1.08	ms	PR, PGND
$t_{HS\_RET\_10}$		***HS_RET_DLY_CFG*** = 10	1.38	1.5	1.62	ms	PR, PGND

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$t_{HS\_RET\_11}$	HS delay between retry attempts	***HS_RET_DLY_CFG*** = 11	1.84	2	2.16	ms	PR, PGND
$t_{RET\_ROUTINE\_DLY}$	Delay between two consecutive retry routines		0.46	0.5	0.54	ms	PR, PGND
$I_{ACT\_PD\_PR}$	PR active pull-down current		0.7	1	1.3	mA	PR

3.7 Diagnostic routine

The IC integrates an intelligent controller designed to automatically perform diagnostic sweeps aimed at guaranteeing the safety targets on deployment and non-deployment.

Figure 18. Diagnostic routine



The diagnostic flow has been specifically designed to ensure that each step validates the circuitry necessary to perform subsequent checks.

In case the routine detects a failure during any of the steps, it immediately stops, setting the corresponding fault flag and asserting the FAULTN line. If there is a fault during ABIST step, the routine does not stop but the corresponding fault flag is set and the FAULTN line is asserted.

3.7.1 Routine execution modes

Every time the routine is triggered, the FSM moves to the DIAG state.

There are two types of triggers available:

- On-demand: triggered by MCU
- Cyclic: autonomously triggered by an internal timer or triggered by an external CWUP pulse

The two execution modes are mutually exclusive: on-demand triggers cannot interrupt cyclic executions and vice-versa.

3.7.1.1 On-demand

This strategy is available every time the IC is in a NORMAL state.

On-demand execution is triggered by MCU writing DIAG_START = 1 in the DIAG_CMD register and configuring the steps to be executed in the same command frame:

1. Writing ABIST = 1 enables the **ABIST (analog built-in self-test)**.
2. Writing ADC_HWSC = 1 enables the **HWSC (hardware self-check)**.
3. Writing VRCM_LEAK_TEST = 1 enables the **VRCM check** and the **pyro outputs leakage test**.
4. Writing PYRO_RES = 1 enables the **pyro igniter resistance measurement**.
5. Writing FET_TEST = 1 enables the **pyro deployment FETs test**. This test includes the VRCM check and the pyro outputs leakage test.
6. Writing ER_CAP = 1 enables the **ER capacitor diagnostic**.

During the diagnostic execution the SPI_DIAG_RUNNING bit is set to 1. Once the on-demand diagnostic is completed, the SPI_DIAG_END bit is set to 1.

On-demand triggers do not increment the internal cycle counter whose value is stored in CYC_DIAG_NCYCLE bit field in CYCLIC_DIAG_STATUS register.

3.7.1.2 Cyclic

This strategy is available in both full-power mode and low-power mode:

- When in full power mode (CWUP = 1, static), the periodicity can be configured programming the $t_{DIAG\_ROUTINE\_PERIOD\_XXX}$ time.
- When in low power mode (periodic CWUP triggers), the periodicity is given by the CWUP signal.

Diagnostic steps can be individually enabled/disabled via dedicated NVM configuration bits:

- ***ADC_HWSC_EN*** = 1 schedules the **HWSC** for cyclic execution
  - ***ADC_HWSC_NCYCLE*** field specifies the periodicity of execution
- ***LEAK_EN*** = 1 schedules the **VRCM check** and **pyro outputs leakage test** for cyclic execution
  - ***LEAK_NCYCLE*** field specifies the periodicity of execution
- ***PYRO_RES_EN*** = 1 schedules the **pyro igniter resistance measurement** for cyclic execution
  - ***PYRO_RES_NCYCLE*** field specifies the periodicity of execution
- ***FET_EN*** = 1 schedules the **pyro deployment FETs test** for cyclic execution
  - ***FET_NCYCLE*** field specifies the periodicity of execution
- ***ER_CAP_EN*** = 1 schedules the **ER capacitor diagnostic** for cyclic execution
  - ***ER_CAP_NCYCLE*** field specifies the periodicity of execution

The NVM configuration guarantees the execution of the diagnostics (CYC_DIAG_RUNNING in CYCLIC_DIAG_STATUS register set to 1) even in the absence of MCU supervision. The routine is executed only after the NVM has been downloaded.

When the device is in full power, a new routine is inhibited if a fail in integrity check occurs (CYC_CFG_CRC_FAIL bit set).

The internal cycle counter CYC_DIAG_NCYCLE bit field is incremented at the end of each diagnostic sweep. In case it reaches saturation, it rolls over restarting from zero.

3.7.2 Routine steps

The following sections list all the diagnostic steps performed during the diagnostic routine.

3.7.2.1 ABIST (analog built-in self-test)

This step aims at verifying the proper behavior of analog comparators.

In cyclic diagnostic it is not possible to disable the ABIST, so it runs at every cycle.

In case of fault, the ABIST_FAIL bit in the INTERNAL_STATUS register is set and the FAULTN pin is asserted.

The ABIST diagnostic step duration is t_{ABIST}.

Note: In cyclic diagnostic the ABIST cannot be disabled, so it runs at every cycle.

3.7.2.2 HWSC (hardware self-check)

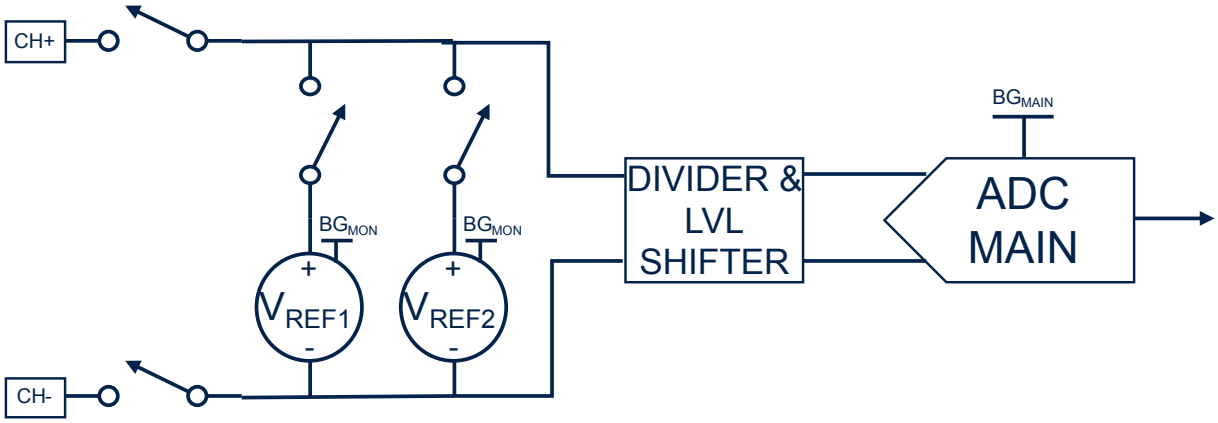
This step aims at verifying the integrity of conversion paths from an input to the ADCs.

The following paths are checked:

- PF vs PR to check the integrity of differential measurement pre-deployment.
- PF vs PR to check the integrity of differential measurement post-deployment.
- VRCM vs PGND to check the integrity of VRCM measurement.

This test does not require any previous diagnostic to be safely executed.

Figure 19. Differential ADC HWSC



The diagnostic for PF vs PR path (differential ADC) works as follows: the pins are disconnected from the inputs and, applying different internal reference voltages (short-circuit, VREF1 and VREF2), the circuitry checks ADC error (vs $V_{OFFSET\_HWSC\_TH}$) and ADC gain (vs $V_{GAIN\_HWSC\_TH}$).

In the specific case of VRCM path, a direct VRCM output conversion takes place to verify the regulator output is in the expected range.

The HWSC diagnostic step duration is t_{HWSC}.

Table 23. ADC HWSC diagnostics

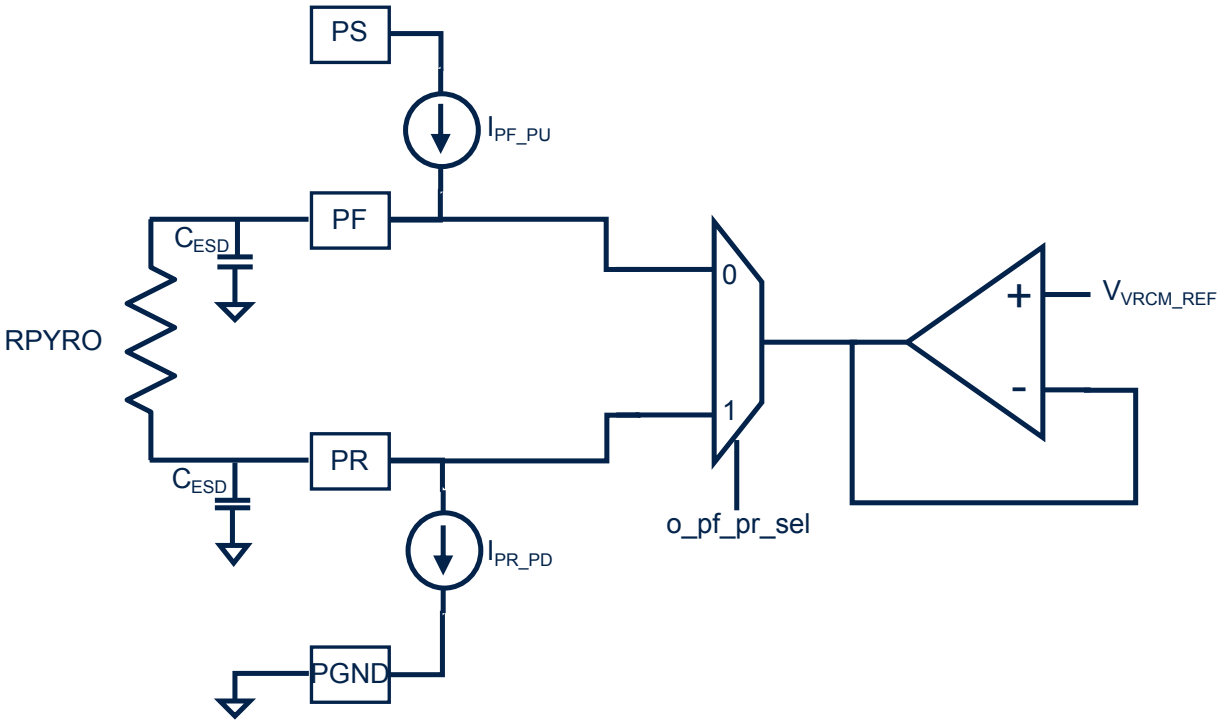
Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
PF vs PR pre-deploy HWSC fail	If either an offset or gain error is detected during the PF vs PR pre-deployment HWSC, the pre-deploy HWSC fail is acknowledged	The PF_PR_PRE_HWSC_FAIL flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of ADC HWSC step Cyclic diagnostic triggers are inhibited	The fault flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***ADC_HWSC_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PF_PR_PRE_HWSC_FAULTN_MSK*** masks fault redirection on FAULTN pin
PF vs PR post-deploy HWSC fail	If either an offset or gain error is detected during the PF vs PR post-deployment HWSC, the post-deploy HWSC fail is acknowledged	The PF_PR_POST_HWSC_FAIL flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of ADC HWSC step Cyclic diagnostic triggers are inhibited	The fault flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***ADC_HWSC_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PF_PR_POST_HWSC_FAULTN_MSK*** masks fault redirection on FAULTN pin
VRCM HWSC fail	If an error is detected during the VRCM vs PGND HWSC, the VRCM HWSC fail is acknowledged	The VRCM_HWSC_FAIL flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of ADC HWSC step Cyclic diagnostic triggers are inhibited	The fault flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***ADC_HWSC_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***VRCM_HWSC_FAULTN_MSK*** masks fault redirection on FAULTN pin

3.7.2.3 *VRCM check*

This step aims at diagnosing the voltage regulator/current monitor (VRCM) works properly.

This test requires **HWSC (hardware self-check)** prior to execution to cover possible faults determining VRCM is out of range. To achieve safety targets, it is strongly recommended to apply such strategy before running this test.

Figure 20. VRCM test



The VRCM can be checked verifying the VRCM multiplexer connections to the PF or PR pins:

- STB check:
  - The I_{PF_PU} generator is connected to PF pin.
  - The VRCM is connected to PF pin.
  - If the VRCM works properly the VRCM_STB_FAIL flag remains zero.
- STG check:
  - The I_{PR_PD} generator is connected to PR pin.
  - The VRCM is connected to PR pin.
  - If the VRCM works properly the VRCM_STG_FAIL flag remains zero.

This test allows to check the $I_{LEAK\_SOURCE\_TH}$ and $I_{LEAK\_SINK\_TH}$ current thresholds.

The VRCM check diagnostic step duration is t_{VRCM_CHECK}.

Table 24. VRCM STB/STG diagnostics

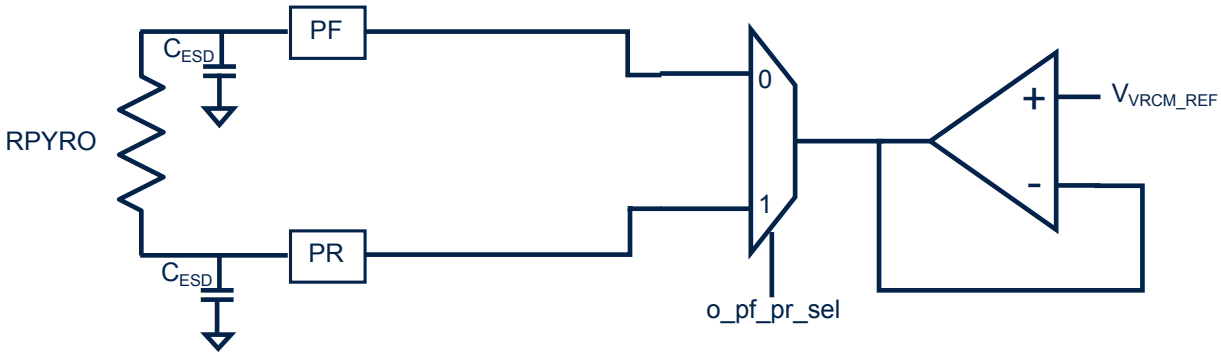
Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
LEAK SINK LOW	When I_{PF_PU} is enabled, if the STB flag is not internally set after $t_{VRCM\_LEAK\_FLT}$ expired, the VRCM_STB_FAIL fault is acknowledged	The VRCM_STB_FAIL flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of the leakage current test step Cyclic diagnostic triggers are inhibited	The VRCM_STB_FAIL flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***LEAK_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***LEAK_LOW_FAULTN_MSK*** masks fault redirection on FAULTN pin
LEAK SOURCE LOW	When I_{PR_PD} is enabled, if the STG flag is not internally set after $t_{VRCM\_LEAK\_FLT}$ expired, the VRCM_STG_FAIL fault is acknowledged	The VRCM_STG_FAIL flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of the leakage current test step Cyclic diagnostic triggers are inhibited	The VRCM_STG_FAIL flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***LEAK_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***LEAK_LOW_FAULTN_MSK*** masks fault redirection on FAULTN pin

3.7.2.4 *Pyro outputs leakage test*

This step aims at verifying that PF/PR pins are floating, with no parasitic leakage towards battery or ground.

This test requires the **VRCM check** to verify that VRCM output and diagnostic thresholds are in range. To achieve safety targets, it is strongly recommended to apply such a strategy before running this test.

Figure 21. Pyro outputs leakage test



The diagnostic works as follows:

- PF leakage test:
  - The VRCM is connected to PF and starts charging the PF node to V_{VRCM_REF}.
  - If no leakage is present, the voltage on PF pin is V_{VRCM_REF} and no current is sunk or sourced by the VRCM.
  - If there is a leakage to battery, the VRCM sinks current trying to force V_{VRCM_REF}. If the sunk current is greater than $I_{LEAK\_SINK\_TH}$ for $t_{VRCM\_LEAK\_FLT}$, the PF_STB flag is set.
  - If there is a leakage to the ground, the VRCM sources current trying to force V_{VRCM_REF}. If the sourced current is greater than $I_{LEAK\_SOURCE\_TH}$ for $t_{VRCM\_LEAK\_FLT}$, the PF_STG flag is set.
- PR leakage test:
  - The VRCM is connected to the PR and starts charging the PR node to V_{VRCM_REF}.
  - If no leakage is present, the voltage on PR pin is V_{VRCM_REF} and no current is sunk or sourced by the VRCM.
  - If there is a leakage to battery, the VRCM sinks current trying to force V_{VRCM_REF}. If the sunk current is greater than $I_{LEAK\_SINK\_TH}$ for $t_{VRCM\_LEAK\_FLT}$, the PR_STB flag is set.
  - If there is a leakage to ground, the VRCM sources current trying to force V_{VRCM_REF}. If the sourced current is greater than $I_{LEAK\_SOURCE\_TH}$ for $t_{VRCM\_LEAK\_FLT}$, the PR_STG flag is set.

The leakage test diagnostic step duration is t_{LEAK_TEST}.

Table 25. PR/PF leakage diagnostics

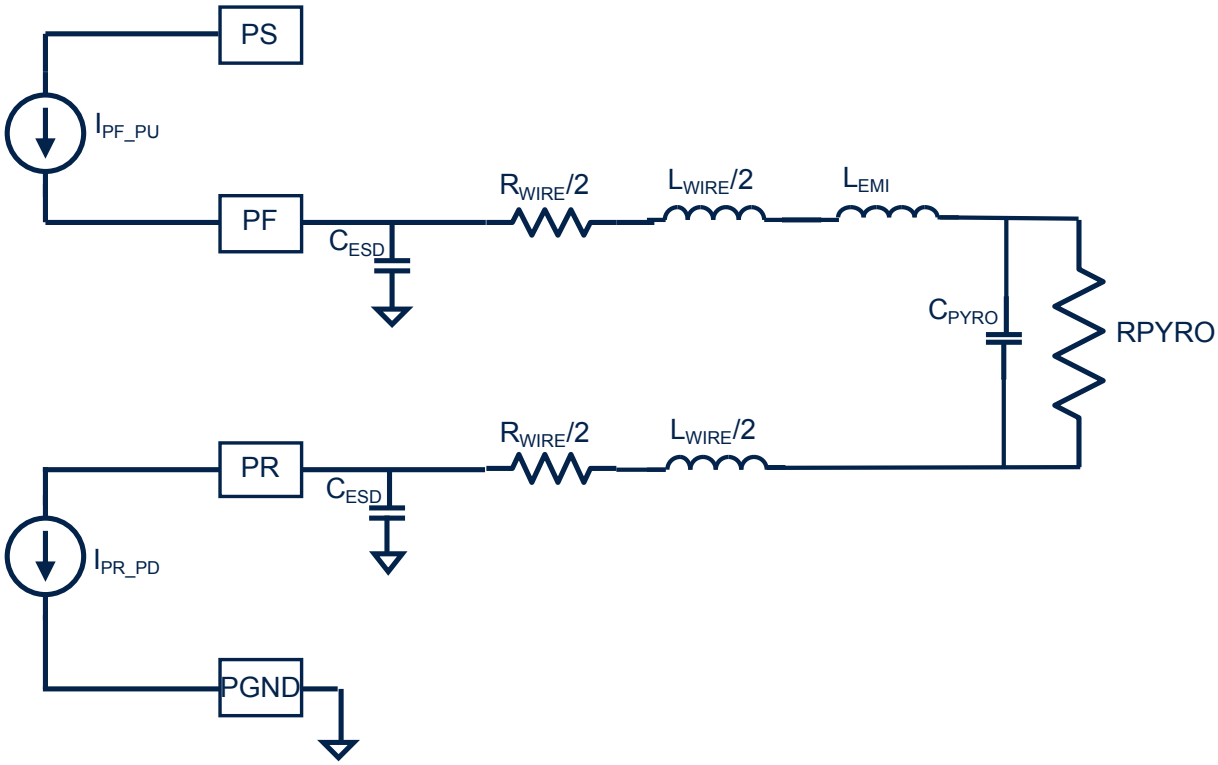
Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
PF STG	If the VRCM current exceeds $I_{LEAK\_SOURCE\_TH}$ for an interval longer than $t_{VRCM\_LEAK\_FLT}$, the PF_STG fault is acknowledged	The PF_STG flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of the leakage step Cyclic diagnostic triggers are inhibited	The PF_STG flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***LEAK_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PF_PR_STB_STG_FAULTN_MSK*** masks fault redirection on FAULTN pin
PF STB	If the VRCM current exceeds $I_{LEAK\_SINK\_TH}$ for an interval longer than $t_{VRCM\_LEAK\_FLT}$, the PF_STB fault is acknowledged	The PF_STB flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of the leakage step Cyclic diagnostic triggers are inhibited	The PF_STB flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***LEAK_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PF_PR_STB_STG_FAULTN_MSK*** masks fault redirection on FAULTN pin
PR STG	If the VRCM current exceeds $I_{LEAK\_SOURCE\_TH}$ for an interval longer than $t_{VRCM\_LEAK\_FLT}$, the PR_STG fault is acknowledged	The PR_STG flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of the leakage step Cyclic diagnostic triggers are inhibited	The PR_STG flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***LEAK_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PF_PR_STB_STG_FAULTN_MSK*** masks fault redirection on FAULTN pin
PR STB	If the VRCM current exceeds $I_{LEAK\_SINK\_TH}$ for an interval longer than $t_{VRCM\_LEAK\_FLT}$, the PR_STB fault is acknowledged	The PR_STB flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of the leakage step Cyclic diagnostic triggers are inhibited	The PR_STB flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***LEAK_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PF_PR_STB_STG_FAULTN_MSK*** masks fault redirection on FAULTN pin

3.7.2.5 *Pyro igniter resistance measurement*

This step aims at measuring the pyro-fuse igniter circuit resistance and verifying that it lays within safety-limits.

This test requires **HWSC (hardware self-check)** prior to execution to cover possible faults determining measurement error out of range. It also requires the **VRCM check** to verify that test currents are in range. To achieve safety targets, it is strongly recommended to apply such a strategy before running this test.

Figure 22. Pyro igniter resistance measurement



The diagnostic works as follows:

- The I_{PF_PU} and I_{PR_PD} currents are enabled, so that a I_{PF_PU} current flows through PF and PR.
- The IC waits for the differential voltage settling between PF and PR.
- The ADC converts the PF vs PR differential voltage and compares the obtained V_{PYRO} result to the $V_{RES\_LOW\_TH}$ and $V_{RES\_HIGH\_TH}$ limits.
- The I_{PF_PU} and I_{PR_PD} currents are disabled.

The pyro resistance sensitivity can be computed as follows:

$$R_{PYRO} = \frac{V_{PYRO}}{I_{PF_{PU}}} \Rightarrow \frac{\partial R_{PYRO}}{\partial V_{PYRO}} = \frac{1}{I_{PF_{PU}}} = 25\frac{\Omega}{V} \cong 16.275\frac{m\Omega}{LSB} \quad (3)$$

The $V_{RES\_LOW\_TH}$ and $V_{RES\_HIGH\_TH}$ thresholds can be programmed in NVM respectively in ***VRES_LOW_TH*** and ***VRES_HIGH_TH*** bit fields.

The result is saved in the RES_MEAS_PRE register.

The resistance measurement diagnostic step duration is t_{RES_MEAS}.

Table 26. Pyro igniter diagnostics

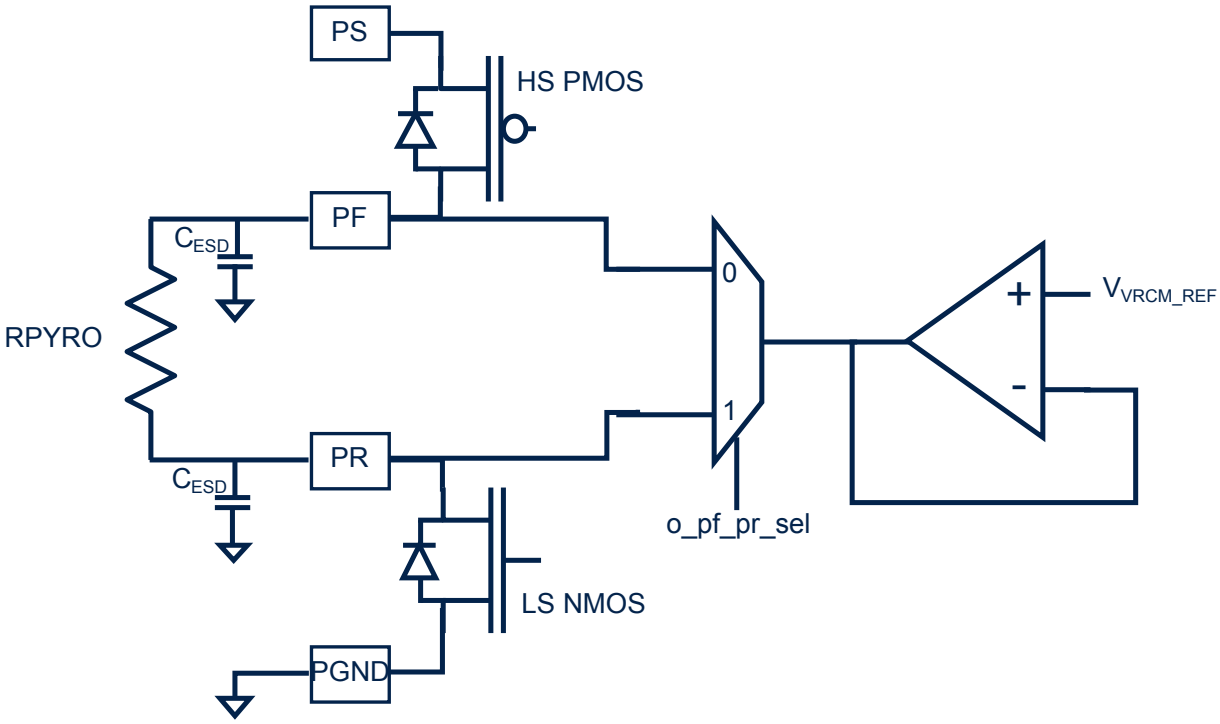
Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Pyro low resistance	If the PF vs PR converted voltage is lower than $V_{RES\_LOW\_TH}$ the PYRO_LOW_RES fault is acknowledged	The PYRO_LOW_RES flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of PYRO RES step Cyclic diagnostic triggers are inhibited	The PYRO_LOW_RES flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***PYRO_RES_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PYRO_LOW_RES_FAULTN_MSK*** masks fault redirection on FAULTN pin
Pyro high resistance	If the PF vs PR converted voltage is higher than $V_{RES\_HIGH\_TH}$ the PYRO_HIGH_RES fault is acknowledged	The PYRO_HIGH_RES flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of PYRO RES step Cyclic diagnostic triggers are inhibited	The PYRO_HIGH_RES flag can always be cleared on read	FAULTN line is released Cyclic diagnostic triggers are unmasked	***PYRO_RES_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PYRO_HIGH_RES_FAULTN_MSK*** masks fault redirection on FAULTN pin

3.7.2.6 *Pyro deployment FETs test*

This step aims at verifying that HS and LS FETs can be switched ON/OFF.

This test requires **HWSC (hardware self-check)** prior to execution to cover possible faults determining VRCM out of range. It also requires the VRCM check to verify that diagnostic currents are in range. To achieve safety targets, it is strongly recommended to apply such a strategy before running this test.

Figure 23. HS/LS deployment FETs test



The diagnostic works as follows:

- PF (HS) switch test:
  - The VRCM is connected to PF pin.
  - The HS FET is turned ON.
  - The VRCM sinks current trying to maintain V_{VRCM_REF}.
  - If the FET is working properly, this current exceeds the threshold $I_{LEAK\_SINK\_TH}$ for the filter time $t_{FET\_TEST\_FLT}$, the PF_FET_STB flag is set and the HS FET is turned off immediately.
- PR (LS) switch test:
  - The VRCM is connected to PR pin.
  - The LS FET is turned ON.
  - The VRCM sources current trying to maintain V_{VRCM_REF}.
  - If the FET is working properly, this current exceeds the threshold $I_{LEAK\_SOURCE\_TH}$ for the filter time $t_{FET\_TEST\_FLT}$, the PR_FET_STG flag is set and the LS FET is turned off immediately.

The FETs test diagnostic step duration is t_{FET_TEST}.

In both tests the current on PF and PR pins will not exceed the VRCM current limits $I_{VRCM\_SOURCE\_LIM}$ or $I_{VRCM\_SINK\_LIM}$. During FETs test, energy available to the load is limited to less than E_{FET_TEST}.

Table 27. HS/LS FETs diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
PF FET STG fail	If, during the HS ON phase, the VRCM current raises above $I_{LEAK\_SOURCE\_TH}$ for longer than $t_{FET\_TEST\_FLT}$, the PF_FET_STG fault is acknowledged	The PF_FET_STG flag is set FAULTN line is asserted Diagnostic routine is stopped immediately and the PF command will be set OFF Cyclic diagnostic triggers are inhibited The “fire inhibit” signal is set	The fault flag can only be cleared in case the diagnostic is retriggered manually and gives a positive outcome	FAULTN line is released Cyclic diagnostic triggers are unmasked	***HS_LS_FET_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PF_FET_FAIL_FAULTN_MSK*** masks fault redirection on FAULTN pin ***PF_FET_FAIL_FIRE_MSK*** masks the inhibition of pyro-fuse fire commands
PF FET fail	If, during HS ON phase, the VRCM current does not exceed the threshold $I_{LEAK\_SINK\_TH}$, after $t_{FET\_TEST\_TO}$ the test is terminated and the FET is turned-off	The PF_FET_FAIL flag is set FAULTN line is asserted Diagnostic routine is stopped immediately Cyclic diagnostic triggers are inhibited The “fire inhibit” signal is set	The fault flag can only be cleared in case the diagnostic is retriggered manually and gives a positive outcome	FAULTN line is released Cyclic diagnostic triggers are unmasked	***HS_LS_FET_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PF_FET_FAIL_FAULTN_MSK*** masks fault redirection on FAULTN pin ***PF_FET_FAIL_FIRE_MSK*** masks the inhibition of pyro-fuse fire commands
PR FET STB fail	If, during the LS ON phase, the VRCM current raises above $I_{LEAK\_SINK\_TH}$ for longer than $t_{FET\_TEST\_FLT}$, the PR_FET_STB fault is acknowledged	The PR_FET_STB flag is set FAULTN line is asserted Diagnostic routine is stopped immediately and the PR command will be set OFF Cyclic diagnostic triggers are inhibited The “fire inhibit” signal is set	The fault flag can only be cleared in case the diagnostic is retriggered manually and gives a positive outcome	FAULTN line is released Cyclic diagnostic triggers are unmasked	***HS_LS_FET_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PR_FET_FAIL_FAULTN_MSK*** masks fault redirection on FAULTN pin ***PR_FET_FAIL_FIRE_MSK*** masks the inhibition of pyro-fuse fire commands
PR FET fail	If, during LS ON phase, the VRCM current does not exceed the threshold $I_{LEAK\_SOURCE\_TH}$, after $t_{FET\_TEST\_TO}$ the test is terminated and the FET is turned-off	The PR_FET_FAIL flag is set FAULTN line is asserted Diagnostic routine is stopped immediately Cyclic diagnostic triggers are inhibited The “fire inhibit” signal is set	The fault flag can only be cleared in case the diagnostic is retriggered manually and gives a positive outcome	FAULTN line is released Cyclic diagnostic triggers are unmasked	**HS_LS_FET_EN** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***PR_FET_FAIL_FAULTN_MSK*** masks fault redirection on FAULTN pin ***PR_FET_FAIL_FIRE_MSK*** masks the inhibition of pyro-fuse fire commands

Table 28. FETs test results

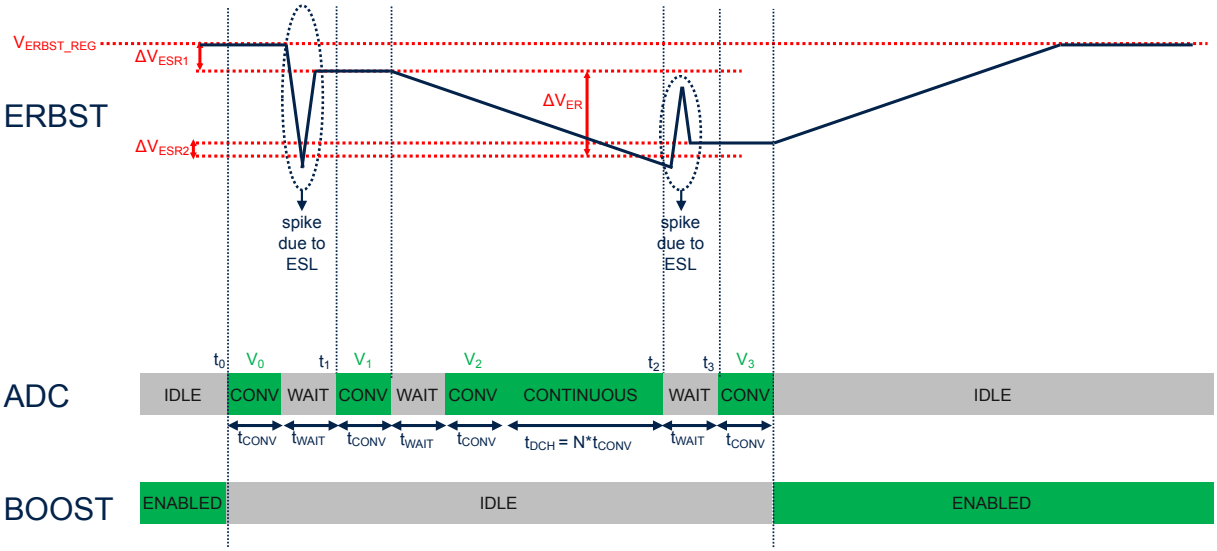
PR_STG	PF_STB	Result
PF(HS) FET test		
0	0	PF FET fail
0	1	PF FET test pass OR leakage to battery
1	0	PF STG fail
1	1	PF FET test pass OR leakage to battery followed by leakage to ground
PR(LS) FET test		
0	0	PR FET fail
0	1	PR STB fail
1	0	PR FET test pass OR leakage to ground
1	1	PR FET test pass OR leakage to ground followed by leakage to battery

3.7.2.7 *ER capacitor diagnostic*

This step aims at verifying the integrity of the energy reserve capacitor (ER CAP). This is achieved by measuring the following quantities:

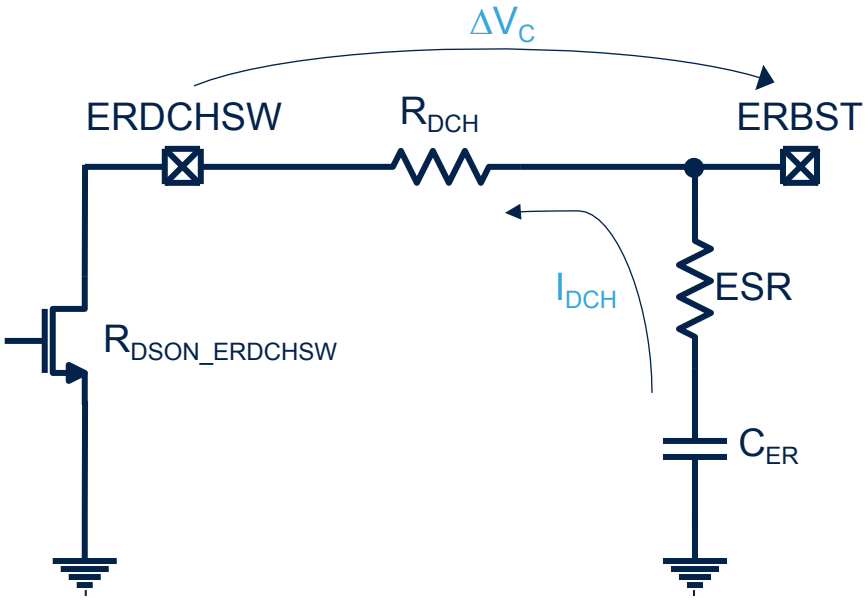
- Effective capacitance value of C_{ERBST} electrolytic capacitor.
- Equivalent series resistance (ESR) of C_{ERBST} electrolytic capacitor.

Figure 24. ER capacitor diagnostic



These two measurements are done by the IC at the same time, by activating the ER discharge switch and measuring the voltage drop on ERBST pin and current flowing in $R_{ERDCHSW}$.

Figure 25. **ER cap discharge path**



The ER discharge switch is an integrated switch that creates a low-ohmic path between the ER capacitor connected to ERDCHSW pin and ground. In the standard application scenario with ERBST mounted, the ERDCHSW is externally connected to the ER capacitor with an external resistor (R_{DCHG}). So, this resistor defines the current used during the discharge phase of the ER capacitor diagnostic.

The ER discharge switch can also be controlled via SPI with the ERDCHSW_EN bit located in the ERCAP register.

The ERDCHSW_EN bit is set by the microcontroller but it is automatically cleared and ERDCHSW is disabled when the energy stored in the ER cap is needed as energy reserve:

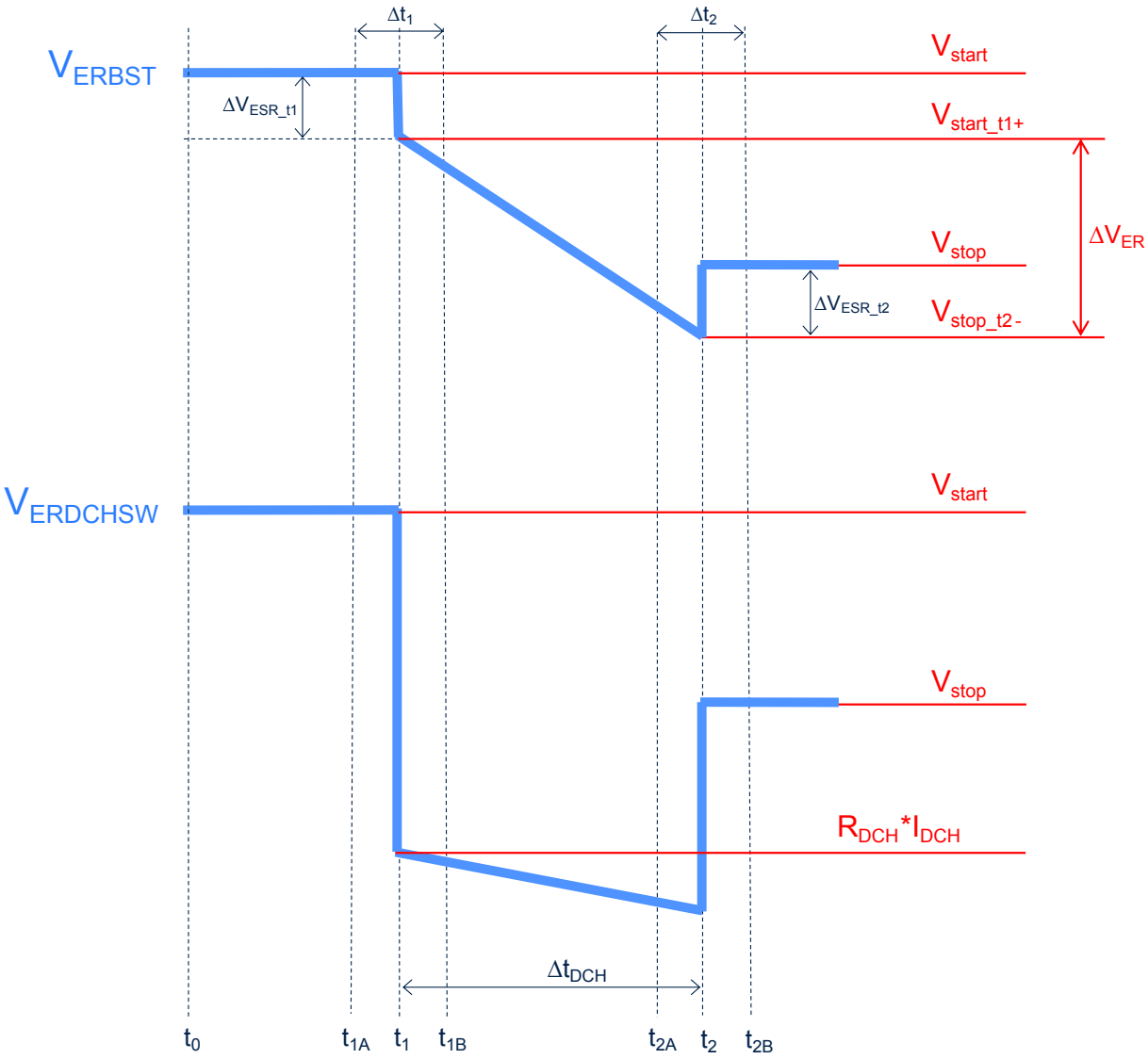
- For the device itself when it enters the DEEP-SLEEP state.
- For deployment event when the IC enters ARM state.
- For ER cap diagnostic when the IC enters DIAG state.

Note: There is no constraint between the ERBST enable and the ERDCHSW enable, so it is under the user's responsibility to prevent a possible conflict and avoid an excessive thermal heating in the integrated ER discharge switch.

The ER discharge switch has an overcurrent protection feature performed through a voltage comparator that monitors the V_{DS} voltage of the switch. When the voltage on ERDCHSW pin exceeds $V_{ERDCHSW\_OV\_H}$ for a time longer than $t_{ERDCHSW\_FLT}$, the switch is disabled, the FAULTN pin goes low and the ERDCHSW_OV bit in the ERCAP register is set to 1. The switch is re-enabled if the voltage on ERDCHSW pin is lower than $V_{ERDCHSW\_OV\_L}$ for a time longer than $t_{ERDCHSW\_FLT}$ (fault is considered as disappeared) and the ERDCHSW_OV bit is read and cleared. The ERDCHSW_OV is mapped to FAULTN. This fault can be triggered only during ER cap diagnostic or if ERDCHSW_EN = 1.

Referring to a simplified schematic of the Figure 25, typical V_{ERBST} and $V_{ERDCHSW}$ discharge profiles are shown in the Figure 26.

Figure 26. **ER cap discharge pins voltage profiles**



To perform capacitance and ESR measurements, the device has two dedicated ADCs: one for voltages' measurement, one for current measurement.

Before to run the diagnostic, the user should write:

- Capacitance threshold via ***ERCAP_C_THR[7:0]*** bit field in NVM, precalculated by the user using the following formula:

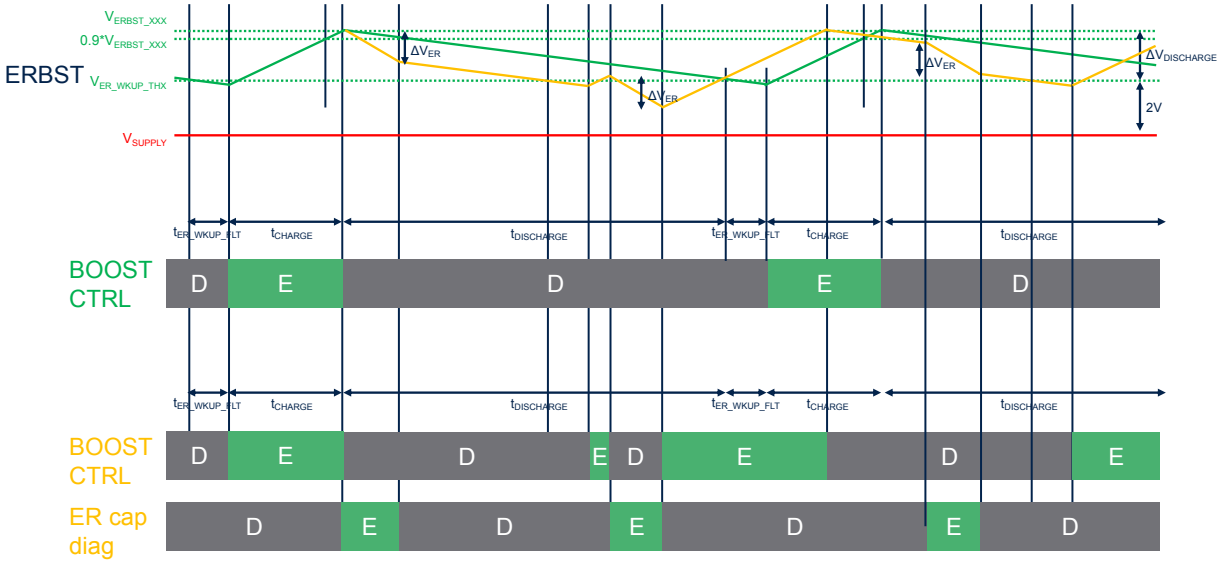
$$C\left[\mu F\right] = \frac{(\text{"00"\&}ERCAP\_C\_THR[7:0]\text{\&"0000"}) \times LSB_C}{R_{ERDCHSW}} \quad (4)$$

- ESR threshold via and ***ERCAP_ESR_THR[6:0]*** bit field in NVM, precalculated by the user using the following formula:

$$ESR\left[m\Omega\right] = \left(ERCAP\_ESR\_THR[6:0]\text{\&"0000"}\right) \times \frac{LSB_{ESR} \times R_{ERDCHSW}}{1000} \quad (5)$$

To reduce the noise during the measurement step, the ERBST is automatically disabled during the ER capacitor diagnostic (see the Figure 27).

Figure 27. **ERBST management during ER cap diag**



The IC performs the sequence of measurements automatically and saves the calculations in the CAP_VALUE[13:0] and ESR_VALUE[12:0] bit fields.

A timeout $t_{ER\_CAP\_DIAG\_TO}$ for diagnostic duration is present. If it is exceeded, the process is halted and the ERCAP_DIAG_END_TO flag is set in the ERCAP register.

If the diagnostic ends within the timeout, the device saves the CAP_VALUE in ERCAP_DIAG_CAP_READ_0 and ERCAP_DIAG_CAP_READ_1 registers, and the ESR_VALUE in ERCAP_DIAG_ESR_READ_0 and ERCAP_DIAG_ESR_READ_1 registers.

At this point the IC automatically compares CAP_VALUE and ESR_VALUE with the thresholds previously saved in NVM, respectively ***ERCAP_C_THR*** and ***ERCAP_ESR_THR***.

The FAULTN line is asserted:

- If CAP_VALUE[13:0] < (“00” & ERCAP_C_THR[7:0] & “0000”), and ERCAP_LOW_C flag is set in the ERCAP register.
- If ESR_VALUE[12:0] > (ERCAP_ESR_THR[6:0] & “0000”), and ERCAP_HIGH_ESR flag is set in the ERCAP register.

Note: A high threshold is defined for capacitance value and a low threshold for ESR since, due to aging and thermal stress, an electrolytic capacitor over the years shows a decrease of the capacitance value and an increase of the ESR.

Knowing $R_{ERDCHSW}$, the MCU can check C and ESR calculation values as follows:

$$C = CAP\_VALUE\left[13:0\right] \times LSB_C \times \frac{1}{R_{ERDCHSW}} \quad (6)$$

$$ESR = ESR\_VALUE[12:0] \times LSB_{ESR} \times R_{ERDCHSW} \quad (7)$$

Once started, the ER capacitor diagnostic process can only be interrupted by a deployment request.

Once a request is over, to proceed with a new one the ER_CAP bit must be left at 1 and the DIAG_START bit in the DIAG_CMD register must be set back to 1 (it returns automatically to 0).

The ER capacitor diagnostic step duration is dependent on the capacitor value, as specified by $t_{ER\_CAP\_DIAG1}$ and $t_{ER\_CAP\_DIAG2}$.

The possible results of ER capacitor diagnostics are reported in the Table 29.

Table 29. ER capacitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Low capacitance value of ER cap	If the converted CAP_VALUE is lower than the capacitance threshold, the low capacitance fault is acknowledged	The ERCAP_LOW_C flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of ER cap diagnostic step	The fault flag can always be cleared on read	FAULTN line is released	***ER_CAP_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***ERCAP_FAULTN_MSK*** masks fault redirection on FAULTN pin
High ESR value of ER cap	If the converted ESR_VALUE is higher than the ESR threshold, the high ESR fault is acknowledged	The ERCAP_HIGH_ESR flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of ER cap diagnostic step	The fault flag can always be cleared on read	FAULTN line is released	***ER_CAP_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***ERCAP_FAULTN_MSK*** masks fault redirection on FAULTN pin
Capacitance or ESR out of range	If the converted CAP_VALUE or the converted ESR_VALUE are out of range, the out of range fault is acknowledged	The ERCAP_OUT_OF_RANGE flag is set FAULTN line is asserted Diagnostic routine is stopped at the end of ER cap diagnostic step	The fault flag can always be cleared on read	FAULTN line is released	***ER_CAP_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***ERCAP_FAULTN_MSK*** masks fault redirection on FAULTN pin
ER cap diagnostic timeout	If the diagnostic time exceeds $t_{ER\_CAP\_DIAG\_TO}$ timeout, the diagnostic timeout fault is acknowledged	The ERCAP_DIAG_END_TO flag is set FAULTN line is asserted Diagnostic routine will be stopped at the end of ER cap diagnostic step	The fault flag can always be cleared on read	FAULTN line is released	***ER_CAP_EN*** = 0 masks cyclic diagnostic trigger (but not the on-demand one) ***ERCAP_FAULTN_MSK*** masks fault redirection on FAULTN pin

3.7.3 Diagnostic routine electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 30. Diagnostic routine electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$t_{DIAG\_ROUTINE\_PERIOD\_00}$	Diagnostic routine execution period in NORMAL	***DIAG_ROUTINE_PERIOD*** = 00	85	100	115	ms	-
$t_{DIAG\_ROUTINE\_PERIOD\_01}$		***DIAG_ROUTINE_PERIOD*** = 01	255	300	345	ms	-
$t_{DIAG\_ROUTINE\_PERIOD\_10}$		***DIAG_ROUTINE_PERIOD*** = 10	425	500	575	ms	-
$t_{DIAG\_ROUTINE\_PERIOD\_11}$		***DIAG_ROUTINE_PERIOD*** = 11	595	700	805	ms	-
N_{CYCLE_00}	Cyclic periodicity configuration	***<DIAG_X>_NCYCLE*** = 00	-	1	-	cycles	-
N_{CYCLE_01}		***<DIAG_X>_NCYCLE*** = 01	-	4	-	cycles	-
N_{CYCLE_10}		***<DIAG_X>_NCYCLE*** = 10	-	16	-	cycles	-
N_{CYCLE_11}		***<DIAG_X>_NCYCLE*** = 11	-	64	-	cycles	-
t_{ABIST}	ABIST duration		-	0.3	-	ms	-
ERR_{HWSC}	ADC HWSC error		-52	-	52	LSB	PS, PF, PR, PGND
t_{HWSC}	HWSC time duration		-	1.5	-	ms	PS, PF, PR, PGND
I_{PF_PU}	PF pullup diagnostic current		38	40	42	mA	PF
SR_{IPF_PU}	PF pullup diag current slew rate		150	200	250	µA/µs	PF
I_{PR_PD}	PR pulldown diagnostic current		50	75	100	mA	PR
V_{VRCM_REF}	VRCM regulated voltage		2.25	2.5	2.75	V	PF, PR
$I_{VRCM\_SOURCE\_LIM}$	VRCM source current limitation		-20	-	-10	mA	PF, PR
$I_{VRCM\_SINK\_LIM}$	VRCM sink current limitation		10	-	20	mA	PF, PR
$t_{VRCM\_LEAK\_FLT}$	Deglitch filter time for STB/STG detection	Guaranteed by SCAN	17	20	23	µs	PF, PR
t_{VRCM_CHECK}	VRCM check time duration		-	-	1.6	ms	PF, PR
$I_{LEAK\_SOURCE\_TH}$	Leakage to ground (STG) threshold for VRCM regulator		57	-	145	µA	PF, PR
$I_{LEAK\_SINK\_TH}$	Leakage to battery (STB) threshold for VRCM regulator		57	-	145	µA	PF, PR
R_{LEAK_TH}	Equivalent leakage resistance threshold	Application information Detection is guaranteed below minimum No detection is guaranteed above maximum	15	-	48	kΩ	PF, PR

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
t_{LEAK_TEST}	Leakage test time duration		-	-	1.6	ms	PF, PR
t_{RES_MEAS}	Pyro igniter resistance measurement time duration		-	-	0.6	ms	PF, PR
$V_{RES\_LOW\_TH}$	Pyro igniter resistance low threshold (7 bit)	$V_{RES\_LOW\_TH}$ = 4 * $V_{ADC\_LSB\_0}$ * CODE Guaranteed by SCAN	0	-	1.21	V	PF, PR
$V_{RES\_HIGH\_TH}$	Pyro igniter resistance high threshold (7 bit)	$V_{RES\_LOW\_TH}$ = 4 * $V_{ADC\_LSB\_0}$ * CODE Guaranteed by SCAN	0	-	1.21	V	PF, PR
ERR_{TOT_PRM}	Pyro igniter resistance measurement total error		-8	-	8	%	PF, PR
$t_{FET\_TEST\_FLT}$	Deglitch filter time for STB/STG detection during FETs test		0.85	1	1.15	µs	PF, PR
$t_{FET\_TEST\_TO}$	LS/HS FET test timeout		190	200	210	µs	PF, PR
t_{FET_TEST}	FET test time duration		-	-	0.2	ms	PF, PR
E_{FET_TEST}	Energy transferred to load during FETs test	Design info	-	-	170	µJ	PF, PR
$R_{DSON\_ERDCHSW}$	ER discharge switch ON resistance	$I_{ERDCHSW}$ = 0.5 A	0.25	-	2.2	Ω	ERDCHSW
$V_{ERDCHSW\_OV\_H}$	ER discharge switch VDS monitor overvoltage threshold	Low to high	3.4	-	3.8	V	ERDCHSW
$V_{ERDCHSW\_OV\_L}$	ER discharge switch VDS monitor overvoltage threshold	High to low	3.0	-	3.4	V	ERDCHSW
$t_{ERDCHSW\_FLT}$	ER discharge switch filter time		8	10	12	µs	ERDCHSW
V_{DCH}	V_{ERBST}-$V_{ERDCHSW}$ input differential measurement range	ER cap diagnostic	15	-	30	V	ERBST ERDCHSW
V_{DCH_LSB}	V_{ERBST}-$V_{ERDCHSW}$ input differential measurement LSB	ER cap diagnostic	-	8.8	-	mV	ERBST ERDCHSW
V_{DCH_ACC}	V_{ERBST}-$V_{ERDCHSW}$ voltage measurement accuracy	15 V < V_{ERBST} – $V_{ERDCHSW}$ < 30 V	-5	-	5	%	ERBST ERDCHSW
$N_{DCH\_INTG\_BIT}$	Integral of V_{ERBST}-$V_{ERDCHSW}$ internal number of bits	Design info	-	12	-	bit	ERBST ERDCHSW
ΔV_{ER}	ER cap discharge voltage range during ER cap diagnostic	Design info	0	-	1.15	V	ERBST
ΔV_{ER_LSB}	ER cap discharge voltage LSB during ER cap diagnostic	Dedicated 12-bit ADC to directly convert differential voltage	-	352	-	µV	ERBST
ΔV_{ER_ACC}	ER cap discharge voltage measurement accuracy	Dedicated 12-bit ADC to directly convert differential voltage	-70	-	+70	mV	ERBST

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ΔV_{ER_CAP}	ER cap discharge voltage due to capacitance		0.4	-	0.7	V	ERBST
ΔV_{ER_ESR}	ER cap discharge voltage due to ESR	Design info	0.1	-	0.45	V	ERBST
$t_{ER\_CAP\_DIAG1}$	ER cap diag total running time	Design info with 100 µF V_{ERBST} = 20 V, R_{DCHG} = 62 Ω	-	0.63	-	ms	ERBST ERDCHSW
$t_{ER\_CAP\_DIAG2}$	ER cap diag total running time	Design info with 1.2 mF V_{ERBST} = 20 V, R_{DCHG} = 62 Ω	-	2.3	-	ms	ERBST ERDCHSW
LSB_{ESR}	ESR/$R_{ERDCHSW}$	Design info	-	38.52	-	µ	-
LSB_C	$R_{ERDCHSW}$*C_{ER}	Design info	-	25.35	-	µF*Ω	-
$t_{S\_ER\_CAP}$	Sample time of each conversion on voltage ADCs	Design info	-	64	-	µs	-
t_{LOCK_ER}	Time needed for t_{START} conversion	Design info	-	464	-	µs	-
$t_{ER\_MEAS\_DELAY}$	Time to reach steady state after ERDCHSW enabled	Design info	-	64	-	µs	-
$t_{ER\_CAP\_DIAG\_TO}$	ER cap diag timeout	Design info	-	-	25	ms	-

3.8 Voltage ADC

The IC implements a multichannel, fully differential 10-bit ADC for internal and external voltage measurements.

The ADC supports the following 7 inputs:

- PS, PF, PR, PGND, used for on-demand conversions and by the diagnostic routine
- VRCM, used by the diagnostic routine
- ERBST, used for on-demand conversions and by the diagnostic routine
- GND, used for on-demand conversions and by the diagnostic routine

The ADC is designed to convert any of the following 7 paths:

- PS vs PGND
- PF vs PGND
- PR vs PGND
- PF vs PR in high resolution (pre-deployment), with I_{PF_PU} and I_{PR_PD} enabled
- PF vs PR in low resolution (post deployment), with I_{PF_PU} and I_{PR_PD} enabled
- ERBST vs GND
- VRCM vs GND (VRCM enabled)

The ADC conversion formula is the following:

$$V_{ADC} = LSB \times CODE \quad (8)$$

Where LSB is $V_{ADC\_LSB\_x}$ (according to conversion requested) and CODE is a 10-bit signed word.

3.8.1 Measurement trigger modes

The ADC supports three different conversion execution modes:

- On-Demand, triggered by MCU writing ADC_CONV_CMD bit equal to 1 and configuring the input channel with the AMUX_CONF bit field in the same command frame (see the Table 31):
  - This type of request does not move the FSM to DIAG state.
  - Results of the on-demand ADC conversions are available in the ADC_CONV_RESULT register when ADC_CONV_RDY bit is set to 1.
  - If the ADC is just busy, the ADC_BUSY bit is set to 1.
- Cyclically:
  - In full-power mode (CWUP = 1, static), the diagnostic routine runs every $t_{DIAG\_ROUTINE\_PERIOD}$. The voltage ADC is involved in some diagnostic steps (if such steps are enabled).
  - In low-power mode (periodic CWUP pulses), the diagnostic routine is executed at every wake-up.
  - These types of requests move the FSM to DIAG state.
- Asynchronously:
  - If the FSM moves to the ARM state, the ADC is used for post-deployment resistance measurement if selected as the FIRE_GOOD source.
  - The result of this conversion is reported in the RES_MEAS_POST register.

Conflict between multiple triggers is managed as follows:

- If the FSM is in DIAG state (either triggered by CWUP in low-power mode or triggered by the MCU in full-power mode), on-demand triggers are discarded.

Note: When in low-power mode, the FSM moves to DIAG upon cyclic powerups. Hence, the cyclic execution of the diagnostic routine is guaranteed by design.

- If an on-demand conversion is being performed, the cyclic execution of the diagnostic routine is skipped and it will be performed upon the next useful trigger period.
- In any case, if the FSM moves to the ARM state, any ongoing conversion is interrupted and the ADC will be set up for post-deployment resistance measurement. This deployment trigger has the highest priority.

Table 31. ADC input channel selection for on-demand conversions

AMUX_CONF	Channel
000	PS vs PGND
001	PF vs PGND
010	PR vs PGND
011	PF vs PR (high resolution - pre deployment)
100	PF vs PR (low resolution - post deployment)
101	ERBST vs GNDx
110	VRCM vs PGND
111	Not used

The ADC LSB is rescaled according to the selected channel and to the diagnostic steps.

3.8.2 Voltage ADC electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 32. Voltage ADC electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V_{AIN\_RANGE\_0}$	AINx differential voltage input measurement operative range	Pyro-res measurement (PF vs PR)	0	-	300	mV
$V_{AIN\_RANGE\_1}$		Pyro-deployment retry (PF vs PR) and VRCM measurement	0	-	5	V
$V_{AIN\_RANGE\_2}$		On-demand conversions (PS, PF, PR and ERBST(1))	0	-	27.3	V
$V_{ADC\_LSB\_0}$	AINx measurement resolution	$V_{AIN\_RANGE\_0}$	-	0.651	-	mV
$V_{ADC\_LSB\_1}$		$V_{AIN\_RANGE\_1}$	-	10.69	-	mV
$V_{ADC\_LSB\_2}$		$V_{AIN\_RANGE\_2}$	-	55.27	-	mV
N_{BIT_ADC}	ADC bit number	Design info (signed word)	-	10	-	bit
$V_{ADC\_OFFSET\_ERR\_0}$	ADC offset error(2)	Pyro-res measurement (PF vs PR)	-5	-	5	LSB
$V_{ADC\_OFFSET\_ERR\_1}$		Pyro-deployment retry (PF vs PR)	-5	-	5	LSB
$V_{ADC\_OFFSET\_ERR\_2}$		On-demand conversions (PS, PF, PR and ERBST)	-5	-	5	LSB
$V_{ADC\_GAIN\_ERR\_0}$	ADC gain error(2)	Pyro-res measurement (PF vs PR)	-2	-	2	%
$V_{ADC\_GAIN\_ERR\_1}$		Pyro-deployment retry (PF vs PR)	-2	-	2	%
$V_{ADC\_GAIN\_ERR\_2}$		On-demand conversions (PS, PF, PR and ERBST)	-2	-	2	%
t_{ADC_CONV}	ADC conversion time	Guaranteed by SCAN	-	350	380	µs

1. *The min voltage for ERBST voltage measurement is 4.7 V (below the device is off).*
2. *Single shot samples are characterized by a superimposed Gaussian noise, with zero-mean and standard deviation.*

3.9 Oscillators

This section describes the device oscillators.

3.9.1 Main oscillator and aux oscillator

The main oscillator operates at f_{MAIN_OSC} and is disabled in DEEP-SLEEP state.

The main oscillator has a spread spectrum feature that varies its frequency instantaneously of D_{MAIN_OSC}, using $f_{MAIN\_OSC\_MOD}$ as the modulation frequency. It is enabled through the OSC_SS_EN bit in the INTERNAL_CFG register.

The aux oscillator operates at f_{STBY_OSC} and is disabled in DEEP-SLEEP state.

3.9.1.1 Oscillators electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 33. Main oscillator electrical parameters

Symbol	Parameter	Min	Typ	Max	Unit
f_{MAIN_OSC}	Main oscillator frequency	15.1	16	16.9	MHz
$f_{MAIN\_OSC\_MOD}$	Main oscillator modulation frequency	-	8	-	kHz
D_{MAIN_OSC}	Main oscillator frequency deviation due to spread spectrum	2	3	4	%
f_{STBY_OSC}	Aux oscillator frequency	460	500	540	kHz

3.9.2 Oscillator monitor

When enabled, the main and aux oscillators are cross-checking each other for detecting frequency deviations or stuck failures.

The frequency drift is detected if the deviation is higher than Δf_{MON_FAIL}, in this case the OSCI_FAIL flag in the INTERNAL_STATUS register is set and any pyro-fuse deployment is inhibited by the “fire inhibit” signal.

If an oscillator is stuck, it is detected in $t_{OSC\_STUCK\_TIMEOUT}$. In this case a POR signal is issued and the IC moves to OFF state and then to DEEP-SLEEP.

3.9.2.1 Diagnostics

Table 34. Oscillator monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Oscillator deviation	If the main oscillator deviation becomes higher than Δf_{MON_FAIL}, the oscillator fail is acknowledged	The OSCI_FAIL flag is set FAULTN line is asserted The “fire inhibit” signal is set	If the main oscillator deviation is lower than Δf_{MON_FAIL}, the fault can be cleared by MCU	FAULTN line is released Deployment is released	Non-maskable This diagnostic is only active in NORMAL and DIAG
Oscillator stuck	If no edges are present for more than $t_{OSC\_STUCK\_TIMEOUT}$, the POR occurs	The “fire inhibit” signal is set The POR occurs	Power cycle (CWUP toggle) is needed to restart again	None	Non-maskable This diagnostic is only active in NORMAL and DIAG

3.9.2.2 *Oscillators diagnostics electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 35. Oscillator monitor electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Δf_{MON_FAIL}	Oscillator delta frequency threshold	Guaranteed by SCAN	22	-	38	%
$t_{OSC\_STUCK\_TIMEOUT}$	Oscillator stuck detection timeout	Guaranteed by SCAN	-	2	-	ms

3.10 GPIOs

The device features the following GPIOs:

- CWUP, FENH, FENL, SCK, NCS are digital inputs whose receivers are available in every device state.
- SDI is a digital input whose receiver is available in DIAG, NORMAL and ARM states.
- FAULTN is an open-drain whose output buffer is available in DIAG, NORMAL and ARM states.
- SDO is a push-pull whose output buffer is available in DIAG, NORMAL and ARM states.

3.10.1 GPIOs electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 36. GPIOs electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
V_{GPIOH}	GPIO high output value	SDO, I_{SOURCE} = 2 mA	V_{VIO}-0.4	-	-	V	SDO
V_{GPIOL}	GPIO low output value	SDO, I_{SINK} = 2 mA	-	-	0.4	V	SDO
t_{GPIO_RISE}	GPIO rise time	SDO, 60 pF load	-	-	50	ns	SDO
t_{GPIO_FALL}	GPIO fall time	SDO, 60 pF load	-	-	25	ns	SDO
V_{GPIOL_OD}	GPIO low output value in open-drain configuration	FAULTN, I_{SINK} = 2 mA	-	-	0.4	V	FAULTN
$R_{FAULTN\_EXT\_PU}$	FAULTN external pull-up resistor for open-drain configurations	Application information	-1%	4.7	+1%	kΩ	FAULTN
C_{FAULTN_EXT}	FAULTN external bypass capacitor	Application information, including parasitics	-	-	1	nF	FAULTN
$R_{GPIO\_WK\_PU}$	GPIO weak pull-up resistor to 3.3 V	***FENH_PU_PD*** = 1 ***FENL_PU_PD*** = 1, NCS	0.6	1.4	2.1	MΩ	FENH, FENL, NCS
$R_{GPIO\_WK\_PD}$	GPIO weak pull-down resistor to GND	***FENH_PU_PD*** = 0 ***FENL_PU_PD*** = 0 SCK, CWUP, SDI	0.6	1.4	2.1	MΩ	FENH, FENL, SCK, CWUP, SDI, AUX3, AUX4
$V_{GPIO\_IN\_HIGH}$	GPIO high input level	FENH, FENL, NCS, SCK, CWUP, SDI	2	-	-	V	FENH, FENL, NCS, SCK, CWUP, SDI
$V_{GPIO\_IN\_LOW}$	GPIO low input level	FENH, FENL, NCS, SCK, CWUP, SDI	-	-	0.7	V	FENH, FENL, NCS, SCK, CWUP, SDI
C_{GPIO_EXT}	GPIO external bypass capacitor	FENH, FENL, NCS, SCK, CWUP, SDI Application information, including parasitics	-	-	100	pF	FENH, FENL, NCS, SCK, CWUP, SDI

3.11 Internal monitors

To guarantee the correct behavior of all the analog circuitry, the IC implements two identical and independent reference generators. They constantly monitor each other while in DIAG, NORMAL and ARM states. In case of failure, FAULTN pin is asserted, BIAS_WARNING bit in the INTERNAL_STATUS register is set and the deployment is inhibited by the “fire inhibit” signal.

There are also two voltage monitors on 3.3 V internal sleep regulator:

- In case an OV event occurs, FAULTN pin is asserted and the V3V3_SLEEP_OV bit in the INTERNAL_STATUS register is set, but the deployment is not inhibited.
- In case an UV event occurs, FAULTN pin is asserted and V3V3_SLEEP_UV bit in INTERNAL_STATUS register is set, but the deployment is not inhibited.

In case there is a supply loss meanwhile the IC is in DEEP-SLEEP state, the NPOR_SLEEP_EVENT bit in the INTERNAL_STATUS register is set.

3.12 Die temperature (T_J) monitor

The IC constantly monitors the junction temperature (T_J) by means of an embedded sensor placed away from the power stage.

Junction temperature measurement is stored in the TEMPERATURE register and can be computed according to the following formula:

$$T_J[°C] = 1.74192 \times TEMPERATURE\_CODE - 89.988 \quad (9)$$

3.12.1 Die temperature monitor electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 37. Die temperature monitor electrical parameters

Symbol	Parameter	Min	Typ	Max	Unit
T_{J_ERR}	Die temperature total conversion error	-10	-	10	°C

3.13 Ground loss monitor (GNDMON)

To detect failures in grounding, the IC integrates a ground loss monitor that is always enabled when it is in DIAG, NORMAL and ARM states.

3.13.1 Ground loss monitor diagnostics

Table 38. Ground loss monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
PGND LOSS	If a differential voltage greater than $V_{PGND\_LOSS\_TH}$ arises between GND and PGND for a time longer than $t_{PGND\_LOSS\_FLT}$, the PGND loss fault is acknowledged	The PGND_LOSS flag is set FAULTN line is asserted The “fire inhibit” signal is set	If the differential voltage between GND and PGND falls below $V_{PGND\_LOSS\_TH}$ for a time longer than $t_{PGND\_LOSS\_FLT}$, the fault flag can be cleared by MCU	Pyro-fuse fire is possible again	Non-maskable
BSTGND LOSS	If a differential voltage greater than $V_{BSTGND\_LOSS\_TH}$ arises between GND and BSTGND for a time longer than $t_{BSTGND\_LOSS\_FLT}$, the BSTGND loss fault is acknowledged	The BSTGND_LOSS flag is set FAULTN line is asserted If enabled, ERBST is disabled If disabled, ERBST is not turned-on (diagnostic is active thanks to I_{BSTGND_PU} internal pull-up) The “fire inhibit” signal is set	If the differential voltage between GND and BSTGND falls below $V_{BSTGND\_LOSS\_TH}$ for a time longer than $t_{BSTGND\_LOSS\_FLT}$, the ERBST is automatically reenabled and the fault flag can be cleared by MCU	Pyro-fuse fire is possible again	***BSTGND_LOSS_MSK*** masks the inhibition of pyro-fuse fire commands

3.13.2 Ground Loss monitor electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 39. Ground Loss monitor electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$V_{PGND\_LOSS\_TH}$	PGND ground loss detection threshold		300	-	920	mV	GND1, GND2, PGND
$t_{PGND\_LOSS\_FLT}$	PGND ground loss detection filter time	Tested by SCAN	46	50	54	µs	GND1, GND2, PGND
$V_{BSTGND\_LOSS\_TH}$	BSTGND ground loss detection threshold		300	-	920	mV	GND1, GND2, BSTGND
$t_{BSTGND\_LOSS\_FLT}$	BSTGND ground loss detection filter time	Tested by SCAN	1.9	2.3	2.7	µs	GND1, GND2, BSTGND
I_{BSTGND_PU}	BSTGND pull-up current		25	40	55	µA	BSTGND

3.14 Serial peripheral interface (SPI)

The IC integrates a Serial Peripheral Interface (SPI) to communicate with host controller.
Internal pullup resistors address open failures on SDI, NCS and SCLK pins.

Table 40. SPI quick look

Parameter	Description
Protocol	Out-of-frame
Single frame length	24-bit
Frame protection	5-bit CRC with poly = x^5+x^2+1 (0x25) and seed = 0b11111 (0x1F)
Max frequency	2 MHz
CPOL	0
CPHA	1

The protocol implements a Global Status Word (GSW) providing info on NVM status and FAULTN signal.
The frame format is shown in the Table 41.

Table 41. SPI frame format

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	R/W	ADDRESS						0	0	DATA WRITE										CRC				
MISO	SPI ERR	ADDRESS FEEDBACK						GSW		DATA READ										CRC				

MOSI frame:

- [23] bit: R/W flag selects if the current operation is a read (0) or write (1) operation
- [22-17] bit field: SPI register address
- [16-15] bit field: reserved, fixed to 00
- [14-5] bit field: data write
- [4-0] bit field: CRC checksum generated by SPI controller

MISO frame:

- [23] bit: SPI error flag: the previous frame has an error due to length (long or short), stuck, wrong CRC, wrong command or wrong address
- [22-17] bit field: SPI register address feedback. Last received valid frame address feedback
- [16-15] bit field: global status word (GSW), provides information related to NVM status and IC high level error (NVM_BUSY on bit 16, FAULTN_ECHO on bit 15)
- [14-5] bit field: data read
- [4-0] bit field: CRC checksum generated by SPI

The following errors can be detected and the correspondent error flag is set in SPI_STATUS register:

- Frame with less than 24 bits. The SPI_FRAME_SHORT bit is set.
- Frame with more than 24 bits. The SPI_FRAME_LONG bit is set.
- Frame with a wrong CRC. The SPI_CRC_ERROR bit is set.
- Frame with a wrong address. The SPI_ADDRESS_ERROR bit is set.
- Frame with an error (OR of previous errors). The SPI_FRAME_ERROR bit is set.

3.14.1 SPI electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Figure 28. SPI timing diagram

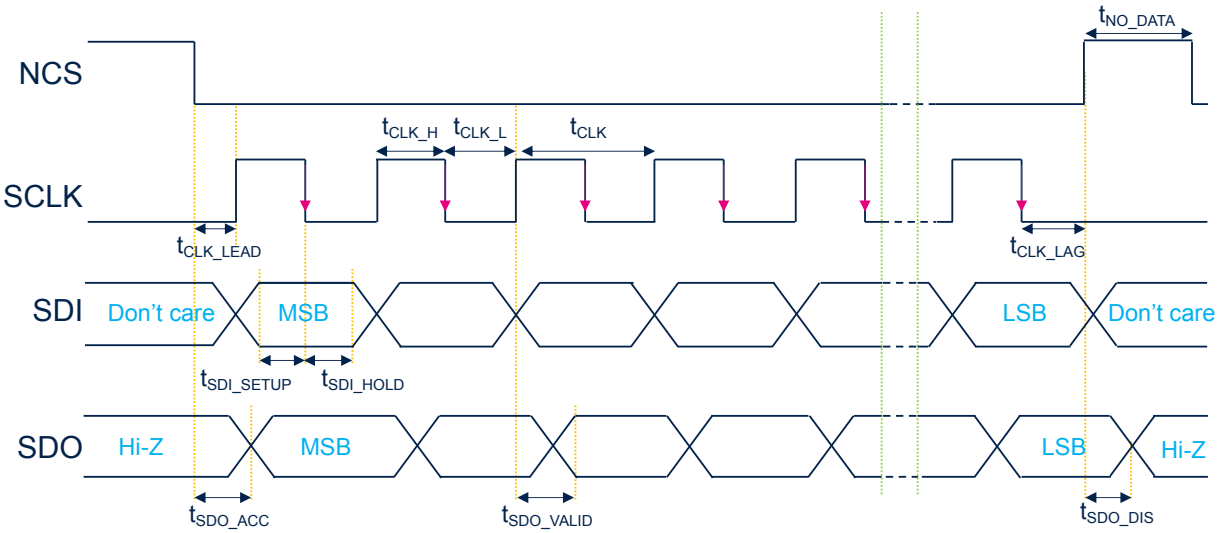


Table 42. SPI electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
f_{CLK}	SPI transfer frequency	Application info	-	-	2	MHz	SCLK
t_{CLK}	Clock period	Application info	500	-	-	ns	SCLK
t_{CLK_H}	Clock high time	Application info	210	-	-	ns	SCLK
$t_{CLK\_}$	Clock low time	Application info	210	-	-	ns	SCLK
t_{CLK_LEAD}	Clock lead time	Application info	200	-	-	ns	SCLK
t_{CLK_LAG}	Clock lag time	f_{CLK} = 2MHz	200	-	-	ns	SCLK
t_{SDI_SETUP}	MOSI input setup time	Application info	50	-	-	ns	SDI
t_{SDI_HOLD}	MOSI input hold time	Application info	50	-	-	ns	SDI
t_{SDO_ACC}	SDO access time	f_{CLK} = 2 MHz, C_{LOAD} = 60 pF	-	-	100	ns	SDO
t_{SDO_VALID}	SDO output valid time	f_{CLK} = 2 MHz, C_{LOAD} = 60 pF	-	-	150	ns	SDO
t_{SDO_DIS}	SDO disable time	f_{CLK} = 2 MHz, C_{LOAD} = 60 pF	-	-	100	ns	SDO
t_{NO_DATA}	SPI interframe time	f_{CLK} = 2 MHz	800	-	-	ns	NCS

3.14.2 SPI register map

Table 43. SPI register map

Register name	Address	Non volatile
BMS_ID	0x00	-
CHIP_ID	0x01	-
FAULT_DIAG_CONFIG	0x02	-
FENH_L_CONFIG	0x03	-
DIAG_CMD	0x04	-

Register name	Address	Non volatile
ADC_CONV_CMD	0x05	-
ADC_CONV_RESULT	0x06	-
CRC	0x07	-
DEPLOY_STATUS	0x08	-
DEPLOY_DIAG_STATUS_0	0x09	-
DEPLOY_DIAG_STATUS_1	0x0A	-
ERCAP	0x0B	-
ERCAP_DIAG_CAP_READ_0	0x0C	-
ERCAP_DIAG_CAP_READ_1	0x0D	-
ERCAP_DIAG_ESR_READ_0	0x0E	-
ERCAP_DIAG_ESR_READ_1	0x0F	-
INTERNAL_STATUS	0x10	-
SPI_STATUS	0x11	-
FENX_INTEGRITY_STATUS	0x12	-
CYCLIC_DIAG_STATUS	0x13	-
ERBOOST	0x14	-
INTERNAL_CFG	0x15	-
RES_MEAS_PRE	0x16	-
RES_MEAS_POST	0x17	-
DEPLOY_CURRENT_MONITOR	0x18	-
TEMPERATURE	0x19	-
CLIENT_NVM_REG_0	0x20	x
CLIENT_NVM_REG_1	0x21	x
CLIENT_NVM_REG_2	0x22	x
CLIENT_NVM_REG_3	0x23	x
CLIENT_NVM_REG_4	0x24	x
CLIENT_NVM_REG_5	0x25	x
CLIENT_NVM_REG_6	0x26	x
CLIENT_NVM_REG_7	0x27	x
CLIENT_NVM_REG_8	0x28	x
CLIENT_NVM_REG_9	0x29	x
CLIENT_NVM_REG_10	0x2A	x
CLIENT_NVM_REG_11	0x2B	x
CLIENT_NVM_REG_12	0x2C	x
SPECIAL_KEY	0x30	
NVM_OP_CMD	0x31	
HS_CMD	0x32	
LS_CMD	0x33	

3.14.2.1 SPI read/write registers

Note:
- *nPOR_MAIN is asserted when the IC moves from ACTIVE to DEEP-SLEEP.*
- *nPOR_SLEEP is used to retain data in DEEP-SLEEP state, and it is asserted when the battery is removed.*

Table 44. BMS_ID - 0x00

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	2	0x0	nPOR_MAIN	
BMS_ID	RO	0	8	0x0	nPOR_MAIN	0x060

Table 45. CHIP_ID - 0x01

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	2	0x0	nPOR_MAIN	
SILICON_ID	RO	5	3	X	X	0x1 = A version
METAL_ID	RO	0	5	X	X	0x1 = A version 0x2 = B version

Table 46. FAULT_DIAG_CONFIG - 0x02

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RW	4	6	0x0	nPOR_MAIN	
FENL_INT_CHECK_EN	RW	3	1	0x0	nPOR_SLEEP	0 = Integrity check masked 1 = Integrity check enabled
FENH_INT_CHECK_EN	RW	2	1	0x0	nPOR_SLEEP	0 = Integrity check masked 1 = Integrity check enabled
FAULTN_FORCE	RW	1	1	0x0	nPOR_MAIN	0 = FAULTN forced high 1 = FAULTN forced low
FAULTN_CYCLIC_PULSE	RW	0	1	0x0	nPOR_MAIN	0 = FAULTN pulses generation disabled 1 = FAULTN pulses generation enabled

Table 47. FENH_L_CONFIG - 0x03

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RW	2	8	0x0	nPOR_MAIN	
FENL_MODE	RW	1	1	0x0	nPOR_MAIN	0 = Level based decoding 1 = PWM based decoding
FENH_MODE	RW	0	1	0x0	nPOR_MAIN	0 = Level based decoding 1 = PWM based decoding

Table 48. **DIAG_CMD - 0x04**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	1	0x0	nPOR_MAIN	
SPI_DIAG_RUNNING	RO	8	1	0x0	nPOR_MAIN	0 = On-demand diag is not running 1 = On-demand diag is running
SPI_DIAG_END	CR	7	1	0x0	nPOR_MAIN	0 = On-demand diag not completed 1 = On-demand diag completed
DIAG_START	WO	6	1	0x0	nPOR_MAIN	1 = Start on-demand diag routine
ABIST	RW	5	1	0x0	nPOR_MAIN	1 = Enable ABIST execution in on-demand diag routine
ADC_HWSC	RW	4	1	0x0	nPOR_MAIN	1 = Enable HWSC execution in on-demand diag routine
VRCM_LEAK_TEST	RW	3	1	0x0	nPOR_MAIN	1 = Enable VRCM check and leak test execution in on-demand diag routine
PYRO_RES	RW	2	1	0x0	nPOR_MAIN	1 = Enable pyro res meas execution in on-demand diag routine
FET_TEST	RW	1	1	0x0	nPOR_MAIN	1 = Enable FET test execution in on-demand diag routine
ER_CAP	RW	0	1	0x0	nPOR_MAIN	1 = Enable ER cap diag execution in on-demand diag routine

Table 49. **ADC_CONV_CMD - 0x05**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RW	6	4	0x0	nPOR_MAIN	
ADC_BUSY	RO	5	1	0x0	nPOR_MAIN	0 = ADC not busy 1 = ADC busy
ADC_CONV_RDY	CR	4	1	0x0	nPOR_MAIN	0 = ADC conversion not available 1 = ADC conversion available
AMUX_CONF	RW	1	3	0x0	nPOR_MAIN	AMUX config: 000 = PS 001 = PF 010 = PR 011 = PF-PR (pre) 100 = PF-PR (post) 101 = ERBST 110 = VRCM 111 = Not used
ADC_CONV_CMD	WO	0	1	0x0	nPOR_MAIN	1 = Start ADC conversion

Table 50. **ADC_CONV_RESULT - 0x06**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ADC_CONVERSION	RO	0	10	0x0	nPOR_MAIN	ADC result

Table 51. **CRC - 0x07**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	6	4	0x0	nPOR_MAIN	
NVM_CRC_FAIL_MSK	RW	5	1	0x0	nPOR_MAIN	0 = Deployment inhibition and FAULTN assertion in case of NVM fail 1 = No deployment inhibition and FAULTN assertion in case of NVM fail
NVM_CRC_CFG_FAIL	CR	4	1	0x0	nPOR_MAIN	0 = No fail in CRC check of configuration sectors 1 = Fail in CRC check of configuration sectors
NVM_CRC_TRIM_CAL_FAIL	CR	3	1	0x0	nPOR_MAIN	0 = No fail in CRC check of trimming sectors 1 = Fail in CRC check of trimming sectors
CYC_CFG_CRC_FAIL	CR	2	1	0x0	nPOR_MAIN	0 = No fail in cyclic CRC check of config sectors 1 = Fail in cyclic CRC check of config sectors
CYC_TRIM_CAL_CRC_FAIL	CR	1	1	0x0	nPOR_MAIN	0 = No fail in cyclic CRC check of trimming sectors 1 = Fail in cyclic CRC check of trimming sectors
CYC_CRC_DIS	RW	0	1	0x0	nPOR_MAIN	0 = Cyclic CRC check (both trim and cfg) enabled 1 = Cyclic CRC check (both trim and cfg) disabled

Table 52. **DEPLOY_STATUS - 0x08**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
FIRE_INHIBIT	CR	9	1	0x0	nPOR_MAIN	0 = Fire inhibit signal not set 1 = Fire inhibit signal set
DEPLOY_CNT	RO	6	3	0x0	nPOR_SLEEP	Number of performed deployments
FIRE_RUNNING	RO	5	1	0x0	nPOR_MAIN	0 = Deployment not ongoing 1 = Deployment ongoing
FIRE_GOOD	CR	4	1	0x0	nPOR_SLEEP	0 = Fire sequence not successful 1 = Fire sequence successful
FIRE_END_BY_FAULT	CR	3	1	0x0	nPOR_SLEEP	0 =Fire sequence not ended 1 = Fire sequence ended by fault
FIRE_END	CR	2	1	0x0	nPOR_SLEEP	0 = Fire sequence not ended 1 = Fire sequence ended
FENL_ARM	CR	1	1	0x0	nPOR_MAIN	0 = FENL ARM condition not detected 1 = FENL ARM condition detected
FENH_ARM	CR	0	1	0x0	nPOR_MAIN	0 = FENH ARM condition not detected 1 = FENH ARM condition detected

Table 53. **DEPLOY_DIAG_STATUS_0 - 0x09**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PR_STB	CR	9	1	0x0	nPOR_MAIN	0 = PR leakage test good 1 = PR leakage test fails (PR STB)
PR_STG	CR	8	1	0x0	nPOR_MAIN	0 = PR leakage test good 1 = PR leakage test fails (PR STG)
PF_STB	CR	7	1	0x0	nPOR_MAIN	0 = PF leakage test good 1 = PF leakage test fails (PF STB)
PF_STG	CR	6	1	0x0	nPOR_MAIN	0 = PF leakage test good 1 = PF leakage test fails (PF STG)
VRCM_STG_FAIL	CR	5	1	0x0	nPOR_MAIN	0 = VRCM STG comparator selftest good 1 = VRCM STG comparator selftest fails
VRCM_STB_FAIL	CR	4	1	0x0	nPOR_MAIN	0 = VRCM STB comparator selftest good 1 = VRCM STB comparator selftest fails
PR_FET_STB	CR	3	1	0x0	nPOR_MAIN	0 = PR FET test good 1 = PR FET test fail (STB)
PR_FET_FAIL	CR	2	1	0x0	nPOR_MAIN	0 = PR FET test good 1 = PR FET test fail (timeout)
PF_FET_STG	CR	1	1	0x0	nPOR_MAIN	0 = PF FET test good 1 = PF FET test fails (STG)
PF_FET_FAIL	CR	0	1	0x0	nPOR_MAIN	0 = PF FET test good 1 = PF FET test fail (timeout)

Table 54. **DEPLOY_DIAG_STATUS_1 - 0x0A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	7	3	0x1	nPOR_MAIN	
PF_PR_PRE_HWSC_FAIL	CR	6	1	0x0	nPOR_MAIN	0 = PF vs PR PRE HWSC test good 1 = PF vs PR PRE HWSC test fail
PF_PR_POST_HWSC_FAIL	CR	5	1	0x0	nPOR_MAIN	0 = PF vs PR POST HWSC test good 1 = PF vs PR POST HWSC test fail
VRCM_HWSC_FAIL	CR	4	1	0x0	nPOR_MAIN	0 = VRCM HWSC test good 1 = VRCM HWSC test fails
PS_OV	CR	3	1	0x0	nPOR_MAIN	0 = PS below OV threshold 1 = PS above OV threshold
PS_UV	CR	2	1	0x0	nPOR_MAIN	0 = PS above UV threshold 1 = PS below UV threshold
PYRO_HIGH_RES	CR	1	1	0x0	nPOR_MAIN	0 = pyro resistance test good 1 = pyro res above high threshold
PYRO_LOW_RES	CR	0	1	0x0	nPOR_MAIN	0 = pyro resistance test good 1 = pyro res below low threshold

Table 55. **ERCAP - 0x0B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	6	4	0x0	nPOR_MAIN	
ERDCHSW_OV	CR	5	1	0x0	nPOR_MAIN	0 = ERDCHSW below OV threshold 1 = ERDCHSW above OV threshold
ERDCHSW_EN	RW	4	1	0x0	ERDCHSW_RST_N	0 = ERDCHSW disabled 1 = ERDCHSW enabled (reset during ERCAP diag or when arming starts)
ERCAP_OUT_OF_RANGE	CR	3	1	0x0	nPOR_MAIN	0 = ERCAP test good 1 = ERCAP test fails (out of range)
ERCAP_DIAG_END_TO	CR	2	1	0x0	nPOR_MAIN	0 = ERCAP test good 1 = ERCAP test fail (timeout)
ERCAP_HIGH_ESR	CR	1	1	0x0	nPOR_MAIN	0 = ERCAP test good 1 = ERCAP test fails (high ESR)
ERCAP_LOW_C	CR	0	1	0x0	nPOR_MAIN	0 = ERCAP test good 1 = ERCAP test fails (low capacitance)

Table 56. **ERCAP_DIAG_CAP_READ_0 - 0x0C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CAP_VALUE_LSB	RO	0	10	0x0	nPOR_MAIN	LSB of capacitance value

Table 57. **ERCAP_DIAG_CAP_READ_1 - 0x0D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	4	6	0x0	nPOR_MAIN	
CAP_VALUE_MSB	RO	0	4	0x0	nPOR_MAIN	MSB of capacitance value

Table 58. **ERCAP_DIAG_ESR_READ_0 - 0x0E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ESR_VALUE_LSB	RO	0	10	0x0	nPOR_MAIN	LSB of ESR value

Table 59. **ERCAP_DIAG_ESR_READ_1 - 0x0F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	3	7	0x0	nPOR_MAIN	
ESR_VALUE_MSB	RO	0	3	0x0	nPOR_MAIN	MSB of ESR value

Table 60. **INTERNAL_STATUS - 0x10**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SPI_WAKEUP	RO	9	1	0x0	nPOR_MAIN	1 = Wake-up from SPI
FENX_WAKEUP	RO	8	1	0x0	nPOR_MAIN	1 = Wake-up from FENH or FENL
CWUP_WAKEUP	RO	7	1	0x0	nPOR_MAIN	1 = Wake-up from CWUP
PGND_LOSS	CR	6	1	0x0	nPOR_MAIN	0 = PGND_LOSS not set 1 = PGND_LOSS set
NPOR_SLEEP_EVENT	CR	5	1	0x1	nPOR_MAIN	0 = NPOR_SLEEP_EVENT not set 1 = NPOR_SLEEP_EVENT set
OSCI_FAIL	CR	4	1	0x0	nPOR_MAIN	0 = OSCI good 1 = OSCI fails
BIAS_WARNING	CR	3	1	0x0	nPOR_MAIN	0 = Bias good 1 = Bias fails
V3V3_SLEEP_UV	CR	2	1	0x0	nPOR_MAIN	0 = V3V3_SLEEP above UV threshold 1 = V3V3_SLEEP below UV threshold
V3V3_SLEEP_OV	CR	1	1	0x0	nPOR_MAIN	0 = V3V3_SLEEP below OV threshold 1 = V3V3_SLEEP above OV threshold
ABIST_FAIL	CR	0	1	0x0	nPOR_MAIN	0 = ABIST good 1 = ABIST fails

Table 61. **SPI_STATUS - 0x11**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SPARE	RW	5	5	0x0	nPOR_MAIN	
SPI_FRAME_SHORT	CR	4	1	0x0	nPOR_MAIN	0 = SHORT_FRAME error not set 1 = SHORT_FRAME error set
SPI_FRAME_LONG	CR	3	1	0x0	nPOR_MAIN	0 = LONG_FRAME error not set 1 = LONG_FRAME error set
SPI_CRC_ERROR	CR	2	1	0x0	nPOR_MAIN	0 = CRC error not set 1 = CRC error set
SPI_ADDRESS_ERROR	CR	1	1	0x0	nPOR_MAIN	0 = ADDRESS error not set 1 = ADDRESS error set
SPI_FRAME_ERROR	CR	0	1	0x0	nPOR_MAIN	0 = No errors 1 = SPI error (OR of previous error bits)

Table 62. **FENX_INTEGRITY_STATUS - 0x12**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
FENH_ECHO	RO	9	1	0x0	nPOR_MAIN	Echo of FENH pin
FENL_ECHO	RO	8	1	0x0	nPOR_MAIN	Echo of FENL pin
FENH_HIGH_FREQ	CR	7	1	0x0	nPOR_MAIN	0 = HIGH_FREQ error on FENH not set 1 = HIGH_FREQ error on FENH set
FENL_HIGH_FREQ	CR	6	1	0x0	nPOR_MAIN	0 = HIGH_FREQ error on FENL not set 1 = HIGH_FREQ error on FENL set
FENH_LOW_FREQ	CR	5	1	0x0	nPOR_MAIN	0 = LOW_FREQ error on FENH not set 1 = LOW_FREQ error on FENH set
FENL_LOW_FREQ	CR	4	1	0x0	nPOR_MAIN	0 = LOW_FREQ error on FENL not set 1 = LOW_FREQ error on FENL set
FENH_PWM_TIMEOUT	CR	3	1	0x0	nPOR_MAIN	0 = PWM_TIMEOUT error on FENH not set 1 = PWM_TIMEOUT error on FENH set
FENL_PWM_TIMEOUT	CR	2	1	0x0	nPOR_MAIN	0 = PWM_TIMEOUT error on FENL not set 1 = PWM_TIMEOUT error on FENL set
FENH_LEV_TIMEOUT	CR	1	1	0x0	PnPOR_MAIN	0 = LEV_TIMEOUT error on FENH not set 1 = LEV_TIMEOUT error on FENH set
FENL_LEV_TIMEOUT	CR	0	1	0x0	nPOR_MAIN	0 = LEV_TIMEOUT error on FENL not set 1 = LEV_TIMEOUT error on FENL set

Table 63. **CYCLIC_DIAG_STATUS - 0x13**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	2	0x0	nPOR_MAIN	
CYC_DIAG_RUNNING	RO	7	1	0x0	nPOR_MAIN	1 = Cyclig diag running
CYC_DIAG_NCYCLE	RO	0	7	0x0	nPOR_SLEEP	Number of cyclic diagnosis routine cycle (restart after 64 cycles).

Table 64. **ERBOOST - 0x14**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	2	0x0	nPOR_MAIN	
BSTGND_LOSS	CR	7	1	0x0	nPOR_MAIN	0 = BSTGND_LOSS not set 1 = BSTGND_LOSS set
ERBST_OC	RO	6	1	0x0	nPOR_MAIN	0 = ERBST_OC not set 1 = ERBST_OC set
ERBST_DLOSS	RO	5	1	0x0	nPOR_MAIN	0 = ERBST_DLOSS not set 1 = ERBST_DLOSS set
ERBST_OT	CR	4	1	0x0	nPOR_MAIN	0 = ERBST_OT not set 1 = ERBST_OT set
ERBST_UV	CR	3	1	0x0	nPOR_MAIN	0 = ERBST_UV not set 1 = ERBST_UV set
ERBST_OV	CR	2	1	0x0	nPOR_MAIN	0 = ERBST_OV not set 1 = ERBST_OV set
ERBST_RDY	RO	1	1	0x0	nPOR_MAIN	0 = ERBST_RDY not set 1 = ERBST_RDY set
ERBST_DIS	RW	0	1	0x0	nPOR_MAIN	0 = ERBST enabled 1 = ERBST disabled

Table 65. **INTERNAL_CFG - 0x15**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	3	7	0x0	nPOR_MAIN	
OSC_SS_EN	RW	2	1	0x0	nPOR_SLEEP	0 = Spread spectrum disabled 1 = Spread spectrum enabled
PR_PD_DIS	RW	1	1	0x0	nPOR_MAIN	0 = PR pull-down enabled 1 = PR pull-down disabled
PS_OV_FIRE_MSK	RW	0	1	0x0	nPOR_SLEEP	0 = PS_OV inhibits deployment 1 = PS_OV masked (deployment possible)

Table 66. **RES_MEAS_PRE - 0x16**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
RES_MEAS_PRE	RO	0	10	0x0	nPOR_MAIN	Resistance measurement result (pre-deployment)

Table 67. **RES_MEAS_POST - 0x17**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
RES_MEAS_POST	RO	0	10	0x0	nPOR_SLEEP	Resistance measurement result (post-deployment)

Table 68. **DEPLOY_CURRENT_MONITOR - 0x18**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	0	1	0x0	nPOR_MAIN	
DEP_CURR_MON	RO	0	9	0x0	nPOR_SLEEP	Deployment current monitor value

Table 69. **TEMPERATURE - 0x19**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	2	0x0	nPOR_MAIN	
TEMPERATURE_CODE	RO	0	8	0x0	nPOR_MAIN	Temperature conversion result

Table 70. **CLIENT_NVM_REG_0 - 0x20**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_ERBST_OV_FIRE_MSK	RW	9	1	0x0	nPOR_SLEEP	1 = Deployment inhibition from ERBST_OV masked
TRIM_ERBST_OV_FAULTN_MSK	RW	8	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from ERBST_OV masked
TRIM_FENL_PU_PD	RW	7	1	0x0	nPOR_SLEEP	0 = FENL pull-up enabled 1 = FENL pull-down enabled
TRIM_FENH_PU_PD	RW	6	1	0x0	nPOR_SLEEP	0 = FENH pull-up enabled 1 = FENH pull-down enabled
TRIM_FENL_FREQ	RW	5	1	0x0	nPOR_SLEEP	Selection of PWM frequency for FENL: 0 = 125 kHz 1 = 16 kHz
TRIM_FENH_FREQ	RW	4	1	0x0	nPOR_SLEEP	Selection of PWM frequency for FENH: 0 = 125 kHz 1 = 16 kHz
TRIM_FENL_LEVEL	RW	3	1	0x0	nPOR_SLEEP	Selection of active level for FENL: 0 = low value, 1 = high value
TRIM_FENH_LEVEL	RW	2	1	0x0	nPOR_SLEEP	Selection of active level for FENH: 0 = low value, 1 = high value
TRIM_FENL_EN	RW	1	1	0x0	nPOR_SLEEP	0 = FENL decoder disabled 1 = FENL decoder enabled
TRIM_FENH_EN	RW	0	1	0x0	nPOR_SLEEP	0 = FENH decoder disabled 1 = FENH decoder enabled

Table 71. **CLIENT_NVM_REG_1 - 0x21**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_FENX_FAULT_PERIOD	RW	8	2	0x0	nPOR_SLEEP	Number of PWM periods as deglitch filter: 00 = 2 01 = 8 10 = 32 11 = 128
TRIM_FENX_DEGLITCH	RW	6	2	0x0	nPOR_SLEEP	Deglitch filter for level signal: 00 = 20 µs 01 = 80 µs 10 = 320 µs 11 = 1280 µs
TRIM_PYRO_HIGH_RES_FAULTN_MSK	RW	5	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from PYRO_HIGH_RES masked
TRIM_PYRO_LOW_RES_FAULTN_MSK	RW	4	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from PYRO_LOW_RES masked
TRIM_I_DEPLOY_CFG	RW	2	2	0x0	nPOR_SLEEP	Deployment current profile: 00 = 1.5 A 01 = 1.75 A 10 = 2 A 11 = 3.5 A
TRIM_FENX_DLY_CFG	RW	0	2	0x0	nPOR_SLEEP	Deployment trigger delay: 00 = No delay 01 = 2 ms 10 = 4 ms 11 = 8 ms

Table 72. **CLIENT_NVM_REG_2 - 0x22**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_ERBSTSW_OT_FAULTN_MSK	RW	9	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from ERBST_OT masked
TRIM_ERBSTSW_OC_FAULTN_MSK	RW	8	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from ERBST_OC masked
RESERVED	RW	7	1	0x0	nPOR_SLEEP	Reserved
TRIM_VRES_LOW_TH	RW	0	7	0x0	nPOR_SLEEP	Low threshold for PYRO_RES measurement

Table 73. **CLIENT_NVM_REG_3 - 0x23**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_HS_RET_CFG	RW	8	2	0x0	nPOR_SLEEP	Max number of deployment auto-retries: 00 = 1, 01 = 2, 10 = 3, 11 = 4
TRIM_VRES_HIGH_TH	RW	1	7	0x0	nPOR_SLEEP	High threshold for PYRO_RES measurement
TRIM_ERBST_DLOSS_FAULTN_MSK	RW	0	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from ERBST_DLOSS masked

Table 74. **CLIENT_NVM_REG_4 - 0x24**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_VRES_POST_TH	RW	9	1	0x0	nPOR_SLEEP	PYRO_RES threshold after deployment: 0 = 99 Ω, 1 = 49 Ω
TRIM_PYRO_RES_EN	RW	8	1	0x0	nPOR_SLEEP	1 = PYRO_RES cyclic diag enabled
TRIM_LEAK_EN	RW	7	1	0x0	nPOR_SLEEP	1 = VRCM and LEAK cyclic diag enabled
TRIM_ADC_HWSC_EN	RW	6	1	0x0	nPOR_SLEEP	1 = ADC_HWSC cyclic diag enabled
TRIM_FET_EN	RW	5	1	0x0	nPOR_SLEEP	1 = FET test cyclic diag enabled
TRIM_ER_CAP_EN	RW	4	1	0x0	nPOR_SLEEP	1 = ER_CAP cyclic diag enabled
TRIM_DIAG_ROUTINE_PERIOD	RW	2	2	0x0	nPOR_SLEEP	Period of diagnostic routine: 00 = 100 ms 01 = 300 ms 10 = 500 ms 11 = 700 ms
TRIM_HS_RET_DLY_CFG	RW	0	2	0x0	nPOR_SLEEP	Delay between deployment autoretries: 00 = 0.5 ms 01 = 1 ms 10 = 1.5 ms 11 = 2 ms

Table 75. **CLIENT_NVM_REG_5 - 0x25**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_FET_NCYCLE	RW	8	2	0x0	nPOR_SLEEP	Periodicity of cyclic FET test: 00 = 1, 01 = 4, 10 = 16, 11 = 64
TRIM_PYRO_RES_NCYCLE	RW	6	2	0x0	nPOR_SLEEP	Periodicity of cyclic resistance measurement: 00 = 1, 01 = 4, 10 = 16, 11 = 64
TRIM_PF_FET_FAIL_FAULTN_MSK	RW	5	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from PF_FET_FAIL masked
TRIM_DEP_MON_THR	RW	0	5	0x0	nPOR_SLEEP	Deployment current monitor threshold

Table 76. **CLIENT_NVM_REG_6 - 0x26**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_ER_CAP_NCYCLE	RW	8	2	0x0	nPOR_SLEEP	Periodicity of cyclic ER_CAP diag: 00 = 1, 01 = 4, 10 = 16, 11 = 64
TRIM_PF_PR_STB_STG_FAULTN_MSK	RW	7	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from PF_STG, PF_STB, PR_STG and PR_STB masked
TRIM_ERCAP_FAULTN_MSK	RW	6	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from ERCAP fails masked
TRIM_LEAK_LOW_FAULTN_MSK	RW	5	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from VRCM_STB_FAIL and VRCM_STG_FAIL masked
TRIM_VRCM_HWSC_FAULTN_MSK	RW	4	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from VRCM_HWSC_FAIL masked
TRIM_PF_PR_POST_HWSC_FAULTN_MSK	RW	3	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from PF_PR_POST_HWSC_FAIL masked
TRIM_PF_PR_PRE_HWSC_FAULTN_MSK	RW	2	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from PF_PR_PRE_HWSC_FAIL masked
TRIM_ADC_HWSC_NCYCLE	RW	0	2	0x0	nPOR_SLEEP	Periodicity of cyclic ADC_HWSC diag: 00 = 1, 01 = 4, 10 = 16, 11 = 64

Table 77. **CLIENT_NVM_REG_7 - 0x27**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_PF_FET_FAIL_FIRE_MSK	RW	9	1	0x0	nPOR_SLEEP	1 = Deployment inhibition from PF_FET_STG and PF_FET_FAIL masked
TRIM_LEAK_NCYCLE	RW	7	2	0x0	nPOR_SLEEP	Periodicity of cyclic VRCM check and LEAK test: 00 = 1, 01 = 4, 10 = 16, 11 = 64
TRIM_T_DEPLOY_CFG	RW	0	7	0x0	nPOR_SLEEP	Deployment time

Table 78. **CLIENT_NVM_REG_8 - 0x28**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
RESERVED	RW	9	1	0x0	nPOR_SLEEP	Reserved
TRIM_VER_WKUP_TH	RW	6	3	0x0	nPOR_SLEEP	ERBST enabled threshold (see the Table 10)
TRIM_ERBST_SET	RW	3	3	0x0	nPOR_SLEEP	ERBST disabled threshold (see the Table 10)
TRIM_PIN_LIMIT	RW	2	1	0x0	nPOR_SLEEP	0 = Input power limitation disabled 1 = Input power limitation enabled
TRIM_PR_FET_FAIL_FIRE_MSK	RW	1	1	0x0	nPOR_SLEEP	1 = Deployment inhibition from PR_FET_STB and PR_FET_FAIL masked
TRIM_PR_FET_FAIL_FAULTN_MSK	RW	0	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from PF_FET_STG and PF_FET_FAIL masked

Table 79. **CLIENT_NVM_REG_9 - 0x29**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_GND_LOSS_BSTGND_MSK	RW	9	1	0x0	nPOR_SLEEP	1 = Deployment inhibition from BSTGND_LOSS masked
TRIM_ERBST_EN	RW	8	1	0x0	nPOR_SLEEP	0 = ERBST disabled 1 = ERBST enabled
TRIM_ERCAP_C_THR	RW	0	8	0x0	nPOR_SLEEP	Threshold for ER CAP capacitance value

Table 80. **CLIENT_NVM_REG_10 - 0x2A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
TRIM_FENX_TIMEOUT_FAULTN_MSK	RW	9	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from FENx_PWM_TIMEOUT and FENx_LEV_TIMEOUT masked
TRIM_FENX_LOW_FREQ_FAULTN_MSK	RW	8	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from FENx_LOW_FREQ masked
TRIM_FENX_HIGH_FREQ_FAULTN_MSK	RW	7	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from FENx_HIGH_FREQ masked
TRIM_ERCAP_ESR_THR	RW	0	7	0x0	nPOR_SLEEP	Threshold for ER CAP ESR value

Table 81. **CLIENT_NVM_REG_11 - 0x2B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NVM_UPLOAD_COUNT	RO	5	5	0x0	nPOR_SLEEP	Number of NVM writing
TRIM_FAULTN_DIS	RW	4	1	0x0	nPOR_SLEEP	0 = FAULTN output enabled 1 = FAULTN output disabled
TRIM_FIRE_GOOD_SEL	RW	2	2	0x0	nPOR_SLEEP	Selection of FIRE_GOOD signal: 00 = Meas res 01 = Dep curr 10 = Meas res and dep curr 11 = None
RESERVED	RW	1	1	0x0	nPOR_SLEEP	Reserved
TRIM_PS_OV_FAULTN_MSK	RW	0	1	0x0	nPOR_SLEEP	1 = FAULTN assertion from PS_OV masked

Table 82. **CLIENT_NVM_REG_12 - 0x2C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RW	8	2	0x0	nPOR_SLEEP	
CLIENT_CONFIG_CRC	RO	0	8	0x0	nPOR_SLEEP	Written internally after NVM download

Table 83. **SPECIAL_KEY - 0x30**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	2	0x0	nPOR_MAIN	
SPECIAL_KEY	RW	0	8	0x0	nPOR_MAIN	0x55 = Partial unlock 0x33 = Full unlock 0xAA= Lock 0xE1 = Partial SW reset 0x1E = Full SW reset 0x77 = Partial GO2SLP 0xCC = Full GO2SLP

Table 84. **NVM_OP_CMD - 0x031**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	6	4	0x0	nPOR_MAIN	
NVM_ERASE_VERIFY_ERROR	CR	5	1	0x0	nPOR_MAIN	1 = Error during NVM erasing
NVM_PROGRAM_VERIFY_ERROR	CR	4	1	0x0	nPOR_MAIN	1 = Error during NVM programming
NVM_BUSY	RO	3	1	0x0	nPOR_MAIN	1 = NVM busy
NVM_OPERATION	WO	0	3	0x0	nPOR_MAIN	0x3 = Upload client NVM sect and download all NVM 0x5 = Download all NVM

Table 85. **HS_CMD - 0x32**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM_HS_SPI	WO	0	10	0x0	nPOR_MAIN	0x155 = High Side SPI arming command

Table 86. **LS_CMD - 0x33**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM_LS_SPI	WO	0	10	0x0	nPOR_MAIN	0x2AA = Low Side SPI arming command

3.15 Configuration Lock

To prevent inadvertent modification of safety relevant registers (SRR) and safety latent registers (SLR), written in ***bold*** in this document, such register map sectors are protected by a lock field.

By default, SRR/SLR registers are locked.

To configure the device, the following procedure shall be implemented:

1. MCU writes 0x55 in the SPECIAL_KEY register to enter in partial unlock.
2. MCU writes 0x33 in the SPECIAL_KEY register to confirm the full unlock.
3. MCU changes any configuration register within $t_{CFG\_TIMEOUT}$.
4. MCU reapplies the lock writing 0xAA in the SPECIAL_KEY.

If the $t_{CFG\_TIMEOUT}$ expires, the lock is automatically reapplied.

Trying to write a protected register (SRR or SLR) without unlocking will result in the data being discarded.

Note:

- *Writing lock-protected registers only alters the current configuration loaded in the SPI registers. To save the configuration and guarantee a correct reload at each power-up, the update has to be pushed into the non-volatile memory (NVM), as described in the dedicated section.*
- *For temporary modifications to the IC configuration, which do not need to be pushed in the non-volatile memory, it is recommended to disable the configuration integrity check (CONF_CRC).*

3.15.1 Configuration lock electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 87. **Configuration Lock electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_{CFG\_TIMEOUT}$	Configuration lock timeout	Tested in SCAN	1.8	2	2.1	s

3.16 Software reset (SW_RST)

It is possible to reset the configuration of the device sending a SW_RST sequence.

Once triggered, the software reset procedure resets all SPI registers to their default values, including diagnostic fault flags and lock protected bit fields.

To reset the device configuration, the following procedure shall be implemented:

1. MCU writes 0xE1 into the SPECIAL_KEY register to enter partial reset mode.
2. MCU writes 0x1E into the SPECIAL_KEY register to confirm the reset.

Frames must be sent exactly in this sequence, otherwise registers will not be reset.

Note: Since the NVM is redownloaded at each wake-up, the new configuration eventually applied shall be pushed into the memory with a "write" instruction. Otherwise, the old configuration will be restored at the next wake-up event.

3.17 Configuration integrity check (CONF_CRC)

To guarantee the integrity over time of NVM downloaded trimming/calibration and configuration data, both safety relevant and latent register content is automatically and cyclically checked against corruption within NORMAL mode. This is possible because local register data is provided with a CRC signature, that is checked every $t_{CONF\_CRC\_PERIOD}$, while no operation on the NVM is being performed (NVM circuit in reset state).

The duration of the calculation is $t_{CONF\_CRC\_TIME}$.

In case of check failure, the following actions are performed:

- In case trimming/calibration data has failed the CRC signature check, CYC_TRIM_CAL_CRC_FAIL latch is set (clear-upon-read).
- In case IC configuration data has failed the CRC signature check, CYC_CFG_CRC_FAIL latch is set (clear-upon-read).
- In both cases, the deployment is inhibited and FAULTN is asserted but there is no interruption/inhibition of other IC functionalities.

In case of permanent data corruption, failure latch set pulse occurs every $t_{CONF\_CRC\_PERIOD}$.

The local register CRC signature is managed in the following way:

- Every time NVM data is downloaded into local registers (either automatically or user-driven), a CRC signature is refreshed as well and written in the CLIENT_CONFIG_CRC bit field.
- Every time the user changes the local register data, the corresponding CRC signature is not automatically updated, thus a CRC check failure is expected at the next execution cycle. By the way, as the user triggers the NVM upload and refresh operation, after the NVM sector CRC has been automatically updated, the local register CRC signature is updated accordingly and no further CRC check failure is expected.

The integrity check can be disabled by setting CYC_CRC_DIS = 1. After the diagnostic has been disabled, it is still possible to clear-upon-read both CYC_TRIM_CAL_CRC_FAIL and CYC_CFG_CRC_FAIL. Disabling such diagnostic can be useful to mask systematic CRC failure detection when updating IC configurations. The deployment inhibition is removed. On the other hand, leaving it enabled while updating register configurations may be used as a fault injection strategy to assess the correct functionality of the diagnostics.

3.17.1 Configuration integrity check electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 88. Configuration integrity check characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_{CONF\_CRC\_PERIOD}$	Configuration integrity check period	Tested by SCAN	-	4	-	ms
$t_{CONF\_CRC\_TIME}$	Configuration integrity check time	Tested by SCAN	175	190	210	µs

3.18 Non-volatile memory (NVM)

The IC allows saving key configuration parameters in the internal NVM.

3.18.1 NVM read/write operations

NVM data is automatically downloaded into local registers every time that the IC FSM transitions from the OFF state to the DEEP-SLEEP state.

When the IC performs FSM transitions to DEEP-SLEEP state, a selected group of data stored in local registers is retained to guarantee IC correct operation (managed by nPOR_SLEEP), while all other data is lost (managed by nPOR_MAIN). Such data will be redownloaded in the next transition to NORMAL or DIAG state.

When the IC performs FSM transitions to OFF state, all data stored in local registers is lost; NVM data will be redownloaded in the next transition to NORMAL or DIAG state.

In NORMAL state, the following commands in NVM_OP_CMD register allow user interaction with the NVM:

- NVM_OPERATION = 0x3 triggers the NVM upload and refresh: this operation fetches the data previously written into configuration registers and writes it to the relative NVM sectors, then it automatically triggers a full NVM redownload to guarantee whole data consistency. The operation lasts t_{NVM_UPLOAD} and during such time interval the MCU will not be able to perform R/W operations (any command will be discarded).
- NVM_OPERATION = 0x5 triggers the NVM refresh, fetching the data from NVM sectors and writing it to the configuration registers. The operation lasts $t_{NVM\_DOWNLOAD}$ and during such time interval the MCU will not be able to perform R/W operations (any command will be discarded).

During NVM upload/download operations, the NVM_BUSY flag indicates that NVM is busy. During such an interval, it is highly recommended to avoid triggering conversions or actuating loads, as the trimming and calibration data is being refreshed, and data through SPI are not available (read commands return all zeros). Once the task is complete, the NVM_BUSY bit is set low and the NVM circuit is kept under reset.

In NVM upload operations, NVM_ERASE_VERIFY_ERROR flag indicates that an error has occurred during NVM erasing, NVM_PROGRAM_VERIFY_ERROR flag indicates that an error has occurred during NVM programming.

Every time a SW_RST is commanded, the parameters not pushed inside the NVM with a write command will be lost.

Note: NVM_ERASE_VERIFY_ERROR and NVM_PROGRAM_VERIFY_ERROR are NOT mapped to FAULTN.

Note: Before interacting with the NVM, the MCU shall hold CWUP high to prevent the IC moving back to DEEP-SLEEP due to communication timeout.

Every time a write operation is performed, the IC automatically decrements by one the NVM write counter that starts from 31. The counter value is stored in the NVM as well and is user-accessible reading NVM_UPLOAD_COUNT bit (read-only). As the number of write operations reaches $N_{NVM\_WRITE\_CYCLES}$ limit, the counter has reached the zero value and it will be never be updated anymore. When such a limit is exceeded, data retention is not guaranteed anymore. By the way, the IC continues to accept and perform every write operation, even if it is beyond $N_{NVM\_WRITE\_CYCLES}$ count.

3.18.2 NVM data integrity checks

NVM content can be categorized in two main groups: trimming/calibration data (used to guarantee function accuracy) and configuration data (used to IC configuration). All this data is organized in sectors, each of them individually protected by CRC. Trimming/calibration data and configuration data are in different sectors.

Every time the IC performs an NVM download operation (either automatic or user-driven), an integrity check against the NVM CRC (sector by sector) is performed as well. In case of check failure, the following actions are performed:

- The sector data that fails CRC check is not downloaded into the local registers and is replaced by all zeros. Hence, depending on the sector content, either function accuracy will not be guaranteed or IC expected configuration will not be applied.
- In case at least one of the trimming/calibration sectors has failed the CRC check, NVM_CRC_TRIM_CAL_FAIL latch is set (clear-upon-read). When NVM_CRC_FAIL_MSK is set to 1, this flag can always be cleared.
- In case at least one of the IC configuration sectors has failed the CRC check, NVM_CRC_CFG_FAIL latch is set (clear-upon-read). When NVM_CRC_FAIL_MSK is set to 1, this flag can always be cleared.
- The deployment is inhibited and FAULTN is asserted but there is no interruption/inhibition of other IC functionalities. It is possible to mask this behavior setting the NVM_CRC_FAIL_MSK bit.

Every time the user triggers an NVM upload and refresh operation, the corresponding sector CRC is updated as well; this is done by IC automatically.

3.18.3 NVM electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: all supplies according to the Table 3; T_J according to the Table 2.

Table 89. NVM electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$N_{NVM\_WRITE\_CYCLES}$	Number of allowed NVM write cycles to guarantee data retention	Guaranteed by SCAN	-	-	31	cycles
t_{NVM_UPLOAD}	NVM upload time duration (as sum of write and download operations)	Guaranteed by SCAN	-	-	12	ms
$t_{NVM\_DOWNLOAD}$	NVM download time duration	Guaranteed by SCAN	-	-	500	µs

4 Application scenarios

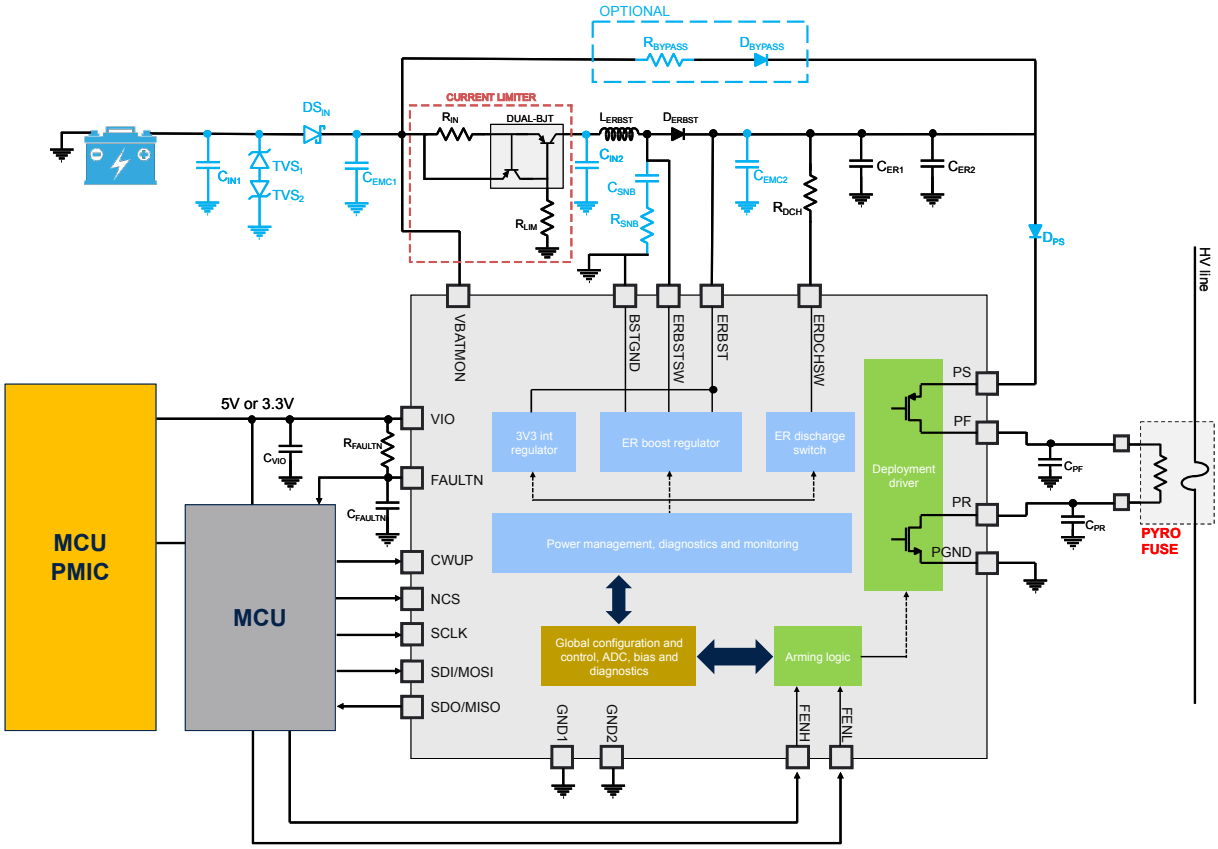
4.1 Typical application circuit

The application scenarios shown in the following are only for reference. Please refer to the Application Notes for more information.

4.1.1 12 V battery with MCU and ERBST mounted

The Figure 29 shows a typical application diagram for a pyro-fuse system using the ERBST regulator and interfaced with a generic MCU.

Figure 29. Application circuit: 12 V battery with MCU and ERBST mounted



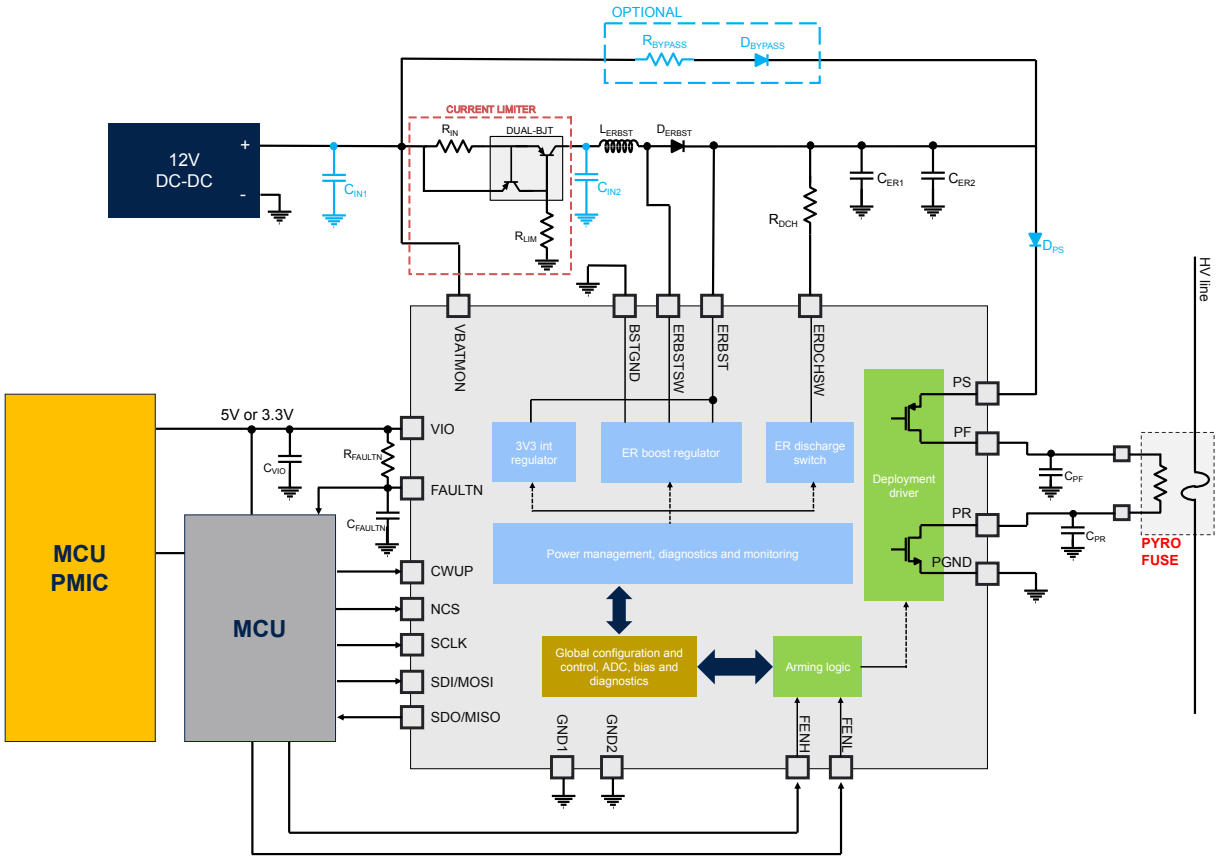
The C_{ER} electrolytic capacitors are connected to ERBST regulator that charges them to a higher voltage respect to battery level V_{BAT}.

ERDCHSW pin is used to allow C_{ER} controlled discharge for safety and diagnostic purposes. R_{DCHG} sets the limit current for the discharge phase.

4.1.2 12 V DC-DC with MCU and ERBST mounted

The Figure 30 shows a typical application diagram for a pyro-fuse system supplied by a low current DC-DC regulator, using the ERBST regulator and interfaced with a generic MCU.

Figure 30. Application circuit: 12 V DC-DC with MCU and ERBST mounted



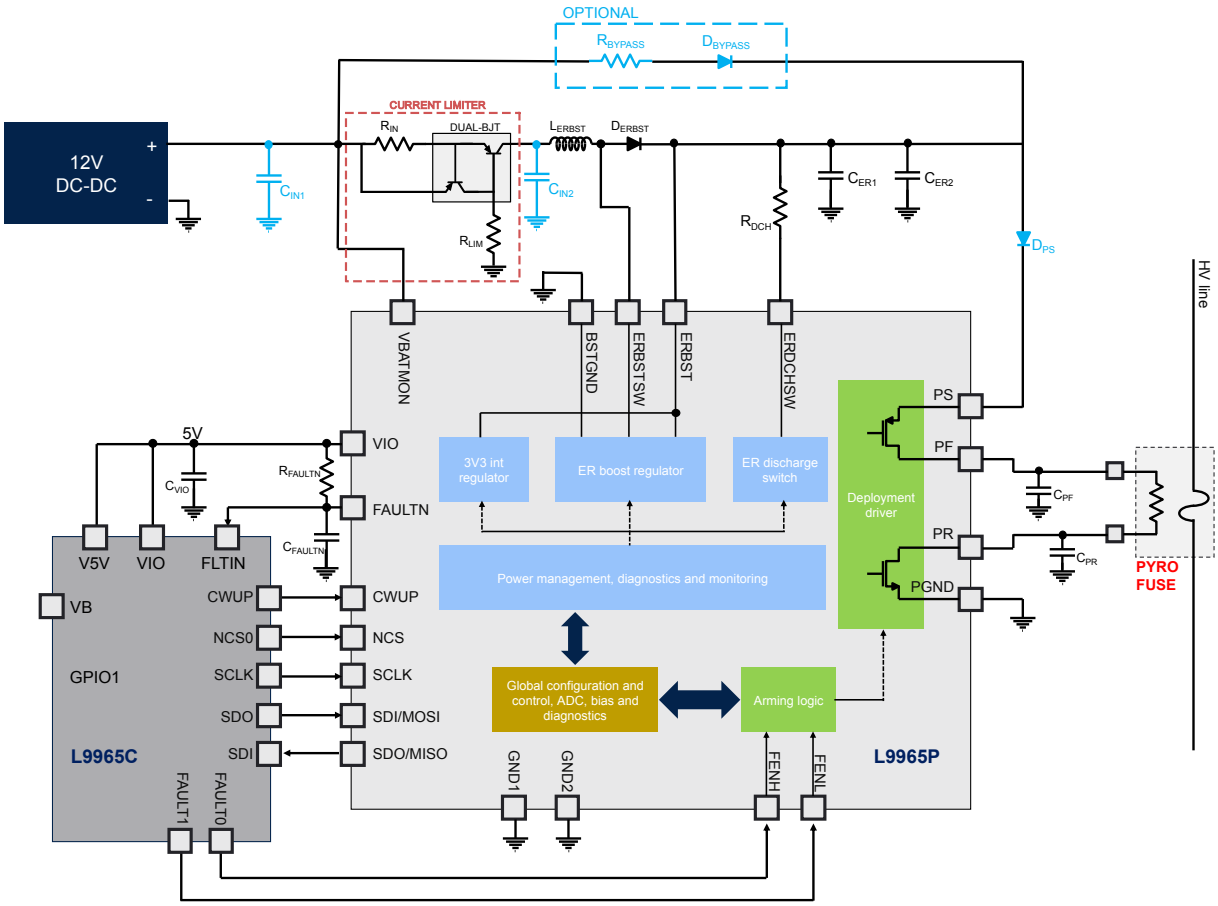
The C_{ER} electrolytic capacitors are connected to ERBST regulator that charge them to a higher voltage respect to battery level V_{BAT}. In this case the ERBST power limit function can be used to limit the ERBST input power and so the power required to the 12 V DC-DC regulator.

ERDCHSW pin is used to allow C_{ER} controlled discharge for safety and diagnostic purposes. R_{DCHG} sets the limit current for the discharge phase.

4.1.3 12 V DC-DC with L9965C/L99BM2C and ERBST mounted

The Figure 31 shows a typical application diagram for a pyro-fuse system supplied by a low current DC-DC regulator, using the ERBST regulator and interfaced with a L9965C/L99BM2C companion chip.

Figure 31. Application circuit: 12 V DC-DC with L9965C and ERBST mounted



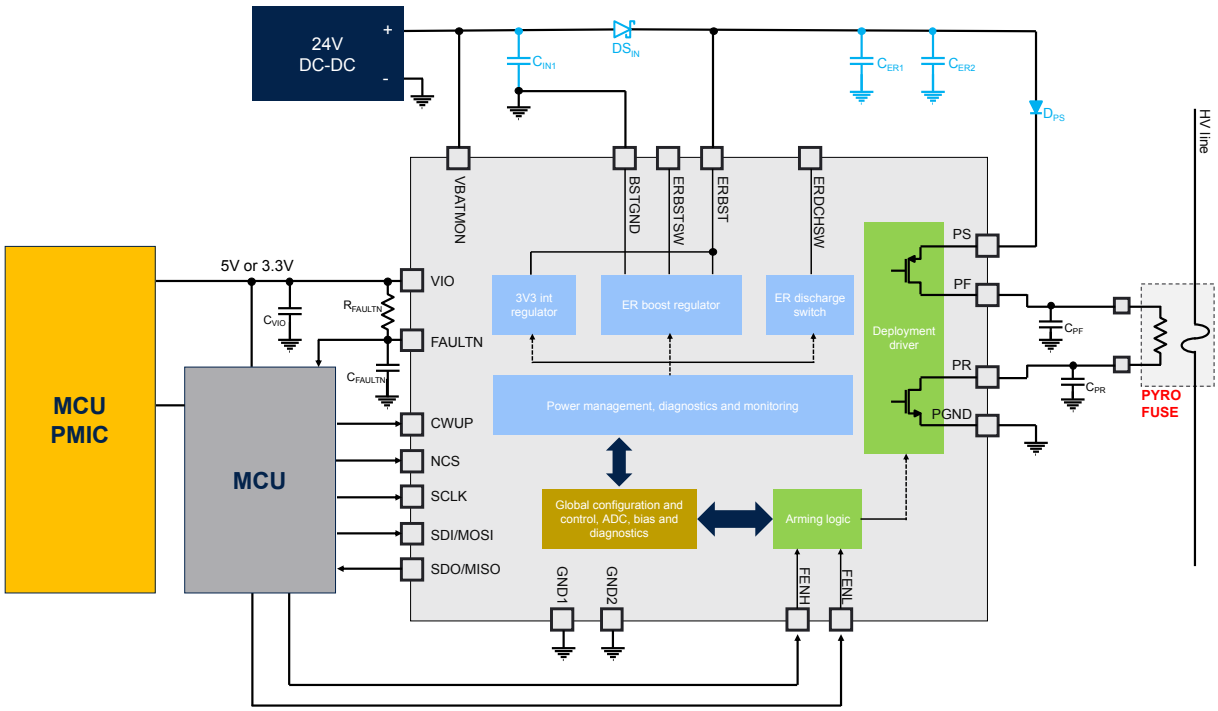
The C_{ER} electrolytic capacitors are connected to ERBST regulator that charge them to a higher voltage respect to battery level V_{BAT}. In this case the ERBST power limit function can be used to limit the ERBST input power and so the power required to the 12 V DC-DC regulator.

ERDCHSW pin is used to allow C_{ER} controlled discharge for safety and diagnostic purposes. R_{DCHG} sets the limit current for the discharge phase.

4.1.4 24 V DC-DC with MCU and ERBST not mounted

The Figure 32 shows a typical application diagram for a pyro-fuse system not using the ERBST regulator and interfaced with a generic MCU.

Figure 32. Application circuit: 24 V DC-DC with MCU and ERBST not mounted

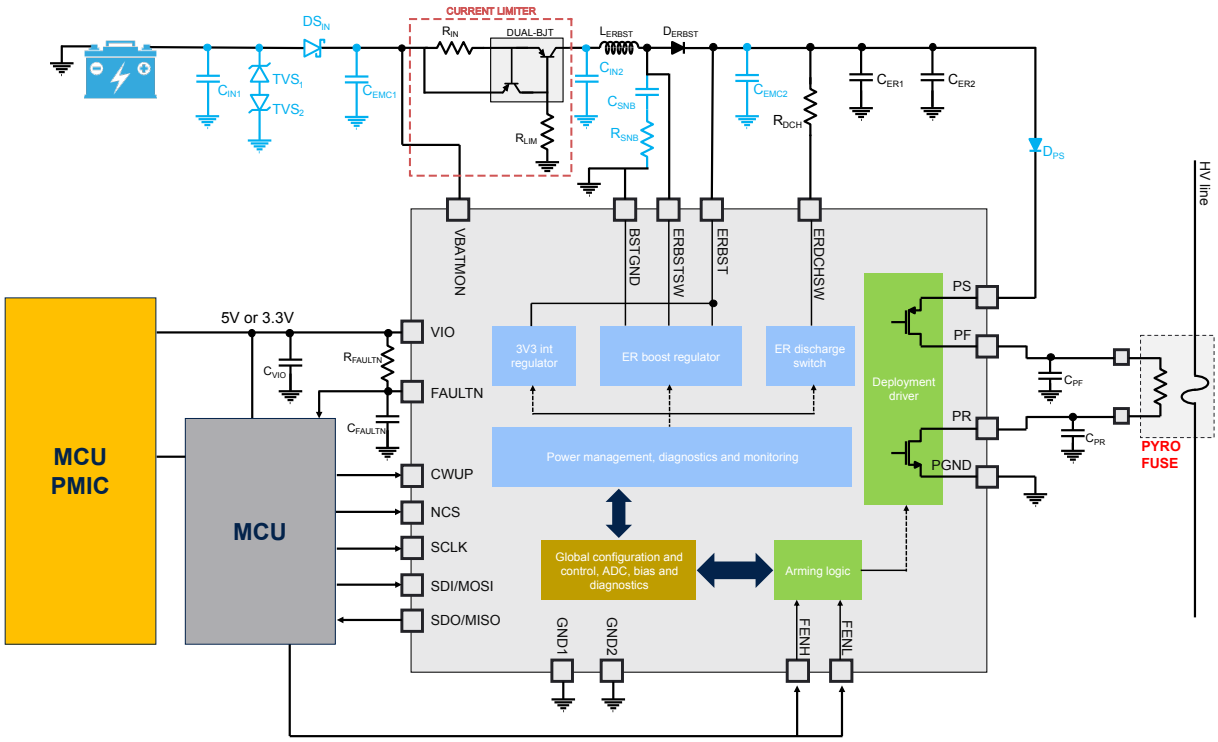


The ERBST regulator is kept disabled and its components are not mounted. The diode D_{IN} is optional and is used to avoid back feeding to the DC-DC regulator.

4.1.5 Single deploy signal to the arming logic

The Figure 33 shows a typical application scenario for a pyro-fuse system where only one external signal is needed for the deployment.

Figure 33. Application circuit: single deploy signal to the arming logic



In this scenario, it is suggested to short-circuit FENH with FENL, and configure the decoder with the same deploy logic on both the FENx. To performs the deploy, both the FENx must be enabled.

4.1.6 Bill of materials (BOM)

Referring to the Figure 16 and Figure 29, the Table 90 reports the bill of materials.

Table 90. Bill of materials (BOM)

Name	Component	Parameter	Min	Typ	Max	Unit
TVS_1 (1)	TVS diode (battery transient protection)	Breakdown voltage		33		V
TVS_2 (1)	TVS diode (reverse battery transient protection)	Breakdown voltage		-14		V
C_{ESD1} (1)	EMC filter	Capacitance		2.31		µF
C_{ESD2} (1)	EMC filter	Capacitance		20		µF
C_{IN1} (1)	Tank capacitor	Capacitance		0.47		µF
C_{IN2} (1)	Tank capacitor	Capacitance		2.2		µF
L_{ERBST} (1)	ERBST inductor	Inductance	27	33	39	µH
		DCR			1.5	Ω
D_{ERBST} (1)	ERBST diode	Forward voltage			1.2	V
R_{DCH} (1)	Discharge resistor	Resistance		68		Ω
C_{ER1} (1)	Primary energy reserve capacitor (electrolytic)	Capacitance	100		600	µF
		ESR	100		500	mΩ
C_{ER2} (1)	Secondary energy reserve capacitor (electrolytic)	Capacitance	100		600	µF
		ESR	100		500	mΩ
C_{SNB} (1)	Snubber circuit	Capacitance		220		pF
R_{SNB} (1)	Snubber circuit	Resistance		10		Ω
Dual-BJT (1)	Current limiter	Max collector current		-500		mA
R_{IN} (1)	Input resistance	Resistance		2.2		Ω
R_{LIM} (1)	Pull down	Resistance		680		Ω
R_{BYPASS} (1)	Bypass resistance	Resistance		4.7		Ω
D_{BYPASS} (1)	Bypass diode	Forward current		3		A
D_{PS} (1)	Back feeding protection	Forward current		3		A
C_{VIO}	VIO bypass capacitor	Capacitance		100		nF
R_{FAULTN}	Pull-up resistor	Resistance		4.7		kΩ
C_{FAULTN}	Bypass capacitor	Capacitance			1	nF
C_{PF}	ESD/EMI capacitor	Capacitance	13	22	138	nF
C_{PR}	ESD/EMI capacitor	Capacitance	13	22	138	nF
Pyrofuse model						
L_{WIRE}	Pyrofuse wire load inductance	Inductance			36	µH
L_{EMI}	Pyrofuse input EMI filter	Inductance			7.7	µH
R_{WIRE}	Pyrofuse wire load resistance	Resistance			1.1	Ω
C_{PYRO}	Pyrofuse differential capacitance between input contacts	Capacitance			100	nF
R_{PYRO}	Pyrofuse igniter resistance	Resistance	1.7		2.5	Ω

1. *These components, based on application circuit, could not be mounted.*

4.2 Device positioning in BMS application

The L9965P/L99BM2P can be interfaced with the companion chip L9965C/L99BM2C which performs the function of monitoring HV battery current, detecting short circuit and triggering pyro-fuse deployment. It also acts as an SPI controller, forwarding frames sent by MCU to L9965P/L99BM2P.

L9965P/L99BM2P is identified in the BMS chipset by the BMS_ID bit field located in the BMS_ID register. It is possible to read the IC version in the CHIP_ID register.

Depending on the source of main supply, the devices can be mounted in HV or LV domain: L9965C/L99BM2C, due to its specific purpose, will always lie in the HV domain, while L9965P/L99BM2P can be mounted in either of the two, depending on the user's hardware and limitations, if any.

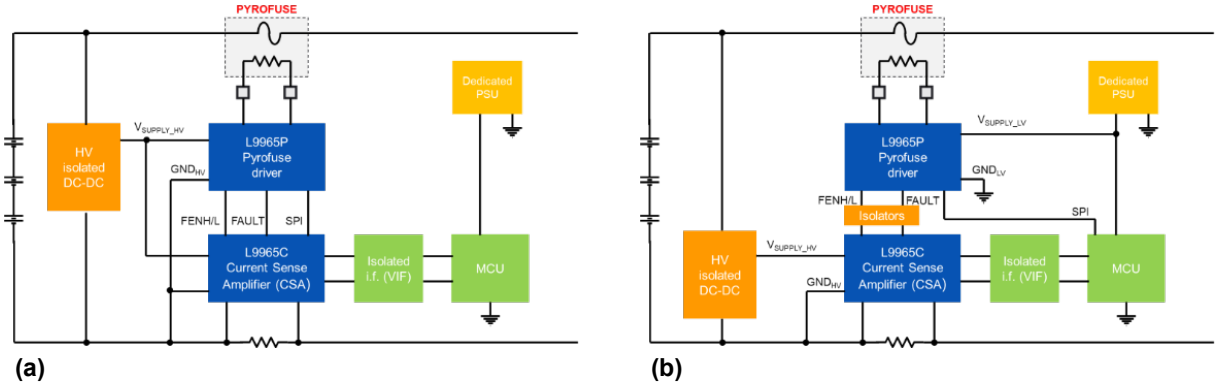
In the HV domain, supply can be sourced from an HV battery through an isolated DC-DC converter and shared between L9965P/L99BM2P and L9965C/L99BM2C (Figure 34 configuration "a").

- Pros:
  - Possible to avoid usage of ER boost regulator and related external components.
  - Deployment trigger pins direct connection to L9965C/L99BM2C.
  - L9965C/L99BM2C acts as a SPI controller to route commands from the MCU.
- Cons:
  - SPI signals suffer a higher delay.

Some pyro-fuse switches might not be compatible with the above solution and require the driving section to be in the LV ground domain (Figure 34 configuration "b").

- Pros:
  - Direct connections to MCU's SPI.
  - Compatibility with all pyro-fuse switches.
- Cons:
  - Cannot avoid ER boost usage (unless minimum V_{BAT} can be guaranteed).
  - Requires additional components (isolators to interface with L9965C/L99BM2C).

Figure 34. Pyro-fuse driver positioning



5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 VFQFN32 (5x5x0.9 mm 32+4L WETT. FLANKS) package information

Figure 35. VFQFN32 (5x5x0.9 mm 32+4L WETT. FLANKS) package outline

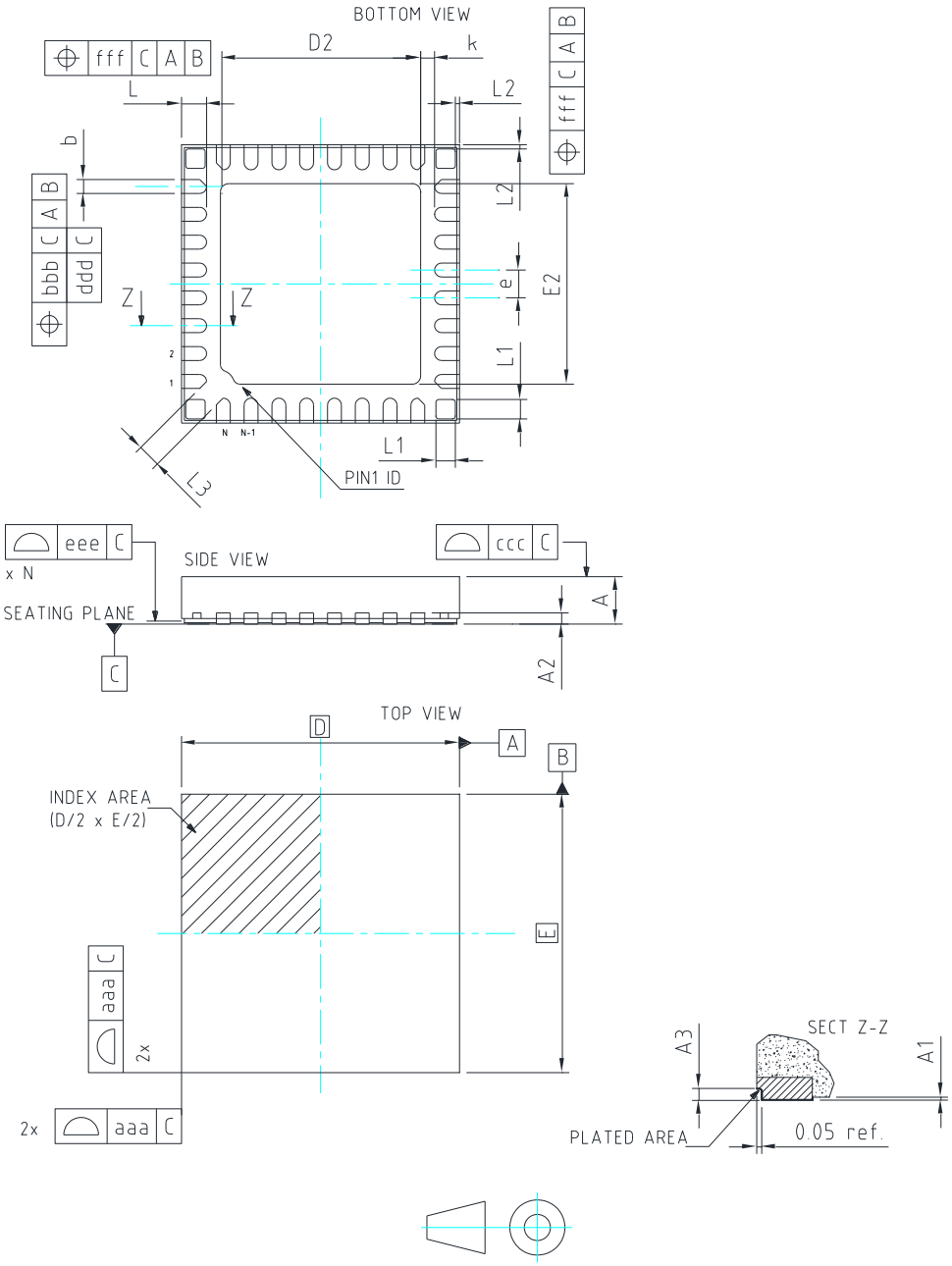
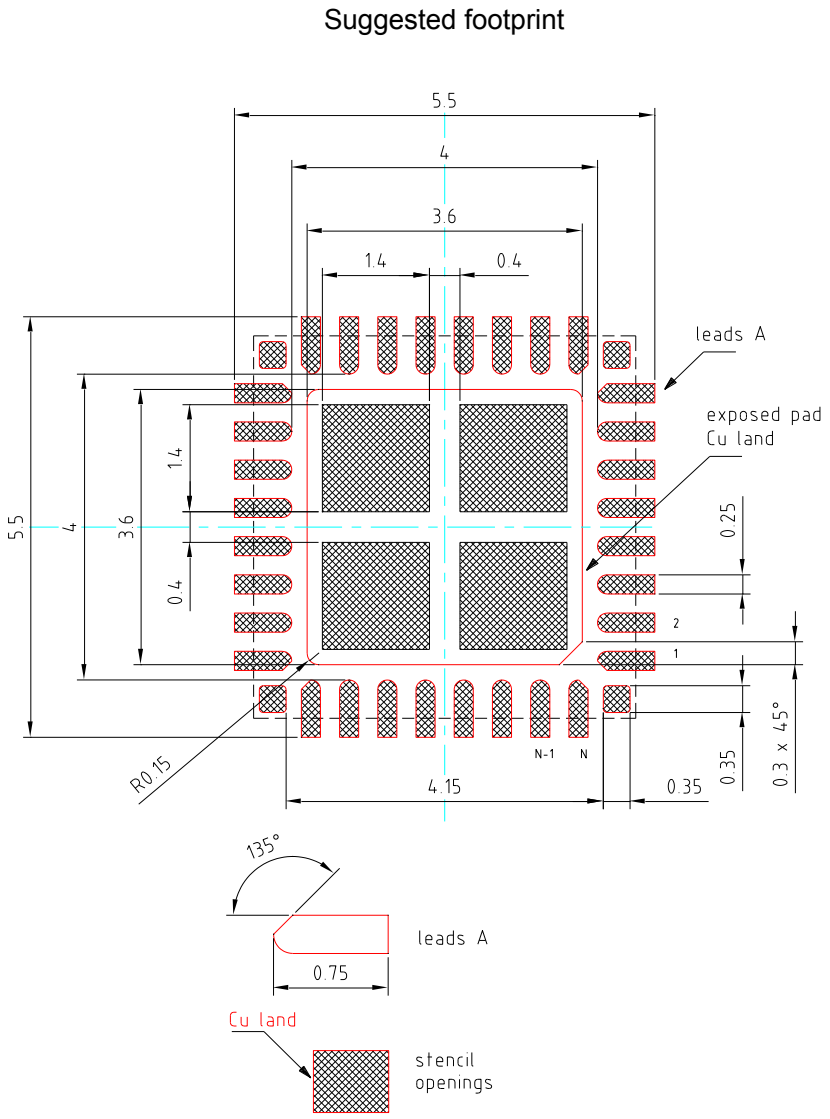


Table 91. **VFQFN32 (5x5x0.9 mm 32+4L WETT. FLANKS) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2		0.2 REF	
A3	0.10	-	-
b	0.20	0.25	0.30
D	-	5.00	-
D2	3.55	3.60	3.65
e	-	0.5	-
E	-	5.00	-
E2	3.55	3.60	3.65
L	0.40	0.45	0.50
L1	0.30	0.35	0.40
L2	-	0.075	-
L3	0.37	0.42	0.47
k	0.20	-	-
N		32+4	
Tolerance of form and position			
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 36. **VFQFN32 (5x5x0.9 mm 32+4L WETT. FLANKS) footprint**



5.2 TQFP32L (7x7x1 mm 32+4L exposed pad down) package information

Figure 37. **TQFP32L (7x7x1 mm 32+4L exposed pad down) package outline**

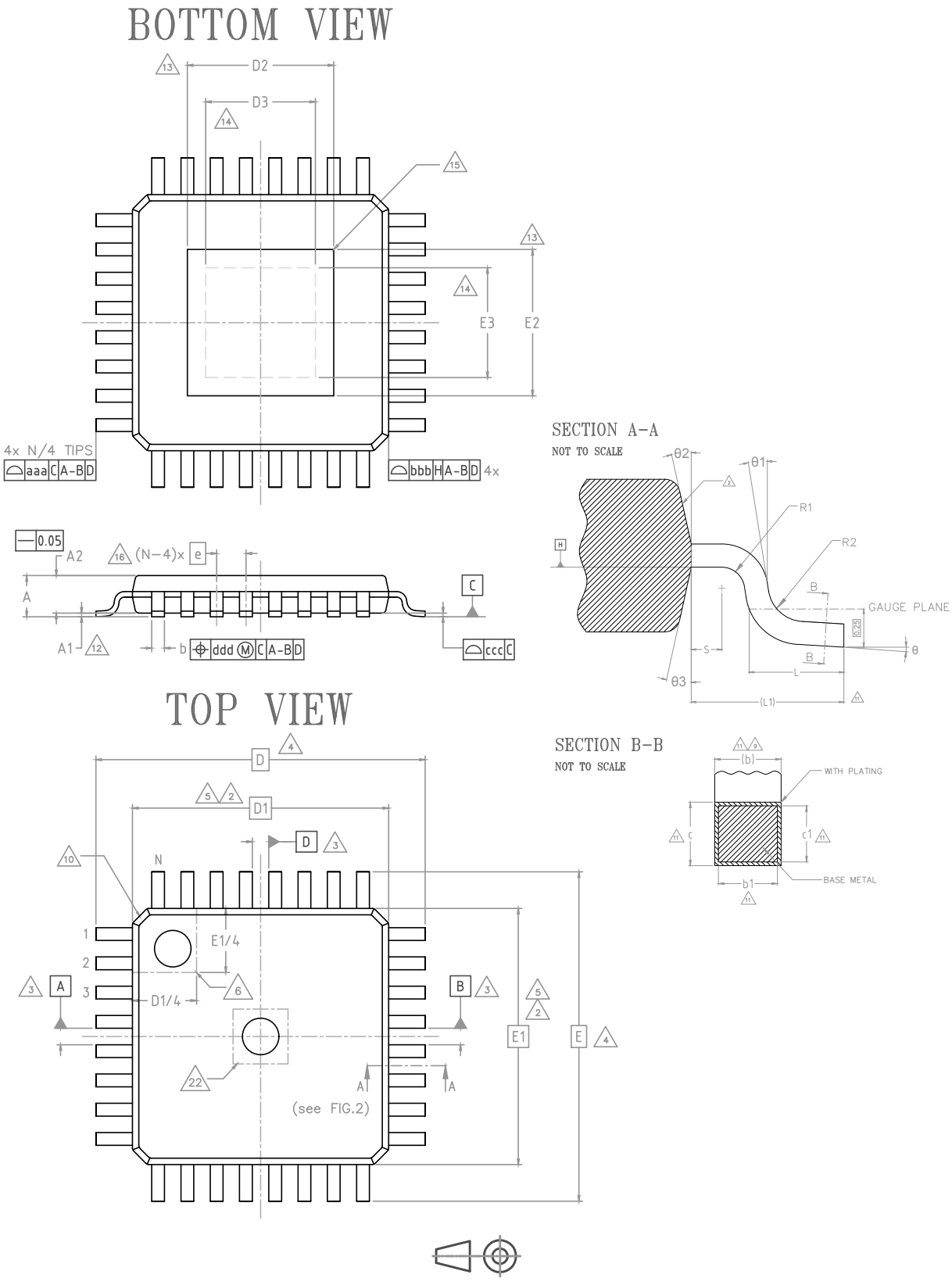
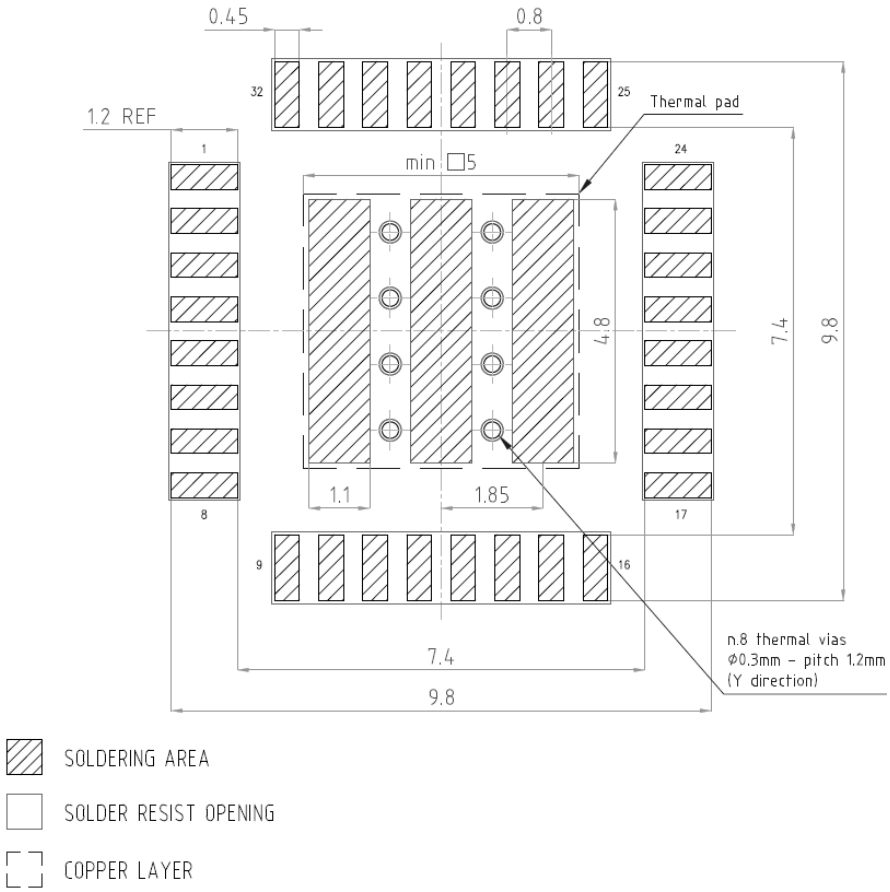


Table 92. **TQFP32L (7x7x1 mm 32+4L exposed pad down) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ	0°	3.5	7°
Θ1	0°	-	-
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
c	0.09	-	0.20
c1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
D2	-	5.00	5.37
D3	3.40	-	-
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
E2	-	5.00	5.37
E3	3.40	-	-
L	0.45	0.60	0.75
L1	1.00 REF		
N	32+4		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		

Figure 38. **TQFP32L (7x7x1 mm 32+4L exposed pad down) pcb land pattern**



Revision history

Table 93. **Document revision history**

Date	Version	Changes
01-Aug-2024	1	Initial release.
12-Aug-2024	2	Minor text changes in Section 5.1: VFQFN32 (5x5x0.9 mm 32+4L WETT. FLANKS) package information.
10-Jan-2025	3	Updated Section 3.5, Section 3.7.2.1, Table 23, Table 27, Section 3.14.2.1, and Section 5.1. Minor text changes.
10-Jun-2025	4	References to FOR removed from Section 2.2. $I_{DELTA\_PR\_PD}$ parameter changed in $I_{DELTA\_ACT\_PD\_PR}$ and its description updated. Power cycle means CWUP toggle:Table 9 and Table 34 modified. Two notes added in Section 3.6.1.1. I_{DP_PR} parameter changed in $I_{ACT\_PD\_PR}$ and its description updated. Note added in Section 3.7.2.1. Section 3.7.2.7 modified: ERDCHSW_OV pulls low the FAULTN pin; detailed description of ER cap diag removed. Section 3.14.2.1: note added, DIAG_CMD description updated. Added references to nPOR_SLEEP and nPOR_MAIN in Section 3.18.1. Added references to Application Notes in Section 4.1. Minor typo fixed.
05-Dec-2025	5	Added L99BM2P part number and updated document title. Updated Table 3 ($V_{ERBSTSW}$ OR_{MAX} value), Table 30 (unit), Table 73 (TRIM_HS_RET_CFG description), Table 74 (TRIM_VRES_POST_TH field name), Table 77 (TRIM_T_DEPLOY_CFG field name), Table 90, and Table 92 (added D2, E2 typ. value). Updated Features, Description, Figure 29, Figure 30, Figure 31, and Figure 32. Updated Section 3.7.2.7, Section 3.16, Section 3.18.1, Section 4.1.6, and added Section 4.1.5. Removed *section Mission Profile*.

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