L9965A/L99BM218

Datasheet

18 Cell battery management IC

Product status link
L9965A/L99BM218

Product label
SUSTAINABLE TECHNOLOGY

Features

- Temperature grade 1: –40°C to +125°C operating temperature range
- HBM ESD classification level 2
- CDM ESD classification level C4B
- Fully synchronized high-accuracy measurements on cell voltage, busbar and stack voltage with dedicated ADC:
  - Total error including aging and post soldering <1.4 mV at 3.3 V, -40°C to 105°C
  - 16-bit resolution
  - Cell range: -1 V to 5.5 V
  - Integrated digital filtering with programmable cut-off frequency from 3.3 kHz to 4.4 Hz
  - Fully redundant architecture
  - Cell and busbar support on every channel
  - Dedicated busbar channel with a ±1 V range
- Passive internal cell balancing up to 400 mA, supporting time-continuous and PWM modes, with automatic cool down based on external NTC sensing. Overcurrent protection during balancing is also available in low-power mode.
- Integrated DC-DC converter for energy efficiency:
  - Deep sleep: <12 µA
  - Cyclic Wake-up Mode: <20 µA
  - Normal Mode: <3 mA
- 10 configurable GPIO
- SPI controller and I2C controller peripherals for interfacing external EEPROMs and sensors
- SPI target for direct MCU interface
- Stackable architecture for high-voltage battery packs up to 59 devices
- Embedded NVM for configuration parameter storage and runtime configuration integrity check
- Ultra-fast vertical interface peripheral for isolated communication
- Compatible with L9965C pack monitoring chip with a max desynchronization time of 7 µs at system level

Applications

- Automotive battery monitoring systems.
- Energy storage systems.
- UPS.

Description

The L9965A/L99BM218 is an 18-channel battery cell monitoring and balancing IC.

The device belongs to the L9965/L99BM2 chipset family for high-voltage battery management system monitoring and control (automotive/industrial respectively).

1 Overview

The L9965A/L99BM218 BMIC device provides all the functions needed to manage battery pack configurations up to 18s. It features a comprehensive set of cell/pack monitoring, balancing, and protection functions designed to achieve the highest FuSa targets in demanding systems (ASIL D for automotive applications).

The device uses dedicated high precision ADCs which synchronously acquire cell, busbar and pack voltage. The cell measurement ranges from -1 V to 5.5 V, making the L9965/L99BM2 family suitable for most battery chemistries.

An arbitrary number of busbars can be monitored by every cell voltage pair and a dedicated BB channel.

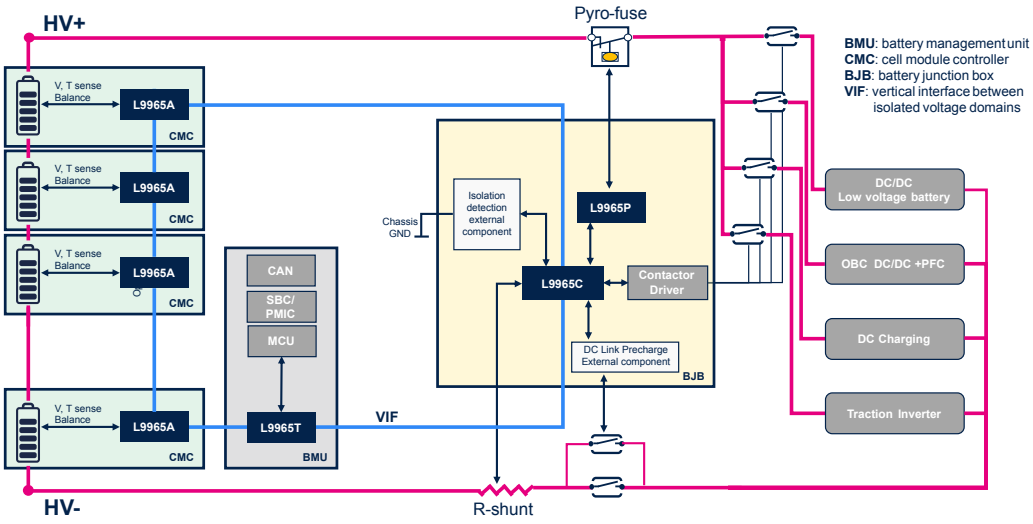
The BMIC is supplied via an efficient buck pre-regulator, thus optimizing energy consumption and heat dissipation. It also integrates a 5 V LDO available for biasing external sensors and supplying external EEPROMs.

A SPI controller and I2C controller peripherals allow interfacing the device with external sensors and EEPROMs.

Passive balancing is available in both continuous and PWM mode.

Up to 59 addressable devices can be stacked in a vertical isolated communication interface. The L9965A implements an ultra-fast isolated communication protocol allowing for transfer of voltage and temperature data of the whole daisy-chain in less than 10 ms.

Figure 1. L9965A battery monitor in an automotive BMS system



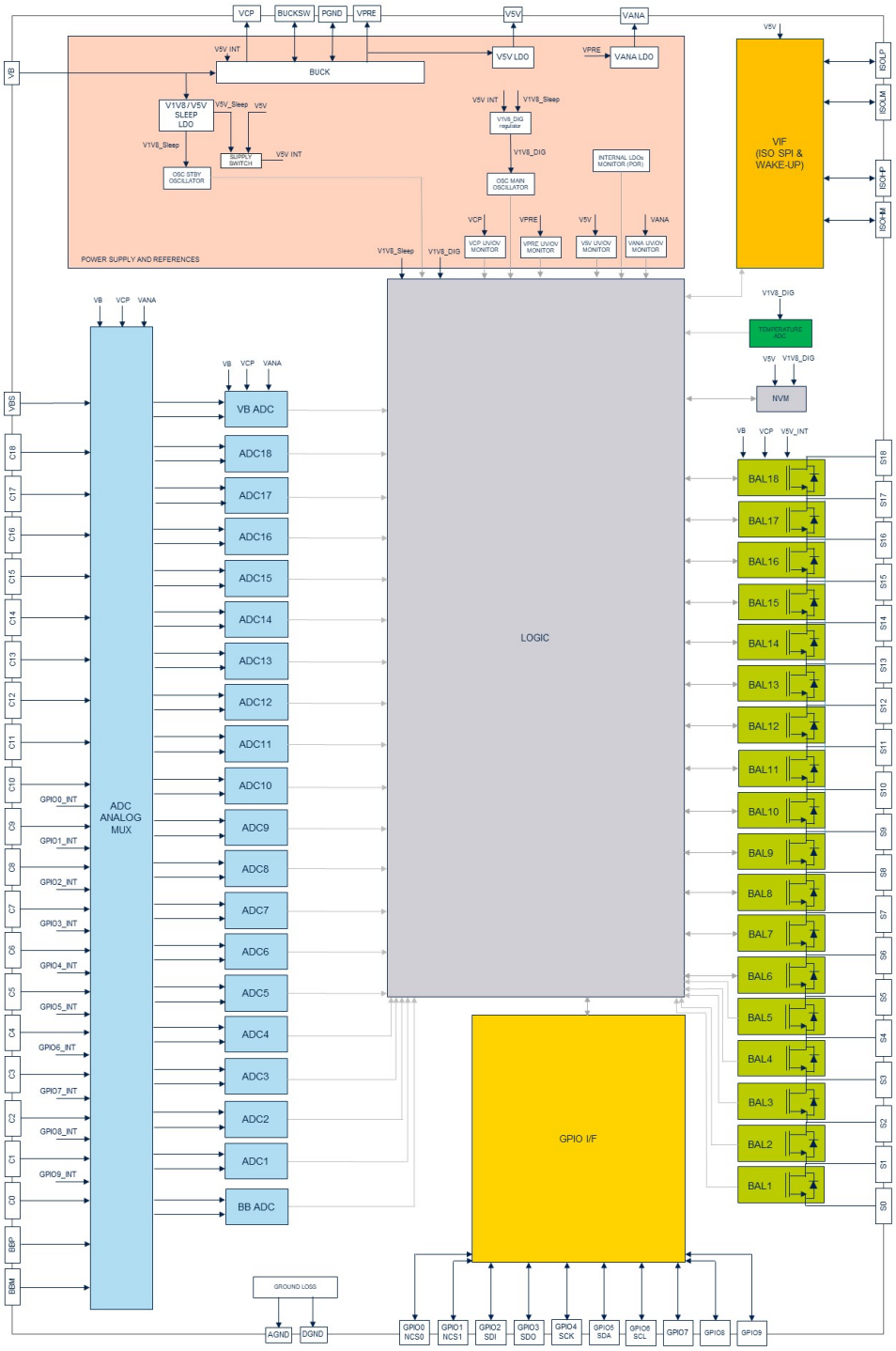
L9965A/L99BM218 embeds a functional state machine to optimize system power consumption without compromising safety functions:

- NORMAL: full operation mode.
- CYCLIC WAKEUP: low-power mode triggered by the L9965T/L99BM2T companion chip, to perform cyclic diagnostics during low-power operation. In this state, the device is sensitive to fault/wake-up tones from the VIF.
- SILENT BALANCING: Low-power state for managing long balancing periods. In this state, the device is sensitive to wake-up tones both from the VIF in case of fault and from the SPI if directly connected to the MCU. Moreover, the balancing overcurrent is active.
- DEEP SLEEP: Ultralow-power state for managing long inactivity periods. In this state, the device is sensitive to wake-up tones both from the VIF in case of fault and from the SPI if directly connected to the MCU.

2 Block diagram and pin description

2.1 Block diagram

Figure 2. **Block diagram**



2.2 Pin description

Figure 3. **L9965A pinout (top view)**

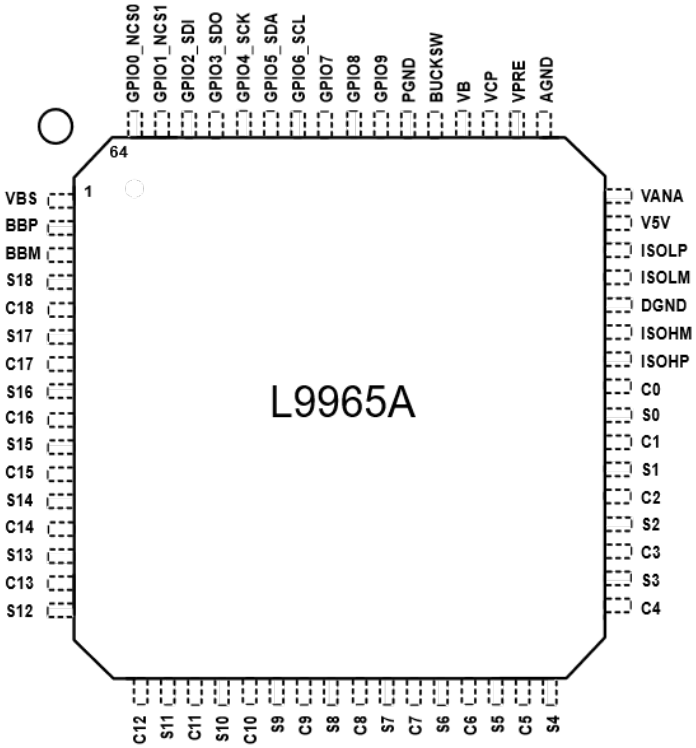


Figure 4. **L99BM218 pinout (top view)**

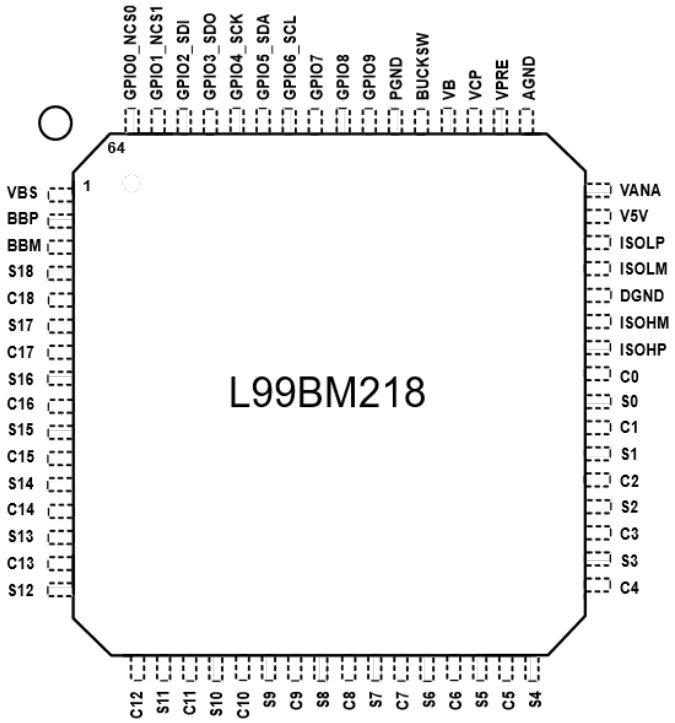


Table 1. Pin function

Pin #	Pin name	Description	Pin type	Pin category
1	VBS	Battery sense line	Analog input	Global
2	BBP	Busbar sense line (positive)	Analog input	Global
3	BBM	Busbar sense line (negative)	Analog input	Global
4	S18	Cell balancing line	Analog I/O	Global
5	C18	Cell sense line	Analog input	Global
6	S17	Cell balancing line	Analog I/O	Global
7	C17	Cell sense line	Analog input	Global
8	S16	Cell balancing line	Analog I/O	Global
9	C16	Cell sense line	Analog input	Global
10	S15	Cell balancing line	Analog I/O	Global
11	C15	Cell sense line	Analog input	Global
12	S14	Cell balancing line	Analog I/O	Global
13	C14	Cell sense line	Analog input	Global
14	S13	Cell balancing line	Analog I/O	Global
15	C13	Cell sense line	Analog input	Global
16	S12	Cell balancing line	Analog I/O	Global
17	C12	Cell sense line	Analog input	Global
18	S11	Cell balancing line	Analog I/O	Global
19	C11	Cell sense line	Analog input	Global
20	S10	Cell balancing line	Analog I/O	Global
21	C10	Cell sense line	Analog input	Global
22	S9	Cell balancing line	Analog I/O	Global
23	C9	Cell sense line	Analog input	Global
24	S8	Cell balancing line	Analog I/O	Global
25	C8	Cell sense line	Analog input	Global
26	S7	Cell balancing line	Analog I/O	Global
27	C7	Cell sense line	Analog input	Global
28	S6	Cell balancing line	Analog I/O	Global
29	C6	Cell sense line	Analog input	Global
30	S5	Cell balancing line	Analog I/O	Global
31	C5	Cell sense line	Analog input	Global
32	S4	Cell balancing line	Analog I/O	Global
33	C4	Cell sense line	Analog input	Global
34	S3	Cell balancing line	Analog I/O	Global
35	C3	Cell sense line	Analog input	Global
36	S2	Cell balancing line	Analog I/O	Global
37	C2	Cell sense line	Analog input	Global
38	S1	Cell balancing line	Analog I/O	Global
39	C1	Cell sense line	Analog input	Global

Pin #	Pin name	Description	Pin type	Pin category
40	S0	Cell balancing line	Analog I/O	Global
41	C0	Cell sense line	Analog input	Global
42	ISOHP	VIF high port (positive)	Analog I/O	Global
43	ISOHM	VIF high port (negative)	Analog I/O	Global
44	DGND	digital ground	GND	Global
45	ISOLM	VIF low port (negative)	Analog I/O	Global
46	ISOLP	VIF low port (positive)	Analog I/O	Global
47	V5V	5V communication line supply	Regulator out	Local
48	VANA	5V internal analog supply	Regulator out	Local
49	AGND	Analog ground	GND	Global
50	VPRE	Pre-regulator supply	Regulator out	Local
51	VCP	Charge pump tank	Regulator out	Local
52	VB	Battery supply	Supply	Global
53	BUCKSW	Buck regulator switching node	Analog I/O	Local
54	PGND	Power ground	GND	Global
55	GPIO9	Analog input	Analog input	Local
56	GPIO8	Analog input	Analog input PU/PD (on-demand)	Local
57	GPIO7	Analog input	Analog input PU/PD (on-demand)	Local
58	GPIO6_SCL	Analog input/serial clock (I2C)	Analog input/digital I/O PU/PD (on-demand)	Local
59	GPIO5_SDA	Analog input/serial data (I2C)	Analog input/digital I/O PU/PD (on-demand)	Local
60	GPIO4_SCK	Analog input/serial clock (SPI)	Analog input/digital I/O PU/PD (on-demand)	Local
61	GPIO3_SDO	Analog input/serial data out (SPI)	Analog input/digital I/O PU/PD (on-demand)	Local
62	GPIO2_SDI	Analog input/serial data in (SPI)	Analog input/digital I/O PU/PD (on-demand)	Local
63	GPIO1_NCS1	Analog input/chip select 2 (SPI)	Analog input/digital I/O PU/PD (on-demand)	Local
64	GPIO0_NCS0	Analog input/chip select 1 (SPI)	Analog input/digital I/O PU/PD (on-demand)	Local
65	EP	Exposed pad - connect to AGND	GND	-

2.3 Unused pins

A cell shall always be present between pins C0 and C1 and enabled by its VCELL1_EN bit. In case the C0-C1 pair is used as a busbar sensing channel, then the first cell shall be connected between the C1 and C2 pins. The remaining cells shall be mounted starting from the top (cell 18) down. Cell pairs (C_X – C_{X-1}) which are completely unused shall be short-circuited and connected to the negative terminal of the first mounted cell upwards. Such cells shall be disabled via their respective VCELL<x>_EN bit.

Unused balancing pairs (S_X – S_{X-1}) shall be short-circuited and connected to the negative terminal of the first balancing stage upwards. Such balancing stages shall be disabled via their respective BAL<x>_EN bit.

Cell pairs (C_X – C_{X-1}) which are used for busbar sensing shall be treated as regular cells and kept enabled. However, their balancing stage shall be unused and managed as described below.

When the busbar pair (BBP – BBM) is unused, BBP-BBM shall be short-circuited and connected to AGND. The channel shall be disabled via the BB_EN pin.

Unused GPIOs (GPIOx) shall be connected to AGND. They shall be left programmed as analog input via GPIO<x>_CONF.

Unused VIF ports (ISOxP – ISOxM) shall be terminated with R_{TERM}.

3 Device ratings

3.1 Electrical ratings

The following section describes the different operational ranges.

For each device pin:

- **Operating Range (OR):** Within this range, functions operate as specified and without parameter deviations. All the device's electrical parameters are tested and guaranteed in this range and are valid over the whole junction temperature operating range, unless otherwise specified.
- **Absolute Maximum Rating range (AMR):** Within this range, functions may not operate properly. However, the IC will not be damaged. Exposure to AMR conditions for extended periods may affect device reliability. Exceeding any AMR may cause permanent damage to the integrated circuit.

Note: Currents are noted with a positive sign when flowing into a pin.

Note: Integrated protections and diagnostics are designed to prevent device destruction under the fault conditions described in the specification. Fault conditions are considered to be outside of the normal operating range. Protection functions are not designed for continuous repetitive operation.

All parameters are tested and guaranteed under the following conditions, unless otherwise noted:

- All supplies according to the operating range in Table 2.
- T_J according to the operating range in Table 4.

Table 2. Electrical Ratings

Parameter	Description	Test Condition	AMR_{MIN}	OR_{MIN}	OR_{TYP}	OR_{MAX}	AMR_{MAX}	Unit	Notes
Power supplies									
V_{VB}	VB voltage range	Vs. AGND	-0.3	11		90	110	V	
V_{VB}-V_{C18}	Differential voltage between VB and C18 pins		-110	-1		20	110	V	For best accuracy, VB normal operating voltage shall be equal to the sum of cells. Differences outside the operating range are tolerated but may cause a degradation in performance
V_{VB}-V_{C17}	Differential voltage between VB and C17 pins		-110	-1		20	110	V	Supports C18/C17 pair used as a busbar
V_{VB}-V_{VBS}	Differential voltage between VB and VBS pins		-110	-1		20	110	V	For best accuracy, VB normal operating voltage shall be equal to the sum of cells. Differences outside the operating range are tolerated but may cause a degradation in performance
V_{VB}-V_{BBx}	Differential voltage between VB and BBx pins		-110	-1			110	V	Supports busbar connection above C18
V_{BUCKSW}	VB: voltage range	vs. AGND	-0.3	13		90	110	V	The max output current recirculating in the lower ESD diode is I_{OUT} = 300 mA
V_{VPRE}	VPRE: voltage range	vs. AGND	-0.3	7		11	110	V	Regulated voltage
V_{V5V}	V5V: voltage range	vs. AGND	-0.3		5		7	V	Regulated voltage
V_{VANA}	VANA: voltage range	vs. AGND	-0.3		5		7	V	Regulated voltage

Parameter	Description	Test Condition	AMR_{MIN}	OR_{MIN}	OR_{TYP}	OR_{MAX}	AMR_{MAX}	Unit	Notes
V_{VCP}	VCP: voltage range	vs. AGND	V_{VB} -0.3		V_{VB} +10		min(V_{VB} + 14; 110)	V	Charge pump voltage
Grounds									
V_{DGND}	DGND: voltage range	vs. AGND	-0.3	-0.1		0.1	0.3	V	
V_{PGND}	PGND: voltage range	vs. AGND	-0.3	-0.1		0.1	0.3	V	
Cell sensing & balancing AFE									
V_{Cx}	C0: voltage range	vs. AGND	-0.3	-0.3		0.3	6.5	V	
	C1: voltage range	vs. AGND	-2	-1		min(V_{VB}-8;5.5)	6.5	V	
	C2: voltage range	vs. AGND	-0.3	0		min(V_{VB}-8;11)	110	V	
	C3…C10: voltage range	DEEP SLEEP vs. AGND	-0.3	0		min(V_{VB}-5;55)	110	V	The AMR in DEEP SLEEP guarantees robustness to hotplug
		NORMAL vs. AGND	-0.3	0		min(V_{VB}-5;55)	65	V	During NORMAL operation, the voltage on these pins is never supposed to be higher than AMR
	C11…C18: voltage range	vs. AGND	-0.3	0		V_{VB}+0.3	110	V	
V_{Cx}-V_{Cx-1}	Differential voltage between adjacent cell pins		-110	-1		5.5	110	V	
V_{VBS}	VBS: voltage range	vs. AGND	-0.3	11		90	110	V	
V_{VBS}-V_{C18}	Differential voltage between VBS and C18 pins		-0.3	-0.3		20	110	V	
V_{Sx}	S0: voltage range	vs. AGND	-0.3	-0.3		0.3	6.5	V	
	S1…S18: voltage range	vs. AGND	-0.3	0		V_{VB}+0.3	Min(110, 6+14*x)	V	x=[1;18]
V_{Sx}-V_{Sx-1}	Differential voltage between adjacent balancing pins		-0.3	0		5.5	14	V	No leakage and cell measurement accuracy guaranteed while in the FOR
V_{Cx}-V_{Sx}	Differential voltage between Cx and Sx pins		-110	-1		5.5	110	V	
V_{BBx}	BBP, BBM: voltage range	vs. AGND	-0.3	-0.3		91	110	V	Supports busbar connection between C0 and C1 pins. See Figure 9.
V_{BBP}-V_{BBM}	Differential voltage between BBP and BBM pins		-2	-1		1	2	V	

Parameter	Description	Test Condition	AMR_{MIN}	OR_{MIN}	OR_{TYP}	OR_{MAX}	AMR_{MAX}	Unit	Notes
GPIOs									
V_{GPIOx}	GPIO0…GPIO9: voltage range	vs. AGND	-0.3	0		V_{V5V}/ V_{VANA}	40	V	The V5V maximum operating voltage applies to GPIOs configured as digital input/output, while the VANA applies to analog inputs. GPIOs connected to external NTCs shall withstand short-circuit to VB maximum operating voltage by means of external series resistors, keeping the injected current below 20 mA. When used as analog inputs, all GPIOs are protected against back-feeding towards V5V.
VIF – ISO SPI									
V_{ISOx}	ISOLM, ISOLP, ISOHM, ISOHP: voltage range	vs. AGND	-9	0		V_{V5V}	18	V	AMR are accounting for the maximum voltage that can be withstood during hotplug, BCI and system level ESD trials

3.2 ESD ratings

Table 3. ESD protection

Test type	Pin	Value	Unit
HBM (1)	All pins	+/-2	kV
HBM (1)(2)	VB, VBS, BB_X, C_X, S_X, $ISOH_X$, $ISOL_X$	+/-4	kV
CDM (3)	All pins	+/-500	V
CDM (3)	Corner pins	+/-750	V
Latch-up (4)	All pins	+/-100	mA

1. *HBM (Human Body Model) according to AEC-Q100-002.*
2. *Each pin is tested vs. GND pins connected together.*
3. *CDM (Charged Device Model) according to AEC-Q100-011.*
4. *Latch-up test according to AEC-Q100-004 Class-2, Level-A.*

3.3 Thermal ratings

All electrical parameters in this document are tested and guaranteed under the conditions specified in Table 4 below.

Table 4. Temperature ranges and thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{amb}	Operating temperature (ECU environment)	-40		125	°C
T_J	Operating junction temperature	-40		140	°C
T_{stg}	Storage temperature	-40		150	°C
$R_{Th\ j\text{-}a}$	Thermal resistance junction-to-ambient (1)		19		°C/W
R_{Th_jb}	Junction to board (1)		7.7		°C/W
R_{Th_jc}	Junction to case thermal resistance (1)		9.1		°C/W

1. *Evaluated according to Jedec JESD51-2, -5, -7 guideline with a 2s2p thermally enhanced PCB.*

4 Current consumption

See below a list of current consumption requirements in different working conditions relevant for the application.

Table 5. Current consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Notes
$I_{VB\_SLEEP\_85C}$	Base current consumption from VB pin, with all resources enabled and in idle state	DEEP SLEEP, -40°C ≤ T_J≤ +85°C		8	12	µA	VB
$I_{VB\_SLEEP\_125C}$	Base current consumption from VB pin, with all resources enabled and in idle state	DEEP SLEEP, +85°C ≤ T_J ≤ +125°C			17	µA	VB
$I_{VB\_SIL\_BAL\_105C}$	Base current consumption from VB pin, with all resources enabled and in idle state	SILENT BALANCING, T_J ≤ +105°C		35	100	µA	VB
$I_{VB\_SIL\_BAL\_125C}$	Base current consumption from VB pin, with all resources enabled and in idle state	SILENT BALANCING, +105°C ≤ T_J ≤ +125°C			120	µA	VB
I_{VB_NORM}	Base current consumption from VB pin, with all resources enabled and in idle state	NORMAL *Note: The I_{VPRE_IDLE} contribution from the buck converter is not included in this parameter*		1	1.3	mA	VB
I_{VPRE_IDLE}	Base current consumption from VPRE pin, with all resources enabled and in idle state	NORMAL		2.5	4	mA	VPRE
$I_{VB\_DELTA\_ADCV1}$	Delta current from VB for voltage ADC conversion	For each voltage ADC continuously converting, ADC11-ADC18, BB		180	225	µA	VB
$I_{VB\_DELTA\_ADCV2}$	Delta current from VB for voltage ADC conversion	For each voltage ADC continuously converting, ADC1-ADC10, VBS		115	150	µA	VB
$I_{VB\_DELTA\_CONV}$	Delta current from VB for voltage ADC conversion	Voltage conversion ongoing		300	480	µA	VB
$I_{VPRE\_DELTA\_CONV}$	Delta current from VPRE for voltage ADC conversion	Voltage conversion ongoing Guaranteed by design.		150	300	µA	VPRE
$I_{VPRE\_DELTA\_ADCV}$	Delta current from VPRE for voltage ADC conversion	One voltage ADC continuously converting		350	480	µA	VPRE
$I_{VB\_DELTA\_BAL}$	Delta current from VB for balancing	During balancing, for each balancing channel enabled, T_J < 125C		16	25	µA	VB
$I_{VPRE\_DELTA\_COMM}$	Delta current consumption from VPRE pin when communication is ongoing	One VIF port continuously transmitting. Using recommended BOM.		8.5	13	mA	VPRE
$I_{VPRE\_DELTA\_GPIO}$	Delta current from VPRE when one GPIO is programmed as digital output			45	100	µA	VPRE
$I_{VB\_SPREAD\_0}$	Process spread of I_{VB}	All devices operating at the same VB, at T_{amb} = 25°C with 5mA load connected to V5V. Guaranteed by design.	-200		200	µA	VB
$I_{VB\_SPREAD\_1}$	Process spread of I_{VB}	All devices operating at the same VB with 5mA load connected to V5V. Guaranteed by design.	-1		1	mA	VB

5 Functional description

5.1 Device functional states

The L9965A/L99BM218 operates according to the following FSM:

Figure 5. Device FSM

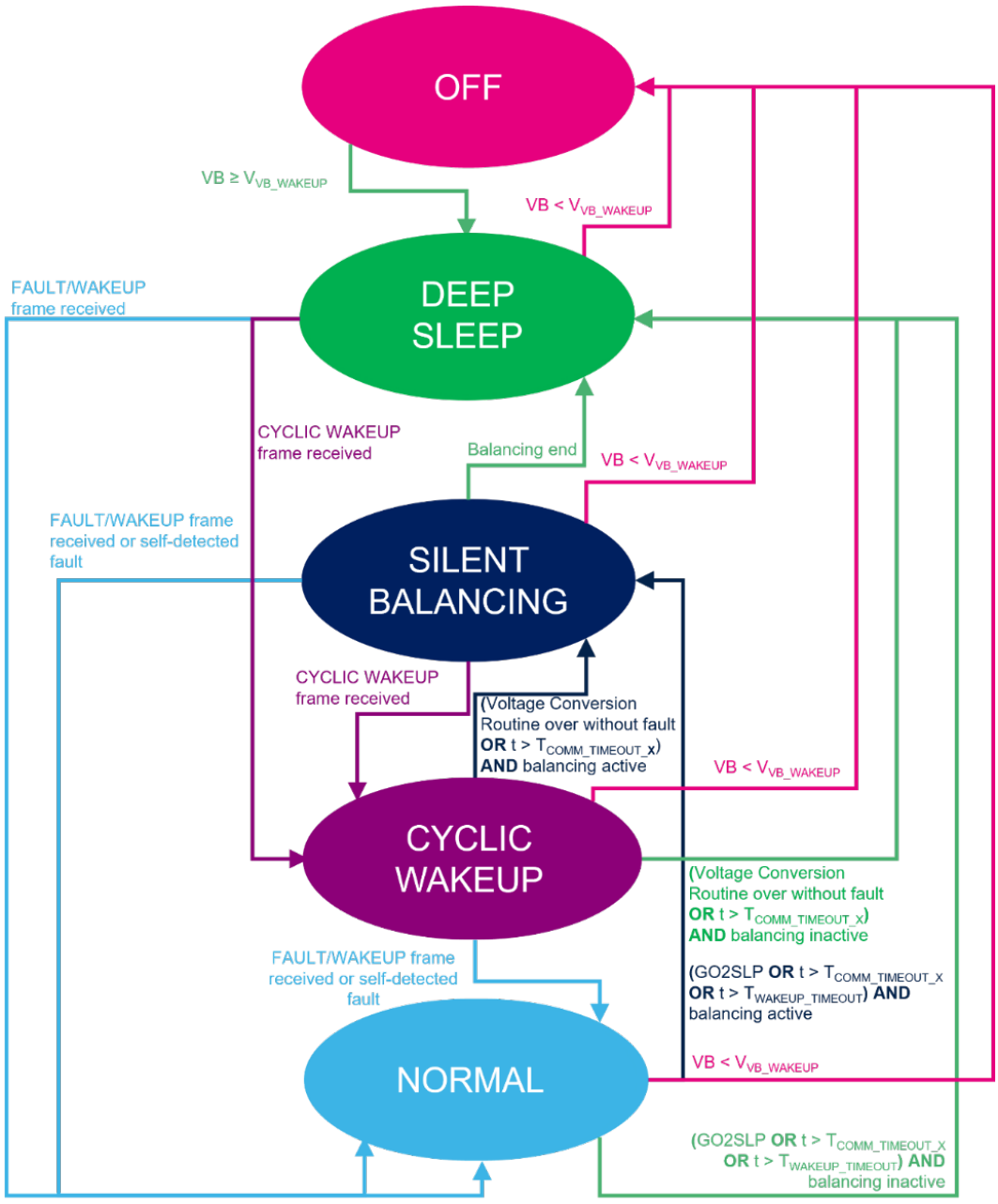


Table 6 summarizes the FSM behavior, describing the transitions and the resources active in each operating state.

Table 6. Device FSM

State	Purpose	Reached from	Condition	Active resources
OFF	Device OFF	Any state	When VB voltage falls below V_{VB_WAKEUP}	None
DEEP SLEEP	Ultralow-power state for managing long inactivity periods	OFF	When VB rises above V_{VB_WAKEUP}	
		NORMAL	GO2SLP command received, or communication timeout expired, with balancing inactive and voltage conversion routine not running	Wakeup via VIF Wakeup via SPI target
		SILENT BALANCING	Balancing task over	
		CYCLIC WAKEUP	Voltage conversion routine over, with balancing inactive	
SILENT BALANCING	Low-power state for managing long balancing periods	NORMAL	GO2SLP command received, or communication timeout expired, with voltage conversion routine not running and balancing active	All resources active in DEEP SLEEP, plus the following: Cell balancing FETs (Sx) Balancing overcurrent (BAL OC)
		CYCLIC WAKEUP	Voltage conversion routine over, with balancing inactive	
CYCLIC WAKEUP	To perform cyclic diagnostics during low-power operation	DEEP SLEEP	CYCLIC WAKEUP frame received	All resources fully operating, except communication timeout (COMM_TIM). Delta diagnostics available for GPIOx and Cx pins. Isolated Vertical Interface (VIF) partially available (passthrough from ISOL to ISOH disabled)
		SILENT BALANCING	CYCLIC WAKEUP frame received	
NORMAL	Full operation	DEEP SLEEP	WAKEUP/FAULT frame received	All resources fully operating. Delta diagnostics performed in CYCLIC WAKEUP are unavailable for GPIOx and Cx pins.
		SILENT BALANCING	WAKEUP/FAULT frame received or self-detected fault	
		CYCLIC WAKEUP	WAKEUP/FAULT frame received or self-detected fault	

Transition from NORMAL to low-power states occurs whenever a GO2SLP is commanded if the Voltage conversion routine is not running. To do so, the MCU has to write the 0xCC code in the SPECIAL_KEY field. The IC will answer with the register content feedback, as for a usual write operation in VIF communication where the device has been addressed with its VIF ID (not valid for broadcast command). Right after that, it will move to the low-power state.

If, after sending GO2SLP, a wake-up via VIF or via SPI target is received from the device, it will abort the shutdown request and will remain in NORMAL state.

The POR_MAIN flag, if asserted, indicates that an event of POR_MAIN_N has occurred or a software reset has been triggered. The POR_MAIN_N event could be caused by a transition from NORMAL/CYCLIC WAKEUP to any other low-power state (SILENT BALANCING /DEEP SLEEP/OFF) or if an oscillator stuck or a ground loss of AGND or DGND have been detected.

The POR_SLEEP flag, if asserted, indicates that a POR_SLEEP_N event has occurred or a software reset has been triggered. The POR_SLEEP_N event could be caused by a transition to the OFF state or if an oscillator stuck has been detected.

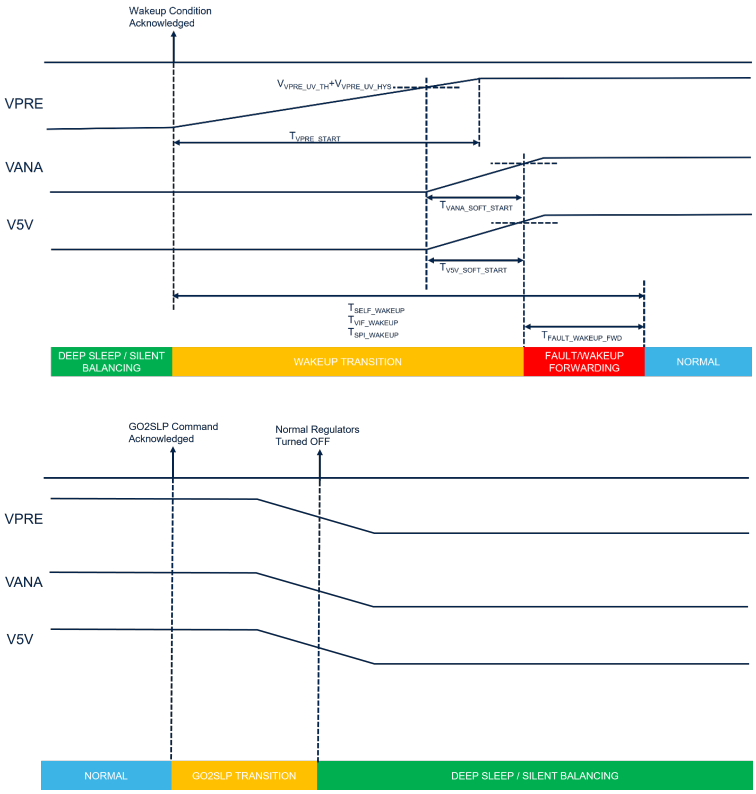
At the first power-up, both flags (POR_MAIN and POR_SLEEP) are asserted. Even if a SW_RST is sent, the default value will be restored.

5.1.1 Wake-up and GO2SLP sequences

Figure 6 illustrates the timing diagram for a wake-up sequence.

For each power-up time duration, please refer to the related paragraphs below.

Figure 6. Wake-up and GO2SLP timing diagrams



5.1.2 Electrical parameters

Table 7. Power up/down electrical parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{pwrup\_blanking}$	Power up masking applied to VPRE_UV, V5V_UV, VANA_UV flags starting at transition from low-power states (DEEP SLEEP/SILENT BALANCING) to NORMAL/CYCLIC WAKEUP	1.4	1.6	1.8	ms
$T_{sleep\_max\_delay}$	Maximum time required to turn off the device in case of GO2SLP command if no other wake-up frames are received			110	ms

Note: Conversion data is only reliable when the trimming and calibration data has been correctly downloaded from the NVM. Before launching the first conversion, it is recommended to verify that NVM_READY = 1 and no corruption has been detected.

5.2 Power supply

The L9965A/L99BM218 is equipped with a comprehensive set of power supply units for feeding both internal and external components.

The device includes 2 voltage references, 1 main reference, 1 auxiliary reference.

This implementation guarantees an internal redundance, which is checked through the connection to regulators and regulator monitors. For this reason, linear regulators receive the main voltage reference as input, while the monitor receives the auxiliary reference. In this way, if one of the two references is out of range, there will be a direct impact on the regulator diagnostic result.

The VB pin represents the main supply:

- Feeds the buck pre-regulator (VPRE)
- Feeds all the internal low-power standby circuitry

When below V_{VB_WAKEUP}, it determines the IC POR.

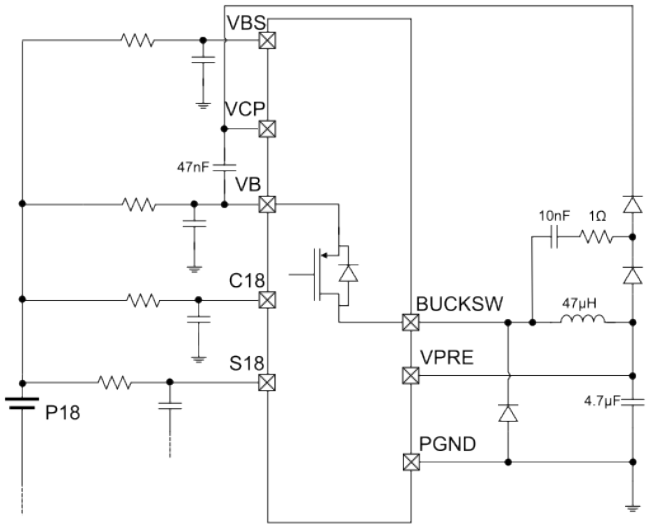
Table 8. Main supply electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Pin
V_{VB_WAKEUP}	Minimum battery voltage to enter DEEP SLEEP	5			V	VB

5.2.1 Buck regulator (VPRE)

The device includes a switching regulator (VPRE), implemented to optimize power dissipation.
Below is a schematic representation.

Figure 7. Buck regulator schematic



This buck pre-regulator:

- Is fed by the main supply (VB)
- Feeds the 5V LDO (V5V)
- Feeds the 5V analog LDO (VANA)
- Feeds the charge pump (VCP)

It regulates V_{VPRE} and guarantees I_{VPRE} output current capability to feed internal circuitries only.

To maximize efficiency, the regulated voltage is dynamically adapted to the VB voltage by means of an internal comparator on the VBS supply:

- If V_{VBS} rises above V_{VBS_HIGH}, the target voltage selector switches to V_{VPRE_HIGH} unless VCR is ongoing.
- If V_{VBS} falls below V_{VBS_HIGH} - $V_{VBS\_HIGH\_HYS}$, the target voltage selector switches to V_{VPRE_LOW} unless VCR is ongoing.

All electrical values are reported in Table 10 below.

5.2.1.1 Diagnostics

Table 9. Buck diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VPRE OV	$V_{VPRE} > V_{VPRE\_OV\_TH}$ for $t > T_{VPRE\_OV\_FIL}$	VPRE_OV flag is set	Clear on read if $V_{VPRE} < V_{VPRE\_OV\_TH} - V_{VPRE\_OV\_HYS}$ for $t > T_{VPRE\_OV\_FIL}$	None	None
VPRE UV	$V_{VPRE} < V_{VPRE\_UV\_TH}$ for $t > T_{VPRE\_UV\_FIL}$	VPRE_UV flag is set	Clear on read if $V_{VPRE} > V_{VPRE\_UV\_TH} + V_{VPRE\_UV\_HYS}$ for $t > T_{VPRE\_UV\_FIL}$	None	None

5.2.1.2 Electrical characteristics

Table 10. VPRE electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
V_{VBS_HIGH}	Input battery voltage for high regulated voltage	Tested in production	27	30	33	V	VBS
$V_{VBS\_HIGH\_HYS}$	Input battery voltage for high regulated voltage hysteresis	Tested in production	6.5	7	8.5	V	VBS
V_{VPRE_HIGH}	Regulated voltage	NORMAL, $V_{VBS} > V_{VBS\_HIGH}$, all loads	9.8		11	V	VPRE
V_{VPRE_LOW}	Regulated voltage	NORMAL, $V_{VBS} < V_{VBS\_HIGH} - V_{VBS\_HIGH\_HYS}$, all loads	7		8.3	V	VPRE
I_{VPRE_LOAD}	Current capability	Design info			70	mA	VPRE
R_{VPRE_HS}	HS resistance	Load=100mA		7	15	Ω	BUCKSW
I_{VPRE_OC}	Overcurrent threshold		190		300	mA	BUCKSW
f_{VPRE}	Switching frequency	Design info		500		kHz	BUCKSW
T_{VPRE_START}	Start timing	From enable to VPRE_UV=0, Guaranteed by design	150	300	500	µs	VPRE
$V_{VPRE\_OV\_TH}$	Buck overvoltage threshold	Tested in production	17		19	V	VPRE
$V_{VPRE\_UV\_TH}$	Buck undervoltage threshold	Tested in production	5.9		6.7	V	VPRE

5.2.2 Charge pump

The charge pump:

- feeds the internal analog circuitry for biasing cell balancing FETs (Sx) during NORMAL
- feeds the internal analog circuitry for biasing the stages executing the voltage conversion routine

The charge pump is only available for IC internal use and cannot be used to bias any external circuitry.

5.2.2.1 Diagnostics

The charge pump is designed to keep balancing stages OFF in case of tank capacitor loss. This diagnostic is available only in NORMAL and CYCLIC WAKEUP.

Table 11. Charge pump diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VCP UV	$V_{VCP} < V_{VCP\_UV\_TH}$ for $t > T_{VCP\_UV\_FIL}$	VCP_UV flag is set Cell balancing FETs (Sx) kept OFF	Clear on read if $V_{VCP} > V_{VCP\_UV\_TH}$ for $t > T_{VCP\_UV\_FIL}$	Cell balancing FETs (Sx) released	VCP_UV_BAL_MSK masks reaction on balancing

5.2.2.2 Electrical parameters

Table 12. Charge pump electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
$V_{VCP\_UV\_TH}$	VCP UV threshold	Tested in production	4.9		5.5	V	VCP
$T_{VCP\_UV\_FIL}$	VCP UV filter time	Tested by SCAN	10		20	us	VCP

5.2.3 5V LDO (V5V)

The V5V LDO:

- is fed by the buck pre-regulator (VPRE)
- feeds the Isolated Vertical Interface (VIF)
- feeds all the output buffers of the GPIOs, SPI , SPI target and I2C
- is used for biasing external NTCs via pullup resistors

5.2.3.1 Diagnostics

V5V overvoltage diagnostic detects V5V pin voltage exceeding the $V_{V5V\_OV\_TH}$ threshold.

V5V undervoltage should be considered a critical failure. In case of soft short-to-ground, the IC will still be able to communicate, but frame corruption may occur. All the functions whose integrity cannot be guaranteed in this condition will be disabled. In case of hard short-to-ground, the communication timeout (COMM_TIM) will be asserted and the device will transition to a low-power state. If the short-to-ground is then removed, the MCU may perform a retry using the wake-up functions.

Table 13. V5V LDO diagnostics

Fault	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
$V5V_{UV}$	$V_{V5V} < V_{V5V\_UV\_TH}$ for $t > T_{V5V\_UV\_OV\_FIL}$	V5V_UV flag is set. The Isolated Vertical Interface (VIF) is disabled	Clear on read if $V_{V5V} > V_{V5V\_UV\_TH} + V_{V5V\_UV\_HYS}$ for $t > T_{V5V\_UV\_OV\_FIL}$ The Isolated Vertical Interface (VIF) is automatically re-enabled.	None	None
$V5V_{OV}$	$V_{V5V} > V_{V5V\_OV\_TH}$ for $t > T_{V5V\_UV\_OV\_FIL}$	The V5V_OV flag is set	Clear on read if $V_{V5V} < V_{V5V\_OV\_TH} - V_{V5V\_OV\_HYS}$ for $t > T_{V5V\_UV\_OV\_FIL}$	None	None

5.2.3.2 Electrical Parameters

Table 14. V5V LDO Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
V_{V5V}	Regulated voltage	All operating lines and loads	-2%	5	+2%	V	V5V
I_{V5V_EXT}	Current budget for external applications	Application info			10	mA	V5V
$dV_{V5V\_LOAD\_REG}$	Transient load regulation	Load step from minimum operating current to I_{V5V_LIMmin}, di/dt = 3mA/µs, all lines, guaranteed by design	-5		+5	%	V5V
$T_{V5V\_SOFT\_START}$	Soft start timing	From 10% to 90% of V_{V5V}, guaranteed by design	100	200	300	µs	V5V
$PSRR_{V5V}$	Power supply rejection ratio	V_{NOISE} = 100mV_{pp} on V_{VPRE}, $f_{NOISE} = f_{VPREmin}$, guaranteed by design	40			dB	V5V
$V_{V5V\_UV\_TH}$	V5V undervoltage threshold	Tested in production	4.2		4.6	V	V5V
$V_{V5V\_OV\_TH}$	V5V overvoltage threshold	Tested in production	5.25		5.9	V	V5V
$T_{V5V\_UV\_OV\_FIL}$	UV/OV filter time	Tested by SCAN	10		20	us	V5V

5.2.4 5V analog LDO (VANA)

The VANA LDO:

- is fed by the buck pre-regulator (VPRE)
- is used for biasing the internal analog circuitry

5.2.4.1 *Diagnostics*

Table 15. VANA LDO diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VANA UV	$V_{VANA} < V_{VANA\_UV\_TH}$ for $t > T_{VANA\_UV\_FIL}$	VANA_UV flag is set	Clear on read if $V_{VANA} > V_{VANA\_UV\_TH} + V_{VANA\_UV\_HYS}$ for $t > T_{VANA\_UV\_FIL}$	None	None
VANA OV	$V_{VANA} > V_{VANA\_OV\_TH}$ for $t > T_{VANA\_OV\_FIL}$	VANA_OV flag is set	Clear on read if $V_{VANA} < V_{VANA\_OV\_TH} - V_{VANA\_OV\_HYS}$ for $t > T_{VANA\_OV\_FIL}$	None	None

5.2.4.2 *Electrical parameters*

Table 16. VANA LDO electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
V_{VANA}	Regulated voltage	All operating lines and loads	-3%	5	+3%	V	VANA
$T_{VANA\_SOFT\_START}$	Soft start timing	From 10% to 90% of V_{VANA}, guaranteed by design	100	200	300	µs	VANA
$PSRR_{VANA}$	Power supply rejection ratio	V_{NOISE} = 1mV_{pp} on VPRE $f_{NOISE} = f_{VPREmin}$, guaranteed by design	40			dB	VANA
$V_{VANA\_UV\_TH}$	VANA undervoltage threshold	Tested in production	4.2		4.6	V	VANA
$T_{VANA\_UV\_FIL}$	VANA undervoltage filter time	Tested by SCAN	10		20	µs	VANA
$V_{VANA\_OV\_TH}$	VANA overvoltage threshold	Tested in production	5.25		5.9	V	VANA
$T_{VANA\_OV\_FIL}$	VANA overvoltage filter time	Tested by SCAN	10		20	µs	VANA

5.3 Oscillators

This section describes the device oscillators.

5.3.1 Low frequency standby oscillator (OSCI_STBY)

The low frequency standby oscillator operates at f_{STBY_OSC}.

5.3.2 Electrical parameters

Table 17. Standby oscillator electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{STBY_OSC}	Oscillator frequency	Tested in production	-8%	500	+8%	kHz

5.3.3 High frequency main oscillator (OSCI_MAIN)

The high frequency main oscillator operates at f_{MAIN_OSC} and is active in NORMAL/CYCLIC WAKEUP state.

Outside the oscillator's frequency operating range, the power-up and down transitions and related timing may be affected. A frequency drift can be detected by the oscillator monitor as described in the dedicated section.

5.3.3.1 Electrical parameters

Table 18. Main oscillator electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{MAIN_OSC}	Oscillator frequency	Tested in production	-6%	16	+6%	MHz

5.3.4 Oscillator monitor

When in NORMAL or CYCLIC WAKEUP, the main and standby oscillators are monitoring each other. In case of failure, the OSCI_FAIL flag is set.

In case either of the two oscillators is stuck, the POR_SLEEP_N and POR_MAIN_N are asserted. So, all device configurations will be restored to their default value and the POR_SLEEP and POR_MAIN flags will be set. The MCU may attempt a retry performing the wake-up sequence. The oscillator stuck fault will be detected within $T_{OSCI\_STUCK\_TIMEOUT}$ time.

The oscillator monitor is BISTed at each wake-up from low-power states to NORMAL. In case of failure, the CLK_MON_SELFTEST_FAIL is set (cleared upon read).

5.3.4.1 Electrical parameters

Table 19. Oscillator monitor electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$f_{OSC\_MON\_ERR}$	Oscillator delta frequency threshold	Tested by SCAN	25		36	%
$T_{OSCI\_STUCK\_TIMEOUT}$	Oscillator stuck detection timeout	Tested by SCAN		2		ms

5.4 GND loss

To detect failures in grounding, the IC integrates a ground loss monitor. This diagnostic is always enabled.

5.4.1 Diagnostics

Table 20. Ground loss monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
DGND LOSS	If a differential voltage greater than $V_{GND\_LOSS\_TH}$ arises between AGND and DGND for an interval longer than $T_{GND\_LOSS\_FIL}$ before a transition to NORMAL state (due to an unconnected pin), the GND_LOSS_DGND fault is acknowledged	The POR_MAIN is asserted Device moves to the previously held low-power state (either DEEP SLEEP or SILENT BALANCING)	The MCU may trigger a wake-up to retry If the differential voltage between AGND and DGND falls below $V_{GND\_LOSS\_TH}$ for an interval longer than $T_{GND\_LOSS\_FIL}$, the POR_MAIN is released Once in NORMAL, POR_MAIN latch can be always cleared by the MCU	None	None
PGND LOSS	If a differential voltage greater than $V_{GND\_LOSS\_TH}$ arises between AGND and PGND for an interval longer than $T_{GND\_LOSS\_FIL}$, the GND_LOSS_PGND fault is acknowledged	The GND_LOSS_PGND flag is set	If the differential voltage between AGND and PGND falls below $V_{GND\_LOSS\_TH}$ for an interval longer than $T_{GND\_LOSS\_FIL}$, the GND_LOSS_PGND can be cleared by the MCU	None	This diagnostic is only active during WAKEUP phase between POR_MAIN de-assertion and VPRE enable and is masked during NORMAL and CYCLIC WAKEUP
AGND LOSS	If a differential voltage greater than $V_{GND\_LOSS\_TH}$ arises between AGND and DGND for an interval longer than $T_{GND\_LOSS\_FIL}$, the GND_LOSS_AGND fault is acknowledged	The POR_MAIN is asserted Device moves to the previously held low-power state (either DEEP SLEEP or SILENT BALANCING)	The MCU may trigger a wake-up to retry If the differential voltage between AGND and DGND falls below $V_{GND\_LOSS\_TH}$ for an interval longer than $T_{GND\_LOSS\_FIL}$, the POR_MAIN is released Once in NORMAL, POR_MAIN latch can be always cleared by the MCU	None	None This diagnostic is only active in NORMAL and CYCLIC WAKEUP

5.4.2 Electrical parameters

Table 21. Ground loss monitor characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
$V_{GND\_LOSS\_TH}$	Ground loss detection threshold	Tested in production	240		470	mV	AGND, DGND, PGND
$T_{GND\_LOSS\_FIL}$	Ground loss detection filter time	Tested by SCAN		300		µs	AGND, DGND
$T_{PGND\_LOSS\_FIL}$	PGND ground loss detection filter time	Tested by SCAN		38		µs	PGND

5.5 Voltage conversion routine

While in NORMAL state, the L9965A/L99BM218 monitors the cells and battery pack voltage with independent ADCs (one ADC per cell, plus one ADC dedicated to busbar and one to the VBS pin).

The ADCs have been designed to guarantee ultra-accurate measurements in the [-40°C ; +85°C] ambient temperature range, to support distributed BMS architectures where the BMIC board is installed close to the battery modules.

Very accurate measurements are also available in the [+85°C ; +105°C] range in order to support integration of the BMS board in the traction inverter module. In this case, the heat generated by the inverter may bring the ECU internal temperature up to +105°C.

In the upper operating range [+105°C;+125°C], the ADC guarantees safe detection of dangerous events such as OV/UV/OT/UT.

Task execution is triggered on-demand by programming SOC = 1. A conversion trigger and individual steps can be enabled/disabled by programming the corresponding bit with a single communication frame:

- VOLT_CONV = 1 enables:
  - Cell voltage monitor (Cx)
  - Busbar measurement channel (BBx)
  - Battery stack voltage measurement (VBS)

The T_{VOLT_FILTER} acquisition window (programmable via TVOLT_FIL) is applied to each sample. Longer acquisition windows will result in a more robust filter ($F_{CUT\_VOLT\_FILTER}$ cutoff frequency).

- VOLT_OPEN = 1 enables the cell AFE open load diagnostic (VOLT_OPEN).
- TEMP_CONV = 1 enables the GPIO conversion.
  - RATIO_CONV = 1 enables the cell temperature monitor (GPIOx).
  - ABS_CONV = 1 enables the GPIO absolute conversion.
  - This allows managing the NTC conversion and other external conversion threads independently.
- TEMP_OPEN = 1 enables the GPIO open load diagnostic (GPIOx_OPEN).
  - RATIO_CONV = 1 enables the cell temperature monitor (GPIOx).
  - ABS_CONV = 1 enables the GPIO absolute conversion.
  - This allows managing the NTC conversion and other external conversion threads independently.
- BIST = 1 enables the Built-In Self-Test (BIST).
  - BIST_FAULT_INJ !=00 enables the fault injection.
- GAIN_ADJ = 1 enables the gain adjustment (GAIN_ADJ). It is recommended to perform this step periodically while in NORMAL (every 100 ms max) in order to guarantee the best accuracy performance.
- ADC_SWAP = 1 enables the ADC swapping (ADC_SWAP).

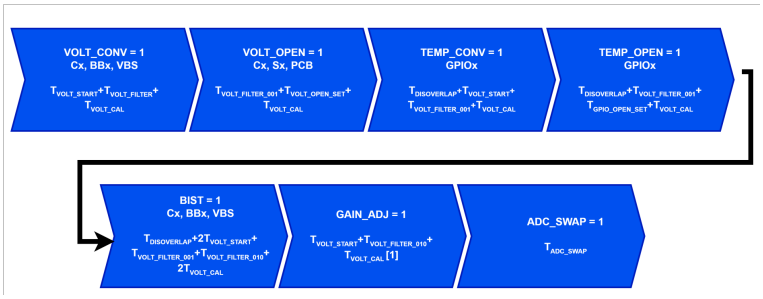
Any ongoing conversion cannot be interrupted and any asynchronous trigger event will be discarded. The status of the routine is reported by the VCR_BUSY flag: when set, the routine is ongoing. In case a routine step does not end within $T_{VOLT\_TIMEOUT}$, the VCR_FAIL latch is set (cleared upon read).

When the device operates in Wakeup By Cyclic Wakeup, the routine is executed once before going to sleep. All steps are executed except gain adjustment (GAIN_ADJ) and BIST fault injection (BIST_FAULT_INJ). Moreover, the TVOLT_FIL_WAKEUP applies to the VOLT_CONV step.

When the device operates in NORMAL state, GAIN_ADJ step is automatically performed during the first SOC request, in order to guarantee ADC precision from the second conversion. Every time the GAIN_ADJ step is executed, the voltage conversion routine duration increases by a time equivalent to $2T_{VOLT\_FILTER\_010}$.

Note: Conversion data is only reliable when the trimming and calibration data has been correctly downloaded from the NVM. Before launching the first conversion, it is recommended to verify that NVM_READY = 1 and no corruption has been detected.

Figure 8. Voltage Conversion Routine



[1] In case GAIN_ADJ = 1 and BIST = 0, the **gain adjustment (GAIN_ADJ)** step duration will be $2T_{VOLT\_FILTER\_010}$.

5.5.1 Cell voltage monitor (Cx)

During the cell voltage monitoring step, the voltage conversion routine measures differential voltages at the Cx pins and stores results in the VCELL<x>_MEAS registers, along with the corresponding DATA_READY<x> bit. This latch is set upon the generation of a new measurement result in NORMAL state only, and it is cleared upon read.

A cell is converted only if its corresponding VCELL<x>_EN bit is enabled. By default, all cells are disabled.

5.5.1.1 Connecting the busbar to a CCx channel

Using the busbar measurement channel (BBx) to handle busbar connection represents the most cost-effective solution for BMS designers. However, there might be some application scenarios where more than one busbar needs to be managed by a single BMIC.

The BB channel cannot be used to measure a busbar connected at the bottom-most of the stack. In this case, the C0-C1 pair shall be used. The BB channel supports the sensing of the busbar at the topmost of the stack (above VB).

Every cell measurement channel can be used for busbar sensing and can be connected using the recommended circuit as in Figure 9.

The PCB needs to be modified. One cell balancing line must be disconnected to avoid any current in the body drain diode of the balancing FET, as shown in Figure 9. In case no PCB_Assembly modifications are requested, consider the schematic in Figure 10.

When a cell is used for measuring a busbar, the corresponding VCELL<x>_BB bit shall be set accordingly in order to allow proper diagnostic masking:

- Regarding the digital sum of cells
  - A cell used as a busbar is not added to the digital sum of cells for checking sum UV/OV conditions.
  - A cell used as a busbar is added to the digital sum of cells when performing the plausibility check between VBS and the sum of cells. This digital sum of cells is stored in the VCELL_SUM_MEAS register, encoded in 17 bit with a resolution of $V_{CELL\_SUM\_RES}$.
- UV/OV and BAL_UV diagnostics are not performed on busbar cells.

Figure 9. **Connecting the busbar to a Cx channel**

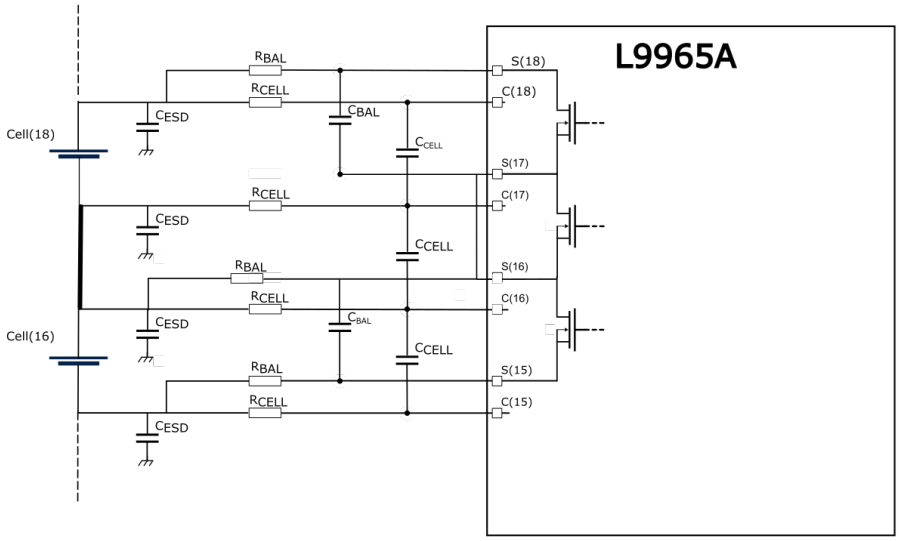
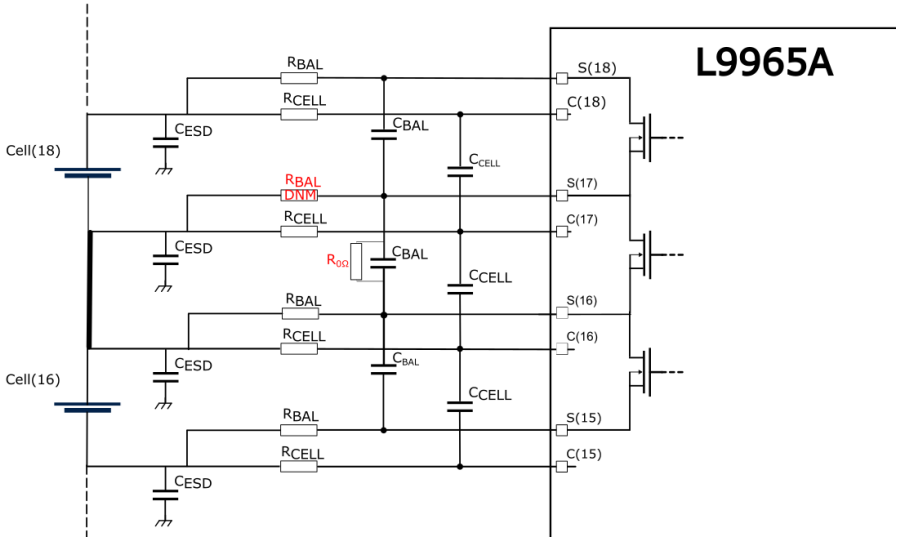


Figure 10. **Connecting the busbar to a Cx_no PCB assembly modifications**



Without doing any PCB assembly modifications, on the positive terminal of the busbar R_{bal} should be set as “DNM”. To perform balancing on the cell above the busbar, the MCU shall enable the switches on both busbar and cell. Moreover, if instead of C_{bal} an $R_{0\Omega}$ with the same footprint as C_{bal} is mounted as in Figure 10, the balancing can be done by enabling the MOSFET just on the desired cell.

5.5.1.2 *Diagnostics*

The IC features a comprehensive set of diagnostics based on cell voltage acquisition. Each diagnostic has been designed to address specific application cases and shall always be validated in conjunction with other safety mechanisms covering failures in the external analog front-end or internal conversion path.

- ***Cell UV*** should be considered as a critical failure, where the cell voltage has dropped below a safety threshold indicating a severe overdischarge condition. In this case, the battery should be disconnected to prevent copper deposition and it is not qualified for a recharge cycle. In a healthy cell exhibiting good impedance, this threshold should never be crossed even if a high discharge current is present.

- ***Cell OV*** should be considered as a critical failure, where the cell voltage has risen above a safety threshold indicating a severe overcharge condition. In this case, the battery should be disconnected to prevent thermal runaway and a fire/explosion hazard. The system should react by performing an emergency discharge on the affected cell. Until then, the battery is not qualified for a recharge cycle. In a healthy cell exhibiting good impedance, this threshold should never be crossed even if a high charge current is present.
- ***Cell balancing UV*** should be considered as a functional guard for balancing purposes. Its main purpose is to act as a target OCV in SILENT BALANCING. When the BMS equalizes the State of Charge (SoC) between cells based on Open Circuit Voltage (OCV) measurements, the balancing UV threshold can be assigned to define the target SoC for a specific cell. This allows automatic detection of the end of balancing, without the need for MCU supervision. The IC also allows setting up timer thresholds in order to prevent cell overdischarge.
- ***Sum UV*** should be considered as a critical failure, where the pack voltage has dropped below a safety threshold indicating a severe overdischarge condition. This fault usually occurs when more than one cell experiences ***Cell UV***. In this case, the battery should be disconnected to prevent copper deposition and it is not qualified for a recharge cycle. In a healthy battery exhibiting good impedance, this threshold should never be crossed even if a high discharge current is present.
- ***Sum OV*** should be considered as a critical failure, where the pack voltage has risen above a safety threshold indicating a severe overcharge condition. This fault usually occurs when more than one cell experiences ***Cell OV***. In this case, the battery should be disconnected to prevent thermal runaway and a fire/explosion hazard. The system should react by performing an emergency discharge on all the affected cells. Until that, the battery is not qualified for a recharge cycle. In a healthy battery exhibiting good impedance, this threshold should never be crossed even if a high charge current is present.
- ***Cell DELTA in CYCLIC WAKEUP*** should be considered as a critical failure, where cell voltage undergoes a rapid and abnormal variation in time, incompatible with cell relaxation time constants. Detection of such a variation while the system is in rest state (BMS operates in CYCLIC WAKEUP mode) possibly indicates the inception of thermal runaway. In this case, the battery should be disconnected through pyro-fuse and/or mechanical relays, and the driver and surrounding people should be immediately alerted about the concrete risk of fire/explosion. It is recommended to program a CYCLIC WAKEUP check at least every 2 minutes. If the system goes to CYCLIC WAKEUP while balancing is active on a specific Cell_x, Cell Delta_x detection may occur on Cell_x, and the adjacent ones at the end of the balancing, due to the voltage drop on the harness cables. In this case, the MCU has to clear the fault and run a voltage conversion routine to check if the system is still in a safe state.
- ***Cell DELTA in NORMAL*** should be considered as a warning for all SoC estimation algorithms. Advanced algorithms based on Kalman filters could select only a few cells (for instance, 3 cells out of 18) and NTCs (for instance, 1 out of 4) where the filter is applied, thus decreasing the MCU computational effort. Such an approach assumes that other cell voltages and temperatures are consistent with the three selected samples. As an advantage, this allows for a dramatic decrease in the amount of data traveling on the Isolated Vertical Interface (VIF), as the MCU only needs to download a few cells'/NTCs' data at each conversion and readout tick time. Hence, power consumption and energy efficiency also increase. However, this requires the BMIC to monitor all the cell voltages and temperature for consistency. Voltage consistency check is achieved thanks to the *Cell DELTA in NORMAL* diagnostic.

Table 22. Cell voltage monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell UV	If the $V_{Cx} – V_{Cx-1}$ voltage falls below $V_{CELL\_UV\_TH}$, the CELL<x>_UV fault is acknowledged.	CELL<x>_UV flag is set Balancing is frozen on the affected cell	If the $V_{Cx} – V_{Cx-1}$ voltage rises above $V_{CELL\_UV\_TH}$, the CELL<x>_UV fault can be cleared by the MCU If a SW_RST is sent, the CELL<x>_UV fault can be cleared by the MCU (after VIF_ID re-programming) or by sending a second SW_RST	Balancing is resumed on the affected cell (unless the MCU has disabled it)	VCELL<x>_EN and VCELL<x>_BB mask diagnostic execution. When a cell is disabled or configured as a busbar, the CELL<x>_UV flag can always be cleared CELL_UV_BAL_MSK masks reaction on balancing FETs

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell OV	If the $V_{Cx} – V_{Cx-1}$ voltage rises above $V_{CELL\_OV\_TH}$, the CELL<x>_OV fault is acknowledged.	CELL<x>_OV flag is set	If the $V_{Cx} – V_{Cx-1}$ voltage falls below $V_{CELL\_OV\_TH}$, the CELL<x>_OV fault can be cleared by the MCU If a SW_RST is sent, the CELL<x>_OV fault can be cleared by the MCU (after VIF_ID re-programming) or by sending a second SW_RST	None	VCELL<x>_EN and VCELL<x>_BB mask diagnostic execution. When a cell is disabled or configured as a busbar, the CELL<x>_OV flag can always be cleared
Cell balancing UV	If the $V_{Cx} – V_{Cx-1}$ voltage falls below $V_{BAL\_UV\_TH}$, the CELL<x>_BAL_UV fault is acknowledged.	CELL<x>_BAL_UV flag is set Balancing is frozen on the affected cell	If the $V_{Cx} – V_{Cx-1}$ voltage rises above $V_{BAL\_UV\_TH}$, the CELL<x>_BAL_UV fault can be cleared by the MCU If a SW_RST is sent, the CELL<x>_BAL_UV fault can be cleared by the MCU (after VIF_ID re-programming) or by sending a second SW_RST	Balancing is resumed on the affected cell (unless the MCU has disabled it)	VCELL<x>_EN and VCELL<x>_BB mask diagnostic execution. When a cell is disabled or configured as a busbar, the CELL<x>_BAL_UV flag can always be cleared BAL_UV_BAL_MSK masks reaction on balancing FETs
Sum UV	If the sum of cells voltage falls below $V_{SUM\_UV\_TH}$, the SUM_UV fault is acknowledged.	SUM_UV flag is set Balancing is frozen on all cells	If the sum of cells voltage rises above $V_{SUM\_UV\_TH}$, the SUM_UV fault can be cleared by the MCU If a SW_RST is sent, the SUM_UV fault can be cleared by the MCU (after VIF_ID re-programming) or by sending a second SW_RST	Balancing is resumed on all cells (unless the MCU has disabled it)	VCELL<x>_EN and VCELL<x>_BB mask diagnostic execution. A cell disabled or used as a busbar is not added to the digital sum. If all cells are disabled or configured as busbar, the SUM_UV flag can always be cleared SUM_UV_BAL_MSK masks reaction on balancing FETs
Sum OV	If the sum of cells voltage rises above $V_{SUM\_OV\_TH}$, the SUM_OV fault is acknowledged.	SUM_OV flag is set	If the sum of cells voltage falls below $V_{SUM\_OV\_TH}$, the SUM_OV fault can be cleared by the MCU If a SW_RST is sent, the SUM_OV fault can be cleared by the MCU (after VIF_ID re-programming) or by sending a second SW_RST	None	VCELL<x>_EN and VCELL<x>_BB mask diagnostic execution. A cell disabled or used as a busbar is not added to the digital sum. If all cells are disabled or configured as busbar, the SUM_UV flag can always be cleared
Cell DELTA in CYCLIC WAKEUP	When in CYCLIC WAKEUP operation, if $\lvert V_{Cx} – V_{Cx-1}\rvert$ voltage undergoes a variation in time higher than ΔV_{Cx_TH} in 2 consecutive samples stored during cells voltage monitoring step in CYCLIC WAKEUP mode the CELL<x>_DELTA fault is acknowledged	CELL<x>_DELTA flag is set The BMIC stays in NORMAL and sends a FAULT wake-up message	CELL<x>_DELTA flag can always be cleared on read or by sending a SW_RST	None	VCELL<x>_EN and VCELL<x>_BB mask diagnostic execution. The CELL<x>_DELTA flag of a masked cell can always be cleared ΔV_{Cx_TH}=0 masks diagnostic execution This diagnostic is only available in CYCLIC WAKEUP
Cell DELTA in NORMAL	When in NORMAL, if $(V_{Cx} – V_{Cx-1}) – V_{Cxmin}$ is higher than ΔV_{Cx_TH}, the VCELL_DELTA_NORMAL fault is acknowledged	VCELL_DELTA_NORMAL flag is set	When in NORMAL, if $V_{Cx} – V_{Cxmin}$ is lower or equal to ΔV_{Cx_TH}, the VCELL_DELTA_NORMAL flag can be cleared by the MCU	None	VCELL<x>_EN and VCELL<x>_BB mask diagnostic execution. ΔV_{Cx_TH}=0 masks diagnostic execution This diagnostic is only available in NORMAL

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
	Note: *V_{Cxmin} represents the minimum differential cell voltage converted at each execution of the Cell voltage monitor (Cx)* *V_{Cxmin} = min(V_{Cx} – V_{Cx-1}), x=1…18*		If a SW_RST is sent, the VCELL_DELTA_NORMAL fault can be cleared by the MCU (after VIF_ID re-programming) or by sending a second SW_RST		

5.5.1.3 Electrical parameters

Table 23. Cell voltage monitor electrical parameters.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
T_{VOLT_START}	ADC settling time	Guaranteed by SCAN		60		µs	Cx, GPIOx
$T_{DISOVERLAP}$	Analog MUX disoverlap time, applied whenever the MUX switches the input pair	Guaranteed by SCAN	0		35	µs	Cx, GPIOx
T_{VOLT_CAL}	ADC post-calibration time, applied after every conversion	Guaranteed by SCAN			70	µs	Cx, GPIOx
$T_{VOLT\_TIMEOUT}$	Routine step timeout	Guaranteed by SCAN	110	130	150	ms	
T_{ADC_SWAP}	ADC swap time			16		µs	
V_{CELL_RANGE}	Cell voltage input measurement range	Design info	-1		5.5	V	Cx
V_{CELL_RES}	Cell voltage measurement resolution	Design info, effective range [-6.6;6.6]V		201.4		µV	Cx
N_{BIT_CELL}	ADC bit number	Design info		16		bit	Cx
$V_{CELL\_SUM\_RES}$	Cell sum voltage measurement resolution, $V_{CELL\_SUM\_RES} = 16V_{CELL\_RES}$	Design info		3.2224		mV	Cx
$I_{CELL\_LEAK\_105C}$	Cx pins absolute leakage current (low)	$T_J \leq +105°C$			100	nA	Cx
$I_{CELL\_LEAK\_140C}$	Cx pins absolute leakage current (high)	$T_J \leq +140°C$			300	nA	Cx
$R_{CELL\_DIFF\_IN}$	Cell differential input impedance between adjacent Cx pins	V_{CELL} =5.5V, current to be considered is I(C+) – I(C-)	10			MΩ	Cx
$V_{CELL\_OFFSET\_ERR\_0}$	ADC offset, including post-soldering and aging effects (1)	V_{CELL} = 0V, pins shorted on PCB, guaranteed by test bench characterization, $-40°C \leq T_J \leq +125°C$	-1		1	LSB	Cx
$V_{CELL\_OFFSET\_ERR\_1}$	ADC offset, including post-soldering and aging effects (1)	V_{CELL} = 0V, pins shorted on PCB, guaranteed by test bench characterization, $125°C \leq T_J \leq +140°C$	-2		2	LSB	Cx

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
$V_{CELL\_TOTAL\_ERR0\_85}$	ADC Total conversion error, including post-soldering and aging effects (1)	-1 < V_{CELL} < 2V, -40°C ≤ T_J ≤ +105°C	-0.9		0.9	mV	Cx
$V_{CELL\_TOTAL\_ERR1\_85}$	ADC Total conversion error, including post-soldering and aging effects (1)	2V < V_{CELL} < 3.4V, -40°C ≤ T_J ≤ +105°C	-1.4		1.4	mV	Cx
$V_{CELL\_TOTAL\_ERR2\_85}$	ADC Total conversion error, including post-soldering and aging effects (1)	3.4 < V_{CELL} < 4.5V, -40°C ≤ T_J ≤ +105°C	-1.8		1.8	mV	Cx
$V_{CELL\_TOTAL\_ERR3\_85}$	ADC Total conversion error, including post-soldering and aging effects (1)	4.5 < V_{CELL} < 5.5V, -40°C ≤ T_J ≤ +105°C	-2.2		2.2	mV	Cx
$V_{CELL\_TOTAL\_ERR0\_105}$	ADC Total conversion error, including post-soldering and aging effects (1)	-1 < V_{CELL} < 2V, +105°C ≤ T_J ≤ +125°C	-1		1	mV	Cx
$V_{CELL\_TOTAL\_ERR1\_105}$	ADC Total conversion error, including post-soldering and aging effects (1)	2V < V_{CELL} < 3.4V, +105°C ≤ T_J ≤ +125°C	-1.7		1.7	mV	Cx
$V_{CELL\_TOTAL\_ERR2\_105}$	ADC Total conversion error, including post-soldering and aging effects (1)	3.4 < V_{CELL} < 4.5V, +105°C ≤ T_J ≤ +125°C	-2.1		2.1	mV	Cx
$V_{CELL\_TOTAL\_ERR3\_105}$	ADC Total conversion error, including post-soldering and aging effects (1)	4.5 < V_{CELL} < 5.5V, +105°C ≤ T_J ≤ +125°C	-2.6		2.6	mV	Cx
$V_{CELL\_TOTAL\_ERR0\_125}$	ADC Total conversion error, including post-soldering and aging effects (1)	-1 < V_{CELL} < 2V, +125°C ≤ T_J ≤ +140°C	-2.3		2.3	mV	Cx
$V_{CELL\_TOTAL\_ERR1\_125}$	ADC Total conversion error, including post-soldering and aging effects (1)	2V < V_{CELL} < 3.4V, +125°C ≤ T_J ≤ +140°C	-3.5		3.5	mV	Cx
$V_{CELL\_TOTAL\_ERR2\_125}$	ADC Total conversion error, including post-soldering and aging effects (1)	3.4 < V_{CELL} < 4.5V, +125°C ≤ T_J ≤ +140°C	-4.7		4.7	mV	Cx
$V_{CELL\_TOTAL\_ERR3\_125}$	ADC total conversion error, including post-soldering and aging effects (1)	4.5 < V_{CELL} < 5.5V, +125°C ≤ T_J ≤ +140°C	-5.6		5.6	mV	Cx
$T_{VOLT\_FILTER\_000}$	Voltage ADC filter time	TVOLT_FIL = 000, TVOLT_FIL_WAKEUP = 000		136		µs	Cx
$T_{VOLT\_FILTER\_001}$	Voltage ADC filter time	TVOLT_FIL = 001, TVOLT_FIL_WAKEUP = 001		264		µs	Cx
$T_{VOLT\_FILTER\_010}$	Voltage ADC filter time	TVOLT_FIL = 010, TVOLT_FIL_WAKEUP = 010’		1.040		ms	Cx
$T_{VOLT\_FILTER\_011}$	Voltage ADC filter time	TVOLT_FIL = 011, TVOLT_FIL_WAKEUP = 011		2.080		ms	Cx
$T_{VOLT\_FILTER\_100}$	Voltage ADC filter time	TVOLT_FIL = 100, TVOLT_FIL_WAKEUP = 100		4.160		ms	Cx
$T_{VOLT\_FILTER\_101}$	Voltage ADC filter time	TVOLT_FIL = 101, TVOLT_FIL_WAKEUP = 101		8.320		ms	Cx
$T_{VOLT\_FILTER\_110}$	Voltage ADC filter time	TVOLT_FIL = 110, TVOLT_FIL_WAKEUP = 110		16.640		ms	Cx
$T_{VOLT\_FILTER\_111}$	Voltage ADC filter time	TVOLT_FIL = 111 TVOLT_FIL_WAKEUP = 111		99.864		ms	Cx
$F_{CUT\_VOLT\_FILTER\_000}$	Voltage ADC 3dB cutoff frequency	TVOLT_FIL = 000, TVOLT_FIL_WAKEUP = 000		3340		Hz	Cx
$F_{CUT\_VOLT\_FILTER\_001}$	Voltage ADC 3dB cutoff frequency	TVOLT_FIL = 001, TVOLT_FIL_WAKEUP = 001		1720		Hz	Cx

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
$F_{CUT\_VOLT\_FILTER\_010}$	Voltage ADC 3dB cutoff frequency	TVOLT_FIL = 010, TVOLT_FIL_WAKEUP = 010'		432		Hz	Cx
$F_{CUT\_VOLT\_FILTER\_011}$	Voltage ADC 3dB cutoff frequency	TVOLT_FIL = 011, TVOLT_FIL_WAKEUP = 011		213.4		Hz	Cx
$F_{CUT\_VOLT\_FILTER\_100}$	Voltage ADC 3dB cutoff frequency	TVOLT_FIL = 100, TVOLT_FIL_WAKEUP = 100		106.4		Hz	Cx
$F_{CUT\_VOLT\_FILTER\_101}$	Voltage ADC 3dB cutoff frequency	TVOLT_FIL = 101, TVOLT_FIL_WAKEUP = 101		53.2		Hz	Cx
$F_{CUT\_VOLT\_FILTER\_110}$	Voltage ADC 3dB cutoff frequency	TVOLT_FIL = 110, TVOLT_FIL_WAKEUP = 110		26.6		Hz	Cx
$F_{CUT\_VOLT\_FILTER\_111}$	Voltage ADC 3dB cutoff frequency	TVOLT_FIL = 111, TVOLT_FIL_WAKEUP = 111		4.4		Hz	Cx
$V_{CELL\_NOISE\_011}$	Standard deviation over a population of 100 samples	TVOLT_FIL = 011, TVOLT_FIL_WAKEUP = 100		110		uVrms	Cx
V_{CELL_REPEAT}	Voltage measurement repeatability, | V_{CELL1} - V_{CELL0}|	Maximum difference between two consecutive samples taken over a rest time of 12h and a T_{amb} shift of 10°C (setpoint unvaried)., 2.5V < V_{CELL} < 5V, -40°C ≤ T_{amb} ≤ +85°C, TVOLT_FIL = 010 or bigger, V_{CELL0} taken at (t0;T_{amb0}), V_{CELL1} taken at (t0+12h;T_{amb0}+/-10°C), guaranteed by bench characterization	-900		+900	µV	Cx
$V_{CELL\_UV\_TH}$	Cell undervoltage threshold (9 bit), $V_{CELL_{UV_{TH}}} = 64V_{CELL\_RES} * CODE$	CELL_UV_TH, Tested by SCAN	0		6.6	V	Cx
$V_{CELL\_OV\_TH}$	Cell overvoltage threshold (9 bit), $V_{CELL_{OV_{TH}}} = V_{CELL_{UV_{TH}}} + 64V_{CELL\_RES} * CODE$	CELL_OV_TH, Tested by SCAN	0		13.2	V	Cx
$V_{BAL\_UV\_TH}$	Balance undervoltage threshold (9 bit), $V_{BAL_{UV_{TH}}} = V_{CELL_{UV_{TH}}} + 64V_{CELL\_RES} * CODE$	BAL_UV_TH, Tested by SCAN	0		6.6	V	Cx
$V_{SUM\_UV\_TH}$	Sum of cells undervoltage threshold (9 bit), $V_{SUM_{UV_{TH}}} = 2048V_{CELL\_RES} * CODE$	SUM_UV_TH, Tested by SCAN	0		210.77	V	Cx
$V_{SUM\_OV\_TH}$	Sum of cells overvoltage threshold (9 bit), $V_{SUM_{OV_{TH}}} = V_{SUM_{UV_{TH}}} + 512V_{CELL\_RES} * CODE$	SUM_OV_TH, Tested by SCAN	0		263.46	V	Cx
$\Delta V_{Cx\_TH\_0}$	Programmable cell variation threshold (4 bit), DELTA_VCX_TH	CYCLIC WAKEUP, absolute check of dV_{Cx}/dt, $\Delta V_{CX_{TH}} = 8V_{CELL\_RES}$ [(2)] $* CODE$	9.668		24.170	mV	Cx
$\Delta V_{Cx\_TH\_1}$		NORMAL, relative check of V_{Cx}-V_{Cxmin}, $\Delta V_{CX_{TH}} = 256V_{CELL\_RES} * CODE$	0		0.773376	V	Cx

1. *Single shot samples are characterized by superimposed gaussian noise, with zero-mean and V_{CELL_NOISE} standard deviation.*
2. *Min configurable CODE is 6.*

5.5.2 Busbar measurement channel (BBx)

Besides the possibility to connect a busbar between any Cx channel pair, the IC offers a dedicated busbar measurement channel.

During the cell voltage monitoring step, the voltage conversion routine measures differential voltages at the BBx pins and stores the results in the BB_MEAS register along with the corresponding DATA_READY bit. This latch is set upon the generation of a new measurement result in NORMAL state only and it is cleared upon read.

Regarding the digital sum of cells:

- The busbar is not added to the digital sum of cells for checking sum UV/OV conditions.
- Depending on the BB_ADD bit, the busbar may be added to the digital sum of cells (VCELL_SUM_MEAS) for the plausibility check between VBS and sum of cells.
  - In case the busbar is placed within the stack (as shown in Figure 11), it is recommended to set BB_ADD = 0 in order to avoid counting the busbar voltage twice. In fact, busbar contribution is already accounted for in the cell voltage measurement.
  - In case the busbar is placed above the stack (that is, above C18), it is recommended to set BB_ADD = 1 in order to account for such a voltage drop when comparing to VBS.

The busbar is converted only if the BB_EN bit is enabled. By default, the busbar channel is disabled.

5.5.2.1 *Connecting the busbar to the BBx channel*

Depending on the application scenario, the busbar can be randomly placed in series with any cell of the stack:

- Figure 11 shows an application scenario where the busbar is placed in the middle of the stack (it applies to any cell between C1 and C18).
  - In this case, one Cell voltage monitor (Cx) channel measures the voltage on the series connection of a cell plus the busbar
  - The Busbar measurement channel (BBx) acquires the busbar voltage synchronously to the Cell voltage monitor (Cx) channel, since it shares the same ADC filtering window. This avoids any error introduced by desynchronization, allowing the MCU to compensate for the IR drop over the busbar via SW, thus extracting precise cell voltage measurement.
- Figure 12 shows an application scenario where the busbar is placed above the stack, between two consecutive BMICs.
  - In this case, there is no need for SW to compensate any cell voltage measurement by subtracting the busbar voltage

The BBx pins have been positioned before the cell sensing pins Cx in order to allow for flexibility while routing them to any possible busbar location within the stack.

Figure 11. Busbar placed in the middle of the stack

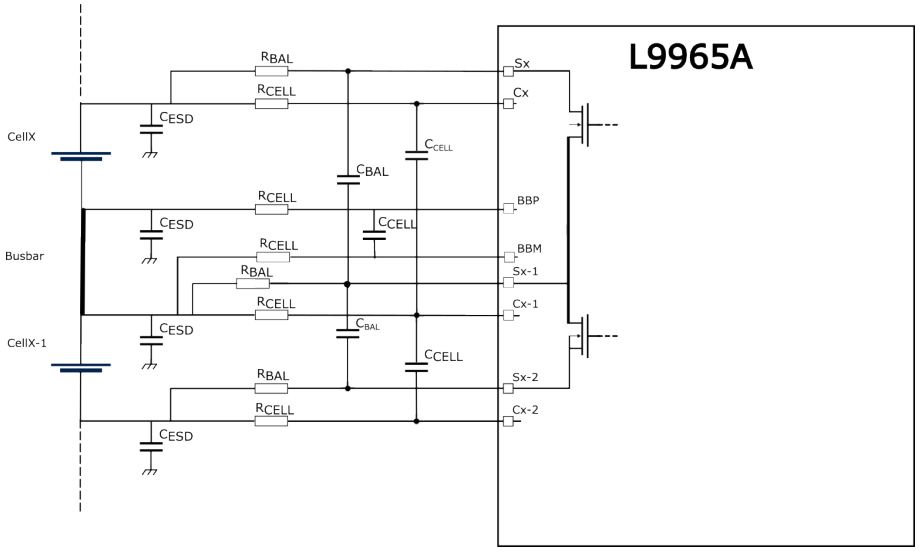
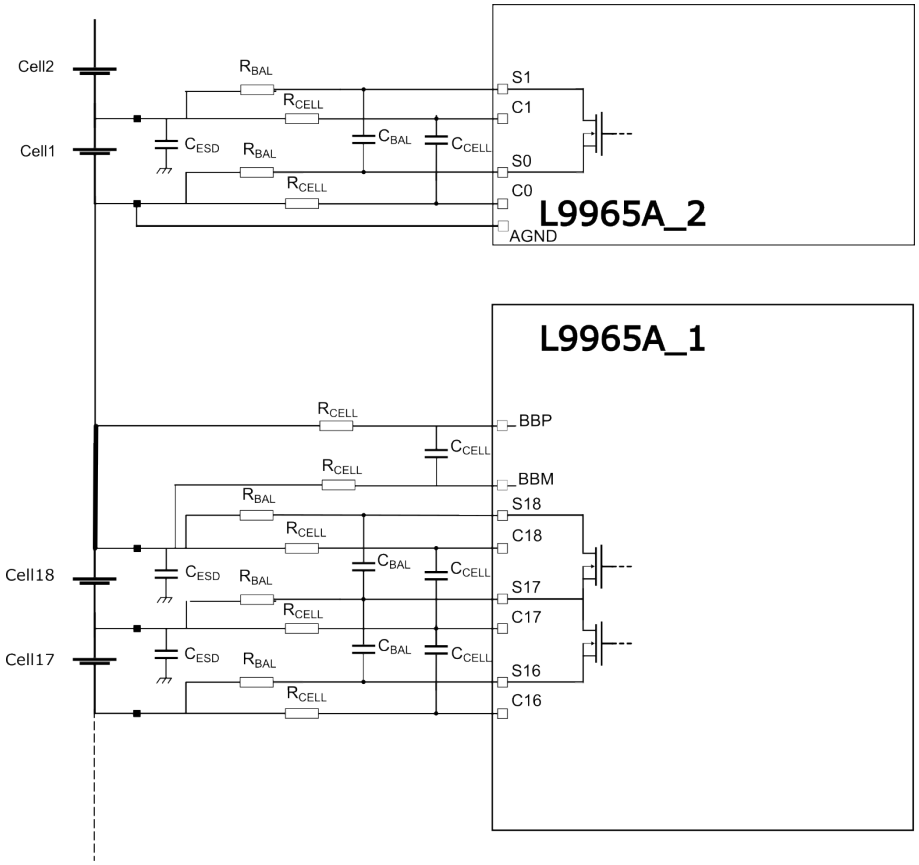


Figure 12. **Busbar placed between two BMICs**



5.5.2.2 *Diagnostics*

The IC features a comprehensive set of diagnostics based on busbar voltage acquisition. Each diagnostic has been designed to address specific application cases and shall always be validated in conjunction with other safety mechanisms covering failures in the external analog front end or internal conversion path.

BB OV should be considered as a warning, where a voltage drop over the busbar metal rises above a certain guard threshold. In a healthy system where the busbar exhibits low resistance, this threshold should never be crossed, even if a high charge/discharge current is present. In this case, the MCU shall evaluate the simultaneous presence of overcurrent/short-circuit failures detected by the L9965C companion chip. If BB OV is detected without overcurrent/short-circuit being present, this indicates a possible degradation of the busbar resistivity, which may lead to a need for urgent vehicle maintenance. Instead, if a BB OV is detected during overload conditions, this may be seen as a normal system response to a transient failure.

Table 24. **Busbar monitor diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
BB OV	If the |BBP – BBM| voltage rises above $V_{BB\_OV\_TH}$, the BB_OV fault is acknowledged.	The BB_OV flag is set	The BB_OV field can always be cleared on read or by sending an SW_RST	None	BB_EN masks diagnostic execution. When disabled, the BB_OV flag can always be cleared

5.5.2.3 *Electrical parameters*

Table 25. Busbar monitor electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
V_{BB_RANGE}	Busbar voltage input measurement Range	Design info	-1		1	V	BBx
V_{BB_RES}	Busbar voltage measurement Resolution	Design info, effective range [-6.6;6.6]V		201.4		uV	BBx
$I_{BB\_LEAK\_105C}$	BBx pins absolute leakage current (low)	$T_J \leq +105°C$			100	nA	BBx
$I_{BB\_LEAK\_140C}$	BBx pins absolute leakage current (high)	$T_J \leq +140°C$			300	nA	BBx
$R_{BB\_DIFF\_IN}$	Differential input impedance	Guaranteed by design	10			MΩ	BBx
$V_{BB\_OFFSET\_ERR\_0}$	ADC offset, including post-soldering and aging effects (1)	V_{BBP}-V_{BBM} = 0V, pins shorted on PCB, guaranteed by test bench characterization, $-40°C \leq T_J \leq +125°C$	-1		1	LSB	BBx
$V_{BB\_OFFSET\_ERR\_1}$		V_{BBP}-V_{BBM} = 0V, pins shorted on PCB, guaranteed by test bench characterization, $T_J \leq +140°C$	-2		2	LSB	BBx
$V_{BB\_TOTAL\_ERR0\_85}$	ADC total conversion error Including post-soldering and aging effects(1)	$-1V < V_{BBP}$-$V_{BBM} < 1V$, $-40°C \leq T_J \leq +105°C$	-0.6		0.6	mV	BBx
$V_{BB\_TOTAL\_ERR0\_105}$	ADC total conversion error Including post-soldering and aging effects(1)	$-1V < V_{BBP}$-$V_{BBM} < 1V$, $+105°C \leq T_J \leq +125°C$	-0.7		0.7	mV	BBx
$V_{BB\_TOTAL\_ERR0\_125}$	ADC Total conversion error Including post-soldering and aging effects(1)	$-1V < V_{BBP}$-$V_{BBM} < 1V$, $+105°C \leq T_J \leq +140°C$	-2.6		2.6	mV	BBx
$V_{BBNOISE\_100}$	Standard deviation over a 100 sample distribution	TVOLT_FIL = 100, TVOLT_FIL_WAKEUP = 100			100	uVrms	BBx
$V_{BB\_OV\_TH}$	Busbar overvoltage threshold (7 bit), $V_{BB_{OV_{TH}}} = 128V_{BB\_RES} * CODE$	BB_OV_TH, Tested by SCAN	0		3.27	V	BBx

1. *Single shot samples are characterized by superimposed gaussian noise, with zero-mean and VBB_NOISE standard deviation.*

5.5.3 Battery stack voltage measurement (VBS)

The BMIC also performs battery stack voltage sensing via a dedicated VBS input. This pin shall be connected to the topmost stack potential, including busbar drop in case the Busbar measurement channel (BBx) is connected above C18.

Results are stored in the VBS_MEAS register and can be compared by the MCU to the digital sum of cells in order to perform plausibility checks. The result is stored along with the corresponding DATA_READY bit. This latch is set upon the generation of a new measurement result in NORMAL state only and it is cleared upon read.

The R_{VBS_IN} pull-down is only enabled while the IC is in NORMAL/CYCLIC WAKEUP. It is however disabled in other operating states.

This monitor can be enabled by setting the VBS_EN bit.

5.5.3.1 *Diagnostics*

The IC features a comprehensive set of diagnostics based on direct battery stack voltage acquisition. Each diagnostic has been designed to address specific application cases and shall always be validated in conjunction with other safety mechanisms covering failures in the external analog front-end or internal conversion path.

- ***Stack OV*** should be considered as a warning corresponding to a situation where voltage over the entire pack raises above a certain guard threshold. In a healthy system where all the cells and the busbar exhibit low impedance, this threshold should never be crossed even if a high charge current is present. In this case, the MCU shall evaluate the simultaneous presence of overcurrent failure detected by the L9965C companion chip. If a Stack OV is detected without overcurrent being present, this indicates a possible degradation of cell or busbar impedance, which may lead to a need for urgent vehicle maintenance. Instead, if a Stack OV is detected during overload conditions, this may be seen as a normal system response to a transient failure.
- ***Stack UV*** should be considered as a warning corresponding to a situation where the voltage over the entire pack falls below a certain guard threshold. In a healthy system where all the cells and the busbar exhibit low impedance, this threshold should never be crossed even if a high discharge current is present. In this case, the MCU shall evaluate the simultaneous presence of overcurrent/short-circuit failures detected by the L9965C companion chip. If a Stack UV is detected without overcurrent/short-circuit being present, this indicates a possible degradation of cells or busbar impedance, which may lead to a need for urgent vehicle maintenance. Instead, if a Stack UV is detected during overload conditions, this may be seen as a normal system response to a transient failure.
- ***Plausibility vs. Sum Of Cells*** should be considered as a warning corresponding to a situation where there is a consistent mismatch between the digital sum of cells and the stack direct measurement. In a healthy system where the analog front end is well connected to the cells and all the ADCs are working properly, this threshold should never be crossed. In this case, the MCU should evaluate the integrity of the analog front end connection by running the **Cell AFE Open Load Diagnostic (VOLT_OPEN)** and should also verify the functionality of all the ADCs running the **Built-In Self-Test (BIST)**.

Table 26. VBS monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Stack OV	If the VBS voltage rises above $V_{VBS\_OV\_TH}$, the VBS_OV fault is acknowledged	The VBS_OV flag is set	If the VBS voltage falls below $V_{VBS\_OV\_TH}$, the VBS_OV fault can be cleared by the MCU If a SW_RST is sent, the VBS_OV fault can be cleared by MCU (after VIF_ID re-programming) or with a second SW_RST	None	VBS_EN masks diagnostic execution. When disabled, the VBS_OV flag can always be cleared
Stack UV	If the VBS voltage falls below $V_{VBS\_UV\_TH}$, the VBS_UV fault is acknowledged	The VBS_UV flag is set Balancing is frozen on all cells	If the VBS voltage rises above $V_{VBS\_UV\_TH}$, the VBS_UV fault can be cleared by the MCU If a SW_RST is sent, the VBS_UV fault can be cleared by the MCU (after VIF_ID re-programming) or with a second SW_RST	Balancing is resumed on the affected cell (unless the MCU has disabled it)	VBS_EN masks diagnostic execution. When disabled, the VBS_OV flag can always be cleared VBS_UV_BAL_MSK masks reaction on balancing FETs
Plausibility vs. Sum of Cells	If the |VBS_MEAS - VCELL_SUM_MEAS| difference is greater than $V_{VBS\_SUM\_TH}$, the VBS_SUM_FAIL fault is acknowledged	The VBS_SUM_FAIL flag is set	If the |VBS_MEAS - VCELL_SUM_MEAS| difference is smaller than $V_{VBS\_SUM\_TH}$, the VBS_SUM_FAIL fault can be cleared by MCU If a SW_RST is sent, the VBS_SUM_FAIL fault can be cleared by MCU (after VIF_ID re-programming) or with a second SW_RST	None	VBS_EN masks diagnostic execution. When disabled, the VBS_SUM_FAIL flag can always be cleared

5.5.3.2 *Electrical parameters*

Table 27. Battery stack monitor electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit.	Pin
V_{BATT_RANGE}	VBS input measurement range	Application info	11		90	V	VBS
V_{BATT_RES}	VBS measurement resolution	Design info, effective range [-108.9:108.9]V		3.323		mV	VBS
N_{BIT_BATT}	ADC bit number	Design info		16		bit	VBS
R_{VBS_IN}	VBS input impedance	Guaranteed by design	1			MΩ	VBS
$V_{BATTERR0\_85}$	VBS total conversion error, average over 100 samples, including post-soldering and aging effects	VBS in V_{BATT_RANGE}, -40°C ≤ T_J ≤ +105°C	-0.1		0.1	%	VBS
$V_{BATTERR0\_105}$	VBS total conversion error, average over 100 samples, including post-soldering and aging effects	VBS in V_{BATT_RANGE}, +105°C ≤ T_J ≤ +125°C	-0.2		0.2	%	VBS
$V_{BATTERR0\_125}$	VBS total conversion error, average over 100 samples, including post-soldering and aging effects	VBS in V_{BATT_RANGE}, +105°C ≤ T_J ≤ +140°C	-1		1	%	VBS
$V_{VBS\_UV\_TH}$	Stack undervoltage threshold (8 bit), $V_{VBS_{UV_{TH}}} = 128V_{BATT_{RES}} * CODE$	VBS_UV_TH, Tested by SCAN	0		108.9	V	VBS
$V_{VBS\_OV\_TH}$	Stack overvoltage threshold (8 bit), $V_{VBS_{OV_{TH}}} = V_{VBS_{UV_{TH}}} + 128V_{BATT_{RES}} * CODE$	VBS_OV_TH, Tested by SCAN	0		217.8	V	VBS
$V_{VBS\_SUM\_TH}$	Threshold for the maximum mismatch between VBS and sum of cells (4 bit), $V_{VBS_{SUM_{TH}}} = 32V_{BATT_{RES}} * CODE$	VBS_SUM_TH, Tested by SCAN	0		1.595	V	VBS

5.5.4 Cell AFE open load diagnostic (VOLT_OPEN)

This diagnostic allows the detection of open load failures on cell sense lines (Cx), cell balancing lines (Sx) and cell harness connected to the PCB. When triggered, the following diagnostic routine is executed in parallel on all cell analog front-end pins.

- *The diagnostic currents are enabled on the Cx pins and Sx pins*
  - *I_{CELL_DIAG} pull-down current is enabled on C_X pins ranging from 2 to 18 and the I_{BAL_DIAG} pull-down current is enabled on the corresponding S_X pins ranging from 2 to 18.*
  - *The $I_{CELL\_DIAG\_FIRST}$ pull-up current is enabled on C0 and, if VCELL1_BB = 0, the $I_{BAL\_DIAG\_FIRST}$ pull-up current is enabled on S0, otherwise no pull-up current is enabled on S0.*
  - *If VCELL1_BB = 0, the I_{CELL_DIAG} pull-down current is enabled on C1, otherwise the $I_{CELL\_DIAG\_FIRST}$ pull-up current is enabled on C1. If VCELL1_BB = 0, the I_{BAL_DIAG} pull-down current is enabled on S1, otherwise the $I_{BAL\_DIAG\_FIRST}$ pull-up current is enabled on S1.*
- *The BMIC waits for $T_{VOLT\_OPEN\_SET}$ settling time*
- *The BMIC performs a conversion of the cell voltage at the C_X pins and of the busbar voltage at the BBx pins using the $T_{VOLT\_FILTER\_001}$ window and unmasks the balancing open comparator at S_X pins. Diagnostic information is processed as summarized in Table 28.*

The VBS channel features an internal resistive pull-down that will discharge the VBS node to ground in case of open failure. Such a failure will result in plausibility check fail vs. sum of cells (refer to Battery stack voltage measurement (VBS)).

5.5.4.1 Diagnostics

Table 28. Cell AFE open load diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell Open	The $V_{Cx} – V_{Cx-1}$ voltage falls below $V_{Cx\_OPEN\_TH}$ The $V_{Sx} – V_{Sx-1}$ voltage is above $V_{Sx\_OPEN\_TH}$	AFE_DIAG<x> code is set to ‘01’	The diagnostic step is re-executed launching SOC = 1 with VOLT_OPEN = 1, and the diagnostic ends with no failure. Then AFE_DIAG<x>=00 is automatically reported by the routine, and the GSW fault bit is cleared	None	VCELL<x>_EN masks diagnostic execution. VCELL<x>_BB masks diagnostic execution.
Busbar Open	The $\|V_{BBP} – V_{BBM}\|$ absolute voltage rises above $V_{BBx\_OPEN\_TH}$	BB_OPEN flag is set	The diagnostic step is re-executed launching SOC = 1 with VOLT_OPEN = 1, and the diagnostic ends with no failure. Then BB_OPEN = 0 is automatically reported by the routine, and the GSW fault bit is cleared	None	BB_EN masks diagnostic execution.
Balancing Open	The $V_{Cx} – V_{Cx-1}$ voltage is above $V_{Cx\_OPEN\_TH}$ The $V_{Sx} – V_{Sx-1}$ voltage falls below $V_{Sx\_OPEN\_TH}$	AFE_DIAG<x> code is set to ‘10’	The diagnostic step is re-executed launching SOC = 1 with VOLT_OPEN = 1, and the diagnostic ends with no failure. Then AFE_DIAG<x>=00 is automatically reported by the routine, and the GSW fault bit is cleared	None	VCELL<x>_EN masks diagnostic execution. VCELL<x>_BB masks diagnostic execution.
PCB Open	The $V_{Cx} – V_{Cx-1}$ voltage falls below $V_{Cx\_OPEN\_TH}$ The $V_{Sx} – V_{Sx-1}$ voltage falls below $V_{Sx\_OPEN\_TH}$	AFE_DIAG<x> code is set to ‘11’	The diagnostic step is re-executed launching SOC = 1 with VOLT_OPEN = 1, and the diagnostic ends with no failure. Then AFE_DIAG<x>=00 is automatically reported by the routine, and the GSW fault bit is cleared	None	VCELL<x>_EN masks diagnostic execution. VCELL<x>_BB masks diagnostic execution.
S0/S1 Open	The V_{Sx} voltage rises above $V_{SFIRST\_OPEN\_TH}$ Note: x = 0 if VCELL1_BB = 0, or 1 if VCELL1_BB = 1	SFIRST_OPEN flag is set	The diagnostic step is re-executed launching SOC = 1 with VOLT_OPEN = 1, and the diagnostic ends with no failure. Then, SFIRST_OPEN is automatically written to 0 and the GSW fault bit is cleared	None	Nonmaskable

5.5.4.2 *Electrical parameters*

Table 29. Cell AFE open load electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
I_{CELL_DIAG}	Cell open load diagnostic PD current	$VC_X \geq 1.4V$	1	1.5	2	mA	C1 to C18, BBM, BBP
I_{BAL_DIAG}	Balancing open load diagnostic PD current	$VS_X \geq 1.4V$	200	300	400	µA	S1 to S18
$I_{CELL\_DIAG\_FIRST}$	Cell open load diagnostic PU current applied to the negative pin of the first connected channel	$VC_X \leq 1.4V$	-2	-1.5	-1	mA	C0-C1
$I_{BAL\_DIAG\_FIRST}$	Balancing open load diagnostic PU current applied to the negative pin of the first connected channel	$VS_X \leq 1.4V$	-400	-300	-200	µA	S0-S1
$T_{VOLT\_OPEN\_SET}$	Open load check settling time	Tested by SCAN		2		ms	Sx
$V_{Cx\_OPEN\_TH}$	Cell open load threshold (4 bit), $V_{COPEN_{TH}} = 2048 V_{CELL_{RES}} * CODE$	CX_OPEN_TH, Tested by SCAN	0		6.187	V	Sx
$V_{BBx\_OPEN\_TH}$	Busbar open load threshold, |BBP – BBM|	Tested by SCAN		1.7		V	Sx
$V_{Sx\_OPEN\_TH}$	Balancing open load threshold, differential comparator between S_X and S_{X-1}, x=1,18	Tested in production	0.4		0.8	V	S1 to S18
$V_{SFIRST\_OPEN\_TH}$	Balancing open load threshold, comparator between S_X and AGND	Tested in production	0.4		0.8	V	S0,S1
$T_{Sx\_OPEN\_FIL}$	Balancing open load comparator filter time	Tested by SCAN		20		µs	Sx
$T_{C0\_OPEN\_FIL}$	C0 open load comparator filter time	Tested by SCAN		20		µs	Sx

5.5.5 GPIO conversion

GPIO conversion can be done in abs or ratio configuration.

Each GPIO channel conversion (abs or ratio) is performed by cell ADCs through internal multiplexing.

GPIO conversion implies that the corresponding cell ADC must be enabled by the VCELL<X>_EN bit. By default, all cell ADCs are disabled. The table below shows ADC cell / GPIO correspondence.

Table 30. GPIO conversion

GPIO	CORRESPONDING CELL ADC, SWAP_ECHO = 0	CORRESPONDING CELL ADC, SWAP_ECHO = 1
GPIO 0	ADC 2	ADC 1
GPIO 1	ADC 4	ADC 3
GPIO 2	ADC 6	ADC 5
GPIO 3	ADC 8	ADC 7
GPIO 4	ADC 10	ADC 9
GPIO 5	ADC 12	ADC 11
GPIO 6	ADC 14	ADC 13
GPIO 7	ADC 16	ADC 15
GPIO 8	ADC 18	ADC 17
GPIO 9	ADC VBS	ADC VBS

5.5.5.1 *Cell temperature monitor (GPIOx)*

The NTC voltage conversion step monitors external temperature sensors connected to the GPIOs. For best performance, it is recommended:

- to supply NTCs using 5V LDO (V5V)
- to configure corresponding GPIOs for ratio-metric measurement (see **GPIOs** chapter)

NTC measurements are stored in the corresponding NTC_GPIO_MEAS_<x> registers along with the corresponding DATA_READY<x> bit. This latch is set upon the generation of a new measurement result in NORMAL state only and it is cleared upon read.

5.5.5.1.1 Diagnostics

The IC features a comprehensive set of diagnostics based on cell temperature acquisition. Each diagnostic has been designed to address specific application cases, and shall always be validated in conjunction with other safety mechanisms covering failures in the external analog front end or internal conversion path.

- ***NTC OT*** should be considered as a critical failure when sensing a cell temperature. It occurs when cell temperature rises above a safety threshold indicating a severe risk of thermal runaway. In this case, the battery should be disconnected from the load to prevent further thermal stress. The battery is not qualified for a discharge/recharge cycle until cell temperature returns within safety limits determined by user SW. In a healthy cell, this threshold should never be crossed even if a high charge/discharge current is present. If an OT event is detected without an overload condition being present, this might indicate a severe cell impedance degradation, which may be an irreversible condition leading to permanent pack disqualification. An OT event when an overload condition is present may however be a temporary and recoverable condition. An NTC OT condition on NTCs used for monitoring the balancing resistor temperature should instead be seen as a warning, which is automatically handled by the IC by means of balancing automatic cooldown feature.
- ***NTC Fast Charge OT*** should be considered as a warning when sensing a cell temperature. It occurs when cell temperature rises above a warning threshold indicating overheating due to huge charge currents. In this case, the system should lower the charge current in order to provide thermal relief. The battery is still qualified for recharge but fast charging should be disabled until cell temperature returns within safety limits determined by user SW. In a healthy system, this threshold might be crossed if a high external ambient temperature and high charge currents are present.
- ***NTC UT*** should be considered as a critical failure when sensing a cell temperature. It occurs when cell temperature falls below a safety threshold indicating the impossibility of delivering the power required by loads in normal operation. When in this condition, the cell impedance may dramatically increase. In this case, the battery should be disconnected from the load to prevent further thermal stress. The battery is not qualified for a discharge/recharge cycle until cell temperature returns within safety limits determined by user SW. In a healthy system, this threshold should never be crossed even in low external ambient temperatures. The battery should be pre-heated before starting operation.
- ***NTC DELTA in Cyclic Wakeup*** should be considered as a critical failure, where cell temperature undergoes a rapid and abnormal variation in time, incompatible with normal evolution of ambient temperature. Detection of such a variation while the system is in rest state (BMS operates in CYCLIC WAKEUP mode) possibly indicates the inception of thermal runaway. In this case, the battery should be disconnected through pyro-fuse and/or mechanical relays, and the driver and surrounding people should immediately be alerted about the concrete risk of fire/explosion. It is recommended to program a CYCLIC WAKEUP check at least every 2 minutes.
- ***NTC DELTA in NORMAL*** should be considered as a warning for all SoC estimation algorithms. Advanced algorithms based on Kalman filters could select just a few cells (for instance, 3 cells out of 18) and NTCs (for instance, 1 out of 4) where the filter is applied, thus decreasing the MCU's computational effort. Such an approach assumes that other cell voltages and temperatures are consistent with the selected samples. As an advantage, this allows dramatically decreasing the amount of data traveling on the Isolated Vertical Interface (VIF), as the MCU only needs to download a few cells'/NTCs' data at each conversion and readout tick time. Therefore, power consumption and energy efficiency also increases. However, this requires the BMIC to monitor all the cell voltages and temperature for consistency. The temperature consistency check is achieved thanks to the ***NTC DELTA in NORMAL*** diagnostic.

Table 31. Cell temperature monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
NTC OT	If the $GPIO_X$ voltage falls below $V_{NTCx\_OT\_TH}$, the NTC_OT_GPIO_UV_x fault is acknowledged	NTC_OT_GPIO_UV_x flag is set Balancing is frozen on all cells	For channels configured as balancing cooldown (BAL_COOLDOWN_EN<x> = 1), if $GPIO_X$ voltage rises above $V_{NTCx\_OT\_TH}$ + $V_{NTC\_OT\_HYS}$, the NTC_OT_GPIO_UV_x flag can be cleared by MCU For channels configured as cell NTCs (BAL_COOLDOWN_EN<x> = 0), if $GPIO_X$ voltage rises above $V_{NTCx\_OT\_TH}$, the NTC_OT_GPIO_UV_x flag can be cleared by MCU If a SW_RST is sent, the NTC_OT_GPIO_UV_x fault can be cleared by the MCU (after VIF_ID re-programming) or with a second SW_RST	For channels configured as balancing cooldown (BAL_COOLDOWN_EN<x> = 1), the balancing is automatically re-engaged if the release condition is verified, even without NTC_OT_GPIO_UV_x flag clear For channels configured as cell NTCs (BAL_COOLDOWN_EN<x> = 0), the balancing is re-engaged only when NTC_OT_GPIO_UV_x flag is cleared	GPIO<x>_CONF different than 00/01 masks measurement execution. The NTC_OT_GPIO_UV_x flag of a disabled NTC can always be cleared SPI_MODE equal to 00 or 11 masks measurement execution for NTC<0>, NTC<1>(depending on GPIO1_NCS1_EN), NTC<2>, NTC<3>, NTC<4> I2C_EN, when enabled, masks measurement execution for NTC<5> and NTC<6> NTC<x>_OT_BAL_MSK masks reaction on balancing pin
NTC Fast Charge OT	If the $GPIO_X$ voltage falls below $V_{NTCx\_FASTCHG\_OT\_TH}$, the NTC_FASTCHG_OT_GPIO_WARN_UV_x fault is acknowledged	NTC_FASTCHG_OT_GPIO_WARN_UV_x flag is set	If $GPIO_X$ voltage rises above $V_{NTCx\_FASTCHG\_OT\_TH}$ the NTC_FASTCHG_OT_GPIO_WARN_UV_x flag can be cleared by the MCU If a SW_RST is sent, the NTC<x>_FASTCHG_OT fault can be cleared by the MCU (after VIF_ID re-programming) or with a second SW_RST	None	GPIO<x>_CONF different than 00/01 masks measurement execution. The NTC_OT_GPIO_UV_x flag of a disabled NTC can always be cleared SPI_MODE equal to 00 or 11 masks measurement execution for NTC<0>, NTC<1>(depending on GPIO1_NCS1_EN), NTC<2>, NTC<3>, NTC<4> I2C_EN, when enabled, masks measurement execution for NTC<5> and NTC<6>
NTC UT	If the $GPIO_X$ voltage rises above $V_{NTCx\_UT\_TH}$, the NTC_UT_GPIO_OV_x fault is acknowledged	NTC_UT_GPIO_OV_x flag is set	If $GPIO_X$ voltage rises above $V_{NTCx\_UT\_TH}$, the NTC_UT_GPIO_OV_x flag can be cleared by the MCU	None	GPIO<x>_CONF different than 00/01 masks measurement execution. The NTC_UT_GPIO_OV_x flag of a disabled NTC can always be cleared

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
			If a SW_RST is sent, theNTC_UT_GPIO_OV_x fault can be cleared by the MCU (after VIF_ID re-programming) or with a second SW_RST		SPI_MODE equal to 00 or 11 masks measurement execution for NTC<0>, NTC<1>(depending on GPIO1_NCS1_EN), NTC<2>, NTC<3>, NTC<4> I2C_EN, when enabled, masks measurement execution for NTC<5> and NTC<6>
NTC DELTA in Cyclic Wakeup	When in Cyclic Wakeup operation, if $\lvert V_{GPIOx} \rvert$ voltage undergoes a variation in time higher than ΔV_{NTC_TH} in 2 consecutive samples, the NTC_DELTA_GPIO_DELTA_<x> fault is acknowledged	NTC_DELTA_GPIO_DELTA_<x> flag is set The BMIC stays in NORMAL and sends a FAULT wakeup message	NTC_DELTA_GPIO_DELTA_<x> flag can always be cleared by the MCU or by sending a SW_RST	None	GPIO<x>_CONF different than 00/01 masks measurement execution. The NTC_DELTA_GPIO_DELTA_<x> flag of a disabled NTC can always be cleared SPI_MODE equal to 00 or 11 masks measurement execution for NTC<0>, NTC<1>(depending on GPIO1_NCS1_EN), NTC<2>, NTC<3>, NTC<4> I2C_EN, when enabled, masks measurement execution for NTC<5> and NTC<6> NTC<x>_DELTA_MSK masks the execution of the diagnostic. The NTC_DELTA_GPIO_DELTA_<x> flag of a masked NTC can always be cleared ΔV_{NTC_TH}=0 masks diagnostic execution This diagnostic is available only in CYCLIC WAKEUP
NTC DELTA in NORMAL	When in NORMAL, if $V_{GPIOx} - V_{GPIOxmin}$ is higher than ΔV_{NTC_TH}, the NTC_DELTA_NORMAL fault is acknowledged *Note:*	NTC_DELTA_NORMAL flag is set	When in NORMAL, if $V_{GPIOx} - V_{GPIOxmin}$ is lower or equal to ΔV_{NTC_TH}, the NTC_DELTA_NORMAL flag can be cleared by the MCU	None	GPIO<x>_CONF different than 00/01 masks measurement execution. The NTC_DELTA_NORMAL flag of a disabled NTC can always be cleared

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
	$V_{GPIOxmin}$ *represents the minimum GPIO voltage converted at each execution of the GPIO conversion* $V_{GPIOxmin}$ = *min(V_{GPIOx}), x=0…9*		If a SW_RST is sent, the NTC_DELTA_NORMAL fault can be cleared by the MCU (after VIF_ID re-programming) or with a second SW_RST		SPI_MODE equal to 00 or 11 masks measurement execution for NTC<0>, NTC<1>(depending on GPIO1_NCS1_EN), NTC<2>, NTC<3>, NTC<4> I2C_EN, when enabled, masks measurement execution for NTC<5> and NTC<6> NTC<x>_DELTA_MSK masks the execution of the diagnostic. The NTC_DELTA_NORMAL flag of a masked NTC can always be cleared ΔV_{NTC_TH}=0 masks diagnostic This diagnostic is available only in NORMAL

5.5.5.1.2 Electrical parameters

Table 32. GPIO measurement electrical parameters (ratiometric)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
V_{NTC_RANGE}	NTC pin voltage input measurement range	Ratiometric, design info	0.2		V_{V5V}	V	GPIOx
V_{NTC_RES}	Cell voltage measurement resolution	Design info, effective range [1.32*V_{V5V}]		201.4		µV	GPIOx
N_{BIT_NTC}	ADC bit number	Design info		15		bit	GPIOx
$I_{NTC\_LEAK\_L}$	NTC leakage current (low)	$T_J \le +105°C$			100	nA	GPIOx
$I_{NTC\_LEAK\_H}$	NTC leakage current (high)	$T_J \le +140°C$			300	nA	GPIOx
$V_{NTC\_GAIN\_ERR0\_85}$	NTC gain error, including nonlinearities, including post-soldering and aging effects (1)	V_{NTC} in range, $-40°C \le T_J \le +105°C$	-0.2		0.2	%	GPIOx
$V_{NTC\_GAIN\_ERR0\_105}$	NTC Gain error, including nonlinearities, including post-soldering and aging effects(1)	V_{NTC} in range, $+105°C \le T_J \le +125°C$	-0.4		0.4	%	GPIOx
$V_{NTC\_GAIN\_ERR0\_125}$	NTC Gain error, including nonlinearities, including post-soldering and aging effects(1)	V_{NTC} in range, $+125°C \le T_J \le +140°C$	-0.6		0.6	%	GPIOx
$V_{NTC\_OFFSET\_ERR\_105}$	NTC offset error, including post-soldering and aging effects(1)	Tested in production, $-40°C \le T_J \le +125°C$	-1		1	LSB	GPIOx
$V_{NTC\_OFFSET\_ERR\_125}$	NTC offset error, including post-soldering and aging effects(1)	Tested in production, $+125°C \le T_J \le +140°C$	-2		2	LSB	GPIOx

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
V_{NTC_NOISE}	Standard deviation over a population of 100 samples	Guaranteed by characterization, -40°C ≤ T_J ≤ +140°C	-200		200	uVrms	GPIOx
$V_{NTC\_OT\_TH}$	Programmable NTC OT threshold (8 bit, one threshold for each channel), $V_{NTC_{OT_{TH}}} = 32V_{NTC\_RES} * CODE$	NTC<x>_OT_TH, tested by SCAN	0		0.33*V_{V5V}	V	GPIOx
$V_{NTC\_OT\_HYS}$	Programmable NTC OT threshold hysteresis (4 bit, steps of 128LSB), $V_{NTC_{OT_{HYS}}} = 128V_{NTC\_RES} * CODE$	NTC_TH_HYS, tested by SCAN	0		0.078* V_{V5V}	V	GPIOx
$V_{NTC\_FASTCHG\_OT\_TH}$	Programmable NTC fast charge OT threshold (5 bit, steps of 128LSB), $V_{NTC_{FASTCHG_{OTTH}}} = V_{NTC_{OT_{TH}}} + 128V_{NTC\_RES} * CODE$	NTC_FASTCHG_OT_TH, tested by SCAN	$V_{NTCOTTH}$		$V_{NTCOTTH}$+0.16*V_{V5V}	V	GPIOx
$V_{NTC\_UT\_TH}$	Programmable NTC UT threshold (8 bit, one threshold for each channel), $V = 128V_{NTC\_RES} * CODE$	NTC<x>_UT_TH, tested by SCAN	0		1.32*V_{V5V}	V	GPIOx
$\Delta V_{NTC\_TH\_0}$	Programmable NTC variation threshold (4 bit), DELTA_VNTC_TH, (CYCLIC WAKEUP)	CYCLIC WAKEUP, absolute check of dV_{GPIOx}/dt, steps of 128LSB corresponding to ~0.39% of 1.32*V_{V5V}, $\Delta V_{NTC_{TH}} = 128V_{NTC\_RES} * CODE$	0		0.078* V_{V5V}	V	GPIOx
$\Delta V_{NTC\_TH\_1}$	Programmable NTC variation threshold (4 bit), DELTA_VNTC_TH, (NORMAL)	NORMAL, relative check of V_{GPIOx}-$V_{GPIOxmin}$, steps of 128LSB corresponding to ~0.39% of 1.32*V_{V5V}, $\Delta V_{NTC_{TH}} = 128V_{NTC\_RES} * CODE$	0		0.078* V_{V5V}	V	GPIOx

1. *Single shot samples are characterized by superimposed gaussian noise, with zero-mean and VNTC_NOISE standard deviation.*

5.5.5.2 *GPIO absolute conversion (GPIOx)*

During the temperature conversion step, the GPIOs can also be used to convert signals from sensors other than NTCs and not necessarily biased by 5V LDO (V5V).

To do so, GPIOs shall be configured for absolute measurement (see **GPIOs** chapter).

Thresholds, diagnostic flags, and measurement results are shared with GPIO conversion. Specifically, in such a case, to prevent misbehavior of the DELTA diagnostics, GPIOs configured as absolute input shall also be programmed with the corresponding NTC<x>_DELTA_MSK =1.

5.5.5.2.1 Electrical parameters

Table 33. GPIO measurement electrical parameters (absolute)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
V_{GPIO_RANGE}	GPIO pin voltage input measurement range	Design info,	0		5	V	GPIOx
V_{GPIO_RES}	GPIO measurement resolution	Design info, effective range [-6.6;6.6]V		201.4		µV	GPIOx
N_{BIT_GPIO}	ADC bit number	Design info		15		bit	GPIOx
$V_{GPIO\_TOTAL\_ERR0\_105}$	ADC total conversion error, including post-soldering and aging effects (1)	0 < V_{GPIO} < 5V, -40°C ≤ T_J ≤ +125°C	-2.6		2.6	mV	GPIOx
$V_{GPIO\_TOTAL\_ERR0\_125}$	ADC total conversion error, including post-soldering and aging effects(1)	0 < V_{GPIO} < 5V, T_J ≤ +140°C	-5.6		5.6	mV	GPIOx
V_{GPIO_NOISE}	Standard deviation over a population of 100 samples		-200		200	uVrms	GPIOx
$V_{GPIO\_UV\_TH}$	Programmable GPIO UV threshold (8 bit, one threshold for each channel), $V_{GPIO_{UV_{TH}}} = 128V_{GPIO\_RES} * CODE$	Tested by SCAN	0		6.6	V	GPIOx
$V_{GPIO\_WARN\_UV\_TH}$	Programmable GPIO WARNING UV threshold (5 bit, steps of 128LSB), $V_{GPIO_{WARN_{UV_{TH}}}} = V_{GPIO_{UV_{TH}}} + 128V_{GPIO\_RES} * CODE$	Tested by SCAN	0		6.6	V	GPIOx
$V_{GPIO\_UV\_HYS}$	Programmable GPIO UV hysteresis (4 bit), $V_{GPIO_{UV_{HYS}}} = 128V_{GPIO\_RES} * CODE$	Tested by SCAN	0		0.39	V	GPIOx
$V_{GPIO\_OV\_TH}$	Programmable GPIO OV threshold (8 bit, one threshold for each channel), $V_{GPIO_{OV_{TH}}} = 128V_{GPIO\_RES} * CODE$	Tested by SCAN	0		6.6	V	GPIOx
ΔV_{GPIO_TH}(2)	Programmable GPIO variation threshold for CYCLIC WAKEUP (4 bit), $\Delta V_{GPIO_{TH}} = 128V_{GPIO\_RES} * CODE$	Tested by SCAN	0		0.3867	V	GPIOx

1. *Single shot samples are characterized by superimposed gaussian noise, with zero-mean and VGPIO_NOISE standard deviation.*
2. *This diagnostic is never executed since it is masked with the NTC<x>_DELTA_MSK bit, which must be set to 1 for all GPIOs configured as absolute input.*

5.5.6 GPIO open load diagnostic (GPIOx_OPEN)

This diagnostic allows detection of open load failures on GPIOs (GPIOx). When triggered, the following diagnostic routine is executed in parallel on all GPIOs configured as analog inputs (GPIO<x>_CONF = 00/01):

1. *The I_{GPIO_DIAG} pull-down current is enabled on GPIOx pins*
2. *The BMIC waits for $T_{GPIO\_OPEN\_SET}$ settling time*
3. *The BMIC performs absolute conversion of the GPIOx pin (regardless of the GPIO<x>_CONF setting) and processes the information as indicated in Table 34 diagnostics.*

Table 34. GPIO open load diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
GPIO Open	If the $GPIO_X$ voltage falls below $V_{GPIO\_OPEN\_TH}$, the GPIO<x>_OPEN fault is acknowledged.	GPIO<x>_OPEN flag is set	The GPIO<x>_OPEN field can always be cleared on read or by sending a SW_RST	None	GPIO<x>_CONF different than 00/01 masks diagnostic execution. When not configured as analog inputs, the GPIO<x>_OPEN flag can always be cleared SPI_MODE equal to 00 or 11 masks measurement execution for GPIO<0>, GPIO<1>(depending on GPIO1_NCS1_EN), GPIO<2>, GPIO<3>, GPIO<4> I2C_EN, when enabled, masks measurement execution for GPIO<5> and GPIO<6>

5.5.6.1 *Electrical parameters*

Table 35. GPIO open load electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
I_{GPIO_DIAG}	GPIO open load diagnostic current	V_{GPIOx}≥1V	20	30	40	µA	GPIOx
$T_{GPIO\_OPEN\_SET}$	Open load check settling time	Tested by SCAN		0.7		ms	GPIOx
$V_{GPIO\_OPEN\_TH}$	GPIO open load threshold	Tested by SCAN		200		mV	GPIOx

5.5.7 Built-In Self-Test (BIST)

The BMIC allows testing the integrity of the ADCs and level shifters, from the Cx, VBS and BBx pins to the digital conversion block output. The routine is designed to validate the full ADC input characteristics using a two setpoints check, covering both offset and gain errors.

This diagnostic is executed in parallel on all enabled cell monitoring channels (VCELL<x>_EN = 1), the busbar measurement channel (BB_EN = 1) and the battery stack monitor (VBS_EN = 1).

The combination of Built-In Self-Test (BIST) and GPIO open load diagnostic (GPIOx_OPEN) also covers the integrity of the GPIOx conversion paths.

When the BIST step is enabled in the Voltage conversion routine, the following procedure is executed:

1. *The C_X-C_{X-1}, VBS and BBP-BBM pins are disconnected from the inputs and an internal short-circuit is applied between the corresponding differential inputs*
2. *The BMIC converts the input above using the $T_{VOLT\_FILTER\_001}$ window and checks if the error exceeds $V_{OFFSET\_BIST\_TH}$*
3. *The C_X-C_{X-1}, VBS and BBP-BBM pins are kept disconnected from the inputs and an internal reference voltage (approximately 4.2 V, independent from the DUT reference) is applied between the corresponding differential inputs*
4. *The BMIC converts the input above using the $T_{VOLT\_FILTER\_010}$ window and checks if the error exceeds $V_{GAIN\_BIST\_TH}$*

While the ADCs are being tested, the following analog comparators are also BISTed:

- **Charge pump (VCP)** UV comparator
- **5V LDO (V5V)** UV/OV comparators
- **5V analog LDO (VANA)** UV/OV comparators
- **Ground loss monitor (GNDMON)** comparators (AGND vs. DGND)

The VADC_BIST_DONE latch is set when the ADC BIST procedure ends, while the ABIST_DONE latch is set at the end of the comparator BIST. They can both be reset upon read.

5.5.7.1 *Fault injection*

To allow MCU self-testing of recovery procedures, the BIST_FAULT_INJ field allows injecting a BIST fail on every Cx, VBS and BBx input.

Table 36. BIST fault injection behavior

BIST_FAULT_INJ	Fault injection	Expected outcome
00	No fault injection	No BIST fail expected
01	Fault injected on ADC BIST and CYCLIC WAKEUP DELTA comparators	BIST<x>_FAIL = 1 on every enabled cell VCELL<x>_DELTA = 1 on every cell BIST_BB_FAIL = 1 if the BB is enabled BIST_VB_FAIL = 1 if the VBS is enabled
10	Fault injection on analog comparators	BIST_ANALOG_COMP_FAIL = 1
11	Fault injection on ADC BIST, CYCLIC WAKEUP DELTA comparators and analog comparators	BIST<x>_FAIL = 1 on every enabled cell VCELL<x>_DELTA = 1 on every cell BIST_BB_FAIL = 1 if the BB is enabled BIST_VB_FAIL = 1 if the VBS is enabled BIST_ANALOG_COMP_FAIL = 1

Writing VADC_TEMP_INT_FAULT_INJ = 1 will trigger a failure in the temperature calibration ADC, which in turn will result in the TEMP_INT_RED_ERR being set (cleared upon read after fault injection removal).

Writing VADC_GAIN_INT_FAULT_INJ = 1 will trigger a gain correction error during SOC execution, which in turn will result in GAIN_INT_RED_ERR being set (cleared upon read after SOC ends).

The correct procedures to perform these fault injection tasks are:

- To test TEMP_INT_RED_ERR:
  - Check that TEMP_INT_RED_ERR is 0.
  - Program VADC_TEMP_INT_FAULT_INJ = 1.
  - Check that TEMP_INT_RED_ERR is 1.
  - Program VADC_TEMP_INT_FAULT_INJ = 0.
  - Perform two read accesses to ensure the flag clear.
- To test GAIN_INT_RED_ERR:
  - Check that GAIN_INT_RED_ERR is 0.
  - Program VADC_GAIN_INT_FAULT_INJ = 1.
  - Program VOLT_CONV and SOC = 1.
  - Wait for the end of the SOC execution.
  - Program VADC_GAIN_INT_FAULT_INJ = 0.
  - Check that GAIN_INT_RED_ERR is 1.
  - Perform a second read access to ensure the flags are cleared. The VADC_BIST_DONE (if at least one cell is enabled) and ABIST_DONE latches would be set anyway at the end of the procedure.

5.5.7.2 *Electrical parameters*

Table 37. GPIO open load electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
$V_{OFFSET\_BIST\_TH}$	ADC conversion error threshold for the offset check of the BIST phase	Tested in production			10	mV	
$V_{GAIN\_BIST\_TH}$	ADC conversion error threshold for the gain check of the BIST phase	Tested in production			10	mV	

5.5.8 Gain adjustment (GAIN_ADJ)

To ensure accuracy in the device's lifetime, considering also ADC component aging, the device embeds a self gain adjustment function.

This step is executed at the first SOC after every transition to NORMAL state, to self-compute corrective factors. Once the GAIN_ADJ step is completed, the computed factors are applied in all next voltage routines.

This procedure, as shown in Figure 8, is launched at the end of the whole voltage routine, and possible corrections will therefore be applied only after first run.

It is recommended to execute the gain adjustment step periodically, at least every 100 ms, to ensure the device performs as specified. Every time the GAIN_ADJ step is executed, the voltage conversion routine duration increases by a time equivalent to 2TVOLT_FILTER_010.

Gain adjustment data are available only in NORMAL state and they are reset each time the device transitions to DEEP SLEEP or SILENT BALANCING states. In case of CYCLIC WAKEUP, this feature is not available.

5.5.9 ADC swapping (ADC_SWAP)

To ensure redundancy, each even/odd ADC pair can be swapped after the execution of the Voltage conversion routine by programming ADC_SWAP = 1 in the Start Of Conversion (SOC) frame. This happens for both cell voltages (cell 1..cell 18) and GPIOs (GPIO0..GPIO8).

Since even/odd ADC pairs are referenced to independent voltages, this ensures full redundancy for both voltage and temperature measurements. ADC swapping also ensures that redundant measurements are executed with the same functional accuracy. Additionally, all redundant conversion paths are checked as discussed in the Built-In Self-Test (BIST) section.

If one ADC of the even/odd pair is faulty, this feature allows for keeping the OV/UV/OT/UT detection functionality by swapping the ADCs at each iteration of the Voltage conversion routine.

In the register map, the SWAP_ECHO bit will toggle at the end of the Voltage conversion routine if the ADC_SWAP bit was set to 1 in the SOC request frame. This will confirm that the ADC swapping has been completed.

5.6 Die temperature monitor (T_J)

The L9965A/L99BM218 monitors the junction temperature with a sensor placed close to the ADC stage in order to feed the calibration algorithm.

The junction temperature measurement is stored in the DIE_ADC_TEMP_MEAS register and can be computed according to the following formula:

$$T(°C) = Code(T) * 0.077338 - 82.30396 \quad (1)$$

Thanks to the improved accuracy of the T_J measurement, the user SW may monitor abnormal differences in the T_J of different BMICs in the stack operating in the same conditions. This SW procedure helps detect failures on the die temperature monitor which may affect measurement accuracy and thermal shutdown/warning detection.

5.6.1 Diagnostics

Table 38. Die temperature monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Thermal warning	If T_J rises above $T_{J\_WARN\_TH}$, the TJ_WARN fault is acknowledged	The TJ_WARN flag is set	If T_J falls below $T_{J\_WARN\_TH}$ - $T_{J\_WARN\_HYS}$, the TJ_WARN flag can be cleared by MCU	None	Nonmaskable
Thermal shutdown	If T_J rises above $T_{J\_SD\_TH}$, the TJ_SD fault is acknowledged	The TJ_SD flag is set BAL_START configuration and BAL_TIMER value are reset to default Balancing is stopped on all cells	If T_J falls below $T_{J\_SD\_TH}$ - $T_{J\_SD\_HYS}$, the TJ_SD flag can be cleared by MCU	The balancing FETs are kept OFF and can be re-engaged by setting the BAL_START bit to 1 again	TJ_SD_BAL_MSK masks reaction on balancing pin

5.6.2 Electrical parameters

Table 39. Die temperature monitor electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{J_ERR}	Die temperature total conversion error		-10		10	°C
$T_{J\_SD\_TH}$	Thermal shutdown threshold	Guaranteed by SCAN	170	185	200	°C
$T_{J\_SD\_HYS}$	Thermal shutdown threshold hysteresis	Guaranteed by SCAN		10		°C
$T_{J\_WARN\_TH}$	Thermal warning threshold	Guaranteed by SCAN	150	165	180	°C
$T_{J\_WARN\_HYS}$	Thermal shutdown threshold hysteresis	Guaranteed by SCAN		10		°C

5.7 Cell balancing FETs (Sx)

The L9965A/L99BM218 provides passive internal balancing, allowing cells to be discharged by means of external resistors.

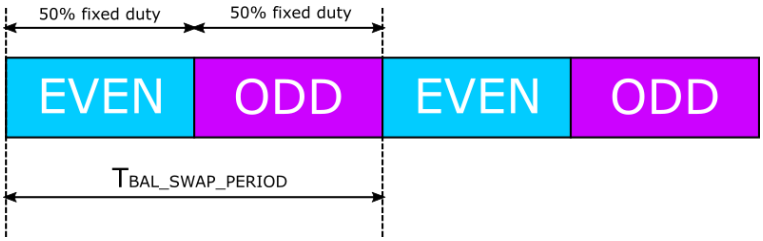
5.7.1 Balancing Modes

The IC implements both Timed mode and PWM-based balancing modes. They can be selected through the BAL_MODE bit, which is latched at the beginning of the balancing (BAL_START 0 → 1) and cannot be changed on-the-fly while balancing is running.

To allow balancing both odd and even cells in a single thread, the balancing controller offers the possibility of enabling a time-window multiplexing strategy. The MCU may enable the odd/even swapping by programming BAL_SWAP = 1 and configuring the swapping period through the BAL_SWAP_PERIOD field. The BAL_SWAP setting is latched upon balancing start (BAL_START 0 → 1) and cannot be updated on-the-fly.

The BAL_SWAP_PERIOD can however be updated on-the-fly and the change will take effect after $T_{BAL\_SWAP\_UPDATE}$.

Figure 13. Balancing swap strategy



5.7.1.1 *Timed mode*

The timed mode is recommended for long, pre-calculated balancing intervals. To configure and launch it, follow this procedure:

Procedure 1: Timed balancing setup

1. Program BAL_MODE = 0
2. Select the cells to be discharged by programming BAL<X>_ON = 1
3. Set the balancing timer prescaler by programming BAL_PRE_SCAL
4. Program the timer threshold (BAL<X>_TH) for each enabled cell
5. (optional) Enable the balancing swap by programming BAL_SWAP = 1 and configuring the BAL_SWAP_PERIOD field to select how often the balancing automatically toggles from even to odd cells.
6. Start the balancing programming BAL_START = 1.
7. The internal balancing timer is reset and started. It is then continuously compared to each channel threshold to evaluate the balancing stop condition (BAL_TIMER >= BAL<X>_TH). The timer status is reported in the BAL_TIMER register.

Note: Since the common BAL_TIMER keeps running while even/odd channels are in their OFF phase, the BAL<X>_TH thresholds shall be programmed taking into account the 50% duty-cycle due to the odd/even swap activity. Therefore, the threshold shall be set to twice the effective calculated balancing period.

Once the balancing is running on a cell:

- The MCU may temporarily pause/re-engage it by toggling the BAL<x>_ON bit. This is only valid for channels that were initially set for balancing, meaning that their corresponding enabled bit (BAL<x>_ON) was set to '1' upon the BAL_START 0 → 1 transition. To add new channels to the balancing, the thread has to be restarted by applying the new configuration and toggling the BAL_START bit.
  - Additionally, certain failures (e.g. NTC OT, cell UV, balancing UV, etc.) have the same effect as a pause commanded by the MCU. As long as failure is present, balancing is inhibited. It is released when the fault disappears and the corresponding flag is cleared by the MCU, unless otherwise indicated in the dedicated section; see the Balancing overcurrent (BAL OC) and Die temperature monitor (T_J) sections for further information.

- The MCU may update the BAL<X>_TH threshold anytime
  - To restart balancing on a cell whose threshold has already been exceeded, simply read the BAL_TIMER and update the BAL<X>_TH accordingly

$$BAL_{X_{TH_{NEW}}} = BAL_{TIMER} + \Delta BAL_{X_{TH}} \quad (2)$$

- The MCU may stop balancing anytime by programming BAL_START = 0
  - In this case, BAL_TIMER will be forced to saturate to its upper bound, so that a stop condition is verified on all cells.

5.7.1.2 *PWM-based*

The BMIC also enables individual cell balancing with a programmable PWM duty-cycle. The PWM period is fixed to $T_{BAL\_PWM\_PERIOD}$, while the duty-cycle can be dynamically adjusted via SW by programming the $T_{BAL\_PWM\_DUTY}$ in 32 steps.

The PWM-based mode is recommended for real-time balancing strategies. The following procedure shall be executed to initiate and manage the PWM balancing task:

Procedure 2: PWM-based balancing setup

1. Program BAL_MODE = 1
2. Select the cells to be discharged by programming BAL<x>_ON = 1
3. Program the cell duty-cycle in respect to TBAL_PWM_PERIOD, by writing the BAL<X>_TH register. The LSBs of these registers are reused to define the duty-cycle.
4. (optional) Enable the balancing swap by programming BAL_SWAP = 1 and configuring the BAL_SWAP_PERIOD field to select how often the balancing automatically toggles from even to odd cells. The swap period timer is designed to be an integer multiple of TBAL_PWM_PERIOD, so that swapping always occurs at the beginning of a PWM cycle and no truncated PWM periods happen.
5. Program the safety timer watchdog threshold in the BAL_TIMER_MAX_TH register. This will define the maximum task duration.
6. Start the balancing by programming BAL_START = 1. Balancing on individual channels can then be fine-tuned by changing the BAL<X>_TH (sampled every TBAL_PWM_PERIOD) and BAL<x>_ON, but the safety timer will keep running in the background. The safety timer status is reported in the BAL_TIMER register.

Note: When enabling the balancing swap, the effective cell balancing duty-cycle will be half the programmed one. For instance, programming a 100% duty-cycle on a cell will result in the cell being balanced 50% of the time.

Note: In case balancing swap is disabled (BAL_SWAP = 0), balancing adjacent cells results in an increment in the balancing current (approximately twice the single cell current). The overcurrent protection might be inadvertently triggered.

Once the balancing is running on a cell:

- The MCU may temporarily pause/re-engage it by toggling the BAL<x>_ON bit. This is only valid for channels that were initially set for balancing, meaning that their corresponding enabled bit (BAL<x>_ON) was set to '1' upon the BAL_START 0 → 1 transition. To add new channels to the balancing, the thread has to be restarted by applying the new configuration and toggling the BAL_START bit.
  - Additionally, certain failures (e.g. NTC OT, cell UV, balancing UV, etc.) have the same effect as a pause commanded by the MCU. As long as a failure is present, balancing is inhibited. It is released when the fault disappears and the corresponding flag is cleared by the MCU, unless otherwise indicated in the dedicated section; see the Balancing overcurrent (BAL OC) and Die temperature monitor (T_J) sections for further information.
- The MCU may update the PWM duty-cycle by writing the BAL<X>_TH time
  - The modification will take effect at the end of the ongoing PWM cycle
- The MCU may update the BAL_TIMER_MAX_TH threshold anytime
- The MCU may stop balancing anytime by programming BAL_START = 0
  - In this case, BAL_TIMER will be forced to saturate to its upper bound, so that a stop condition is verified on all cells.

5.7.2 Electrical parameters

Table 40. Balancing electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
$R_{DSON\_BAL\_NORMAL}$	Balancing FET resistance	NORMAL			1.4	Ω	Sx
$R_{DSON\_BAL\_SILENT\_LO}$	Balancing FET resistance	SILENT BALANCING, FET between S_{X+1} and S_X, V_{VB} - V_{Sx} ≥ 2.7V, with x=14-17			1.8	Ω	Sx
$R_{DSON\_BAL\_SILENT\_MID}$	Balancing FET resistance	SILENT BALANCING, FET between S_{X+1} and S_X,, V_{VB} - V_{Sx} ≥ 2.2V, with x=14-17			2.6	Ω	Sx
$R_{DSON\_BAL\_SILENT\_HI}$	Balancing FET resistance	SILENT BALANCING, FET between S_{X+1} and S_X, V_{VB} - V_{Sx} ≥ 1.8V, with x=14-17			3	Ω	Sx
$R_{DSON\_BAL\_SILENT}$	Balancing FET resistance	SILENT BALANCING, FET between S_{X+1} and S_X, V_{VB} - V_{Sx} ≥ 5V, with x=0-13 Guaranteed by design			1.8	Ω	Sx
I_{BAL}	Balancing current	Design Info			400	mA	Sx
$T_{BAL\_TIMER\_0}$	Balancing timer threshold BAL<x>_TH (7 bit), $T_{BAL_{TIMER\_0}} = 512s * CODE$	BAL_PRE_SCAL = 1	0		65024	s	Sx
$T_{BAL\_TIMER\_1}$	Balancing timer threshold BAL<x>_TH (7 bit), $T_{BAL_{TIMER\_1}} = 4s * CODE$	BAL_PRE_SCAL = 0	0		508	s	Sx
$T_{BAL\_TIMER\_MAX}$	Safety timer watchdog threshold used in PWM mode BAL_TIMER_MAX_TH (16 bit), $T_{BAL_{TIMER_{MAX}}} = 1s * CODE$	Guaranteed by SCAN	0		65536	s	Sx
$T_{BAL\_SWAP\_PERIOD}$	Balancing swap period between even and odd channels, available in Timed mode (3 bit), $T_{BAL_{SWAP_{PERIOD}}} = 4s * 2^{CODE}$	Guaranteed by SCAN	4		512	s	Sx
$T_{BAL\_SWAP\_UPDATE}$	Balancing swap period settling time	Guaranteed by SCAN	3.5		555	s	Sx
$T_{BAL\_PWM\_PERIOD}$	Balancing base period for PWM mode	Guaranteed by SCAN	-8%	32	+8%	s	Sx
$T_{BAL\_PWM\_DUTY}$	Balancing ON period for PWM mode (5 bit), $T_{BAL_{PWM_{DUTY}}} = 1s * \left(CODE + 1\right)$	Guaranteed by SCAN	1		32	s	Sx

5.7.3 Balancing overcurrent (BAL OC)

Balancing FETs are protected with overcurrent detection via a VDS monitor:
This diagnostic is always active when balancing is enabled and covers the failures listed in Table 41.

Table 41. Balancing diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
BAL OC	When the balancing channel is turned ON, in case the FET current rises above I_{BAL_OC} for an interval longer than T_{BAL_OC}, the BAL<x>_OC fault is acknowledged	BAL<x>_OC flag is set. BAL<x>_ON configuration is reset to default value. The balancing FET is turned OFF. The IC moves to NORMAL state to perform Section 5.10.4.	When the FET is in the OFF state, the BAL<x>_OC flag can be cleared by the MCU	The balancing FET is kept OFF and shall be re-engaged by setting the BAL<x>_ON bit to 1 again	BAL<x>_ON masks diagnostic execution. When disabled, the BAL<x>_OC flag can always be cleared. BAL_OC_BAL_MSK* masks balance turn OFF, does not mask transition to NORMAL state
*Exceptionally, the BAL_OC_BAL_MSK bit is active even in low-power states					

5.7.3.1 *Electrical parameters*

Table 42. Balancing electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
I_{BAL_OC}	Balancing overcurrent threshold	Tested in production	500			mA	Sx
T_{BAL_OC}	Balancing overcurrent filter time	Tested in production	8		24	µs	Sx

5.8 GPIO

The device features 10 GPIOs configurable according to the following table:

All GPIOs configured as input are protected against back-feeding towards V5V in case of an external short-to-battery event.

Table 43. GPIO configuration

GPIO<x>_CONF	Configuration
00 (default config, for pins not configured as alternate functions by default)	ADC input (absolute)
01	ADC input (ratiometric)
10	Generic digital input
11	Generic digital output (push/pull)

GPIOs can be used as simple I/Os, driven/read via dedicated registers:

- When configured as digital output, the GPIOs can be driven according to the GPO<x> bit.
- The input buffer status can be read via the GPI<x> bit.
  - When configured as digital input, an internal weak pull-down/pull-up can be configured by programming GPIO<x>_PU_PD.

Table 44. GPIO weak pull-up/pull-down configuration

GPIO<x>_PU_PD	Configuration
0 (default)	Weak pull-down ($R_{GPIO\_WK\_PD}$)
1	Weak pull-up ($R_{GPIO\_WK\_PU}$)

The dedicated bitfield can be used to force alternate special functions:

Table 45. Alternate functions activation

SPI_MODE	Configuration
00 (default)	SPI target
01, 10	SPI disabled
11	SPI
I2C_EN	**Configuration**
0 (default)	I2C disabled
1	I2C

The following table summarizes the GPIO configurations in NORMAL and CYCLIC WAKEUP states.

Table 46. GPIO configurations in NORMAL and CYCLIC WAKEUP[end]

Pin	Generic	SPI controller (SPI_MODE)	SPI target (SPI_MODE)	I2C controller (I2C_EN)
GPIO0_NCS0	IN(HiZ/PU/PD) / OUT*	OUT	IN(PU)	X
GPIO1_NCS1	IN(HiZ/PU/PD) / OUT*	OUT**	X	X
GPIO2_SDI	IN(HiZ/PU/PD) / OUT*	IN(PD)	IN(PD)	X
GPIO3_SDO	IN(HiZ/PU/PD) / OUT*	OUT	OUT	X

Pin	Generic	SPI controller (SPI_MODE)	SPI target (SPI_MODE)	I2C controller (I2C_EN)
GPIO4_SCLK	IN(HiZ/PU/PD) / OUT*	OUT	IN(PD)	X
GPIO5_SDA	IN(HiZ/PU/PD) / OUT*	X	X	INOUT(OD)
GPIO6_SCL	IN(HiZ/PU/PD)/OUT*	X	X	OUT(OD)
GPIO7	IN(HiZ/PU/PD) / OUT	X	X	X
GPIO8	IN(HiZ/PU/PD) / OUT	X	X	X
GPIO9	IN(HiZ/PU/PD) / OUT	X	X	X

Legend: PU = Pull-Up; PD = Pull-Down; OD = Open Drain; X = Don't care; HiZ = High Impedance
** depending on configuration (GPIOx_CONF, GPIOx_PU_PD)*
*** depending on configuration (GPIO1_NCS1_EN)*

The following table summarizes the GPIO management in DEEP SLEEP and SILENT BALANCING states.

Table 47. GPIO configuration in DEEP SLEEP and SILENT BALANCING

Pin	1ST Deep Sleep	1ST Normal*	NTH Deep sleep/silent balancing	NTH Normal
GPIO0_NCS0	IN(PU) for wake-up	IN(PU) for SPI target	IN(PU) for wake-up only if SPI target mode is configured; otherwise HiZ	Latest configuration
GPIO1_NCS1	HiZ	Hiz	HiZ	Latest configuration
GPIO2_SDI	HiZ	IN(PD) for SPI target	HiZ	Latest configuration
GPIO3_SDO	HiZ	OUT for SPI target	HiZ	Latest configuration
GPIO4_SCLK	IN(PD) for wake-up	IN(PD) for SPI target	IN(PD) for wake-up only if SPI target mode is configured; otherwise, HiZ	Latest configuration
GPIO5_SDA	HiZ	HiZ	HiZ	Regmap configuration
GPIO6_SCL	HiZ	HiZ	HiZ	Regmap configuration
GPIO7	HiZ	HiZ	HiZ	Regmap configuration
GPIO8	HiZ	HiZ	HiZ	Regmap configuration
GPIO9	HiZ	HiZ	HiZ	Regmap configuration

Legend: PU = Pull-Up; PD = Pull-Down; OD = Open Drain; X = Don't care; HiZ = High Impedance
** NVM configuration with default factory values*

Note: If VB is removed and the IC goes back to the OFF state, the first DEEP SLEEP will behave as described in the table above. The first NORMAL configuration will depend on the NVM content: if the NVM has been previously programmed, the configurations stored in the memory will be re-downloaded and applied.

5.8.1 Electrical parameters

Table 48. SPI controller electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
V_{GPIOH}	GPIO high output value	I_{SOURCE} = 2mA	V5V-0.4			V	GPIOx
V_{GPIOL}	GPIO low output value	I_{SINK} = 2mA			0.4	V	GPIOx
$R_{GPIO\_WK\_PU}$	GPIO weak pullup resistor to internal 1.8V	GPIO<x>_PU_PD = 1	0.5	1.2	1.9	MΩ	GPIOx
$R_{GPIO\_WK\_PD}$	GPIO weak pull-down resistor to GND, 1V applied on the GPIO pin (internally protected to 1.8V)	GPIO<x>_PU_PD = 0	0.5	1.2	1.9	MΩ	GPIOx
C_{GPIO_EXT}	GPIO external bypass capacitor	Application information, including parasitics			140	pF	GPIOx
$R_{GPIO\_EXT\_PU}$	GPIO external pull-up resistor for open-drain configurations	Application information	-1%	4.7	+1%	kΩ	GPIOx
$V_{HIGH\_GPIO\_IN}$	GPIO, input mode, high level at GPIO input		1.35			V	GPIOx
$V_{LOW\_GPIO\_IN}$	GPIO, input mode, low level at GPIO input				0.8	V	GPIOx
$I_{LEAK\_GPIO\_IN\_HIZ}$	GPIO, input mode, leakage current in HiZ state	Disable PU/PD paths, 0V < V_{GPIOx} < V_{V5V}	-300		300	nA	GPIOx
$V_{OL\_GPIO\_OPEND}$	GPIO, open-drain mode, low output voltage	I = 2mA, valid only for GPIO5_SDA and GPIO6_SCL			0.4	V	GPIOx

5.9 Communication interfaces

5.9.1 SPI controller

The IC integrates an SPI controller peripheral to manage connection to external sensors and NVMs.

When enabled, the following pins are configured as an SPI controller:

- GPIO0_NCS0 → Chip select (digital output)
- GPIO2_SDI → Serial data input (digital input, weak pull-down $R_{GPIO\_WK\_PD}$)
- GPIO3_SDO → Serial data output (digital output)
  - The output buffer is connected to 5V LDO (V5V)
- GPIO4_SCK → Serial clock (digital output)

Additionally, GPIO1_NCS1 can be configured as a second chip select by programming it as digital output and setting GPIO1_NCS1_EN = 1.

Weak pull-down is automatically enabled in NORMAL and CYCLIC WAKEUP to address open failures on SDI pin.

The SPI peripheral can communicate with one SPI slave at a time, but if both chip selects (GPIO0_NCS0 and GPIO1_NCS1) had been configured as such, to actively drive high the chip selects in idle state it is necessary to set respectively the GPIO0_NCS0_ACTIVE_IDLE and GPIO1_NCS1_ACTIVE_IDLE configuration bits, otherwise the pins are left in HiZ.

The SPI peripheral manages transfers using GPIO_SPI_MISO and GPIO_SPI_MOSI registers, whose size is 40 bit. In order to adapt to different protocols, the peripheral can be configured to handle frame sizes with multiples of 8 bit. Such a configuration can be independently chosen for each of the two supported SPI targets. Frame size can be chosen by programming the SPI_FRAME_SIZE<x> registers.

Table 49. SPI controller protocol configuration

SPI_FRAME_SIZE<x>	Frame size
000	8 bit
001	16 bit
010	24 bit
011	32 bit
100	40 bit
101	40 bit
110	40 bit
111	40 bit

The MCU can trigger a SPI transfer by writing SPI_TRANSFER = 1, along with the desired SPI_NCS<x> bit. Writing both SPI_NCS<x> to ‘1’ in the same frame is not allowed; the command will be discarded, and no transfer will take place. The same happens if a transfer is commanded while another is still ongoing. Only one target transfer can be managed at a time.

Data on the SPI controller bus is not decoded, and CRC errors and other safety mechanisms shall be managed by the MCU.

The clock phase and polarity can be configured by programming the SPI_MASTER_CPOL<x> and SPI_MASTER_CPHA<x> bits.

The MCU can verify that the SPI master transmission has been completed by monitoring the flag SPI_MASTER_BUSY.

5.9.1.1 *Electrical parameters*

For the main oscillator frequency, see the operating range in Table 18.

Figure 14. SPI controller timing diagram (example with CPOL = 0 & CPHA = 1)

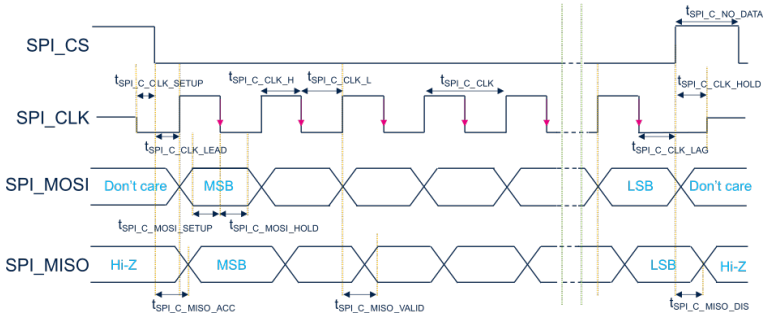


Table 50. SPI controller electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
$f_{SPI\_C\_CLK}$	SPI controller clock frequency, $f_{SPI\_M\_CLK} = 1/t_{SPI\_C\_CLK}$	Tested by SCAN		500		kHz	GPIO4_SCLK
$t_{SPI\_C\_CLK\_SETUP}$	Time elapsed after CLK -> CPOL @ NCS H/L edge	Cload=60pF	500			ns	GPIO0_NCS0, GPIO1_NCS1, GPIO4_SCLK
$t_{SPI\_C\_CLK\_HOLD}$	Time elapsed after CLK -> CPOL @ NCS L/H edge	Cload=60pF	500			ns	GPIO0_NCS0, GPIO1_NCS1, GPIO4_SCLK
$t_{SPI\_C\_CLK\_L}$	Minimum time CLK = LOW	Tested by SCAN	900			ns	GPIO4_SCLK
$t_{SPI\_C\_CLK\_H}$	Minimum time CLK = HIGH	Tested by SCAN	900			µs	GPIO4_SCLK
$t_{SPI\_C\_MISO\_VALID}$	Propagation delay (time elapsed after propagating SCLK edge @ SDI active)	Application info			468.7	ns	GPIO2_SDI, GPIO4_SCLK
$t_{SPI\_C\_CLK\_LEAD}$	CLK toggle after NCS = low	Tested by SCAN	4		7.72	µs	GPIO0_NCS0, GPIO1_NCS1, GPIO4_SCLK
$t_{SPI\_C\_MOSI\_SETUP}$	SDO setup time (time elapsed after SDO data valid @ sampling SCLK edge)	Tested by SCAN	93.74			ns	GPIO3_SDO, GPIO4_SCLK
$t_{SPI\_C\_MOSI\_HOLD}$	SDO hold time (time elapsed after propagating SCLK edge @ SDO data “not valid anymore”)	Tested by SCAN	93.74			ns	GPIO3_SDO, GPIO4_SCLK
$t_{SPI\_C\_CLK\_LAG}$	CLK toggle before NCS = high	Tested by SCAN	4		7.72	µs	GPIO0_NCS0, GPIO1_NCS1, GPIO4_SCLK
$t_{SPI\_C\_NO\_DATA}$	Inter-frame delay: minimum NCS inactive time between two consecutive frames	Tested by SCAN	4			µs	GPIO0_NCS0, GPIO1_NCS1
$t_{SPI\_C\_MISO\_DIS}$	NCS L/H to SDI high impedance	Application info			1	µs	GPIO0_NCS0, GPIO1_NCS1, GPIO2_SDI
$t_{SPI\_C\_MISO\_ACC}$	NCS H/L to SDI active	Application info			3	µs	GPIO0_NCS0, GPIO1_NCS1, GPIO2_SDI

The following procedure shows a step sequence to be followed to execute a communication through the SPI controller.

The SPI controller communication can be configured through the following parameters stored in the NVM memory:

- SPI_MASTER_CPHA1: it configures the SPI controller clock phase when chip select #1 is selected (GPIO1_NCS1)
- SPI_MASTER_CPHA0: it configures the SPI controller clock phase when chip select #0 is selected (GPIO0_NCS0)
- SPI_MASTER_CPOL1: it configures the SPI controller clock polarity when chip select #1 is selected (GPIO1_NCS1)
- SPI_MASTER_CPOL0: it configures the SPI controller clock polarity when chip select #0 is selected (GPIO0_NCS0)
- GPIO0_NCS0_ACTIVE_IDLE: it configures chip select #0 idle state when both chip selects have been enabled
- GPIO1_NCS1_ACTIVE_IDLE: it configures chip select #1 idle state when both chip selects have been enabled

Below is an example of the procedure for communicating through the SPI controller

Procedure 3 - SPI controller transmission sequence

1. Writing of the data to be sent on MOSI
   a. MOSI_39_32: fifth byte to send;
   b. MOSI_31_24: fourth byte to send;
   c. MOSI_23_16: third byte to send;
   d. MOSI_15_8: second byte to send;
   e. MOSI_7_0: first byte to send.
2. Setting the byte number and the NCS to be used(*):
   a. SPI_FRAME_SIZE1: sets the frame size for SPI communication on GPIO1_NCS1 (000 – 8 bits; 001 – 16 bits; 010 – 24 bits; 011 – 32 bits; others – 40 bits).
   b. SPI_FRAME_SIZE0: sets the frame size for SPI communication on GPIO0_NCS0. Same codifications as for SPI_FRAME_SIZE1.
   c. SPI_NCS1: it selects GPIO1_NCS1 to be used as chip select for SPI controller communication.
   d. SPI_NCS0: it selects GPIO0_NCS0 to be used as chip select for SPI controller communication.
3. Launching of the signal triggering the start of communication:
   a. SPI_TRANSFER: it triggers the start of the transmission of SPI communication. Since the device is the controller, it sends a MOSI frame.
4. Reading of the SPI_MASTER register to check the communication status(**).
   a. MISO_39_32: Fifth byte received;
   b. MISO_31_24: Fourth byte received;
   c. MISO_23_16: Third byte received;
   d. MISO_15_8: Second byte received;
   e. MISO_7_0: First byte received.

(*)ATTENTION: it is not allowed to set SPI_NCS0 = 1 and SPI_NCS1 = 1.

(**)Once the communication is finished, the MCU can read the MISO received message.

5.9.2 I2C controller

The IC integrates an I2C controller peripheral to manage connection to external sensors and NVMs.

When enabled, the following pins are configured as an I2C controller:

- GPIO5_SDA → Chip select (open drain)
- GPIO6_SCL → Serial clock (open drain)

The clock frequency can be configured by programming the I2C_MASTER_CLK bit.

The I2C peripheral manages transfers using the GPIO_I2C_DATA_IN and GPIO_I2C_DATA_OUT registers, whose size is 32 bit. In order to adapt to different protocols, the peripheral can be configured to handle frame sizes with multiples of 8 bit. Frame size can be chosen by programming the I2C_FRAME_SIZE register.

The MCU can trigger an I2C transfer by writing I2C_TRANSFER = 1. A transfer cannot be interrupted: concurrent triggers will be discarded.

Data on the I2C bus is not decoded and CRC errors and other safety mechanisms shall be managed by the MCU.

Below are the fields used to set the parameters concerning the communication through the I2C controller.

- I2C_STOP_AFTER_NACK: if it is set to 1, it sends a STOP after it has received/sent a NACK;
- I2C_FORCE_NACK: if it is set to 1, it forces a NACK (when the device drives NACK);
- I2C_RD_WRN: it defines which component (controller or target) takes control of the SDA line (0 – writing operation (controller); 1 – reading operation (target));
- I2C_OP_CODE: it codifies the operation required (3-bit field: bit2 – START; bit1 – DATA; bit0 – STOP. Codes 000, 100,101 are reserved);
- I2C_FRAME_SIZE: it sets the frame size for I2C communication (00 – 1 byte; 01 – 2 bytes; 10 – 3 bytes; 11 – 4 bytes. For handling 40-bit frames, bytes must be sent in two steps);
- I2C_TRANSFER: if it is set to 1, it triggers the start of I2C communication (the device is the controller).

Two bits are available to check if something went wrong during the reading/writing operation:

- I2C_TX_ERR: if this flag is asserted, the data has not been sent correctly on the SDA line;
- I2C_RX_ACK_ERR: if this flag is asserted, an error in the receiver acknowledgment has occurred.

5.9.2.1 *Electrical parameters*

Figure 15. I2C controller timing

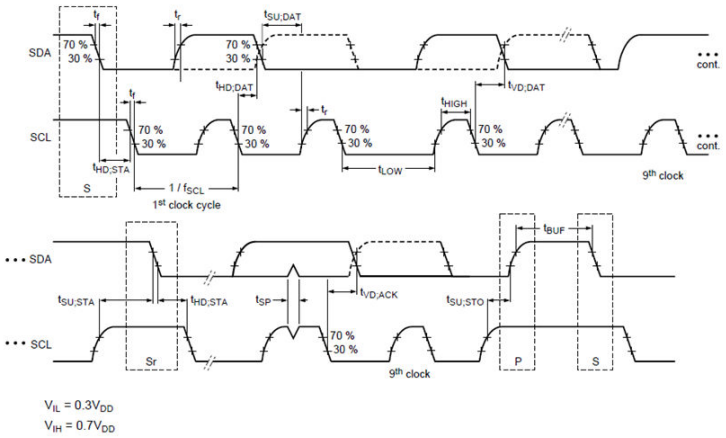


Table 51. I2C controller electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
f_{I2C_CLK0}	I2C controller clock frequency	I2C_MASTER_CLK = 0	40	62.5	100	kHz	GPIO5_SDA, GPIO6_SCL
f_{I2C_CLK1}	I2C controller clock frequency	I2C_MASTER_CLK = 1	200	250	400	kHz	GPIO5_SDA, GPIO6_SCL
t_{LOW_100}	LOW period of the SCL clock	f_{I2C_CLK0} = 100kHz	4.26		12.75	µs	GPIO5_SDA, GPIO6_SCL
t_{LOW_400}	LOW period of the SCL clock	f_{I2C_CLK1} = 400kHz	1.18		2.75	µs	GPIO5_SDA, GPIO6_SCL
t_{HIGH_100}	HIGH period of the SCL clock	f_{I2C_CLK0} = 100kHz	4.26		12.75	µs	GPIO5_SDA, GPIO6_SCL
t_{HIGH_400}	HIGH period of the SCL clock	f_{I2C_CLK1} = 400kHz	1.18		2.75	µs	GPIO5_SDA, GPIO6_SCL

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
t_{HD_STA}	SCL hold (High) time, after SDA falling edge has created the START condition, for the START condition to be correctly detected		0.6			µs	GPIO5_SDA, GPIO6_SCL
t_{SU_STA}	SCL set-up time to High (SDA already High) before SDA falling edge creates the START condition sequence (by falling when SCL is steadily High)		0.6			µs	GPIO5_SDA, GPIO6_SCL
t_{HD_DAT}	SDA hold time after SCL falling edge		300		-	ns	GPIO5_SDA, GPIO6_SCL
t_{SU_DAT}	SDA set-up time before SCL rising edge		100		-	ns	GPIO5_SDA, GPIO6_SCL
t_r	Rise time of SDA signal	With 4.7kΩ pull-up resistor and 40pF load	0		300	ns	GPIO5_SDA, GPIO6_SCL
t_f	Fall time of SDA signal	With 4.7kΩ pull-up resistor and 40pF load	0		300	ns	GPIO5_SDA, GPIO6_SCL
t_{rf_SCL}	Rise/fall time SCL signal		0		300	ns	GPIO5_SDA, GPIO6_SCL
t_{SU_STO}	SCL set-up time to High (SDA already Low) before SDA rising edge creates the STOP condition sequence (by rising when SCL is steadily High)		0.6			µs	GPIO5_SDA, GPIO6_SCL
t_{HD_STO}	SCL hold (High) time, after SDA rising edge has created the STOP condition, for the STOP condition to be correctly detected		0.6			µs	GPIO5_SDA, GPIO6_SCL
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs	GPIO5_SDA, GPIO6_SCL
C_b	Capacitive load for each bus line				400	pF	GPIO5_SDA, GPIO6_SCL
$t_{VD\_DAT\_ACK}$	Data (ACK) valid time				0.9	µs	GPIO5_SDA, GPIO6_SCL

It is possible to set, the I2C controller clock frequency in the NVM memory, through the I2C_MASTER_CLK (0 = 62.5 kHz, 1 = 250 kHz) bit.

Below are four examples of procedures for communicating through the I2C controller, covering the case of reading, writing, in the case of up to 4 bytes and in the case of more than 4 bytes.

Procedure 4 - I2C controller transmission sequence (Write 3-bytes message)

1. Writing of the data to be sent
   a. I2C_DATA_OUT_7_0: first byte to send; [write device address of target + 0 (write command bit)]
   b. I2C_DATA_OUT_15_8: second byte to send
   c. I2C_DATA_OUT_23_16: third byte to send
2. Setting of I2C communication parameters and launching of the signal triggering the start of communication
   a. I2C_STOP_AFTER_NACK = 0
   b. I2C_FORCE_NACK = 0
   c. I2C_RD_WRN = 0
   d. I2C_OP_CODE = 111
   e. I2C_FRAME_SIZE = 10
   f. I2C_TRANSFER = 1
3. Checking of communication. If the I2C_TX_ERR flag is asserted, the data has not been sent correctly on the SDA.

Procedure 5 - I2C controller transmission sequence (Read of 3-bytes message)

1. Writing of the data to be sent in order to set the reading address
   a. I2C_DATA_OUT_7_0: first byte to send; [write device address of target + 0 (write command bit)]
   b. I2C_DATA_OUT_15_8: second byte to send. [write register address of target]
2. Launching of the trigger for starting the READ communication
   a. I2C_STOP_AFTER_NACK = 0
   b. I2C_FORCE_NACK = 0
   c. I2C_RD_WRN = 0
   d. I2C_OP_CODE = 110
   e. I2C_FRAME_SIZE = 01
   f. I2C_TRANSFER = 1
3. Writing of device address to prepare the reading: I2C_DATA_OUT_7_0 must be written with the device address of target + 1 (read command bit)
4. Launching of the trigger to indicate device address + read the command bit
   a. I2C_STOP_AFTER_NACK = 0
   b. I2C_FORCE_NACK = 0
   c. I2C_RD_WRN = 0
   d. I2C_OP_CODE = 110
   e. I2C_FRAME_SIZE = 00
   f. I2C_TRANSFER = 1
5. Launching of the trigger to start READ
   a. I2C_STOP_AFTER_NACK =0
   b. I2C_FORCE_NACK =0
   c. I2C_RD_WRN = 1
   d. I2C_OP_CODE = 011
   e. I2C_FRAME_SIZE = 10
   f. I2C_TRANSFER = 1
6. Reading of the received message
   a. I2C_DATA_IN_7_0: first byte to receive
   b. I2C_DATA_IN_15_8: second byte to receive
   c. I2C_DATA_IN_23_16: third byte to receive
7. Checking of communication
   a. If the I2C_TX_ERR flag is asserted, the data has not been sent correctly on the SDA.
   b. If the I2C_RX_ACK_ERR flag is asserted, an error in the receiver acknowledgment occurred.

Procedure 6 - I2C controller transmission sequence (Write 5-bytes message)

1. Writing of the data to be sent covering the first four bytes
   a. I2C_DATA_OUT_7_0: first byte to send; [write device address of target + 0 (write command bit)]
   b. I2C_DATA_OUT_15_8: second byte to send
   c. I2C_DATA_OUT_23_16: third byte to send
   d. I2C_DATA_OUT_31_24: fourth byte to send
2. Setting of I2C communication parameters and launching of the signal triggering the start of communication for the first 4 bytes
   a. I2C_STOP_AFTER_NACK = 0
   b. I2C_FORCE_NACK = 0
   c. I2C_RD_WRN = 0
   d. I2C_OP_CODE = 110
   e. I2C_FRAME_SIZE = 11
   f. I2C_TRANSFER = 1

3. Writing of the data to be sent for the fifth byte
   a. I2C_DATA_OUT_7_0: fifth byte to send
4. Setting of I2C communication parameters and launching of the signal triggering the start of communication for the fifth byte
   a. I2C_STOP_AFTER_NACK = 0
   b. I2C_FORCE_NACK = 0
   c. I2C_RD_WRN = 0
   d. I2C_OP_CODE = 011
   e. I2C_FRAME_SIZE = 00
   f. I2C_TRANSFER = 1
5. Checking of communication. If the I2C_TX_ERR flag is asserted, the data has not been sent correctly on the SDA.

Procedure 7 - I2C controller transmission sequence (Read 5-bytes message)

1. Writing of the data to be sent in order to set the reading address
   a. I2C_DATA_OUT_7_0: first byte to send; [write device address of target + 0 (write command bit)]
   b. I2C_DATA_OUT_15_8: second byte to send. [write register address of target]
2. Launching of the trigger to start the READ communication
   a. I2C_STOP_AFTER_NACK =0
   b. I2C_FORCE_NACK =0
   c. I2C_RD_WRN = 0
   d. I2C_OP_CODE = 110
   e. I2C_FRAME_SIZE = 01
   f. I2C_TRANSFER = 1
3. Writing of the device address to prepare the reading: I2C_DATA_OUT_7_0 must be written with the device address of target + 1 (read command bit)
4. Launching of the trigger to indicate device address + read command bit
   a. I2C_STOP_AFTER_NACK = 0
   b. I2C_FORCE_NACK = 0
   c. I2C_RD_WRN = 0
   d. I2C_OP_CODE = 110
   e. I2C_FRAME_SIZE = 00
   f. I2C_TRANSFER = 1
5. Launching of the trigger to start READ (first four bytes)
   a. I2C_STOP_AFTER_NACK = 0
   b. I2C_FORCE_NACK = 0
   c. I2C_RD_WRN = 1
   d. I2C_OP_CODE = 010
   e. I2C_FRAME_SIZE = 11
   f. I2C_TRANSFER = 1
6. Reading of the received message (first four bytes)
   a. I2C_DATA_IN_7_0: first byte to receive
   b. I2C_DATA_IN_15_8: second byte to receive
   c. I2C_DATA_IN_23_16: third byte to receive
   d. I2C_DATA_IN_31_24: fourth byte to receive.

7. Launching of the trigger to start READ (fifth byte)
   a. I2C_STOP_AFTER_NACK = 0
   b. I2C_FORCE_NACK = 0
   c. I2C_RD_WRN = 1
   d. I2C_OP_CODE = 011
   e. I2C_FRAME_SIZE = 00
   f. I2C_TRANSFER = 1
8. Reading of the received message (fifth byte)
   a. I2C_DATA_IN_7_0: fifth byte to receive
9. Checking of communication
   a. If the I2C_TX_ERR flag is asserted, the data has not been sent correctly on the SDA.
   b. If I2C_RX_ACK_ERR flag is asserted, an error in the receiver acknowledgment occurred.

5.10 Communicating with the BMS controller

5.10.1 Physical layer

The BMS controller can access the device registers using two physical communication interfaces:

- Isolated Vertical Interface (VIF)
  - This interface is typically used when the IC is daisy-chained on the VIF bus along with other companion ICs. The BMS controller is typically placed in a different voltage domain and needs an isolated communication interface to access each target on the VIF bus.
- SPI target
  - This interface is typically used when the IC operates in a standalone application (e.g. 48 V systems) along with the MCU which is local to the ECU.

When the SPI target is selected, in case one of the following errors occurs, the corresponding bit will be set in the SPI error frame:

1. ADDR: in case the previous MOSI was specifying an inexistent address field, the WRONG_ADDR latch is set
2. WRONG VIF ID: see Table 66 for a list of fault cases handled by this bit. All these lead to the VIF_ID_ERR latch being set.
3. LONG: in case the previous MOSI was longer than 40 bit, the LONG_FRAME latch is set
4. SHORT: in case the previous MOSI was shorter than 40 bit, the SHORT_FRAME latch is set
5. CRC ERR: in case the previous MOSI was corrupted and a wrong CRC has been decoded, the COMM_CRC_ERR latch is set

Note: These errors will be set by any device on the daisy chain, regardless of its VIF_ID.

However, VIF and SPI are considered mutually exclusive during normal operation. After the first IC configuration, only one interface shall be left enabled.

The IC does not manage concurrent access to registers via both physical layers, as there is no arbitration/ semaphore mechanism. As such, using the two interfaces simultaneously may result in unpredictable behavior and is not recommended.

Note: If GPIO0_NCS0 is pulled up to V5V, at first power-up with the device not yet configured, a communication error could be set in the COMM_ERR register during V5V ramp-up. For this reason, after completing the addressing procedure, eventual spurious communication errors shall be cleared reading the COMM_ERR register.

5.10.1.1 Isolated Vertical Interface (VIF)

The IC integrates two isolated communication ports (ISOH and ISOL) allowing to stack up to N_{VIF_STACK} devices in daisy chain.

The VIF supports both capacitive and transformer-based isolation. The architecture supports a dual ring-shaped daisy-chain in order to be robust against a single open failure on the VIF harness.

Each port features two VIF receivers:

- A wake-up receiver that senses and decodes FAULT/WAKEUP and CYCLIC WAKEUP tones
- A main receiver that senses and decodes functional VIF frames in NORMAL state

They are enabled according to the following logic:

Table 52. VIF receiver enable conditions

FSM_STATE	Wakeup RX	Main RX
DEEP SLEEP/SILENT BALANCING	Used	Disabled
CYCLIC WAKEUP	Not used	Used
NORMAL	Not used	Used

The ISOH and ISOL transmitters are enabled based on several conditions, listed in the following tables.

Table 53. **ISOH transmitter (TX) interface enable conditions**

Device VIF_ID	FSM_STATE	ISOH_TX_EN	ISOH TX enable state	Note
0	X	X	Disabled	Needed to perform the addressing procedure
X	DEEP SLEEP/SILENT BALANCING	X	Disabled	
X	CYCLIC WAKEUP	X	Enabled	The passthrough between ISOL/ISOH is disabled.
≠0	NORMAL	0	Disabled	
≠0	NORMAL	1	Enabled (default at POR_MAIN)	

The following table summarizes the enable state of the ISOL transmitter interface.

Table 54. **ISOL transmitter (TX) interface enable conditions**

FSM_STATE	ISOL_TX_EN	ISOL TX enable state	Note
DEEP SLEEP/SILENT BALANCING	X	Disabled	
CYCLIC WAKEUP	X	Enabled	The passthrough between ISOL/ISOH is disabled.
NORMAL	0	Disabled	
NORMAL	1	Enabled (default at POR_MAIN)	

The MCU may selectively enable/disable the ISOL/ISOH transmitters in order to implement dual access commands (refer to Single/dual access commands).

In an ISO port, both positive and negative terminals are biased to a V_{VIF_CM} common-mode voltage. The information resides in the differential signal propagating along the twisted pair used to interconnect the stacked nodes. The proprietary protocol adopts the following encoding logic, where each bit lasting T_{VIF_BIT} is decoded observing differential signal transitions:

- A negative to positive transition indicates a logic ‘0’
- A positive to negative transition indicates a logic ‘1’

The TX circuit has an $R_{TX\_DIFF\_OUT}$ differential output impedance and shall be terminated using R_{TERM} resistors.

Signals at the ISO port terminals shall be in the V_{VIF_CM} +/- (V5V/2) range in order to be correctly decoded by the RX circuit.

Additional external components like D_{TVS}, R_{VIF_FIL} and C_{VIF_FIL} are needed in order to withstand hotplug and pass BCI trials.

5.10.1.1.1 Monodirectional/bidirectional answers

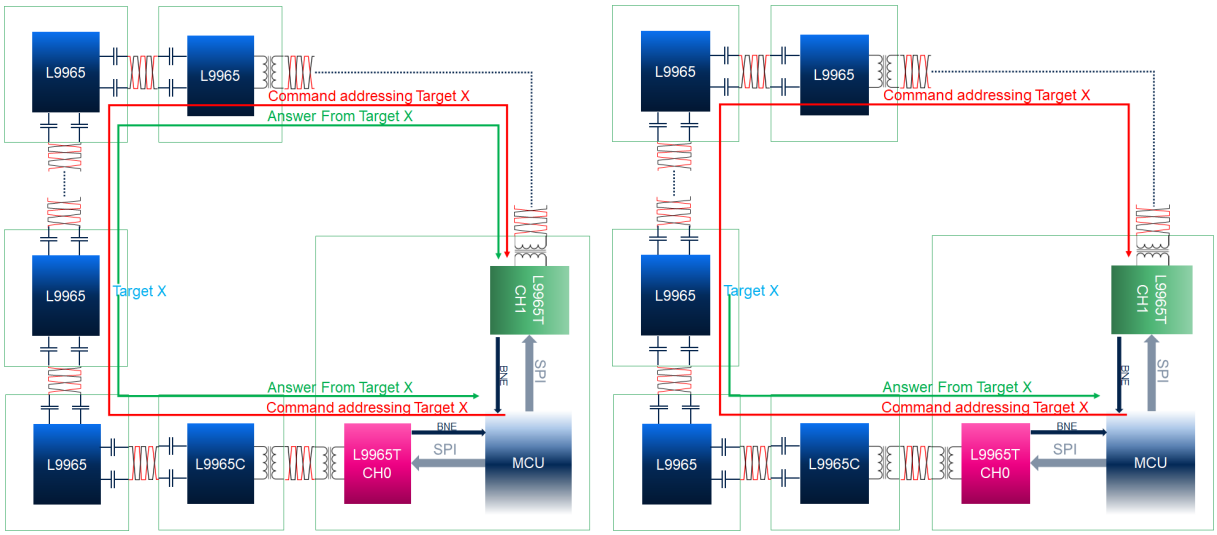
When answering commands, the IC can be configured to generate either mono or bi-directional answers:

- When BIDI_ANSW = 1 (default) the IC generates bi-directional answers on both ISOH and ISOL ports
  - This strategy allows full redundancy of the information on both channels of the L9965T/L99BM2T transceiver
  - It is only meaningful when a dual-ring architecture is put in place

- When BIDI_ANSW = 0, the IC answers using the same ISO port that received the command
  - This strategy is recommended to optimize power consumption or when dual-ring is not implemented
  - Implementing this strategy is mandatory when doubling the data rate through simultaneous north/south access (refer to Single/dual access commands)
  - In order to preserve pack balancing, it is recommended to swap the dual ring access between consecutive sampling & readout routines.
    - For instance, at the n^{th} thread tick time, the user SW sends a broadcast conversion command from the south side, and performs the data readout procedure by always accessing the dual ring from the south side
    - At the $n+1^{th}$ thread tick time, the user SW sends a broadcast conversion command from the north side, and performs the data readout procedure always accessing the dual ring from the north side

This allows for perfect power balancing by equalizing the amount of usage of each target's transmitters.

Figure 16. Left: bidirectional answer; right: monodirectional answer



5.10.1.1.2 Single/dual access commands

When the VIF bus consists in a dual ring, the architecture is designed to allow simultaneous access from the north/south side of the ring, thus enabling double data-rate.

As shown in Figure 17, the ring can be cut into two halves by disabling the transmitters between the X and the $X+1^{th}$ targets. This allows commands to be sent simultaneously from the south and north sides without creating conflicts.

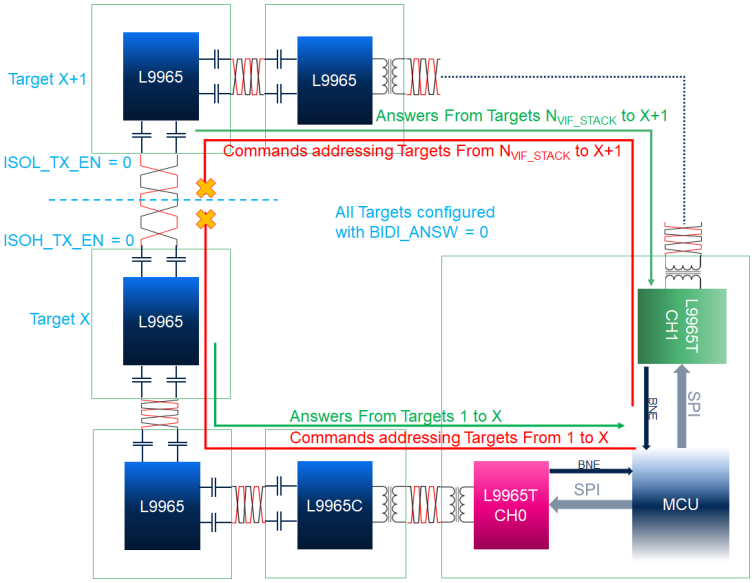
Having also configured the devices for monodirectional answers (BIDI_ANSW = 0, see Monodirectional/bidirectional answers), the different target answers will simultaneously return to both sides of the dual ring and the MCU will be able to retrieve the data from the corresponding RX queues of L9965T/L99BM2T.

This strategy allows the data-rate to be doubled by maximizing the channel usage, thus enabling running conversion & readout threads with half the tick time.

As a minor drawback, a little unbalancing between packs may arise due to the different utilization of the transmitter between targets. For instance, when Target X answers, all targets below it will re-transmit the frame in pass-through mode. However, when the Target X-1 answers, the Target X will not be propagating the answer since the system works in monodirectional mode. Hence, the TX duty of the Target X will be reduced compared to the TX duty of the Target X-1. This unbalancing can be effectively recovered through a pack balancing strategy.

Note: To allow safe fault propagation in bidirectional mode and correct execution of the cyclic wake-up strategy, transmitters are always re-enabled every time the IC transitions to CYCLIC WAKEUP or NORMAL. Hence, once the BMS controller wakes up the system, the daisy-chain always needs to be re-split into two halves before running the threads in dual access mode. This operation is quick and only requires two additional ISO frames.

Figure 17. **Double data rate using dual access commands**



5.10.1.1.3 Electrical parameters

Table 55. **VIF electrical parameters**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
N_{VIF_STACK}	Number of addressable devices stacked in a single daisy-chain (including L9965T/L99BM2T, L9965C)	Application information. There are 64 available addresses, 5 of which are reserved for broadcast commands	1		59	-	ISOx
L_{VIF_WIRE}	Maximum length of twisted pair cables between two VIF nodes, using the recommended AWG_{VIF_WIRE} size and supporting operation in high frequency	Application information			10	m	ISOx
V_{VIF_VCM}	ISO port positive/negative terminals common-mode voltage	Tested in production	0	V5V/2	V5V	V	ISOx
$V_{TX\_DIFF\_OUT}$	TX output differential pulse	Tested in production using recommended R_{TERM}	0		V5V	V	ISOx
T_{VIF_BIT}	VIF bit time	Guaranteed by SCAN	230	250	270	ns	ISOx
$T_{VIF\_LATENCY}$	VIF insertion delay. Latency introduced by the insertion of one IC in the daisy-chain	Guaranteed by SCAN	115	125	135	ns	ISOx
$T_{VIF\_ANSW\_DELAY}$	VIF answer delay. Time interval between receipt of the last command bit and the generation of the 1st answer bit	Guaranteed by SCAN	8.1	8.8	9.5	us	ISOx
$T_{VIF\_RX\_IDLE\_TIMEOUT}$	VIF RX IDLE condition timeout	Guaranteed by SCAN	1.725	1.875	2.025	us	ISOx
$V_{RX\_DIFF\_TH\_POS}$	RX differential threshold positive	Tested in production	80	200	400	mV	ISOx
$V_{RX\_DIFF\_TH\_NEG}$	RX differential threshold negative	Tested in production	-400	-200	-80	mV	ISOx
$R_{RX\_DIFF\_IN}$	RX differential input impedance	Tested in production	15	40	60	Ω	ISOx

5.10.1.2 *SPI target*

The IC integrates an SPI target peripheral to be used as a standalone device in systems where pack voltage does not exceed 60 V. When galvanic isolation is not needed, the IC can be directly driven by an MCU via SPI.

By default, at the first power-up, the following pins are configured as SPI target:

- GPIO0_NCS0 → Chip select (digital input, weak pullup $R_{GPIO\_WK\_PU}$)
- GPIO2_SDI → Serial data input (digital input, weak pull-down $R_{GPIO\_WK\_PD}$)
- GPIO3_SDO → serial data output (digital output)
  - The output buffer is connected to 5V LDO (V5V)
- GPIO4_SCLK → Serial clock (digital input, weak pull-down $R_{GPIO\_WK\_PU}$)

The MCU cannot disable this peripheral inadvertently, since any attempt to write the SPI_MODE field from the SPI target peripheral will be ignored.

The SPI_MODE setting is also retained in DEEP SLEEP.

Table 56. SPI target quick look

Parameter	Description
Protocol	Out of frame
Single frame length	40 bit
Frame protection	6 bit CRC
Max. frequency	2 MHz
CPOL	0
CPHA	1

5.10.1.2.1 Electrical parameters

Figure 18. SPI target timing diagram

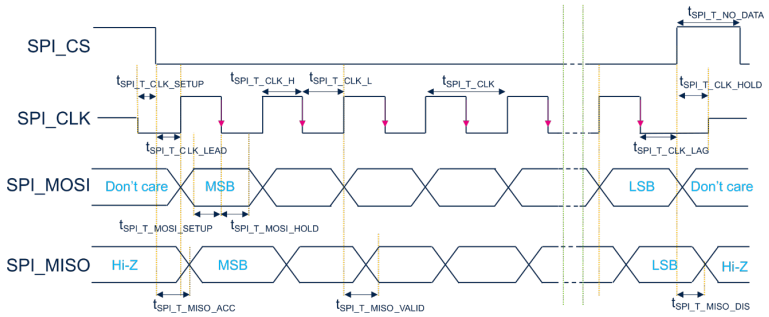


Table 57. SPI target electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
$f_{SPI\_T\_CLK}$	CLK frequency (50% duty cycle)	Application info			2	MHz	GPIO4_SCLK
$t_{SPI\_T\_CLK\_L}$	Time interval for CLK = LOW	Application info	210			ns	GPIO4_SCLK
$t_{SPI\_T\_CLK\_H}$	Time interval for CLK = HIGH	Application info	210			ns	GPIO4_SCLK
$t_{SPI\_T\_MISO\_VALID}$	Propagation delay (time elapsed after propagating SCK edge @ at SDO active)	Cload = 60pF			150	ns	GPIO3_SDO, GPIO4_SCLK
$t_{SPI\_T\_CLK\_LEAD}$	Time elapsed after NCS H/L edge @ first SCK edge	Application info	200			ns	GPIO0_NCS0, GPIO4_SCLK
$t_{SPI\_T\_MOSI\_SETUP}$	SDI input setup time (time before sampling SCK edge SDI must keep stable)	Application info	50			ns	GPIO2_SDI, GPIO4_SCLK

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
$t_{SPI\_T\_MOSI\_HOLD}$	SDI input hold time (time after sampling SCK edge SDI must keep stable)	Application info	50			ns	GPIO2_SDI, GPIO4_SCLK
$t_{SPI\_T\_CLK\_LAG}$	Time passed after CLK -> CPOL @ NCS L/H edge	$f_{SPI\_T\_CLK}$ = 2 MHz	200			ns	GPIO0_NCS0, GPIO4_SCLK
$t_{SPI\_T\_NO\_DATA}$	NCS min high time	$f_{SPI\_T\_CLK}$ = 2 MHz	8.25			µs	GPIO0_NCS0,
$t_{SPI\_T\_MISO\_DIS}$	NCS L/H to SDO @ high impedance	$f_{SPI\_T\_CLK}$ = 2 MHz Cload = 60pF			100	ns	GPIO0_NCS0, GPIO3_SDO
$t_{SPI\_T\_MISO\_ACC}$	NCS H/L to SDO active	$f_{SPI\_T\_CLK}$ = 2 MHz Cload = 60pF			100	ns	GPIO0_NCS0, GPIO3_SDO
$t_{SPI\_T\_CLK\_HOLD}$	Time elapsed after CLK -> CPOL @ NCS L/H edge		100			ns	GPIO0_NCS0, GPIO4_SCLK

5.10.2 Protocol layer

This section defines the communication protocol layer. The protocol is 40 bit, out of frame.

Small differences depending on the chosen physical layer (Isolated Vertical Interface (VIF) or SPI target) are also highlighted in the following paragraphs.

5.10.2.1 Single read/write

The following table describes the protocol for managing single read/write commands.

All registers of the IC can be accessed by performing single read/write operations.

Table 58. Single read/write frame format

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	P.A = 1	R/W	DEV_ID						ADDRESS							RSVD	DATA WRITE																				CRC					
MISO	P.A = 0	Burst=0	DEV_ID						ADDRESS FEEDBACK							FAULT	DATA READ																				CRC					

In the following table, all fields of the MISO/MOSI frame are described:

Table 59. Read/write frame fields

Field	Size [bit]	Description	Value
P.A.	1	Used to distinguish between a command sent by the BMS controller and an answer coming from a target unit	0 = Answer 1 = Command
R/W	1	Used to distinguish between read/write operations	0 = Read 1 = Write
DEV_ID	6	Identifies the target unit address in the daisy chain. Also used for broadcast commands.	[0-63]
ADDRESS / ADDRESS FEEDBACK	7	Identifies the register address for the read/ write operation. Used also for burst commands.	[0-127]
RSVD	1	Reserved for MOSI	X
FAULT	1	Global status bit asserted when the device has self-detected a fault	See Table 60
DATA WRITE	18	Specifies the register content to be written in write operations. Don't care in read operations	Read: X

Field	Size [bit]	Description	Value
			Write: [0 to 2^{18}-1]
DATA READ	18	Returns the register content in both read/write operations	[0 to 2^{18}-1]
CRC	6	Checksum sized for high coverage (hamming distance ≥ 3)	[0-63]

In the following table, all self-detected faults that assert the FAULT bit of the MISO frame are listed:

Table 60. FAULT bit

Macro failure group	Sub failure group	Register map field
VCR failures	Diagnostic on conversion failures	VCR_FAIL VBS_OV VBS_UV VBS_SUM_FAIL VCELL<X>_BAL_UV VCELL<X>_OV VCELL<X>_UV VCELL_DELTA_NORMAL SUM_OV SUM_UV BB_OV NTC_OT_GPIO_UV<X> NTC_UT_GPIO_OV<X> NTC_FASTCHG_OT_GPIO_WARN_UV<X> NTC_DELTA_NORMAL
	CYCLIC WAKEUP failures	VCELL<X>_DELTA NTC_DELTA_GPIO_DELTA_<X>
	Open failures	AFE_DIAG<X> SFIRST_OPEN GPIO<X>_OPEN BB_OPEN
	BIST failures	BIST<X>_FAIL BIST_BB_FAIL BIST_VB_FAIL BIST_ANALOG_COMP_FAIL CLK_MON_SELFTEST_FAIL TEMP_INT_RED_ERR GAIN_INT_RED_ERR
Digital safety failures	-	NVM_CRC_CFG_FAIL NVM_CRC_TRIM_CAL_FAIL CYC_CFG_CRC_FAIL CYC_TRIM_CRC_FAIL RAM_ECC_FAIL OSCI_FAIL
Communication failures	-	COMM_CRC_ERR

Macro failure group	Sub failure group	Register map field
		LONG_FRAME SHORT_FRAME WRONG_ADDR VIF_ID_ERR I2C_RX_ACK_ERR I2C_TX_ERR
Die thermal failures	-	TJ_SD TJ_WARN
Power failures	-	VCP_UV V5V_OV V5V_UV VANA_OV VANA_UV VPRE_OV VPRE_UV GND_LOSS_PGND
Balancing overcurrent failures	-	BAL<X>_OC

5.10.2.2 *Broadcast write*

Broadcast write commands allow simultaneous write operations to be performed on all devices or a subset.

The MCU can exploit different kinds of broadcast commands by programming the “VIF ID” field of the MOSI (refer to Table 58). Every IC is sensitive to the following types of broadcast commands:

- *Global broadcast*
  - Purpose: for addressing, writing common configurations and executing common tasks for all devices in the stack
  - DEV_ID = 0x0
- *Selective broadcast*
  - Purpose: for writing common configurations and executing common tasks for a specific subset of devices in the stack
  - DEV_ID = 0x3C + BROADCAST_SEL<x>
  - BROADCAST_SEL<x> is a 2-bit field allowing to configure a specific address filter
  - Two selective broadcast filters have been implemented

If the DEV_ID field of the frame is equal to a global or selective broadcast filter, the IC will accept the frame and execute the write operation. Otherwise, the frame content will be discarded and only used to refresh the communication timeout (COMM_TIM).

The IC generates no answer upon receipt of broadcast commands.

Table 61. Broadcast write frame format

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	PA = 1	R/W = 1	DEV_ID						ADDRESS							RSVD	DATA WRITE																				CRC					

Using broadcast commands is only meaningful when the IC is stacked in a daisy chain and accessed via the Isolated Vertical Interface (VIF). Nevertheless, to ensure SW portability, broadcast commands are also accepted by the SPI target.

As reported in Table 61, broadcast commands generate no answer on the Isolated Vertical Interface (VIF).

Burst read

To enable quick data retrieval, the IC implements a flexible burst read mode available only on the Isolated Vertical Interface (VIF). Burst packets can be requested as follows:

- Performing a read access to register address 0x6A (see Single read/write)
- Specifying the BURST_MODE
  - BURST_MODE = 0 selects the standard burst
    - The IC will shift out a flexible number of registers, starting at the BURST_OFF address and ending at the BURST_OFF + BURST_WD address
    - This strategy can be used to quickly retrieve diagnostic and configuration data
  - BURST_MODE = 1 selects the compressed burst
    - The IC will answer with the compressed packet shown in Table 62.
    - This strategy is recommended to achieve a high data rate with negligible impact on the power consumption. It enables very fast conversion & readout threads, while still maintaining power consumption low, due to the reduced VIF transmitter duty-cycle.
    - The compressed packet answer size is variable and depends on the following parameters:
      - Number of enabled cells and GPIOs
      - Additional inputs enabled (VBS and BBx)
      - Maximum cell voltage imbalance
      - Maximum temperature imbalance

The packet becomes very efficient when cell voltage and temperature are balanced, since the delta data to be transmitted is very small.

Broadcast burst reads are not supported.

5.10.2.3 *Compressed burst*

Compressed burst is designed to optimize data read out via the VIF protocol after an SOC command in NORMAL state.

When a compressed burst is requested after an SOC command, the device provides ADC results according to actual configuration (enable for cells and configuration for GPIOs) as follows:

- Compression data is properly performed according to delta among cells and GPIOs.
- Busbar and VBS monitor measurements, if enabled, are properly provided.
- D RDY (Cx, BB, VBS) and D RDY (GPIOx) will be 1 (and then cleared for all read data) if, for each group, at least an ADC is enabled and new data have not been read yet.
- Each GPIO is considered enabled if GPIOx_CONF = 00,01 (considering SPI_MODE with higher priority), NTC<x>_DELTA_MSK = 0 and TEMP_CONV/ABS_CONV/RATIO_CONV during last SOC command.

However, it is possible to also exploit compressed burst to read starting values before first SOC after the device moves to NORMAL state.

In case the device moves from DEEP SLEEP or SILENT BALANCING to NORMAL and a compressed burst is requested without a new SOC first, the device provides previous measurements (related to the last CYCLIC WAKEUP or NORMAL) according to the actual configuration (enable for cells and configuration for GPIOs) and the following points:

- No compression is performed and therefore delta data are computed with a minimum value equal to 0.
- Busbar and VBS monitor measurements, if enabled, are not provided and data will be 0 (aligned to their SPI registers).
- D RDY (Cx, BB, VBS) will be 0, whereas D RDY (GPIOx) may be 1 if no last data have been read (not included ones related to last CYCLIC WAKEUP).
- Each GPIO is considered enabled if GPIOx_CONF = 00,01 (considering SPI_MODE with higher priority) and NTC<x>_DELTA_MSK = 0, regardless of ABS_CONV and RATIO_CONV.

In case the device moves from CYCLIC WAKEUP to NORMAL for a fault detection and a compressed burst is requested without a new SOC first, the device provides previous measurements (related to the last CYCLIC WAKEUP) according to the actual configuration (enable for cells and configuration for GPIOs) and the following points:

- Compression is properly performed according to delta among cells and GPIOs.
- Busbar and VBS monitor measurements, if enabled, are properly provided.
- D RDY (Cx, BB, VBS) and D RDY (GPIOx) will be 1 (and then cleared for all read data) if, for each group, at least an ADC is enabled.
- Each GPIO is considered enabled if GPIOx_CONF = 00,01 (considering SPI_MODE with higher priority) and NTC<x>_DELTA_MSK = 0, regardless of ABS_CONV and RATIO_CONV.

If a compressed burst is requested with all cells, GPIOs, busbar and VBS disabled (or masked in case of cells or GPIOs), only a part of header is transmitted. In this atypical scenario, the L9965T/L99BM2T will properly receive the short burst, but no data will be written into the FIFO.

Table 62. Burst read packet format

FIELD	P.A.	BURST	VIF ID	CELLS EN(1)	BB EN	VBS EN	GPIO EN	D RDY (Cx, BB, VBS)	D RDY (GPIOx)	ΔC WDTH(1)	ΔG WDTH	MIN C(2)	MIN GPIO(2)	FAULT	ΔC1 (1)(3)	ΔC[2...17](3)(1)	ΔC18(3)(1)	BUSBAR(3)	VBS(3)	ΔG1(4)	ΔG[2...8](4)	ΔG9(4)	CRC
WIDTH	1	1	6	18	1	1	10	1	1	4	4	16	15	1	ΔC WDTH	ΔC WDTH	ΔC WDTH	16	16	ΔG WDTH	ΔG WDTH	ΔG WDTH	10
VALUE [dec]	0	1	[1-63]	[0-262143]	[0-1]	[0-1]	[0-1]	[0-1]	[0-1]	[1-16]	[1-16]	[0-65535]	[0-32767]	[0-1]	[0-$2^{\Delta C\ WDTH}$-1]	[0-$2^{\Delta C\ WDTH}$-1]	[0-$2^{\Delta C\ WDTH}$-1]	[0-65535]	[0-65535]	[0-$2^{\Delta G\ WDTH}$-1]	[0-$2^{\Delta G\ WDTH}$-1]	[0-$2^{\Delta G\ WDTH}$-1]	[0-1023]

1. *Cells configured as busbar (VCELL<x>_BB = 1) will not be included in the compressed packet, and formatted in the same way as in single read/write, they will be treated as disabled. They shall be downloaded separately. Their data-ready bit will not be used to compute the "D RDY (Cx,BB,VBS)" field.*
2. *Field transmitted only if at least one cell/GPIO is enabled.*
3. *Field transmitted only if corresponding cell/VBS/busbar is enabled.*
4. *Field transmitted only if corresponding GPIO is enabled. If a GPIO is used as balancing resistor monitor, so that NTC<x>_DELTA_MSK = 1, its measurement data will not be part of the burst packet: it will be treated as a disabled GPIO from the information compressor.*

The L9965T/L99BM2T companion chip already features the decompressor, thus freeing the MCU from implementing complex routines to recover original cell/temperature/pack/busbar data. Information will be presented to the MCU MISO.

5.10.2.4 *Special frames*

This section lists the special frames associated with specific events.

Table 63. Special frames on the Isolated Vertical Interface (VIF)

Frame	Description	IC STATE	IC reaction upon frame receipt
0x0 (longer tone)	FAULT/WAKEUP tone. Can be sent by the MCU simultaneously on both daisy-chain ends to wake up the ICs. It will only be propagated by the L9965T/L99BM2T operating in SENDER mode. Can be autonomously sent by an IC that has self-detected a failure in SILENT BALANCING or CYCLIC WAKEUP operation. This tone is not a functional packet and does not encode any meaningful data. It is characterized by a different number of bit and a different frequency.	NORMAL	Tone is propagated on the opposite VIF port. Communication timeout (COMM_TIM), if running, is restarted.
		CYCLIC WAKEUP	The device moves to NORMAL within T_{VIF_WAKEUP} and tone is propagated on the opposite VIF port. Communication timeout (COMM_TIM) is restarted. The cyclic wakeup routine still runs in the background until the end; if a fault is latched, no further FAULT/WAKEUP tones will be sent.
		SILENT BALANCING	The device moves to NORMAL within T_{VIF_WAKEUP} and tone is propagated on the opposite VIF port.
		DEEP SLEEP	The device moves to NORMAL within T_{VIF_WAKEUP} and tone is propagated on the opposite VIF port.
0x0 (shorter tone)	CYCLIC WAKEUP tone. Can be autonomously sent by the L9965T/L99BM2T transceiver when in CYCLIC WAKEUP state. This tone is not a functional packet and does not encode any meaningful data. It is characterized by a different number of bit and a different frequency.	NORMAL	Tone discarded.
		CYCLIC WAKEUP	Tone discarded.
		SILENT BALANCING	The device moves to CYCLIC WAKEUP within T_{VIF_WAKEUP} (tone propagation depends on the cyclic wakeup routine outcome).
		DEEP SLEEP	The device moves to CYCLIC WAKEUP within T_{VIF_WAKEUP} (tone propagation depends on the cyclic wakeup routine outcome).
Functional frame (see Table 58)	Functional R/W frame.	DEEP SLEEP / SILENT BALANCING / CYCLIC WAKEUP	The device moves to NORMAL within T_{VIF_WAKEUP} and a longer tone is propagated on the opposite VIF port.
		NORMAL	Frame decoded. Communication timeout (COMM_TIM), if running, is restarted.

Table 64. Special frames on SPI target

Frame	Description	IC STATE	IC reaction upon frame receipt
Functional frame (see Table 58)	Functional R/W frame.	DEEP SLEEP / SILENT BALANCING / CYCLIC WAKEUP	The device moves to NORMAL within T_{VIF_WAKEUP}.
		NORMAL	Frame decoded. Communication timeout (COMM_TIM), if running, is restarted.
0x10	Default frame. Since the protocol is out of frame, this is the first answer issued by the IC after a wakeup condition moves it to NORMAL.	NORMAL	NA (this is an answer frame)
SPI ERROR frame (See Table 65)	SPI ERROR frame. Issued by the IC when a wrong MOSI has been received on the SPI target.	This frame will not travel on the Isolated Vertical Interface (VIF), since it is only generated by the SPI target.	

Table 65. SPI error frame

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	PA = 0	Burst=0	Dev ID = 0x0					ADDRESS FEEDBACK = 0x7F							FAULT	0x0													WRONG VIF ID	WRONG ADDR	LONG	SHORT	CRC ERR	CRC					

When the SPI target is being used, if any of the following errors occurs, the corresponding bit will be set in the SPI error frame:

- WRONG ADDR: the previous MOSI was specifying an inexistent address field
  - WRONG_ADDR latch set
- WRONG VIF ID: see Table 66 for a list of fault cases handled by this bit
  - VIF_ID_ERR latch set
- LONG: the previous MOSI was longer than 40 bit
  - LONG_FRAME latch set
- SHORT: the previous MOS was shorter than 40 bit
  - SHORT_FRAME latch set
- CRC ERR: the previous MOSI was corrupted (wrong CRC decoded)
  - COMM_CRC_ERR latch set

Note: These errors will be set by any device on the daisy chain, regardless of its VIF_ID.

5.10.2.5 *Addressing procedure*

As explained in Isolated Vertical Interface (VIF), after the first power-up, every device holds an address (VIF_ID) equal to 0x0 (see Section 5.10.2.1) and starts with the ISOH transmitter disabled (ISOH_TX_EN = 0).

To allow a correct addressing procedure, all the ICs in the daisy chain shall be oriented with the ISOH port connected to the ISOL port of the upper device.

The BMS controller shall access the daisy chain from the bottom-side and the following procedure shall be put in place to perform daisy chain addressing:

Procedure 8: VIF addressing

1. For x = 1 to N_{VIF_STACK}
   a. Send a broadcast command with DEV_ID = 0 to disable the configuration integrity check (CONF_CRC). The command will only reach up to the x-th device of the chain and will not be propagated to upper devices since the x-th device has the ISOH transmitter disabled.
   b. Send a broadcast command with DEV_ID = 0 to remove the configuration lock.
   c. Send an SPI frame with DEV_ID = 0 to program the desired VIF_ID value. Now, any command will also reach the x+1st device (which is still holding VIF_ID = 0)
   d. (optional, for L9965A/L99BM218 BMIC only) Send an addressed write command with DEV_ID = x to program the mailbox BROADCAST_SEL<x> shared by every BMIC device (e.g. BROADCAST_SEL_0 = 0x1)
   e. To enable selective broadcast, send an SPI frame with DEV_ID = VIF_ID to write the BROADCAST_SEL register with values matching those programmed in the IC in the chain that will be addressed by broadcast communication (L9965A/C or L99BM218/2C) (e.g. BROADCAST_SEL_1 = 0x3)
2. Finalization
   a. Send a broadcast command with DEV_ID = 0 to push the configuration in the NVM using a write command (see NVM read/write operations)
   b. Send a broadcast command with DEV_ID = 0 to reapply the configuration lock
   c. Send a broadcast command with DEV_ID = 0 to re-enable the configuration integrity check (CONF_CRC)

Once a device has been addressed with a DEV_ID different than the default (0x0), the VIF_ID field is no longer writable using global broadcast commands (DEV_ID = 0x0). This avoids inadvertent change to the VIF_ID while performing the addressing procedure.

Table 66. Behavior according to DEV_ID

SPI MODE			
Device VIF_ID	**Received frame DEV_ID**	**READ CMD behavior**	**WRITE CMD behavior**
0	0	Discard cmd and answer with VIF_ID error frame	Perform WRITE operation and answer with updated reg content
0	≠0	Discard cmd and answer with VIF_ID error frame	Discard cmd and answer with VIF_ID error frame
≠0	0	Discard cmd and answer with VIF_ID error frame	Perform WRITE operation and answer with updated reg content
≠0	Device VIF_ID	Perform READ operation and answer with reg content	Perform WRITE operation and answer with updated reg content
≠0	Nonmatching device VIF_ID	Discard cmd and answer with VIF_ID error frame	Discard cmd and answer with VIF_ID error frame
≠0	≠0 (matching mailbox)	Discard cmd and answer with VIF_ID error frame	Perform WRITE operation and answer with updated reg content

VIF MODE			
Device VIF_ID	**Received DEV_ID**	**DEV_ID CMD behavior**	**WRITE CMD behavior**
0	0	Discard cmd and no answer (no passthrough since ISOH is disabled)	Perform WRITE operation and no answer (no passthrough since ISOH is disabled)
0	≠0	Discard cmd and no answer (no passthrough since ISOH is disabled)	Discard cmd and no answer (no passthrough since ISOH is disabled)
≠0	0	Discard cmd and no answer (passthrough if ISOH is enabled)	Perform WRITE operation and no answer (passthrough if ISOH is enabled)
≠0	Device VIF_ID	Perform READ operation and answer with reg content (passthrough if ISOH is enabled)	Perform WRITE operation and answer with updated reg content (passthrough if ISOH is enabled)
≠0	Nonmatching device VIF_ID	Discard cmd and no answer (passthrough if ISOH is enabled)	Discard cmd and no answer (passthrough if ISOH is enabled)
≠0	≠0 (matching mailbox)	Discard cmd and no answer (passthrough if ISOH is enabled)	Perform WRITE operation and no answer (passthrough if ISOH is enabled)

5.10.2.6 *CRC*

Each frame is equipped with a 6-bit CRC code in order to guarantee information integrity. Whatever physical layer is used for communicating, corrupted commands (identified by P.A = 1, see Section 5.10.2.1) will be discarded and will not refresh the communication timeout (COMM_TIM)

Table 67. SPI target CRC calculation information

Parameter	Value
Length	6 bit
Polynomial	$x^6 + x^5 + x^2 + x + 1$
Seed	0x38

The device answer depends on the physical layer:

- Corrupted frames received on the Isolated Vertical Interface (VIF) will generate no answer.
- Corrupted frames received on the SPI target will result in the SPI ERROR special frame issued on the next iteration.

5.10.3 Communication timeout (COMM_TIM)

The IC features a communication watchdog listening to messages incoming on the Isolated Vertical Interface (VIF) or SPI tTarget.

The watchdog timer is reset at every valid frame detection (correct frame length, no CRC error), regardless of the P.A. bit and DEV_ID (see Table 58)

Any frame recognized as a compressed burst (P.A. = 0 and BURST = 1) will reset the communication timeout after the last bit of the sequence has been detected and the line is assessed idle.

If no valid frame is received for an interval exceeding T_{COMM_TIM}, the COMM_TIM fault is latched, and the IC moves to a low-power state according to the FSM shown in Figure 5.

The communication timeout is enabled by default and can be disabled by programming COMM_TIM_EN = 0, and the value of the watchdog threshold T_{COMM_TIM} can be selected through COMM_TIM_TH. It is mandatory to enable the communication timeout to achieve safety targets at system level.

5.10.3.1 Electrical parameters

Table 68. Communication timeout electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{COMM\_TIM\_00}$	Communication timeout threshold	COMM_TIM_TH = 00		100		ms
$T_{COMM\_TIM\_01}$	Communication timeout threshold	COMM_TIM_TH = 01		500		ms
$T_{COMM\_TIM\_10}$	Communication timeout threshold	COMM_TIM_TH = 10		1		s
$T_{COMM\_TIM\_11}$	Communication timeout threshold	COMM_TIM_TH = 11 (default)		2		s

5.10.4 Fault notification (FAULT)

Self-detected faults are reported by the FAULT bit of the Protocol layer. The FAULT bit being set to ‘1’ indicates that the IC has self-detected a failure.

When in NORMAL state, a device that self-detects a failure does not take over the Isolated Vertical Interface (VIF). The MCU is supposed to poll the device within system FTTI, thus retrieving the fault status.

When in SILENT BALANCING or CYCLIC WAKEUP states, a device that self-detects a failure will behave as follows:

- Moves to NORMAL
- Takes over the Isolated Vertical Interface (VIF)
- Sends a FAULT/WAKEUP tone on both VIF ports
- The IC then waits for $T_{VIF\_RX\_IDLE\_TIMEOUT}$ to allow lower and upper units on the daisy chain to also get to the RX IDLE state.
- Enables the VIF passthrough.

5.10.5 Wakeup functions

The IC can be woken up via communication interfaces. There are three wakeup sources:

- Wakeup via VIF
  - In this scenario, the IC is daisy-chained on the VIF bus along with other companion chips, and can be woken up by special frames received on the Isolated Vertical Interface (VIF)
- Wakeup via SPI target
  - In this scenario, the IC operates in a standalone module (e.g. 48V applications) and it is directly connected to the MCU via SPI target. Therefore, it can be woken up by dummy frames received on the SPI target. This wakeup source is only available when the SPI_MODE field is configured as SPI target
- Self-wakeup
  - In this scenario, the wakeup trigger is generated internally by the IC low-power logic.

As explained in the Physical layer section, the VIF and SPI target interfaces are considered mutually exclusive in application. In case the SPI target is selected as the host communication interface, the Isolated Vertical Interface (VIF) pins shall be managed as explained in the Unused pins section.

Whenever a wakeup source is validated, the wakeup sequence is initiated and shall successfully end within $T_{WAKEUP\_TIMEOUT}$. Otherwise, the IC will return to the previously held low-power state.

5.10.5.1 *Electrical parameters*

Table 69. Global wake-up electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{WAKEUP\_TIMEOUT}$	Timeout for completing the wake-up sequence	Tested by SCAN	20		25	ms

5.10.5.2 *Self-wakeup*

When in SILENT BALANCING the IC is able to detect the balancing overcurrent failure. In case this fault is detected, the IC triggers a self-wakeup in order to perform Fault notification (FAULT). Such a wakeup is accomplished within T_{SELF_WAKEUP}.

When in CYCLIC WAKEUP the IC is able to detect failures depending on the diagnostics performed. At the end of the voltage conversion routine execution, in case a fault is detected, the IC triggers a self-wakeup in order to perform the Fault notification (FAULT).

5.10.5.2.1 Electrical parameters

Table 70. Self-wakeup parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{SELF_WAKEUP}	Self-wakeup latency	From the assertion of a fault in silent balancing to the release of V5V undervoltage			1.8	ms

5.10.5.3 *Wake-up via VIF*

When in low-power modes (DEEP SLEEP, SILENT BALANCING and CYCLIC WAKEUP), the IC is sensitive to wake-up signals incoming on both VIF ports (refer to Special frames).

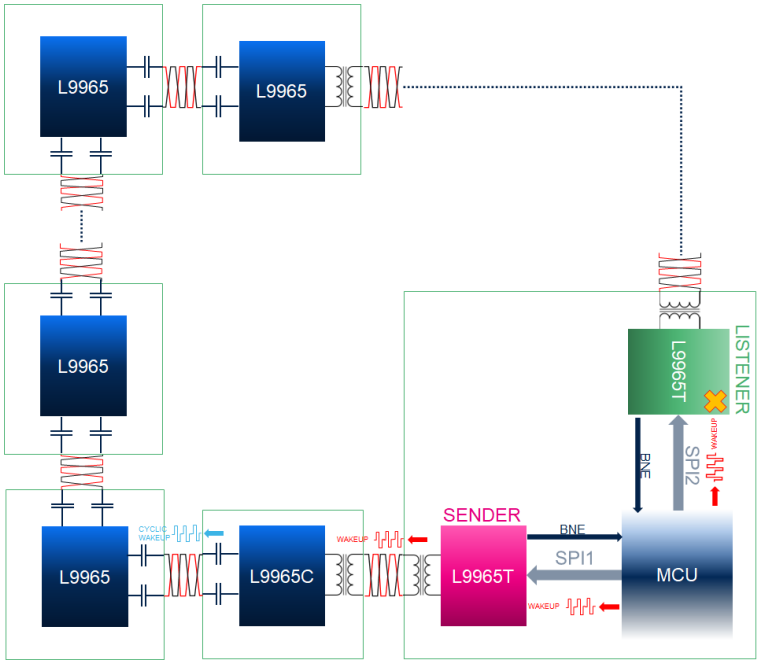
This section explains how the ICs react to wake-up signals in different application conditions. A brief summary of reactions is listed in Table 63.

5.10.5.3.1 Wake-up by MCU

The wake-up by MCU is an asynchronous event in respect to the cyclic wakeup thread managed in the background by the L9965T/L99BM2T. As such, it shall be properly managed in order to avoid conflicts that may prevent a correct system wakeup.

Figure 19 shows a typical application scenario where the MCU wakes up the daisy chain that was previously operating in CYCLIC WAKEUP mode.

Figure 19. Wake-up by MCU



A device generating a CYCLIC WAKEUP tone while a FAULT/WAKEUP tone is incoming on the opposite port will first complete the transmission of the CYCLIC WAKEUP tone, and then schedule the propagation of the FAULT/WAKEUP tone. This is possible since the VIF passthrough is disabled when in CYCLIC WAKEUP state.

Note: If the Communication timeout (COMM_TIM) is enabled, the MCU is supposed to serve it as soon as it receives the wake-up interrupt from the L9965T/L99BM2T. Otherwise, the ICs will go back to low-power state.

5.10.5.3.2 Wake-up by fault

The wake-up by fault is an asynchronous event in respect to the cyclic wakeup thread managed in background by the L9965T/L99BM2T. As such, it shall be properly managed in order to avoid conflicts that may prevent a correct system wake-up.

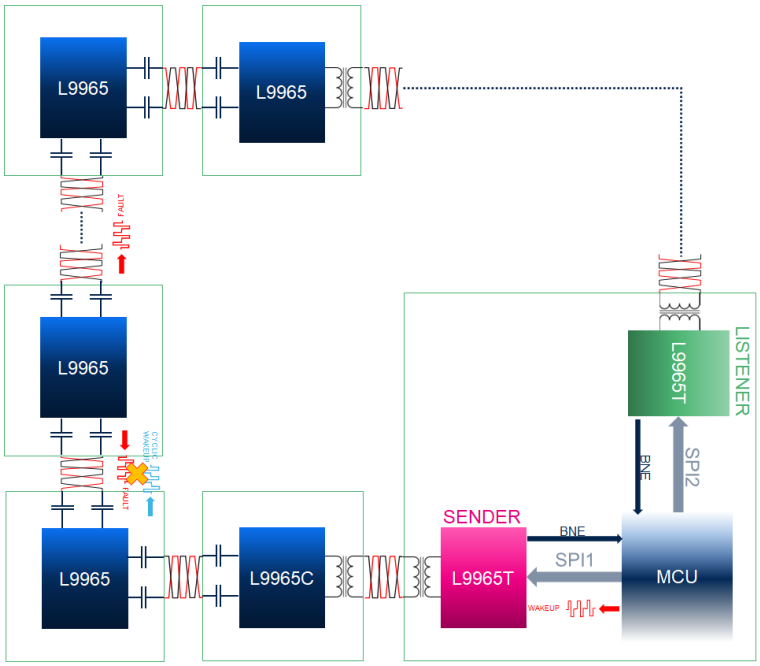
Figure 20 shows a typical application scenario where a BMIC has self-detected a fault and wakes up the daisy chain by sending a FAULT/WAKEUP tone on both VIF ports.

Fault notification (FAULT) has been designed to guarantee that the FAULT/WAKEUP tone is correctly propagated at least in one direction, even in the remote case of a conflict with the CYCLIC WAKEUP tone.

Depending on the position of the affected BMIC in the daisy chain, the wake-up interrupt will reach the MCU in approximately less than $½*N_{VIF\_STACK}*T_{VIF\_WAKEUP}$, but in the worst case it may take up to $N_{VIF\_STACK}*T_{VIF\_WAKEUP}$ to complete whole daisy chain wake-up.

When the MCU is woken up by a L9965T/L99BM2T, it is supposed to wait also for the other L9965T/L99BM2T to generate the BNE interrupt in order to confirm the daisy chain wakeup. If this event does not occur within the $N_{VIF\_STACK}*T_{VIF\_WAKEUP}$ timeout, the MCU shall run the wake-up by MCU procedure.

Figure 20. Wake-up by fault



5.10.5.3.3 Wake-up by CYCLIC WAKEUP

When in low-power modes (DEEP SLEEP or SILENT BALANCING), the IC is designed to support standalone operation without MCU intervention. Such an operating mode is needed to keep monitoring the battery pack even when the system undergoes long periods of inactivity (e.g. vehicle parked and set for holiday mode).

The CYCLIC WAKEUP mode in dual ring configuration has been designed to offer high redundancy, being robust to any single failure point. This enables achieving ASIL D (for L9965A) ratings on monitoring functions even when the BMS is in low-power mode and the MCU is sleeping.

To address the CYCLIC WAKEUP operation mode, the MCU shall:

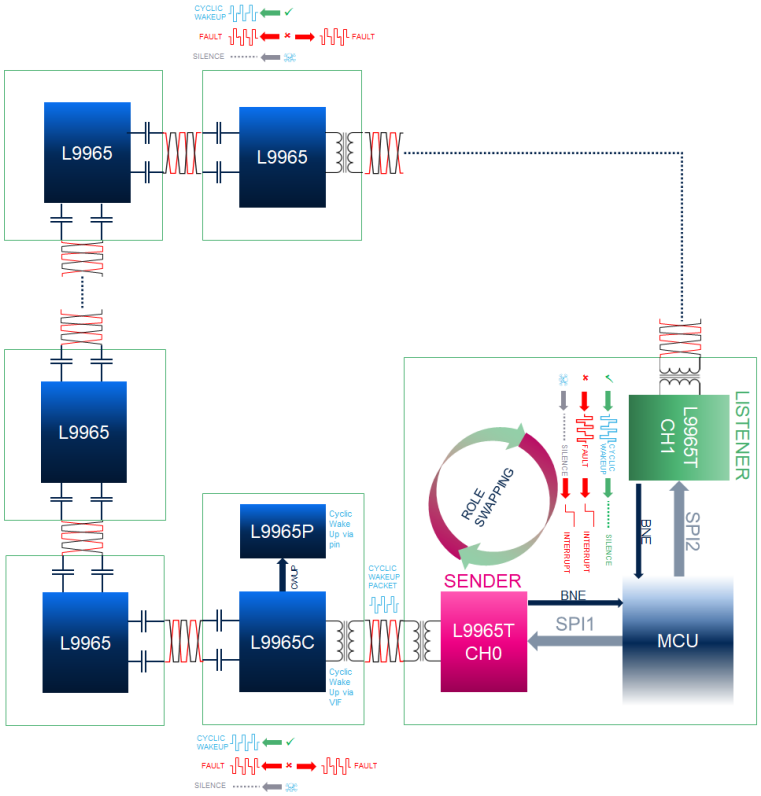
- Command all the ICs to DEEP SLEEP via a global broadcast GO2SLP
- Move the L9965T/L99BM2T transceivers to CYCLIC WAKEUP state simultaneously

In such conditions, the system operates as depicted in Figure 21:

- L9965T/L99BM2T transceivers operate as follows
  - One L9965T/L99BM2T acts as *sender*
    - Depending on the daisy chain configuration, two scenarios are possible
      - If the $T_{CYCLIC\_WAKEUP\_TIMEOUT}$ is disabled (single transceiver scenario), it generates a cyclic wake-up frame every T_{CYCLIC_WAKEUP} period
      - If the $T_{CYCLIC\_WAKEUP\_TIMEOUT}$ is enabled (dual ring scenario), once it expires the transceiver swaps to *listener* mode
    - The transceiver is still sensitive to fault wake-up/wake-up by MCU frames
  - The other L9965T/L99BM2T on the opposite end of the ring acts as *listener*
    - Depending on the daisy chain configuration, two scenarios are possible
      - If the $T_{CYCLIC\_WAKEUP\_TIMEOUT}$ is disabled (single transceiver scenario), the listener mode is disabled
      - If the $T_{CYCLIC\_WAKEUP\_TIMEOUT}$ is enabled (dual ring scenario), L9965T/L99BM2T waits for the receipt of the cyclic wakeup tone
        - If the tone arrives within $T_{CYCLIC\_WAKEUP\_TIMEOUT}$, the “no fault” condition is acknowledged, but the $T_{CYCLIC\_WAKEUP\_TIMEOUT}$ timer is left running. Once it expires, the L9965T/L99BM2T swaps to *sender mode*
        - If the cyclic wake-up tone is not received within $T_{CYCLIC\_WAKEUP\_TIMEOUT}$, the transceiver moves to NORMAL and alerts the MCU via the BNE interrupt pin
    - The transceiver is still sensitive to fault wake-up/wake-up by MCU frames.
- L9965A/L99BM218 BMIC operates as follows:
  - When the cyclic wake-up tone is received on a VIF port, it moves to CYCLIC WAKEUP and performs a complete execution of the Voltage conversion routine (as defined in section Section 5.5)
  - In the duty-phase, the BMIC uses the filter specified by the TVOLT_FIL_WAKEUP field for the VOLT_CONV step. It is recommended to use longer filters during the CYCLIC WAKEUP phase, in order to detect ΔV and ΔT with a higher precision, reducing the noise impact. This is possible since the duty-cycle in the CYCLIC WAKEUP phase is supposed to be really small.
  - When the Voltage conversion routine is over, the ADCs are automatically swapped in order to already be correctly preconfigured for the next wake-up cycle. After that, the outcome of the routine execution is evaluated.
    - In case no failure has been detected, the cyclic wakeup tone is propagated on the opposite VIF port. After that, the BMIC moves back to DEEP SLEEP.
    - In case a failure has been detected, the BMIC stays in NORMAL and sends a fault wake-up tone on both VIF ends.

In case a fault tone is received while in the NORMAL duty-phase, the BMIC propagates the fault tone and cancels the GO2SLP event, thus staying in NORMAL. This allows correct propagation of the fault signal and MCU intervention.

Figure 21. **Cyclic wakeup operation**



5.10.5.3.4 Electrical parameters

Table 71. **VIF wakeup parameters**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{CYCLIC_WAKEUP}	Transceiver cyclic wake-up tone generation period	Sender mode	-	See L9965T/ L99BM2T DS	-	-
$T_{CYCLIC\_WAKEUP\_TIMEOUT}$	Transceiver cyclic wake-up timeout	Listener mode	-	See L9965T/ L99BM2T DS	-	-
T_{VIF_WAKEUP}	IC wakeup latency	From receipt of the 1st bit of the wake-up tone to the propagation of the 1st bit on the opposite VIF port			2	ms

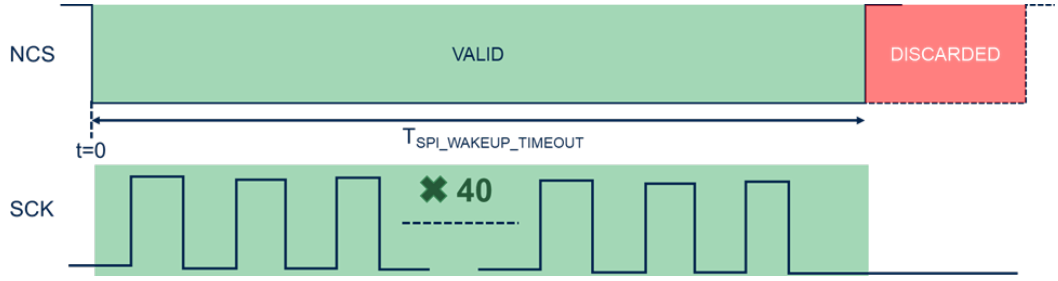
5.10.5.4 *Wake-up via SPI target*

When the SPI target is enabled, the IC can be woken up by any valid SPI frame. A wake-up condition is acknowledged when the following pattern is received:

1. An NCS high-to-ow transition
2. 40 SCK pulses
3. An NCS low-to-high transition

To prevent the logic being stuck in the wake-up detection state upon incomplete patterns, the $T_{SPI\_WAKEUP\_TIMEOUT}$ is started upon every NCS assertion, and the wakeup pattern shall end before timeout expiration, otherwise it will be discarded.

Figure 22. **Wakeup condition by SPI target**



Wake-up frames are not decoded: their content may be arbitrary. However, it is strongly recommended to send READ commands in order to avoid inadvertent write operations in case the device is already awake.

5.10.5.4.1 Electrical parameters

Table 72. **SPI wake-up parameters**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{SPI\_WAKEUP\_TIMEOUT}$	Timeout for receipt of wake-up frame	Tested in production	0.4		2	ms
T_{SPI_WAKEUP}	IC wake-up latency	From the NCS low-to-high transition to the IC in NORMAL state and ready to communicate (V5V_UV released & NVM com sectors downloaded)			2	ms

5.11 Config lock

To prevent inadvertent modification of Safety Relevant Registers (SRR) and Safety Latent Registers (SLR) (highlighted with this color code in the register map), these register map sectors are protected by a lock field.

By default, SRR/SLR registers are locked. To configure the device, the following procedure shall be implemented:

Procedure 9: Configuration lock/unlock

1. MCU writes 0x55 in the SPECIAL_KEY register to enter a partial unlock
   – The $T_{CFG\_TIMEOUT}$ is started
2. The MCU writes 0x33 in the SPECIAL_KEY register to confirm the unlock
3. The MCU changes any configuration register within TCFG_TIMEOUT
4. The MCU reapplies the lock by writing 0xAA in the SPECIAL_KEY
   a. The $T_{CFG\_TIMEOUT}$ is reset and stopped
   b. If the $T_{CFG\_TIMEOUT}$ expires, the lock is automatically reapplied

Trying to write a protected register (SRR or SLR) without unlocking it will result in data being discarded.

Note: Writing lock-protected registers only alters the current configuration loaded in the SPI registers. To save the configuration and guarantee a correct reload at each power-up, the update has to be pushed into the Non-volatile Memory (NVM) as described in the dedicated section.

*Note: For temporary modifications to the IC configuration, which do not need to be pushed into the **Non-volatile Memory (NVM)**, it is recommended to disable the **configuration integrity check (CONF_CRC)**.*

5.11.1 Electrical parameters

Table 73. Configuration timeout

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{CFG\_TIMEOUT}$	Configuration lock timeout	Tested in SCAN		2		s

5.12 Software reset (SW_RST)

It is possible to reset the configuration of the device by sending a SW_RST sequence.

Once triggered, the software reset procedure will reset all SPI registers (including the clear-on-read flags if its set condition is released) to their default values, including the lock-protected ones. Read-only and write-only fields represent exceptions.

To reset the device configuration, the following procedure shall be implemented

Procedure 10: Software reset

1. The MCU writes 0xE1 into the SPECIAL_KEY register to enter partial reset mode
2. The MCU writes 0x1E into the SPECIAL_KEY register to confirm reset

Frames must be sent exactly in this sequence, or registers will not be reset.

User SW can eventually trigger a redownload of the configuration from the NVM.

Since the NVM is redownloaded at each wake-up, the new configuration eventually applied shall be pushed into the memory with a “write” instruction (refer to NVM read/write operations). Otherwise, the old configuration will be restored at the next wake-up event.

5.13 Conf int check

In order to guarantee the integrity over time of NVM downloaded trimming/calibration and configuration data, both safety relevant (highlighted with this color code in the register map) and latent register content is automatically and cyclically checked against corruption within NORMAL and CYCLIC WAKEUP mode. This is possible because local register data is provided with a CRC signature, which is checked every T_{CONF_CRC}, while no operation on the NVM is being performed (NVM circuit in reset state). Furthermore, as some key calibration parameters are dumped into a RAM memory, also the latter is checked against data corruption upon each access, since it is equipped with local CRC signature as well.

In case of check failure, the following actions are performed:

- In case trimming/calibration data has failed the CRC signature check, the CYC_TRIM_CRC_FAIL latch is set (clear-upon-read)
- In case safety relevant data has failed the CRC signature check, the CYC_CFG_CRC_FAIL latch is set (clear-upon-read)
- In case calibration data stored in the RAM has failed the CRC signature check, the RAM_ECC_FAIL latch is set (clear-upon-read)
- No other action is taken, i.e. no interruption/inhibition of IC functionalities

In case of permanent data corruption, a failure latch set pulse occurs every T_{CONF_CRC}. Hence, the MCU is supposed to confirm permanent corruption by performing multiple latch clear attempts with a periodicity larger than T_{CONF_CRC}.

The local register CRC signature is managed in the following way:

- Every time NVM data is downloaded into local registers (either automatically or user-driven), a CRC signature is refreshed as well
- Every time the user changes the local register data, the corresponding CRC signature is not automatically updated, thus a CRC check failure is expected at the next execution cycle. By the way, as the user triggers the NVM upload and refresh operation, after the NVM sector CRC has been automatically updated, the local register CRC signature is updated accordingly and no further CRC check failure is expected.

The integrity check can be disabled by setting CYC_CFG_CRC_DIS = 1. After the diagnostic has been disabled, it is still possible to clear upon read both CYC_TRIM_CRC_FAIL, CYC_CFG_CRC_FAIL and RAM_ECC_FAIL. Disabling this diagnostic can be useful to mask systematic CRC failure detection when updating IC configurations. On the other hand, leaving it enabled while updating register configurations may be used as a fault injection strategy to assess the correct functionality of the diagnostics. When RAM_ECC_FAIL_MSK is set to 1, this fault can be cleared.

5.13.1 Electrical parameters

Table 74. Configuration integrity check characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{CONF_CRC}	Configuration integrity check period	Tested by SCAN			90	ms

5.14 NVM

The IC allows key configuration parameters to be stored in the internal NVM. For further details about the register map, please contact your local ST support. All registers marked with this color code throughout the document are configuration registers stored in the NVM.

5.14.1 NVM read/write operations

NVM data is automatically downloaded into local registers every time that the IC performs the following FSM transitions:

- DEEP SLEEP to NORMAL
- DEEP SLEEP to CYCLIC WAKEUP
- SILENT BALANCING to NORMAL
- SILENT BALANCING to CYCLIC WAKEUP

When the IC performs FSM transitions to either DEEP SLEEP or SILENT BALANCING states, a selected group of data stored in local registers is retained in order to guarantee correct IC operation (all bits dependent on the POR_SLEEP_N source reported in **Register map** section), while all other data is lost. Such data will be redownloaded in next transition to NORMAL/CYCLIC WAKEUP.

When the IC performs FSM transitions to OFF state, all data stored in local registers is lost; NVM data will be redownloaded upon the next transition to NORMAL/CYCLIC WAKEUP.

As the IC reaches NORMAL state, the following commands allow user interaction with the NVM:

- NVM_OP_CMD=0x3 triggers the NVM upload and refresh: this operation fetches the data previously written into configuration registers and writes it to the relative NVM sectors, then it automatically triggers a full NVM redownload in order to guarantee whole data consistency. The operation lasts for T_{NVM_UPLOAD} and during this time interval, the MCU will not be able to perform R/W operations on configuration registers (any command will be discarded). The other registers remain accessible.
- NVM_OP_CMD=0x5 triggers the NVM refresh, fetching the data from NVM sectors and writing it to the configuration registers. The operation lasts for $T_{NVM\_DOWNLOAD}$ and during this time interval, the MCU will not be able to perform R/W operations on configuration registers (any command will be discarded). The other registers remain accessible.

During NVM upload/download operations, NVM_READY flag is reset to ‘0’, indicating that the NVM is busy. During this interval, it is highly recommended to avoid triggering conversions or actuating loads, as the trimming and calibration data is being refreshed. Once the task is complete, the NVM_READY is set high; as no NVM read/write operation is running, the NVM circuit is kept under reset. In case of error during the NVM upload procedure, the NVM_VERIFY_ERR (clear-upon-read) flag is asserted, and a correct upload cannot be guaranteed.

In order to guarantee data retention, the NVM write operation number must not exceed $N_{NVM\_WRITE\_CYCLES}$; if this limit is exceeded, data retention is not guaranteed. By the way, the IC will continue to accept and perform every write operation, even if it is beyond the $N_{NVM\_WRITE\_CYCLES}$ count. Every time a write operation is performed, the IC automatically updates the NVM_UPLOAD_COUNT counter field, which is stored in the NVM as well. The counter value is user-accessible, reading NVM_UPLOADS_COUNT bit (read-only): the counter value saturates at $N_{NVM\_WRITE\_CYCLES}$: as the new write operation is done above the $N_{NVM\_WRITE\_CYCLES}$ limit, the counter value is increased to $N_{NVM\_WRITE\_CYCLES}+1$ and will never be updated anymore.

5.14.2 NVM data integrity checks

The NVM content can be categorized in two main groups: trimming/calibration data (used to guarantee function accuracy) and configuration data (used to configure IC operation). All this data is organized in sectors, each of them individually protected by CRC. Trimming/calibration data and configuration data do not share the same sectors.

Every time the IC performs an NVM download operation (either automatic or user-driven), an integrity check against the NVM CRC (sector by sector) is performed as well. In case of check failure, the following actions are performed:

- The CRC check failing sector data is not downloaded into the local registers. This data is replaced by all zeros. It is possible to mask this replacement by setting the NVM_CRC_FAIL_MSK bit. Hence, depending on the sector content, either function accuracy will not be guaranteed, or IC expected configuration will not be applied.
- In case at least one of the trimming/calibration sectors has failed the CRC check, NVM_CRC_TRIM_CAL_FAIL latch is set (clear-upon-read).

- In case at least one of the IC configuration sectors has failed the CRC check, NVM_CRC_CFG_FAIL latch is set (clear-upon-read).
- No other action is taken, i.e. no interruption/inhibition of IC functionalities.

Every time the user triggers an NVM upload and refresh operation, the corresponding sector CRC is updated as well; this is done by the IC automatically.

5.14.3 Electrical parameters

Table 75. NVM electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$N_{NVM\_WRITE\_CYCLES}$	Number of allowed NVM write cycles to guarantee data retention	Guaranteed by SCAN			1000	cycles
$N_{NVM\_WRITE\_COUNT}$	Number of write cycles measured by internal logic				31	
T_{NVM_UPLOAD}	NVM upload time duration	Guaranteed by SCAN	43	48	53	ms
$T_{NVM\_DOWNLOAD}$	NVM download time duration	Guaranteed by SCAN	3.7	4	4.4	ms

5.15 Device identification (DEVICE_NAME)

The Isolated Vertical Interface (VIF) allows the bus to be populated with different devices of the L9965x family. To enable the MCU to quickly recognize the device type and launch the proper initialization, configuration and diagnostic procedures, the NAME_ID field holds a unique code identifying the product type. Specifically, NAME_ID = 0x1A identifies the L9965A/L99BM218 BMIC.

6 Application information

6.1 Bill Of Materials (BOM)

Referring to Figure 23, this section lists the components to be used in a typical application scenario.

Figure 23. Typical application circuit

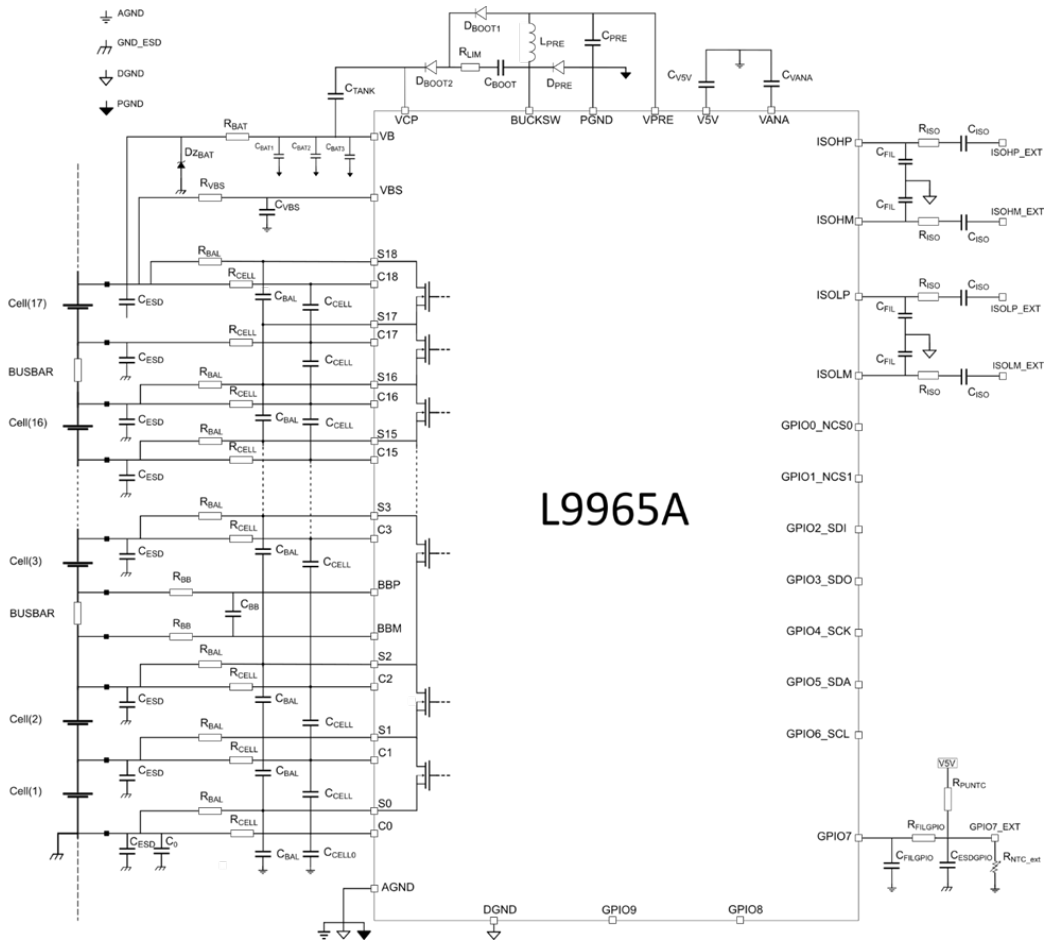


Figure 24. **Application circuit with BB on first cell and unused cells**

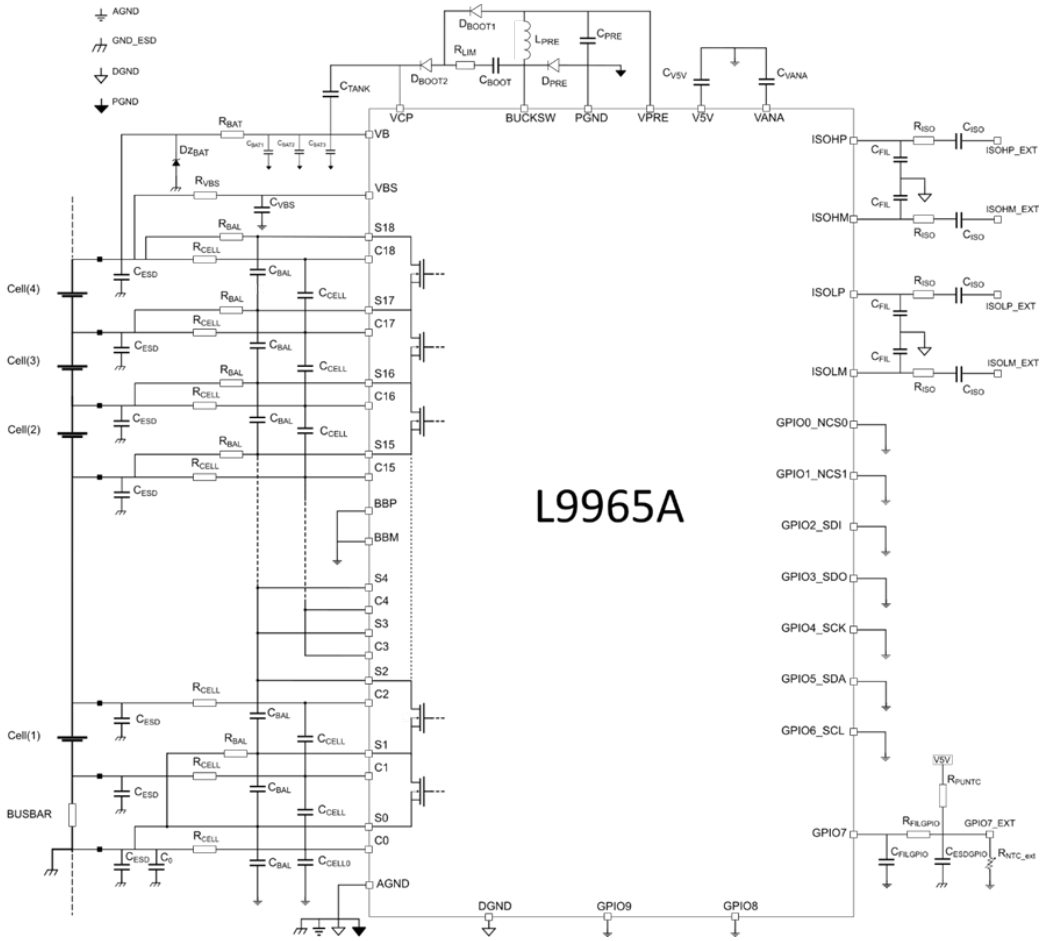


Figure 25. **Application circuit with external SPI and I2C EEPROMs**

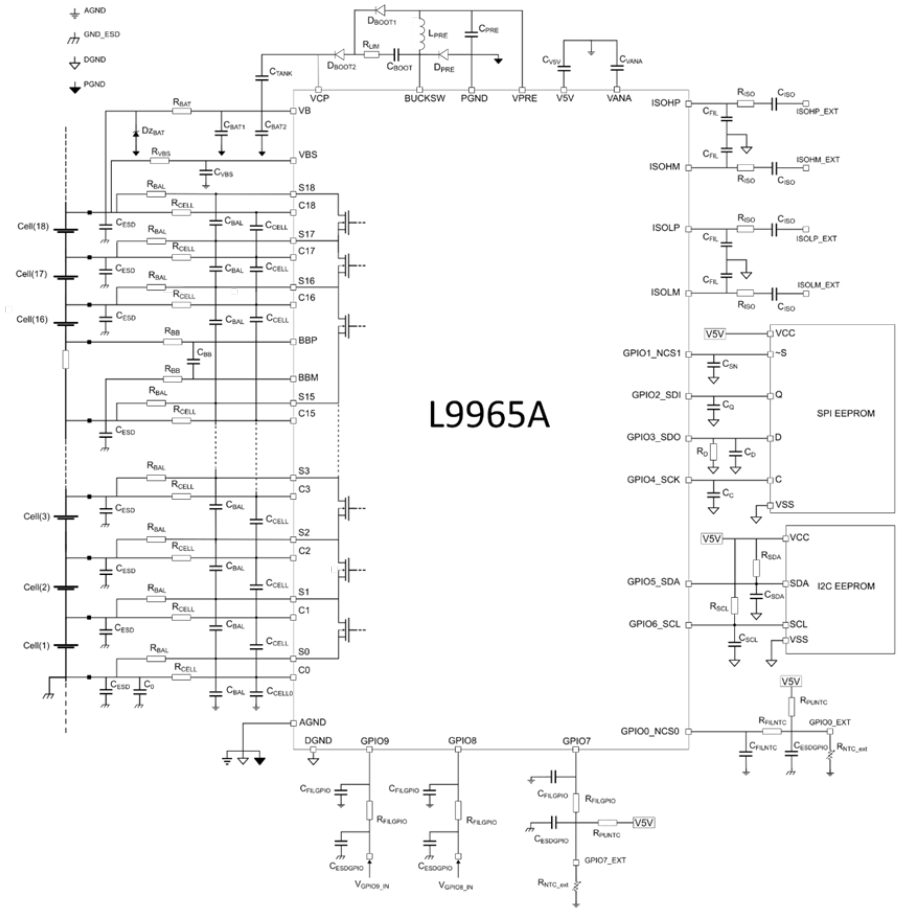


Table 76. **Bill of materials**

Symbol	Parameter	Value	Rating	Tolerance	Note
Battery supply					
R_{BAT}	Series resistor for battery supply line	10Ω	125mW	10%	Optional, it can be useful to limit possible hot plug spikes, according to specific customer application conditions. It shall be sized so that its voltage drop is kept < 1V.
D_{ZBAT}	TVS for battery supply line	SM30T100AY	NA	NA	Optional. Can be mounted to comply with surge and EFT tests.
C_{BAT1}	Tank capacitor for battery supply line	2.2uF to 4.7uF	100V	20%	Lower rating is possible according to module maximum voltage.
C_{BAT2}	Filtering capacitor for battery supply line	100nF	100V	20%	Optional, to improve EMC performances. Consider increasing voltage rating to compensate DC bias effect.
C_{BAT3}	Filtering capacitor for battery supply line	10nF	100V	20%	Optional, to improve EMC performances. Consider increasing voltage rating to compensate DC bias effect.

Symbol	Parameter	Value	Rating	Tolerance	Note
Battery sensing					
R_{VBS}	Filtering resistor for battery sensing line	240Ω	62.5mW	5%	VBS gain conversion error due to RVBS can be computed as R_{VBS}/R_{VBS_IN}. Equalize $R_{VBS}C_{VBS}$ filter cutoff frequency to cells.
C_{VBS}	Filtering capacitor for battery sensing line	220nF	100V	10%	Consider increasing voltage rating to compensate DC bias effect. Lower rating is possible according to module maximum voltage.
Cell and busbar sensing					
R_{CELL}	Filtering resistor for cell sensing line	240Ω	62.5mW	5%	R_{CELL} and C_{CELL} values can be chosen to form an RC filter with ~3.3kHz as cutoff frequency. Cell gain conversion error due to R_{CELL} can be computed as $2R_{CELL}/R_{CELL\_DIFF\_IN}$. Do not go below 100Ω for hot plug robustness. Do not go above 300Ω to avoid false cell 1 open flagging.
C_{CELL}	Differential filtering capacitor for cell sensing line	100nF	16V	10%	
C_{C0}	Grounded capacitor for improved BCI immunity on C0 connector	1nF	16V	10%	
C_{Cell0}	Consist of 3 grounded capacitors for improved BCI immunity on C0	100nF1nF, 100pF	16V	10%	
R_{BB}	Filtering resistor for busbar sensing line	240Ω	62.5mW	5%	Equalize $R_{BB}C_{BB}$ filter cutoff frequency to cells.
C_{BB}	Filtering capacitor for busbar sensing line	100nF	16V	10%	
Cell balancing					
R_{BAL}	Balancing resistor for cell sensing line	12Ω	500mW	5%	Sized to have a 180mA max. balancing current when cell voltage is 4.3V.
C_{BAL}	Filtering capacitor for cell balancing line	22nF to 68nF	16V	20%	The maximum $R_{BAL}C_{BAL}$ cutoff frequency of 100kHz is recommended for BCI robustness
ESD					
C_{ESD}	ESD capacitor for pack connectors	22nF to 47nF	100V	20%	Optional, according to specific customer application requirements. Smaller values are possible if ESD-Safe MLCCs are used. Going below 6.8nF is not recommended as it may jeopardize BCI performance
LDOs					
C_{V5V}	5V LDO tank capacitor	1uF	10V	10%	Consider increasing voltage rating to compensate DC bias effect.
C_{VANA}	3.3V LDO tank capacitor	470nF	10V	10%	Consider increasing voltage rating to compensate DC bias effect.
VIF					
CMC	Common-mode choke for VIF H/L ports	ACT1210R-101-2P			Optional. Can be mounted to improve EMC performance

Symbol	Parameter	Value	Rating	Tolerance	Note
EMIF	Compact analog front end for VIF ports H/L	EMIF04-0410 M8			Optional. Can be used in place of R_{ISO} and C_{FIL} components
R_{ISO}	Series resistor for ISO pins	35Ω to 41Ω 39Ω typical	100mW	1%	Optional. Can be used in place of EMIF component. Filters common-mode and differential noise. Keep tolerance low to maximize differential line balancing.
C_{ISO}	Isolation capacitor for VIF ports H/L	2.2nF to 6.8nF	100V/1kV	2%	Optional. Can be used in place of XFMR component. Voltage rating shall be sized according to the maximum isolation voltage to be guaranteed in the application. Keep tolerance low to maximize differential line balancing.
XFMR	Isolation transformer for VIF ports H/L	ESMIT-4180/C			Optional. Can be used in place of C_{ISO} component. Key parameters are: • Inductance ≥ 120µH @-40°C • Winding resistance ≤ 0.5Ω *Note: EMC trials performed with recommended P/N.*
C_{FIL}	Filtering capacitor for ISO termination	100pF	25V	2%	Optional. Can be used in place of EMIF component. Filters common-mode and differential noise. Keep tolerance low to maximize differential line balancing.
R_{TERM}	Termination resistor for unused port	200Ω	0.5W	10%	Optional. To be used only on unused VIF port.
GPIOs					
R_{PUNTC}	Pull-up biasing for NTC measurement	10kΩ	125mW	10%	Pull-up resistor for NTC lines. Rating is to be increased to 0.5W to protect and withstand short-to-battery.
$R_{FILGPIO}$	Series resistor for GPIO pins	3.3kΩ	125mW	10%	Filters noise on GPIO pin. Rating is to be increased to 0.5W to protect and withstand short-to-battery.
$C_{FILGPIO}$	Filtering capacitor for GPIO pins	100nF	16V	20%	Filters noise on GPIO pin. Rating is to be increased to 100V to withstand short-to-battery.
$C_{ESDGPIO}$	ESD capacitor for GPIO pins connected to external lines	6.8nF	16V	20%	Optional, according to specific customer application requirements. Rating is to be increased to 100V to withstand short-to-battery.
Charge pump					
D_{BOOT1}, D_{BOOT2}	Charge pump bootstrap diodes	BAV99-QVL	100V	NA	Bootstrap diodes rated to withstand maximum operating battery voltage.
C_{TANK}	Charge pump tank capacitor	47nF	100V	10%	Rated to withstand maximum operating battery voltage.
C_{BOOT}	Charge pump flying bootstrap	10nF	100V	10%	Rated to withstand maximum operating battery voltage.

Symbol	Parameter	Value	Rating	Tolerance	Note
R_{LIM}	Bootstrap peak current limiter	1Ω	100mW	10%	Needed to limit the current peak at start-up, when C_{TANK} is discharged.
Buck pre-regulator					
C_{PRE}	Buck tank capacitor	4.7uF	16V	10%	Rating is to be increased to 100V to withstand short-to-battery.
L_{PRE}	Buck inductor	47µH	ISAT >> 220mA	20%	Inductance value shall be constant up to 220mA.
D_{PRE}	Freewheeling diode	BAS19LT1G	120V		Key parameters are: • $V_R \geq 110V$ • $I_F \geq 100mA_{DC}$ • $T_J \geq 150°C$ • $P_D \geq 100mW$ • $V_F \leq 0.75V$ @10mA @25°C • $C_J \leq 10pF$@0V

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

PACKAGE OUTLINE ASSEMBLY

TITLE: TQFP 10x10 64L EXPOSED PAD DOWN

PACKAGE CODE: 9I
JEDEC REFERENCE NUMBER: MS-026-ACD-HD

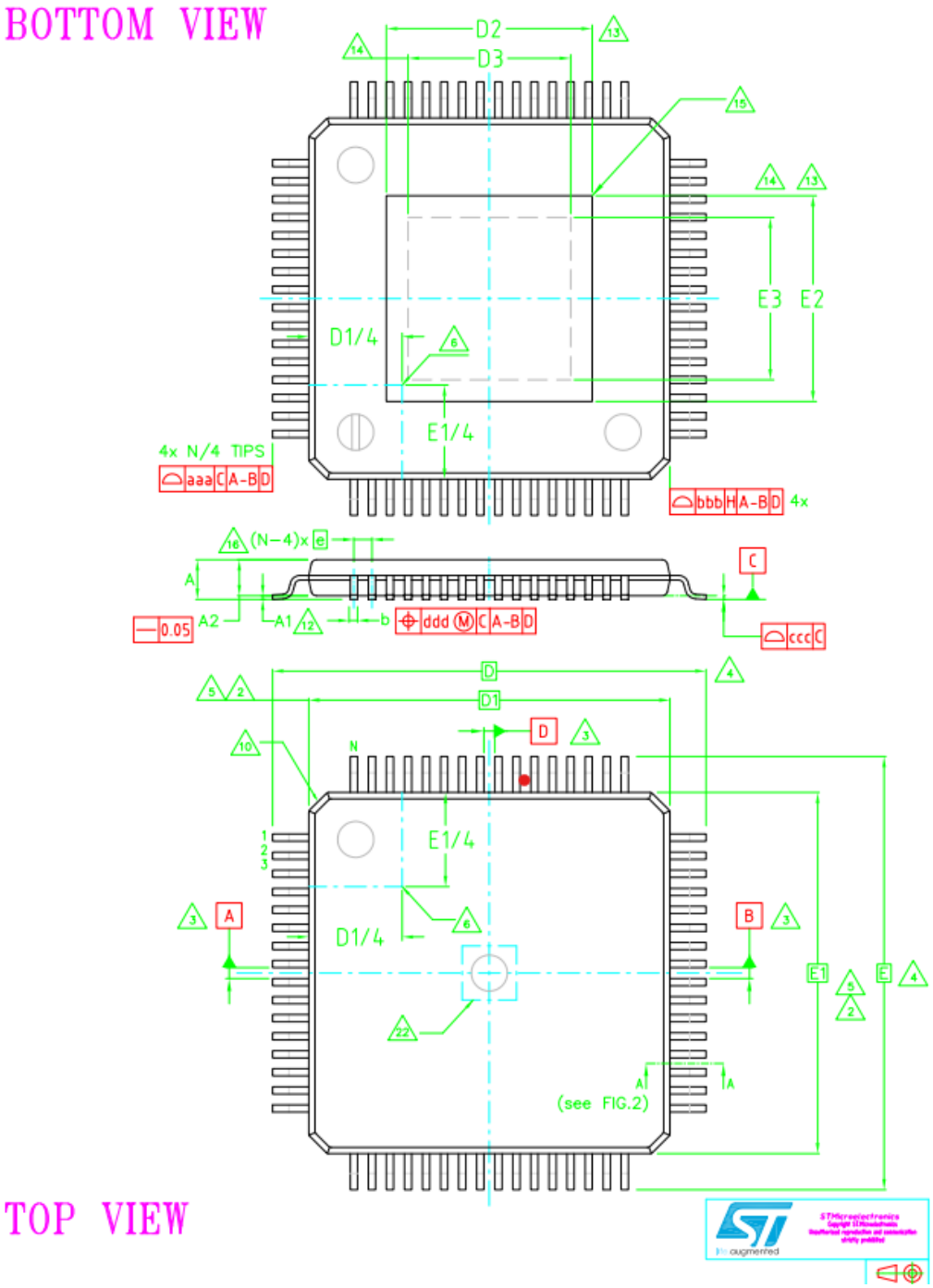
PACKAGE DIMENSIONS

ST DATABOOK				
SYMBOL	MIN.	NOM.	MAX.	NOTE
Θ	0°	3.5°	7°	
Θ1	0°	-	-	
Θ2	10°	12°	14°	
Θ3	10°	12°	14°	
A	-	-	1.20	15
A1	0.05	-	0.15	12
A2	0.95	1.00	1.05	15
b	0.17	0.22	0.27	9,11
b1	0.17	0.20	0.23	11
c	0.09	-	0.20	11
c1	0.09	-	0.16	11
D	12.00 BSC			4
D1	10.00 BSC			2,5
D2	VARIATIONS			13
D3	VARIATIONS			14
e	0.50 BSC			
E	12.00 BSC			4
E1	10.00 BSC			2,5
E2	VARIATIONS			13
E3	VARIATIONS			14
L	0.45	0.60	0.75	
L1	1.00 REF			
N	64			16
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	

TOLERANCE OF FORM AND POSITION		
SYMBOL	ST DATABOOK	NOTE
aaa	0.20	1,7,20
bbb	0.20	
ccc	0.08	
ddd	0.08	

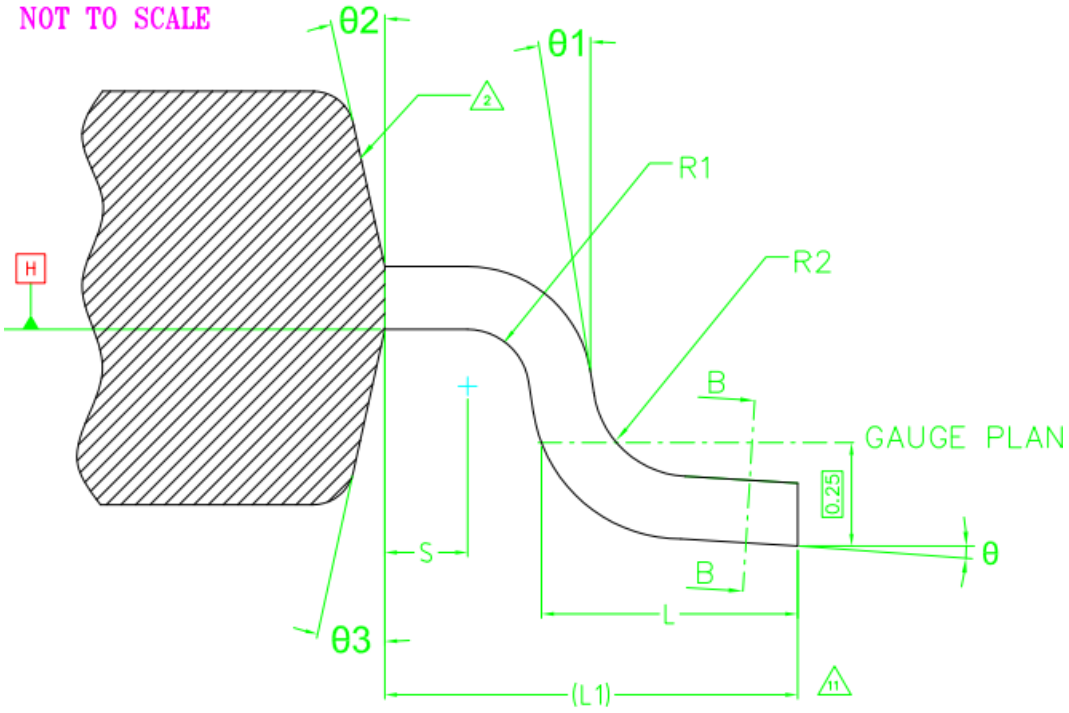
VARIATIONS				
ST DATABOOK				
SYMBOL	MIN.	NOM.	MAX.	PAD OPT.
D2	-	-	4.65	4.3x4.3 (T3)
E2	-	-	4.65	
D3	2.90	-	-	
E3	2.90	-	-	
D2	-	-	4.98	4.5x4.5 (T1-T3)
E2	-	-	4.98	
D3	3.29	-	-	
E3	3.29	-	-	
D2	-	-	5.85	5.5x5.5 (T3)
E2	-	-	5.85	
D3	4.10	-	-	
E3	4.10	-	-	
D2	-	-	6.37	6.0x6.0 (T1)
E2	-	-	6.37	
D3	4.60	-	-	
E3	4.60	-	-	
D2	-	-	6.40	6.0x6.0 (T3)
E2	-	-	6.40	
D3	4.80	-	-	
E3	4.80	-	-	
D2	-	-	6.93	6.65x6.65 (T3)
E2	-	-	6.93	
D3	5.25	-	-	
E3	5.25	-	-	

PAD OPTION 6.0x6.0 (T3) has to be taken into account for L9965A/L99BM218.



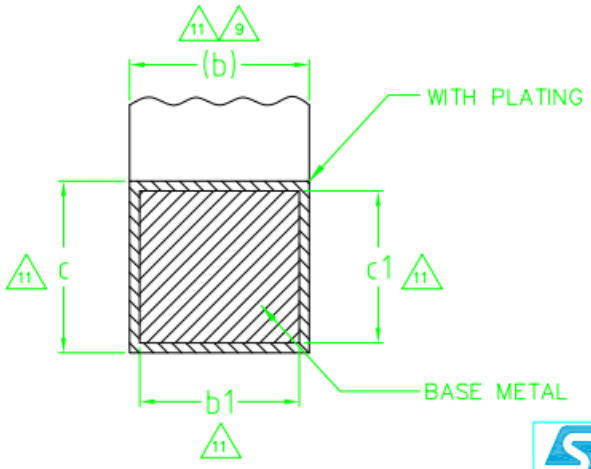
SECTION A-A

NOT TO SCALE

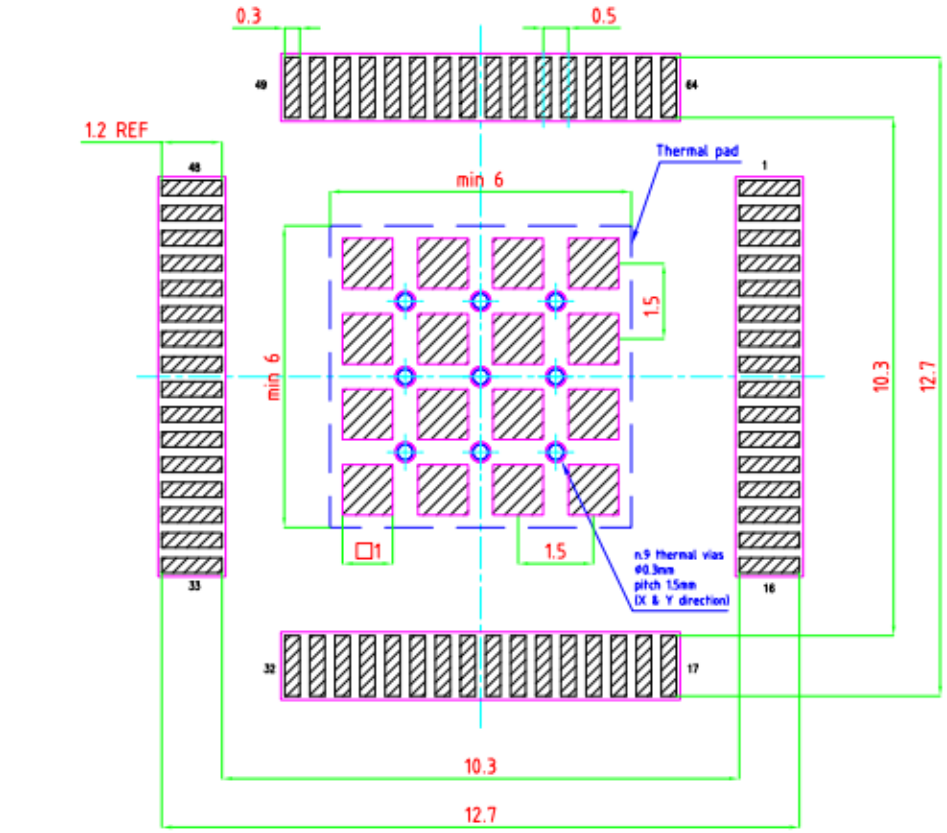


SECTION B-B

NOT TO SCALE



TQFP 10x10 64L - 6.0x6.0 EP DOWN
PCB LANDPATTERN

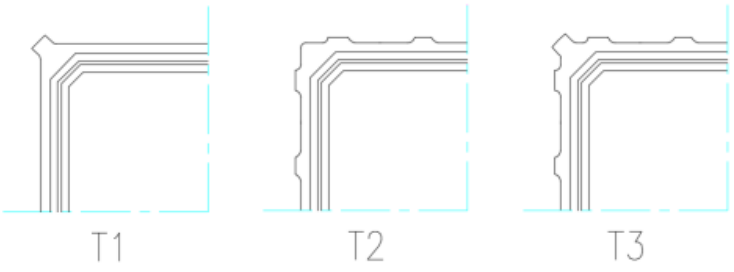


PICTURE

NOTES

△

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "*0.25 mm*" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. End user should verify D2 and E2 dimensions according to specific device application.



NOTE: number, dimensions and position of shown grooves are for reference only.

14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. "N" is the number of terminal positions for the specified body size.
17. For Tolerance of Form and Position see Table.

18. Critical dimensions:
    - 18.1 Stand-Off
    - 18.2 Overall Width
    - 18.3 Lead Coplanarity
19. ST component cross reference: see DMS spec. 7469776, 8232885, 8521844, DM00198457.
20. For Symbols, Recommended Values and Tolerances see Table below:

SYMBOL	DEFINITION	NOTES
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the "coplanarity" of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by "b".

21. POA FORMAT & CONTENT spec. reference number is CD10033601.
22. Notch may be present in this area (MAX 1.5mm square) if center top gate molding technology is applied. Resin gate residual protrusion from package top surface: 0.035mm MAX.

8 Ordering information

Table 77. **Ordering information**

Order code	Package	Packing	FuSa	Qualification
L9965A-TR	TQFP64	Tape and reel	ISO26262 compliant, ASIL-D systems ready, documentation available	AEC-Q100 qualified
L99BM218-TR	TQFP64	Tape and reel	-	-

Revision history

Table 78. **Document revision history**

Date	Version	Changes
21-Nov-2025	1	Initial release.

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