L6462A

Datasheet

Current mode six-pin boost PFC controller

Product status link

L6462A

Product label

SUSTAINABLE TECHNOLOGY

Features

- PFC Transition-Mode current control without input voltage sensing
- Valley skipping with valley lock
- Very low THD in all operating conditions
- Demagnetization sensing via gate driver
- Overvoltage and feedback failure protections
- Inductor saturation detection
- Automatic burst-mode at light load
- Low (<60 µA) start-up current
- Low (<1.1 mA) quiescent current
- 2% overall internal reference voltage accuracy
- -300/+600 mA totem pole gate driver with active pull-down during UVLO and voltage clamp
- 6-pin package

Application

- PFC pre-regulators for:
  - AC-DC adapters and other EN61000-3-2 or JEITA-MITI compliant applications
  - LED-based lamps and luminaires

Description

The L6462A is a control IC for Transition Mode (TM) Boost PFC converters, suitable for building cost-sensitive, energy-efficient solutions.

It embeds a special implementation of current-mode control that enables wide-range mains operation with low THD over a broad load range with no need for input voltage sensing and without a classical analog multiplier.

A pair of special circuits (Current Reference Generator, RCG, and Current Reference Shaper, CRS) shape the reference for the peak current of the inductor to maintain a sinusoidal input current regardless of the converter's operation, whether TM or DCM. This way, it is possible to improve efficiency at intermediate and light loads with minimum impact on input current distortion.

At full load and low AC line, the device synchronizes the turn-on of the power switch to the valley of the ringing following demagnetization of the boost inductor (valley switching – quasi-resonant operation). At high AC line, and as the load is reduced, the IC skips ringing valleys to reduce the operating frequency progressively, so that the converter operates in Discontinuous Conduction Mode (DCM) to optimize efficiency, while maintaining valley switching.

Boost inductor demagnetization sensing is done via the gate driver output. No auxiliary winding or other interface components are needed.

The output voltage is controlled by means of a transconductance type error amplifier and an accurate (2% overall) internal voltage reference. The dynamic response to large-load transients is improved by an enhanced error amplifier that prevents excessive overshoots or undershoots in the output.

The device features low consumption (<60 µA before start-up and 2.3 mA while driving a 1nF capacitive load at 70 kHz) and includes a disable function suitable as a protection or for IC remote ON/OFF from a cascaded conversion stage.

The device offers protection functions against overcurrent, output overvoltage, feedback failure and inductor saturation/shorts in the by-pass diode.

The totem pole output stage, capable of at least 300 mA source and 600 mA sink current, is suitable for MOSFET driving. All these features make the device an excellent low-cost solution for EN 61000-3-2 compliant SMPS.

L6462A is optimized to address 90 V_{AC} - 264 V_{AC} / 400 V_{OUT} applications.

1 Block diagram and typical application

Figure 1. **Block diagram**

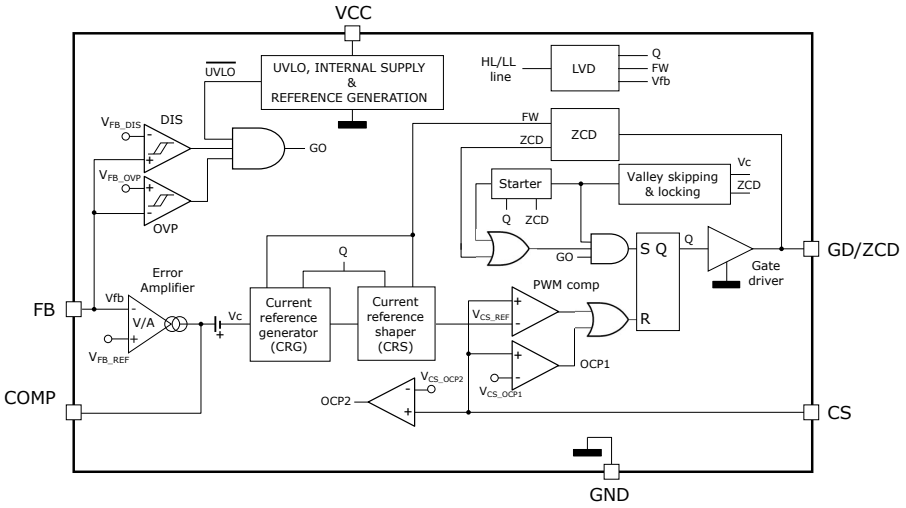
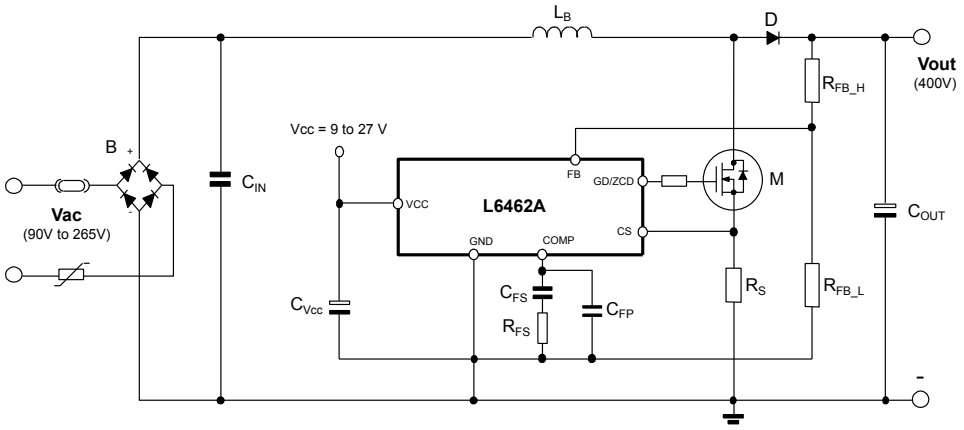


Figure 2. **Typical application**



2 Pin connection and functions

Figure 3. **Pin connection (top view)**

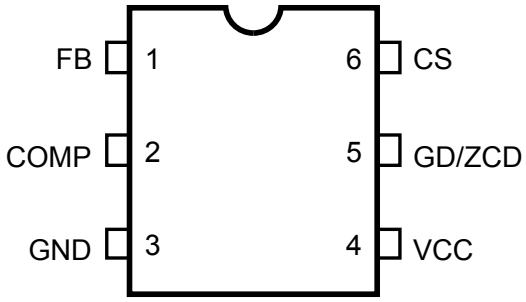


Table 1.

No.	Name	Function
1	FB	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into this pin through a resistor divider. The pin also provides overvoltage and feedback failure protections. Additionally, it can be used as a remote ON/OFF control input.
2	COMP	Output of the internal transconductance error amplifier. Typically, a resistor/capacitor network placed between this pin and GND provides stability of the voltage control loop and ensures high power factor and low THD.
3	GND	Ground. Current return for both the signal part of the IC and the gate driver.
4	VCC	Supply voltage of both the signal part of the IC and the gate driver. The operating supply voltage range goes from 9 V to 27 V.
5	GD/ZCD	Gate driver output/zero current detector input. The totem pole output stage can drive power MOSFETs with a peak current in excess of 300 mA source and 600 mA sink. The high-level voltage of this pin is clamped at 10 V to avoid excessive gate voltages and save driving energy when the IC is supplied with a high V_{CC}. This pin also serves as boost inductor demagnetization sensing input (if using an external pull-down gate resistor, select a value > 100 kΩ).
6	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor Rs, the resulting voltage is applied to this pin and compared with the internal reference, generated by the Current Reference Shaper (CRS), to determine MOSFET turn-off. If the voltage on the pin goes above V_{CS_OCP1}, the internal overcurrent comparator is triggered and terminates the conduction cycle of the external power MOSFET before the normal PWM circuit does. In this way, the peak inductor current is limited at a maximum of V_{CS_OCP1} /Rs. The value depends on the input voltage range: V_{CS_OCP1} = 0.5 V at low AC line and V_{CS_OCP1} = 0.33 V at high AC line. A second overcurrent level set at V_{CS_OCP2} (0.75 V/0.5 V typ. respectively) detects abnormal current values (e.g., due to boost inductor saturation) and, in this case, activates a safety procedure that immediately stops the converter for 1 ms (typ).

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Min.	Max.	Unit
V_{CC}	4	IC supply voltage	-0.3	30	V
GD/ZCD	5	Gate driver voltage, V_{CC} > 14.2 V	-0.3	14	V
		Gate driver voltage, V_{CC} ≤ 14.2 V	-0.3	VCC-0.2	V
FB	1	Feedback input (I_{FB} < 0.5 mA)	-0.3	Self-limited	V
COMP	2	OTA output	-0.3	4	V
CS	6	Current sensing input	-0.3	4	V

3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Min.	Max.	Unit	Remarks
VCC	4	IC supply voltage	-0.3	27	V	
COMP	2	OTA output	-0.3	3.3	V	Values referred to an externally forced condition
FB	1	Feedback Input	-0.3	3.1	V	Internal clamp at 3.1V min.
CS	6	Current sensing input	-0.3	3.6	V	
GD/ZCD	5	GD/ZCD current during OFF-time after t_{PD_ON}	-10	30	mA	

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Max. thermal resistance, junction-to-ambient	250	°C/W
T_j	Junction temperature operating range	-40 to +150	°C
T_{stg}	Storage temperature	-55 to +150	°C

4 Electrical characteristics

T_j = -40 to +125 °C, V_{CC} = 12 V, C_{GD} = 1 nF unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	9		27	V
V_{CC_ON}	Turn-on threshold	Voltage rising(1)	10.4	11.3	12.2	V
V_{CC_OFF}	Turn-off threshold	Voltage falling(1)	8.0	8.5	9.0	V
Hys	Hysteresis		2.2		3.45	V
Supply current						
$I_{START-UP}$	Start-up current	Before turn-on, V_{CC} = 10 V		40	60	µA
I_Q	Quiescent current	After turn-on, no switching		1	1.21	mA
		During OVP & burst-mode		0.33	0.405	
		Disabled		0.19	0.24	
I_{CC}	Operating supply current	@ 70 kHz		2.3	3	mA
Transconductance error amplifier						
V_{FB_REF}	Feedback reference	T_j = 25 °C	2.47	2.5	2.53	V
		9 V < V_{CC} < 27 V(1)	2.45		2.55	
I_{FB}	Input bias current	V_{FB} = 0 to 2.8 V	-120		120	nA
V_{FB_CLAMP}	Internal clamp level	I_{FB} = 0.5 mA	3.1			V
g_m	Transconductance - linear range	| V_{FB} - V_{FB_REF} | < 75 mV V_{COMP} = 1 V	78	100	122	µS
I_{COMP}	Max. source current	V_{COMP} = 3 V, V_{FB} = 2.1 V		-200		µA
	Max. sink current	V_{COMP} = 1 V, V_{FB} = 2.9 V		200		µA
	Sink current OCP2	OCP2, V_{COMP} > V_{COMP_BM}	1.2	3		mA
V_{COMP}	Upper saturation voltage	I_{SOURCE} = 0.1 mA(1)	3.1			V
	Lower clamp voltage	V_{FB} - V_{FB_REF} =100 mV(1)	0.150	0.185	0.230	
V_{COMP_BM}	Burst-mode threshold	Negative-going edge(1)	0.285	0.300	0.315	V
V_{COMP_Hys}	Burst-mode hysteresis	Above V_{COMP_BM}		25		mV
Current sense & overcurrent comparators						
I_{CS}	Input bias current	V_{CS} = 0 to V_{CS_OCP2}	-1		1	µA
V_{CS_OCP1}	OCP1 triggering voltage	Low AC line detected(1)	480	500	520	mV
		High AC line detected(1)	315	330	345	
V_{CS_OCP2}	OCP2 triggering voltage	Low AC line detected(1)	715	750	790	mV
		High AC line detected(1)	475	500	537	
$t_{d(H-L)}$	Delay to output	From V_{CS} = V_{CS_REF} to GD/ZCD going low		75	160	ns
T_{LEB}	Leading-edge blanking	From GD/ZCD going high	190	300	420	ns
T_{OCP2}	OCP2 restart timer	From OCP2 detection	0.75	1	1.25	ms

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{ON_MAX}	Maximum on-time	After GD/ZCD rising	50	65	86	µs
Line voltage detector (LVD)						
$Line_H$	High AC line threshold	V_{OUT} = 400 V, AC voltage rising		159		V_{AC}
		V_{OUT} = 450 V, AC voltage rising		178		V_{AC}
T_{FF_LAT}	Debounce time high AC line detection		375	500	625	µs
T_{FF_DB}	Debounce time low AC line detection		15	20	25	ms
Current reference generator & shaper						
G_{CR}	Equivalent multiplier gain(2)	Low AC line detected	0.534	0.580	0.626	V/V
		High AC line detected	0.115	0.125	0.135	V/V
Valley skipping & valley lock function						
V_{COMP_TB1-2}	From valley#1 to valley #2	Voltage falling & low AC line(1)	0.665	0.700	0.735	V
		Forced at high AC line		---		
V_{COMP_TB2-3}	From valley#2 to valley #3	Voltage falling(1)	0.594	0.625	0.656	V
V_{COMP_TB3-5}	From valley#3 to valley #5	Voltage falling(1)	0.523	0.550	0.578	V
V_{COMP_TB5-8}	From valley#5 to valley #8	Voltage falling(1)	0.451	0.475	0.499	V
V_{COMP_TB8-13}	From valley#8 to valley #13	Voltage falling(1)	0.380	0.400	0.420	V
V_{COMP_TB13-8}	From valley#13 to valley #8	Voltage rising(1)	0.570	0.600	0.630	V
V_{COMP_TB8-5}	From valley#8 to valley #5	Voltage rising(1)	0.641	0.675	0.709	V
V_{COMP_TB5-3}	From valley#5 to valley #3	Voltage rising(1)	0.713	0.750	0.788	V
V_{COMP_TB3-2}	From valley#3 to valley #2	Voltage rising(1)	0.784	0.825	0.866	V
V_{COMP_TB2-1}	From valley#2 to valley #1	Voltage rising & Low AC line(1)	0.855	0.900	0.945	V
		Disabled at high AC line		---		
Minimum switching frequency (n-th valley >= 3)						
t_{FORCE_FSWMIN}	Timer period	After GD/ZCD rising	22.5	30	43.75	µs
$T_{TIMEOUT\_FSWMIN}$	Timeout	After t_{FORCE_FSWMIN} rising	3.2	4	5	µs
Starter / Restart Timeout						
t_{START}	Timer period	After GD/ZCD falling	160	200	240	µs
		After $I_{GD} < I_{GD\_T}$	9.6	12	14.54	
		After first 12 µs-timer pulse	1.6	2	2.54	
Output overvoltage / feedback disconnection protection						
V_{FB_OVP} / V_{FB_REF}	OVP triggering	FB rising edge(1)	107	108	109	%
V_{FB_R} / V_{FB_REF}	OVP restart level	FB falling edge(1)	101	102	104	%
V_{FB_DIS}	Disable threshold	Negative-going edge(1)	280	300	315	mV
V_{FB_EN}	Enable threshold	Positive-going edge(1)	430	450	470	mV
Zero current detector (ZCD)						
I_{GD_A}	ZCD arming current	(1)	-80	-60	-45	µA

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{GD_T}	ZCD triggering current	(1)	-51	-40	-30	µA
$t_{d(ZCD)}$	ZCD triggering delay	From I_{GD} = I_{GD_T} to GD/ZCD rising			100	ns
t_{ZCD_BLK}	ZCD blanking time	From GD/ZCD falling(1)	500	700	920	ns
Gate driver						
V_{GDL}	Output low voltage during t_{PD_ON} time	I_{sink} = 100 mA			0.6	V
		I_{sink} = 5 mA			0.05	
V_{GDH}	Output high boltage	V_{CC} = 8 V, I_{source} = 5 mA	6.75	7.25		V
		V_{CC} ≥ 12 V, I_{source} = 5 mA	9	10	11	
I_{srcpk}	Peak source current		-0.3	-0.6		A
I_{snkpk}	Peak sink current		0.6	1		A
t_f	Voltage fall time	$V_{GD/ZCD}$ from 8 V to 1 V	7	10	16	ns
t_r	Voltage risetime	$V_{GD/ZCD}$ from 1 V to 8 V	10	16	23	ns
V_{GDsat}	UVLO saturation	V_{CC} = 0 to V_{CC_ON}, I_{sink}= 1 mA			1.1	V
V_{GDzcd}	Output low voltage during ZCD detection	After t_{PD_ON} from GD/ZCD falling, I_{GD} = 0 mA	0.90	1.08	1.17	V
		After t_{PD_ON} from GD/ZCD falling, I_{GD} = 30 mA (sink)	1.9	2.3	2.75	
t_{PD_ON}	Low output impedance time interval	From GD/ZCD falling(1)	390	530	730	ns

1. *Parameters tracking each other*
2. $$V_{CS\_REF}(\theta) = G_{CR} \cdot V_C \cdot \frac{V_{IN,pk}}{V_{OUT}} \cdot \sin\theta \cdot \frac{T(\theta)}{T_{ON}(\theta) + T_{FW}(\theta)}$$

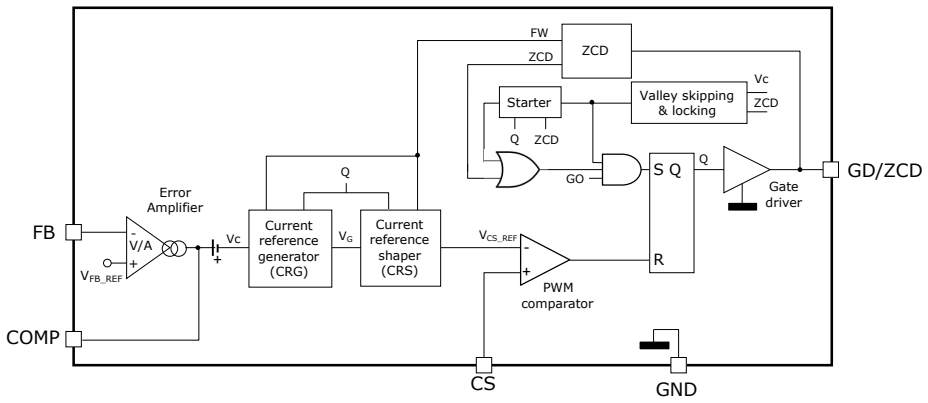
5 Application information

5.1 Theory of operation

The L6462A implements a peak-current mode control operating in TM/DCM (skipping the valleys) with valley turn-on as illustrated by the basic schematic in Figure 4.

Figure 5 and Figure 6 show the key waveforms both on the switching cycle time scale and on the line frequency time scale when the boost PFC converter works in TM. Figure 7 and Figure 8 show the same when the Boost PFC converter works in DCM.

Figure 4. L6462A current mode control scheme: block diagram



The basic turn-on and off mechanisms of the MOSFET are no different from those of the traditional current-mode control method. Switching cycles (i.e., MOSFET turn-on) can be initiated by either the ZCD (Zero Current Detector) block that senses boost inductor demagnetization, or by the starter block when no signal is coming from the ZCD block. In steady-state operation, all cycles are initiated by the ZCD block by synchronizing them to the drain voltage, reaching the first valley of the ringing that occurs after demagnetization (valley switching). The distance in time between the demagnetization instant and the first valley of the ringing (T_V in the timing diagram of Figure 5) equals half the ringing period T_R:

Equation 1

$$T_V = \frac{T_R}{2} = \pi \cdot \sqrt{L_B \cdot C_d} \quad (1)$$

where L_B is the inductance value of the boost inductor and C_d the total parasitic capacitance of the MOSFET drain, which includes MOSFET C_{oss} as well as other contributions such as the junction capacitance of the boost diode and the interwinding capacitance of the boost inductor.

With valley switching, the MOSFET is turned on with zero (when the instantaneous input voltage $V_{IN}(\theta)$ is less than half the output voltage V_{OUT}) or minimum drain-to source voltage (when $V_{IN}(\theta) = V_{INpk} \cdot \sin\theta$), which minimizes capacitive losses at turn-on.

The end of the ON-time of the power MOSFET is determined by comparing the signal on the CS pin in the PWM comparator (which is a ramp proportional to the instantaneous inductor current $I_L(t,\theta)$) to the current reference $V_{CS\_REF}(\theta)$. When the two signals are equal, a reset signal is given to the PWM latch and the power MOSFET is switched off.

The peculiarity of the control method is how the current reference $V_{CS\_REF}(\theta)$ is generated. The control voltage V_C (= V_{COMP} - 0.25 V) is processed by two cascaded functional blocks: the Current Reference Generator (CRG) block that outputs a first reference voltage $V_G(\theta)$, which is fed into the Current Reference Shaper (CRS) block that outputs $V_{CS\_REF}(\theta)$.

The trans-conductance V/A error amplifier compares a portion of the output voltage V_{OUT}, brought to its inverting input externally available on the FB pin via the resistor divider R_{FB_H}-R_{FB_L}, as shown in the typical application schematic in Figure 2, with an accurate internal reference V_{FB_REF} (2.5 V typ.) connected to the non-inverting input, and generates an error signal V_C proportional to their difference.

If the bandwidth of the error amplifier, essentially determined by the frequency compensation network connected between the COMP pin and ground, is narrow enough – typically below 20 Hz – and a steady-state operation is assumed, the V_C error signal available at the COMP pin can be regarded as a DC level, at least as a first approximation. The V_C voltage is then used by the CRG circuitry, which, based also on the FW and Q signals, generates a voltage expressed by:

Equation 2

$$V_G(\theta) = K_1 \cdot V_C \cdot \frac{V_{INpk}}{V_{OUT}} sin\,\theta \tag{2}$$

where K_1 is the circuitry gain (constant term) and $V_{IN}(\theta) = V_{INpk} \cdot sin\,\theta$ (with $0 \le \theta \le \pi$, as a result of the rectification operated by the input bridge) is the instantaneous line input voltage.

Equation (2) shows that the $V_G(\theta)$ voltage is proportional to the $V_{IN}(\theta)$ input voltage and to the V_C control voltage like in a standard current-mode PFC, but without using the standard multiplier block and without the AC line sensing.

The $V_G(\theta)$ voltage is then managed by the CRS circuitry that shapes the $V_G(\theta)$ voltage accordingly, in order to achieve an ideally sinusoidal input current. The resulting current reference voltage is then:

Equation 3

$$V_{CS\_REF}(\theta) = V_G(\theta) \cdot K_2 \cdot \frac{T(\theta)}{T_{ON}(\theta) + T_{FW}(\theta)} = G_{CR} \cdot V_C \cdot \frac{T(\theta)}{T_{ON}(\theta) + T_{FW}(\theta)} \cdot \frac{V_{INpk}}{V_{OUT}} \cdot sin\,\theta \tag{3}$$

where $G_{CR} = K_1 K_2$ is the equivalent multiplier gain (see Electrical characteristics table for details), $T_{ON}(\theta)$ is the power switch on-time interval (Q=High) and $T_{FW}(\theta)$ is the time interval while the boost inductor is demagnetizing (FW=High).

Neglecting the mainly negative contribution of the ringing current to the average inductor current during T_V in DCM operation, the relationship between the peak value $I_{Lpk}(\theta)$ and the average value $I_L(\theta)$ of the inductor current in a switching cycle becomes:

Equation 4

$$I_L(\theta) = \frac{1}{2} \cdot \frac{T_{ON}(\theta) + T_{FW}(\theta)}{T(\theta)} \cdot I_{Lpk}(\theta) \tag{4}$$

Keeping in mind that $I_{Lpk}(\theta) = V_{CS\_REF}(\theta) / Rs$, the resulting average inductor current and then input current $I_{IN}(\theta)$ can be obtained from equation (3) and equation (2):

Equation 5

$$I_{IN}(\theta) = I_L(\theta) = \frac{1}{2} \cdot \frac{G_{CR}}{Rs} \cdot V_C \cdot \frac{V_{IN,pk}}{V_{OUT}} \cdot sin\,\theta. \tag{5}$$

which is sinusoidal and in phase with the $V_{IN}(\theta)$ input voltage (ideally zero-THD and unity-PF) regardless of whether the boost PFC converter works in TM or in DCM (valley skipping).

Figure 5. Key waveforms of the circuit in Figure 4 in TM (valley switching) operation - Switching cycle time scale

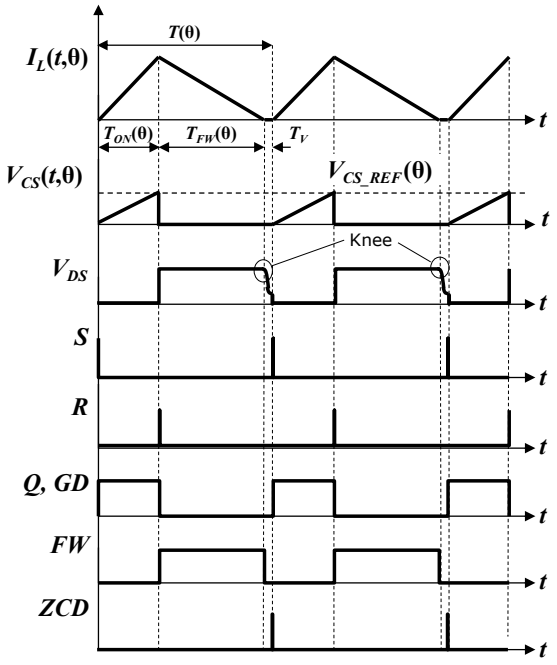


Figure 6. Key waveforms of the circuit in Figure 4 in TM (valley switching) operation - Line cycle time scale

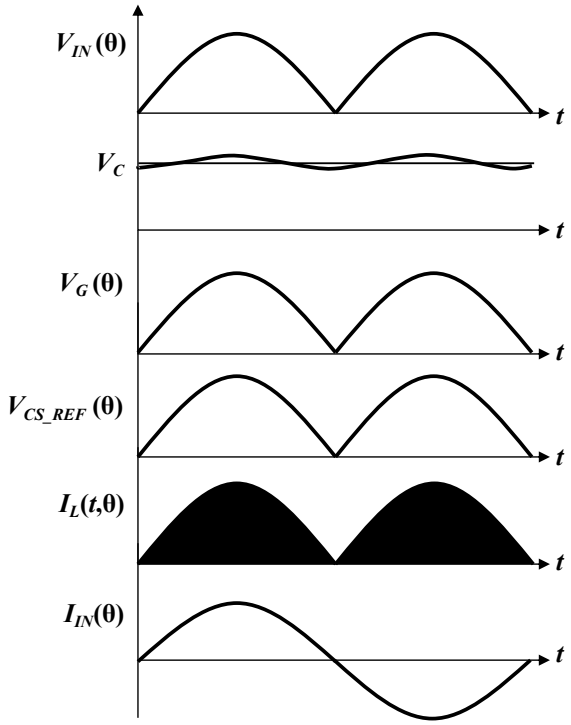


Figure 7. Key waveforms of the circuit in Figure 2 in DCM operation with valley switching - Switching cycle time scale

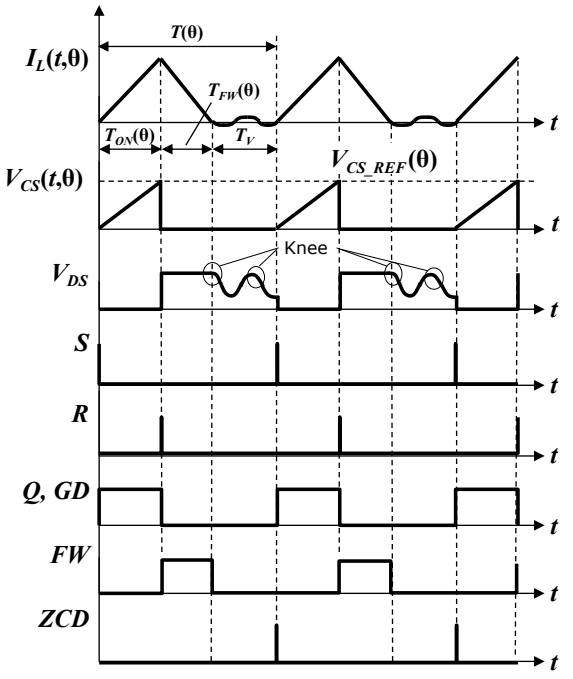
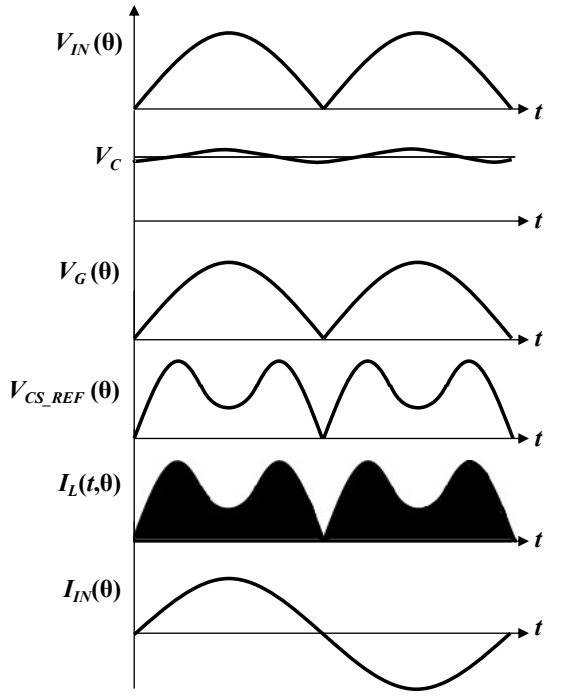


Figure 8. Key waveforms of the circuit inFigure 2 in DCM operation with valley switching - Line cycle time scale



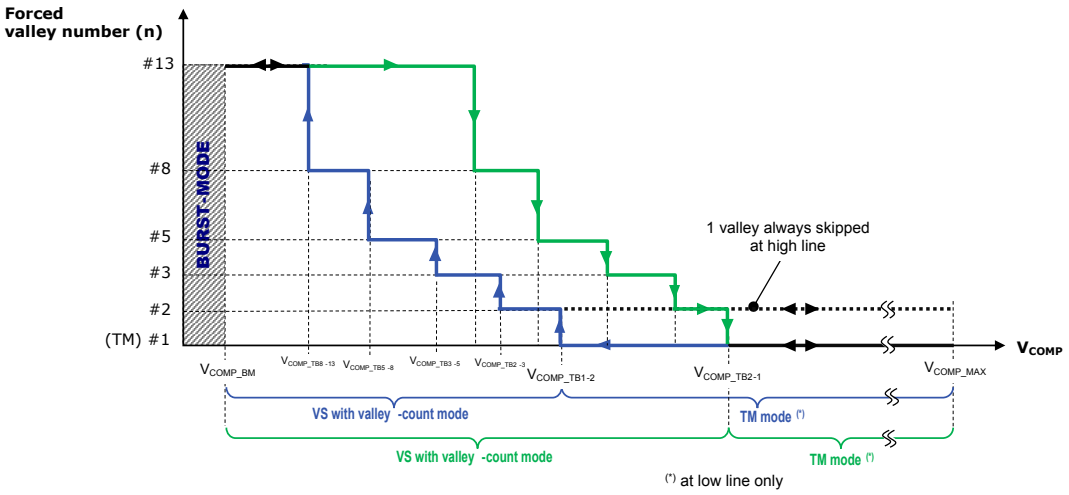
5.2 Valley skipping (VS) and valley lock function

With TM operation, as the load decreases, f_{sw} increases and a mechanism of frequency limitation and foldback is introduced in the L6462A to prevent f_{sw} from reaching excessively high values and to stop efficiency from quickly dropping at medium/light load.

Specifically, at low AC line, when V_{COMP} voltage is lower than the V_{COMP_TB1-2} threshold, the turn-on of the MOSFET is no longer commanded on the first valley of the drain voltage ringing after the demagnetization, but on the n-th valley of the ringing. A “valley counter” based on the ZCD pulse detection is implemented and the number of skipped valleys (n-1) is increased in discrete steps which become progressively longer and longer, as V_{COMP} gets lower and lower due to a load decrease, as shown in the diagram in Figure 9 (turn-on at valley number n=1, n=2, n=3, n=5, n=8, n=13). In this way, the converter’s switching frequency is forced to increasingly lower values (Frequency foldback), thus also reducing all frequency-related losses.

At high AC line, VS operation is always enabled regardless of V_{COMP} voltage. This reduces the THD of the input current by improving its shape close to the zero crossings of the line voltage (crossover distortion) and may slightly improve efficiency as well.

Figure 9. Turn-on valley number (n) vs. V_{COMP} map

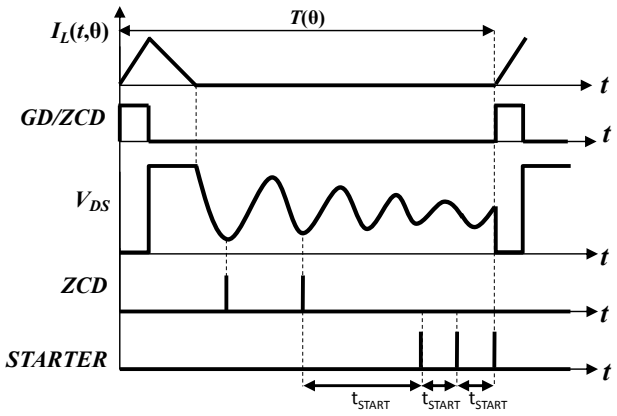


Once transitioning from TM operation to VS operation, the time interval T_V jumps from $T_R/2$ to a new value $T_{V1} = T_R$ (n - 1/2), which depends on the number of valleys skipped (n-1), so the boost now operates in DCM, but still uses valley switching to minimize turn-on losses.

Appropriate hysteresis in the comparators that set the value of the valley turn-on number (n) ensures that no “blanking jump” occurs. Once the number of valleys skipped is set to (n-1) based on the COMP pin voltage, it will stay locked to that value along the entire line half cycle if the load stays the same. Only a significant change in load conditions will change the number of valleys skipped, depending on whether the load increases or decreases.

At very light load, it is very likely that the damped oscillations of the drain ringing are so small that they cannot be detected by the ZCD circuit anymore. In this case, to prevent the converter from getting stuck, an appropriate timeout circuit forces the MOSFET to turn on. Specifically, to maximize compatibility with valley switching operation, including with power switches with large C_{OSS}, the restart timer t_{START} is 12 µs until the ZCD is detected and is then reduced to 2 µs as shown in Figure 10.

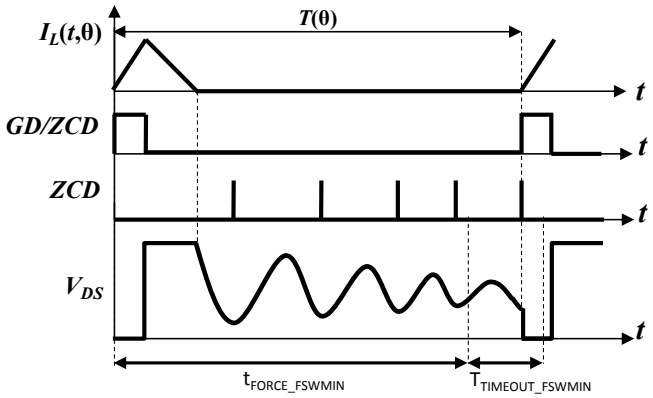
Figure 10. **Missing ZCD - starter behavior**



Of course, in this case, valley switching is most likely lost, but when the drain oscillations are so small that they cannot be detected any more, turning on the MOSFET at any instant does not make a difference in terms of turn-on losses.

To guarantee switching frequency (f_{sw}) above the audible frequency in all operating conditions, the power switch turn-on can be forced after a t_{FORCE_FSWMIN} time (30 µs typ.) from its previous turn-on (GD/ZCD rising edge). In addition, to keep valley switching operation active during this condition, the power switch is not immediately turned on after the time t_{FORCE_FSWMIN}, but on the first valley detected by ZCD circuitry within the timeout $T_{TIMEOUT\_FSWMIN}$ (4 µs typ.).

Figure 11. **Minimum switching frequency - timer**



To allow the design of a PFC converter with 30 kHz as a minimum switching frequency at full load, the minimum frequency timer is active only if the controller is skipping at least two valleys, so it is operating on the n-th valley with n >= 3. The device also limits the maximum switching frequency operation by embedding a frequency limiter at 550 kHz typical.

5.3 Zero-current detection (ZCD) function

The valley turn-on instant (also known as a ZCD detection) is detected through the multifunction pin GD/ZCD during power switch off-time. Considering that the drain voltage waveform after demagnetization can be described by the following equation:

Equation 6

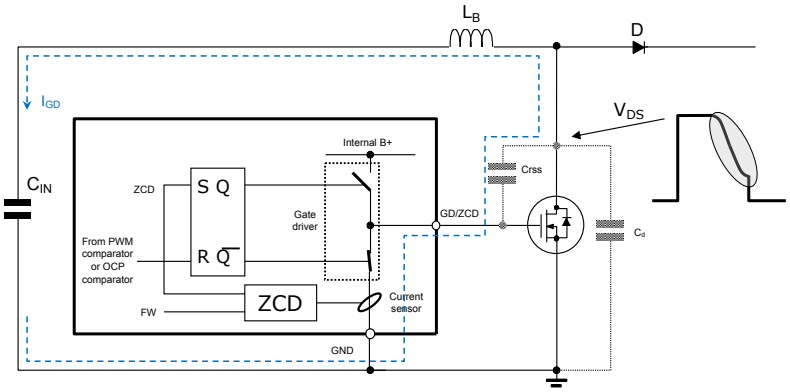
$$V_{DS}(t) \cong V_{IN} + (V_{OUT} - V_{IN}) \cdot \cos 2\pi f_R t \quad (6)$$

where V_{IN} is the instantaneous line voltage (the argument θ is omitted for simplicity) and $f_R = 1/T_R$ with T_R given by equation (1) (damping is neglected for simplicity, due to essentially being interested in the first ringing cycle).

This oscillation reaches its valley, equal to $2V_{IN} - V_{OUT}$ at $t = T_R/2$, where the argument of the cosine function is π. However, in case it is $2V_{IN} - V_{OUT} < 0$, the drain voltage is clamped by the body diode of the power MOSFET at essentially zero.

During this oscillation, electrical charge flows through C_{rss}, the parasitic capacitance that exists between the gate and the drain terminals of the power MOSFET, as illustrated in Figure 12. Since the drain voltage is falling (the region highlighted in grey in the waveform of Figure 12) and the gate voltage is kept at essentially zero (see Section 5.4 for more details), this current, I_{GD}, comes out from the drain terminal, goes through L_B and C_{IN}, and then enters the GND pin, flows through the internal pull-down of the gate driver and finally exits from the GD/ZCD pin and enters the gate terminal.

Figure 12. Operating principle of the ZCD circuit



The amplitude of I_{GD} is given by:

Equation 7

$$I_{GD}\left(t\right) = C_{rss} \cdot \frac{dV_{DS}(t)}{dt} = 2\pi \cdot f_R \cdot C_{rss} \cdot (V_{OUT} - V_{IN}) \cdot sin\, 2\pi f_R t \tag{7}$$

and reaches its maximum I_{GD_max} where the argument of the sine function is π/2. This maximum is:

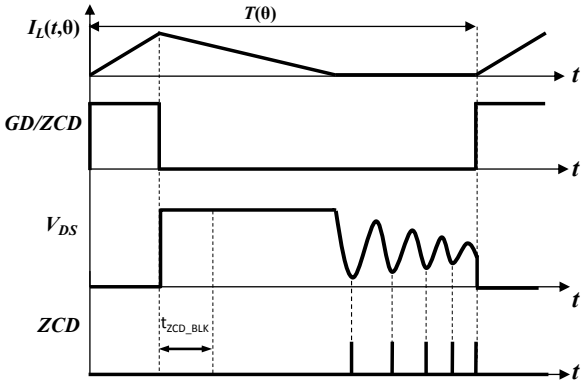
Equation 8

$$I_{GDmax} = 2\pi \cdot f_R \cdot C_{rss} \cdot (V_{OUT} - V_{IN}) = \frac{C_{rss}}{\sqrt{L_B C_d}} \cdot (V_{OUT} - V_{IN}) \tag{8}$$

The ZCD block, therefore, comprises a current sensor that monitors the current I_{GD} exiting the GD/ZCD pin in a time interval (ZCD observation window) that starts when the MOSFET is turned off (with an appropriate delay t_{ZCD_BLK} as shown in Figure 13 to avoid noise injected by the rising edge of the drain voltage) and normally ends when a *ZCD* pulse (the first one in case of TM operation, or the first one after the (n-1) valley skipped in VS operation) causes the power MOSFET to turn on.

As I_{GD} exceeds a preset threshold I_{GD_A} (60 µA typ.), the ZCD circuit assumes that demagnetization has just occurred, sets the *FW* signal low, and gets armed; as I_{GD} falls below a second threshold I_{GD_T} (40 µA typ.), the circuit assumes that the drain voltage has reached its valley or has reached zero, gets triggered and delivers a *ZCD* pulse. If the boost PFC converter is working in TM mode, this *ZCD* pulse will set the PWM latch, cause the power MOSFET to turn on and the ZCD observation window to close. In case of VS operation, the pulse will not reach the S input, but will increment the “valley counter”, the MOSFET will stay off and the drain will go on ringing. After reaching the next peak, the drain voltage will go down again and if I_{GD} is still large enough to cause another arm-trigger sequence, a new *ZCD* pulse will be generated. This continues until a *ZCD* pulse is eventually output after the “valley counter” permits to turn on on the n-th valley selected by the COMP pin voltage, the PWM latch is set, the ZCD observation window closed and the MOSFET turned on.

Figure 13. **GD behavior - ZCD blanking time**



It is worth remembering that the drain oscillations are damped, so at the end of the valley count that permits to skip the (n-1) valley, their amplitude may become too small to be detected, as indicated in Section 5.2, in which case the already mentioned 12 µs/2 µs timer provides for the missing ZCD pulses.

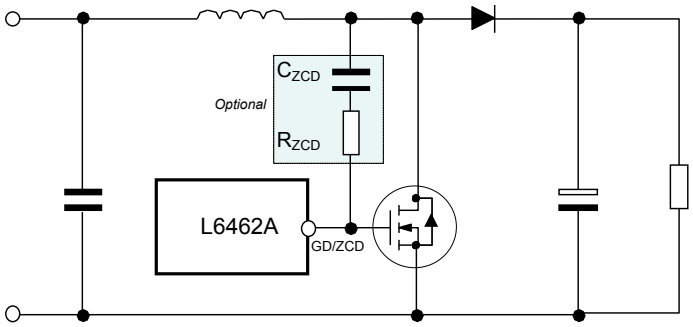
A more severe condition is when the ZCD circuit fails to detect the demagnetization, i.e., the *ZCD* pulse is not released even on the first valley of the ringing. To prevent the converter from getting stuck in this case, a long starter (200 µs typ.) is activated at every falling-edge of the GD pulse, to force the power MOSFET turn-on in that case.

This missed ZCD detection occurs whenever the difference $V_{OUT} - V_{IN}$ is too small. This typically happens at start-up or when the output voltage is recovering after a line drop, or if the input voltage is higher than the maximum value specified because of an anomaly. These are transient conditions where it is important to just keep the system up and running.

If there are steady-state conditions where the difference $V_{OUT} - V_{IN}$ is too small for the ZCD circuit to detect the demagnetization, these are likely to occur close to the peak input voltage at maximum line voltage, because the output voltage set point is too low or the output ripple too large. When this occurs, it is possible to observe a slight degradation of the performance (lower efficiency, higher THD of the input current) but no severe system functionality impairment.

In case one wants to increase the sensitivity of the internal current sensor, it is possible to add an external capacitor of a few pF between the drain and the gate of the power MOSFET, with a series resistor in the tens of kΩ, to limit noise injection into the gate driver pin as shown in Figure 14.

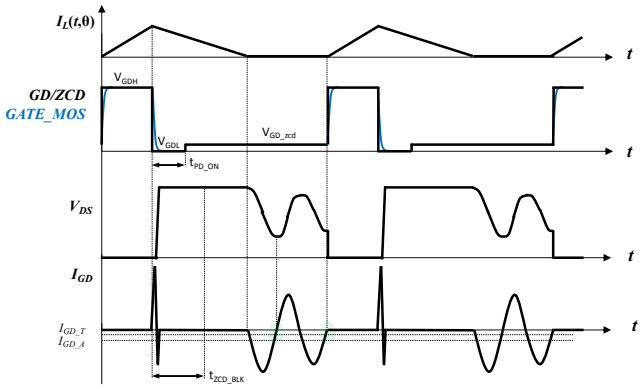
Figure 14. **Optional supplementary external RC to increase ZCD circuit sensitivity**



5.4 GD/ZCD multifunction pin

The GD/ZCD pin is a multifunction pin to drive the power MOSFET and to detect the ZCD condition for valley turn-on. Specifically, as shown in Figure 15, during the power MOSFET on-time, the GD/ZCD pin is forced high to V_{GDH} (10 V typ.) and during the off-time is initially forced low (V_{GDL}) to guarantee the power switch turn-off, also in case of a large current injected by the fast rising edge of the MOSFET drain. After a t_{PD_ON} time (530 ns typ.), the GD/ZCD pin is then forced to a positive voltage V_{GD_zcd} (1.08 V typ.) to measure the I_{GD} current for the ZCD detection.

Figure 15. GD/ZCD pin voltage behavior



5.5 Enhanced error amplifier

The error amplifier consists of a transconductance amplifier (OTA). Its inverting input is externally available (FB pin) to sense the output voltage of the PFC pre-regulator via a resistor divider, and its non-inverting input is internally connected to an accurate reference voltage V_{FB_REF} = 2.5 V +/-2%, all inclusive. The output is externally available on the COMP pin, which outputs a current depending on the voltage difference between the inverting and the non-inverting input:

Equation 9

$$I_{COMP} = g_m(V_{FB} - V_{FB\_REF}) \quad (9)$$

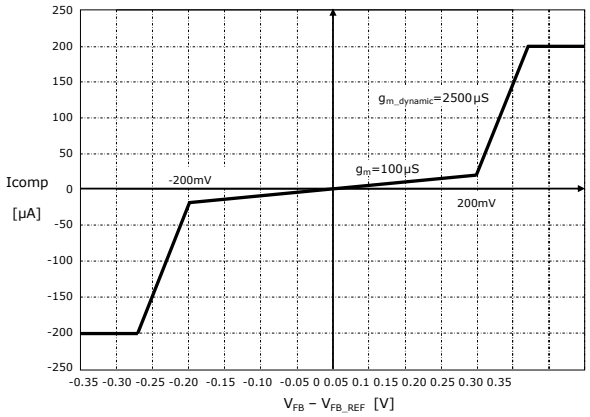
This current is delivered to the frequency compensation network, which is connected between the COMP pin and ground. This network determines the performance of the boost PFC converter both in terms of input power factor and THD of the input current, and in terms of dynamic response to line or load changes.

The OTA in the L6462A mediates between these two requirements with a specially shaped no linearity of its transconductance g_m.

As shown in Figure 16, g_m has quite a low value around the steady-state operating point (V_{FB} = V_{FB_REF}) and rapidly increases as V_{FB} significantly deviates from V_{FB_REF}. In this way, under steady-state conditions, the overall loop gain at twice the line frequency can be easily kept low enough for the input current distortion due to the residual AC ripple superimposed on V_{COMP} to be low as well.

On the other hand, if perturbations in line or load conditions cause the output voltage to significantly deviate from its steady-state value (which is reflected in a proportional deviation of V_{FB} from V_{FB_REF}), the gain-bandwidth product of the voltage loop will increase, resulting in a quicker response to such perturbations than with a conventional linear gain characteristic.

Figure 16. **OTA characteristic vs. input voltage differential from reference**



5.6 No-load operation (burst-mode function)

To avoid an uncontrolled rise of the output voltage at light or zero load, when $V_{COMP} < V_{COMP\_BM}$ (0.3 V typ.), the device stops the switching activity and reduces its power consumption. As soon as the $V_{COMP} > V_{COMP\_BM} + V_{COMP\_Hys}$ (25 mV typ., and in tracking with the threshold V_{COMP_BM}), the device restarts the switching activity.

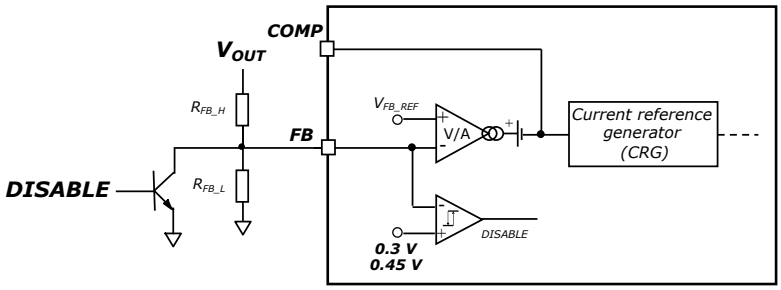
If the burst-mode condition is triggered when the gate driver GD/ZCD is “high”, the device completes the current ON-time and the system stoppage takes place after the GD/ZCD falling edge.

5.7 Disable operation

When forcing the FB pin lower than the internal threshold V_{FB_DIS} (300 mV typ.), the device stops operation and enters low-power consumption (the error amplifier is turned off). Once the FB pin is released, the device starts operation as soon as the FB pin (pulled up by the R_{FB_H} resistor connected to the output voltage) is higher than the internal threshold V_{FB_EN} (450 mV typ.).

A de-bounce time T_{DIS_DB} (50 µs typ.) is provided to avoid false triggering.

Figure 17. **Disable function - circuit details**



5.8 Protections

A comprehensive set of protections is embedded to ensure a high level of reliability of the final application without adding extra components and/or circuitry.

5.8.1 Output overvoltage (OVP)

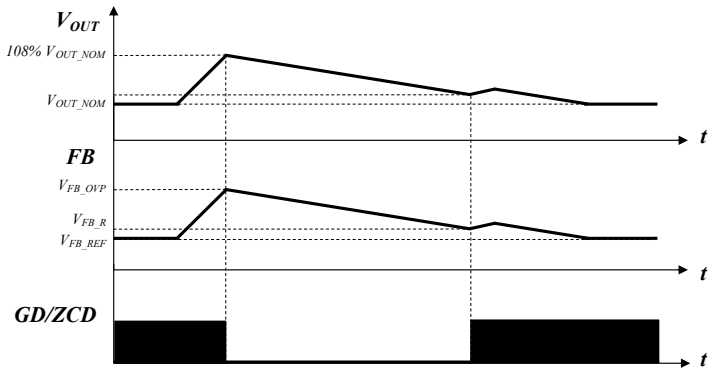
To limit an output voltage overshoot, e.g. due to a heavy load release or at start-up with light-load, the device stops the switching activity as soon as the instantaneous output voltage V_{OUT} is higher than 8% typ. compared to the programmed value.

In fact, the device detects an overvoltage condition by monitoring the FB pin, which is proportional to the instantaneous value of the output voltage V_{OUT} and, in steady-state conditions, sits at the internal reference of the error amplifier (V_{FB_REF} = 2.5 V).

As soon as the FB voltage exceeds the steady-state value by 8% ($V_{FB} > V_{FB\_OVP}$), the switching activity is stopped until it returns closer to it ($V_{FB} < V_{FB\_R}$).

A de-bounce time T_{DOVP_DB} (50 µs typ.) is provided to avoid false activation of the protection.

Figure 18. OVP timing



5.8.2 Overcurrent (OCP1)

To limit the peak inductor current in case of an extra request (e.g. heavy load changes), the device implements a cycle-by-cycle overcurrent protection. The device monitors the CS pin during the power switch on-time and, as soon as the voltage on the CS pin goes above V_{CS_OCP1} (500 mV typ. at low-line and 330 mV typ. at high AC line), the internal overcurrent comparator is triggered and terminates the conduction cycle of the power switch before the normal PWM circuit does. In this way, the peak inductor current is limited to a maximum of V_{CS_OCP1}/R_S.

5.8.3 Inductor saturation detection (OCP2)

A second overcurrent level set at V_{CS_OCP2} (750 mV typ. at low-line and 500 mV typ. at high-line) detects abnormal current values (e.g. due to boost inductor saturation) and, if this is the case for two consecutive switching cycles, activates a safety procedure that immediately stops the converter for T_{OCP2} time (1 ms typ.) and then restarts. During OCP2 condition, the device sinks a current (3 mA typ.) from the COMP pin to discharge the external compensation network.

5.8.4 Feedback failure detection

The device handles the possible disconnection of the output voltage feedback by checking the FB pin. If the pin voltage goes below the V_{FB_DIS} threshold (300 mV typ.), the device stops operation immediately.

5.9 Line feedforward

To keep the maximum output power deliverable by the converter almost constant with regards to to the AC input voltage, a two-level discrete voltage feedforward is integrated in the controller. Basically, the AC input voltage is internally rebuilt and compared with a fixed threshold to properly set the value of the equivalent multiplier gain G_{CR} (see Table 5 for details).

The controller starts operation by selecting the multiplier gain G_{CR}=0.58 typ. (low AC line condition) and then, once the AC input voltage becomes higher than the high-line AC input threshold, $Line_H$ (see Table 5) the controller reduces the multiplier gain G_{CR}= 0.125 typ. (high AC line condition). The controller implements a hysteresis, typically in the range of 4 V to 20 V, to avoid unwanted commutations in case of very slow transition of the AC input voltage.

The proper operation of the converter, with the right G_{CR} multiplier gain, is then guaranteed for an AC input voltage below 140 V_{rms} and above 175 V_{rms} in a 400 V_{OUT} application.

In case of a different V_{OUT} output voltage setpoint, it is necessary to consider that the resulting feedforward input voltage threshold follows this equation:

Equation 10

$$Vinrms_{\_TH\_H} = Line_H \cdot \frac{V_{OUT}}{400V} \quad (10)$$

where $Line_H$ is the high-line AC input threshold and where V_{OUT} is the programmed output voltage.

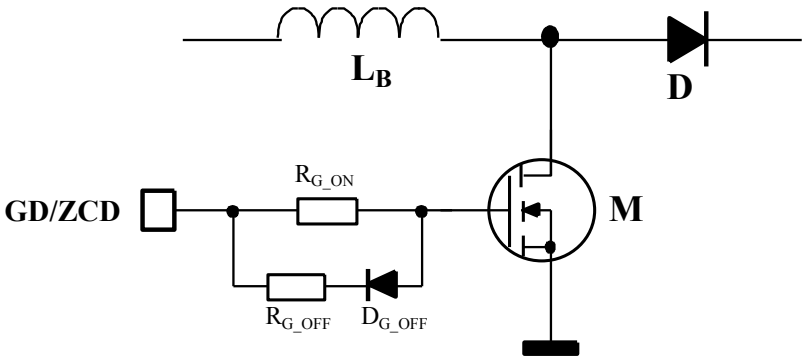
5.10 Gate driver

The GD/ZCD pin is the output of the driver block and is able to drive an external power MOSFET with at least 0.3 A source and 0.6 A sink capability.

The high-level voltage of this pin (V_{GDH}) is internally clamped at 10 V typ. to avoid excessive gate voltages in case the controller is supplied with a high V_{CC} value.

To avoid undesired switch-on of the external MOSFET due to any leakage current when the supply of the L6462A is below the UVLO threshold, an internal pull-down circuit holds the pin low (the circuit guarantees 1.1 V maximum at I_{SINK}=1 mA). In case of using an external pull-down gate resistor, select a value > 100 kΩ to avoid reducing the sensitivity of the ZCD detection circuitry.

Figure 19. Typical gate driver network



A gate resistor R_{G_ON} in series with the GD/ZCD pin is typically added to limit the high dv/dt at power MOSFET turn-on. To avoid excessive slowdown at power MOSFET turn-off, a second resistor R_{G_OFF} plus a signal diode can be used as shown in Figure 19.

Typical values of these resistors are in the range of 15 Ω÷30 Ω for R_{G_ON} and 4.7 Ω÷10 Ω for R_{G_OFF} in a standard PCB layout. In case of a PCB layout with long GD/ZCD and power GND return tracks, higher gate resistor values should be used to avoid excessive high-frequency spikes due to parasitic inductance (e.g., 30 Ω÷47 Ω for R_{G_ON} and 8.2 Ω÷20 Ω for R_{G_OFF}).

5.11 Layout guidelines

The L6462A does not require any special attention to its layout, only that the general layout rules for any switching power converter be carefully applied.

Referring to Figure 20, the basic rules are:

• Keep the power and GND signal separated. Connect the return pins of the components carrying the high current switched at high frequency, such as the PFC sense resistor (R_S), the input and output capacitors (C_{IN}, C_{OUT}) as close as possible. This point is the GND star point. A downstream converter must be connected to this return point.

• Connect the GND pin (#3) to the GND star point, making the connections as short as possible and using a track width suitable to minimize its impedance. Keep this connection separated from any other GND connection, especially if carrying high currents.

• Minimize the length of the tracks relevant to the boost inductor (L_B), MOSFET drain (M), boost rectifier (D) and the output capacitor (C_{OUT}).

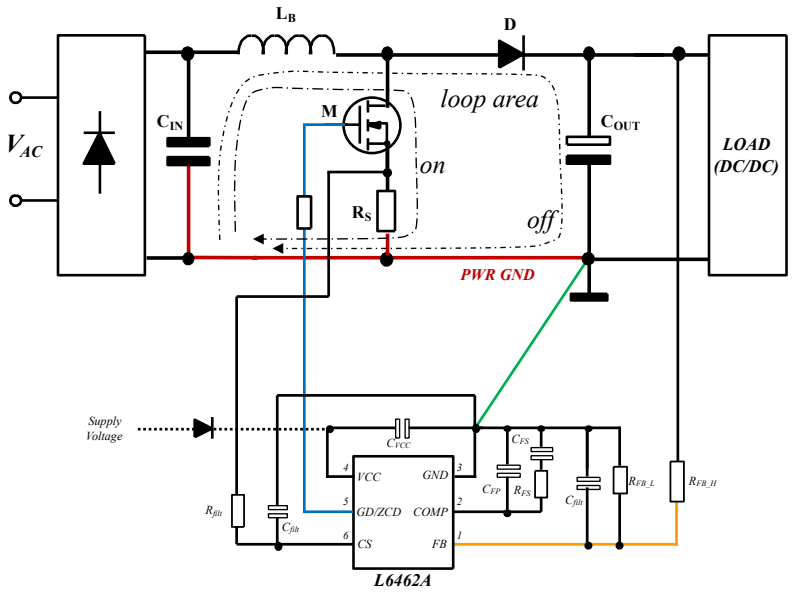
• Minimize the track length of the GD/ZCD pin (blue net) and keep it away from other high dV/dt signal tracks (to avoid noise injection during valley detection time).

• Minimize the track length of the FB pin and keep it away from high dV/dt signal tracks, such as the MOSFET drain (FB is a high-impedance pin).

• Minimize the loop area of the high-frequency paths (dotted lines).

• Minimize the length of the power GND return paths (red nets).

Figure 20. Power section and signal component connections



• Place the V_{CC} ceramic filter capacitor (e.g., 100 nF÷1 µF) close to the L6462A controller, connecting it to the VCC pin (#4) and to the GND pin (#3).

• Keep signal components as close as possible to each relevant pin of the L6462A. Specifically:

• Place the compensation network (C_{FP}, R_{FS}, C_{FS}) close to the COMP pin (#2) and connected to GND signal.

• Place the current sense filter (C_{filt}, R_{filt}) close to the CS pin (#6) and connected to GND signal.

• Place the output voltage resistors divider (R_{FB_L}, R_{FB_H}) close to the FB pin (#1) and connected to GND signal.

• Place the high-frequency filter of the feedback net (C_{filt}) close to the FB pin (#1) and connected to GND signal.

6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-6L package information

Figure 21. SOT23-6L package information

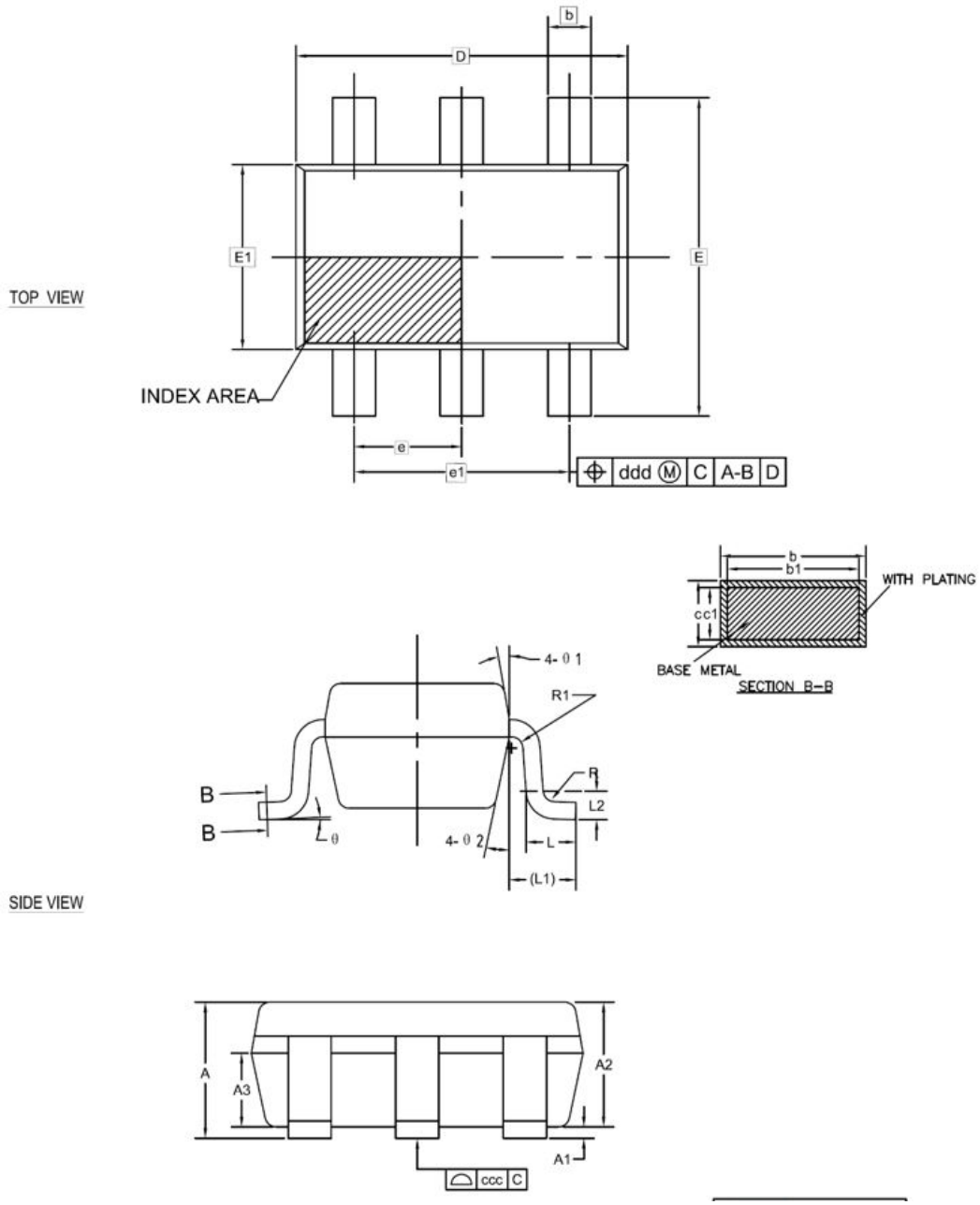
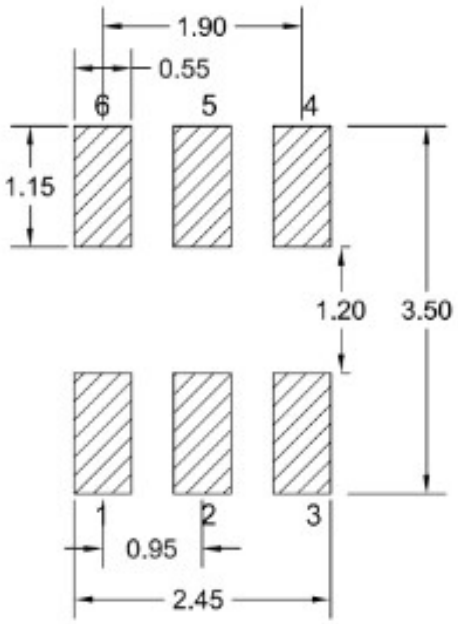


Table 6. **SOT23-6L package mechanical data**

DATABOOK			
Symbol	**Min.**	**Nom.**	**Max.**
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.34	-	0.45
b1	0.34	0.38	0.41
c	0.12	-	0.20
c1	0.12	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.700
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.40	0.60
L1	0.59REF		
L2	0.25REF		
R	0.05	-	0.20
R1	0.05	-	0.20
θ	0°	-	8°
Θ1	8°	10°	12°
θ	10°	12°	14°

Figure 22. **SOT23-6L recommended footprint, dimensions in mm (inches)**



7 Ordering information

Table 7. **Ordering information**

Order code	Package	Packing
L6462A	SOT23-6L	Tape and reel

Revision history

Table 8. **Document revision history**

Date	Version	Changes
14-Oct-2025	1	Initial release.
05-Nov-2025	2	Watermark removal.
07-Nov-2025	3	• Added sustainability label • Update the features

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.