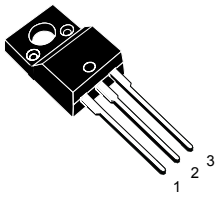
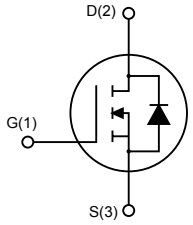
N-channel 200 V, 0.29 Ω typ., 9 A, STripFET™ Power MOSFET in a TO-220FP package



TO-220FP



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
IRF630FP	200 V	0.40 Ω	9 A

- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Gate charge minimized

Applications

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

STPOWER

Product status link
IRF630FP

Product summary	
Order code	IRF630FP
Marking	IRF630FP
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DDS}	Drain-source voltage (V_{GS} = 0 V)	200	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	9	A
	Drain current (continuous) at T_C = 100 °C	6.5	A
I_{DM}(1)	Drain current (pulsed)	36	A
P_{TOT}	Total power dissipation at T_C = 25 °C	36	W
E_{AS}(2)	Single pulse avalanche energy	110	mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2000	V
dv/dt(3)	Drain-body diode dynamic dv/dt ruggedness	5.8	V/ns
T_{stg}	Storage temperature range	-65 to 175	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *Starting T_J = 25 °C, I_D = 4.5 A*
3. *I_{SD} = 9 A, di/dt = 520 A/µs, V_{DD} = 50 V, T_J < T_{Jmax}*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	4.17	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

T_{CASE} = 25 °C unless otherwise specified

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	200			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 200 V			1	µA
		V_{GS} = 0 V, V_{DS} = 200 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A		0.29	0.40	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	370	-	pF
C_{oss}	Output capacitance		-	77	-	pF
C_{rss}	Reverse transfer capacitance		-	14	-	pF
Q_g	Total gate charge	V_{DD} = 160 V, I_D = 9 A V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	11.6	-	nC
Q_{gs}	Gate-source charge		-	2.2	-	nC
Q_{gd}	Gate-drain charge		-	5.5	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V, I_D = 4.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	5.6	-	ns
t_r	Rise time		-	2.6	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 9 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs, V_{DD} = 50 V (see Figure 17. Switching time waveform)	-	118.5		ns
Q_{rr}	Reverse recovery charge		-	393		nC
I_{RRM}	Reverse recovery current		-	6.6		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

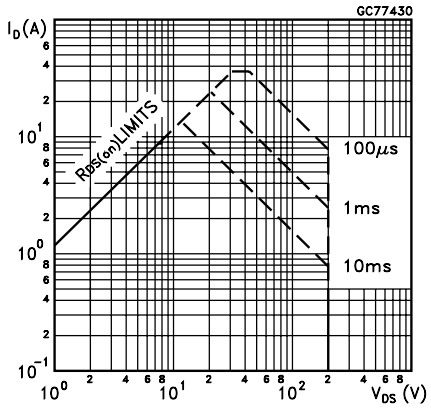


Figure 2. Thermal impedance

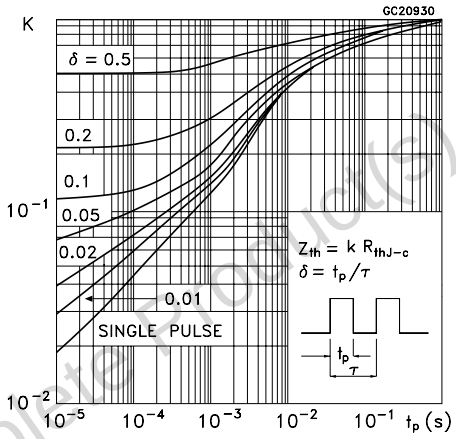


Figure 3. Output characteristics

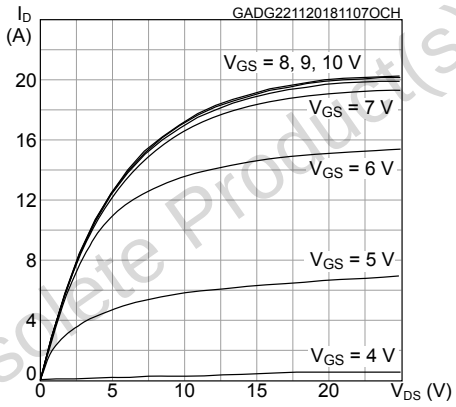


Figure 4. Transfer characteristics

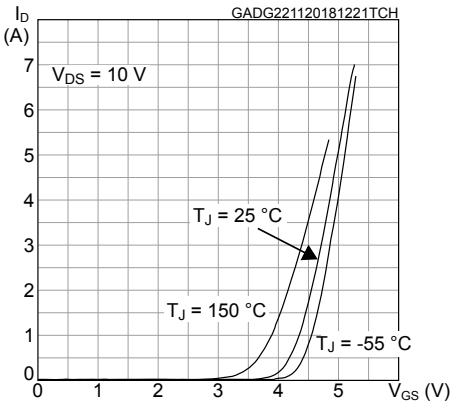


Figure 5. Gate charge vs gate-source voltage

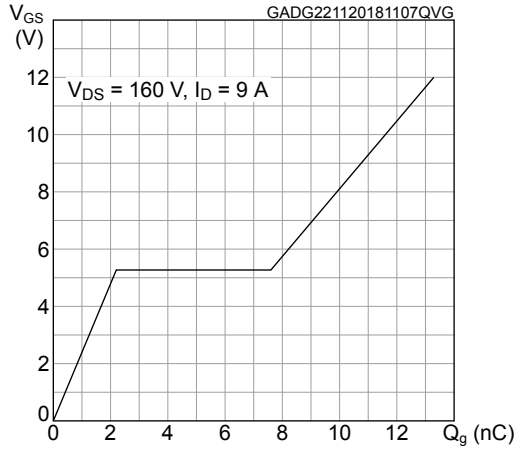


Figure 6. Static drain-source on-resistance

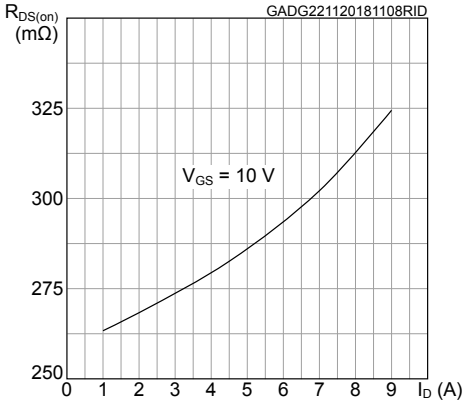


Figure 7. Capacitance variations

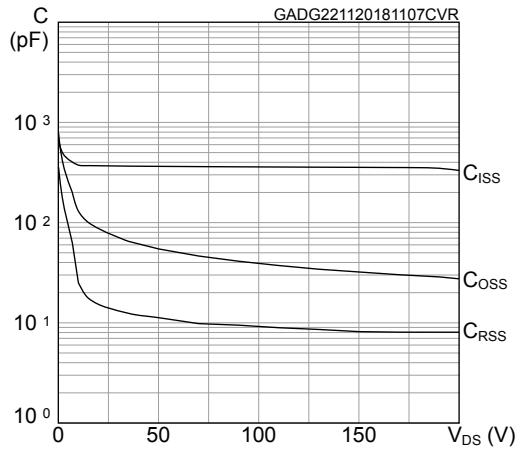


Figure 8. Normalized gate threshold voltage vs temperature

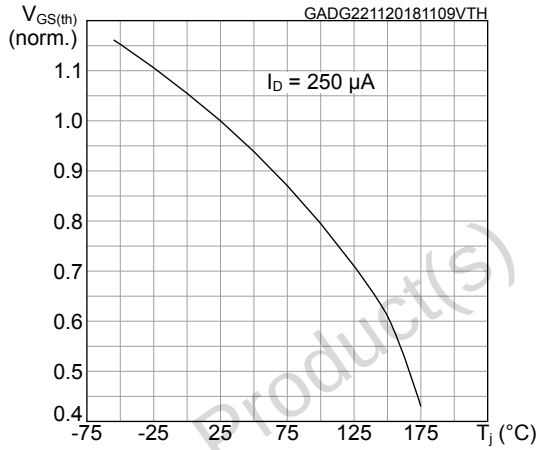


Figure 9. Normalized on-resistance vs temperature

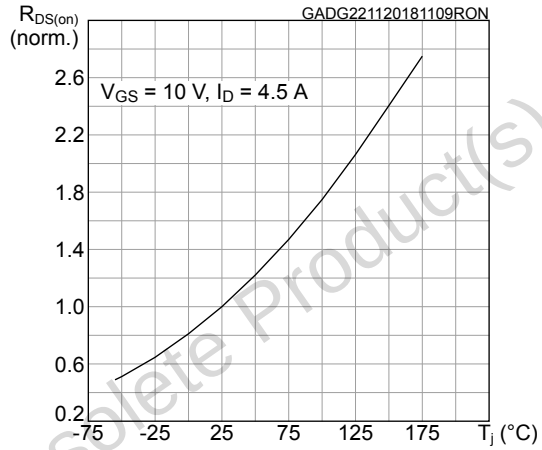


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

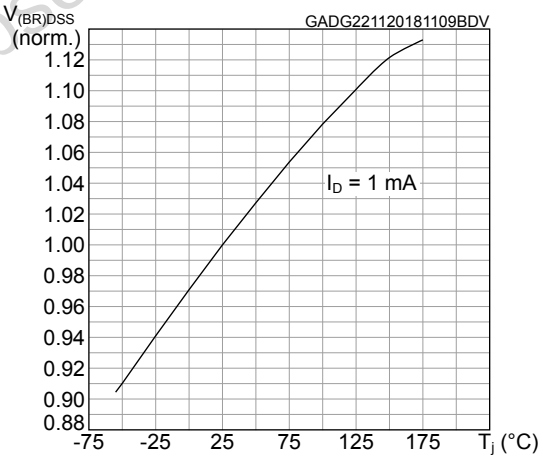
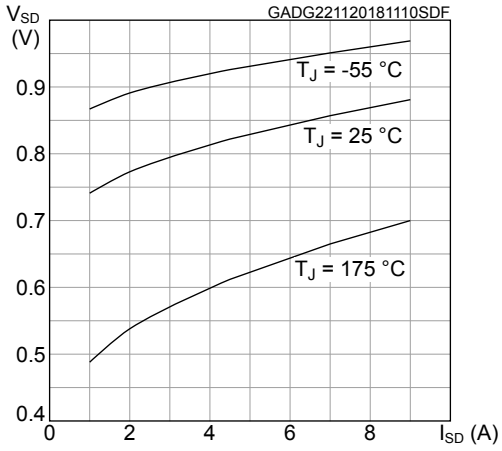


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

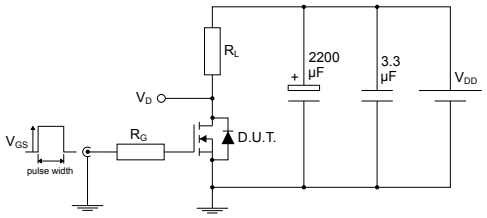


Figure 13. Test circuit for gate charge behavior

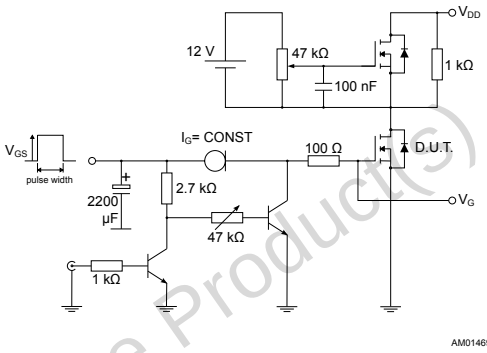


Figure 14. Test circuit for inductive load switching and diode recovery times

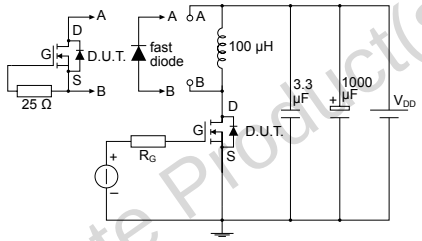


Figure 15. Unclamped inductive load test circuit

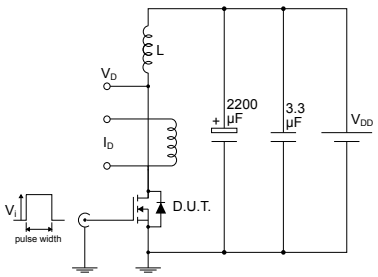


Figure 16. Unclamped inductive waveform

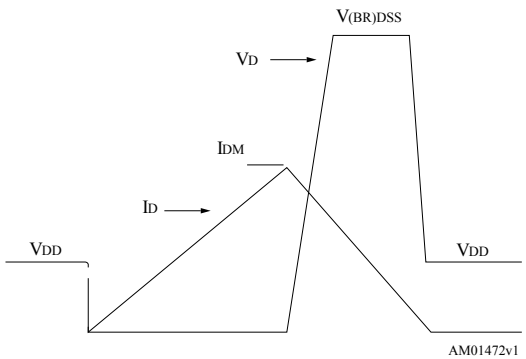
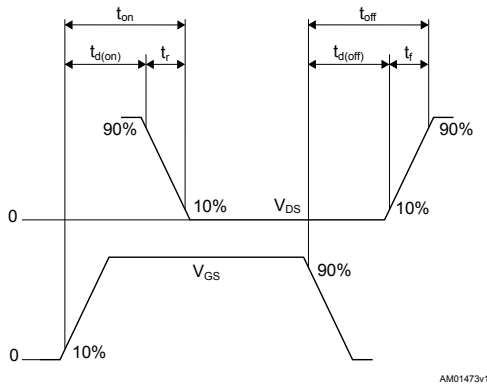


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 18. **TO-220FP package outline**

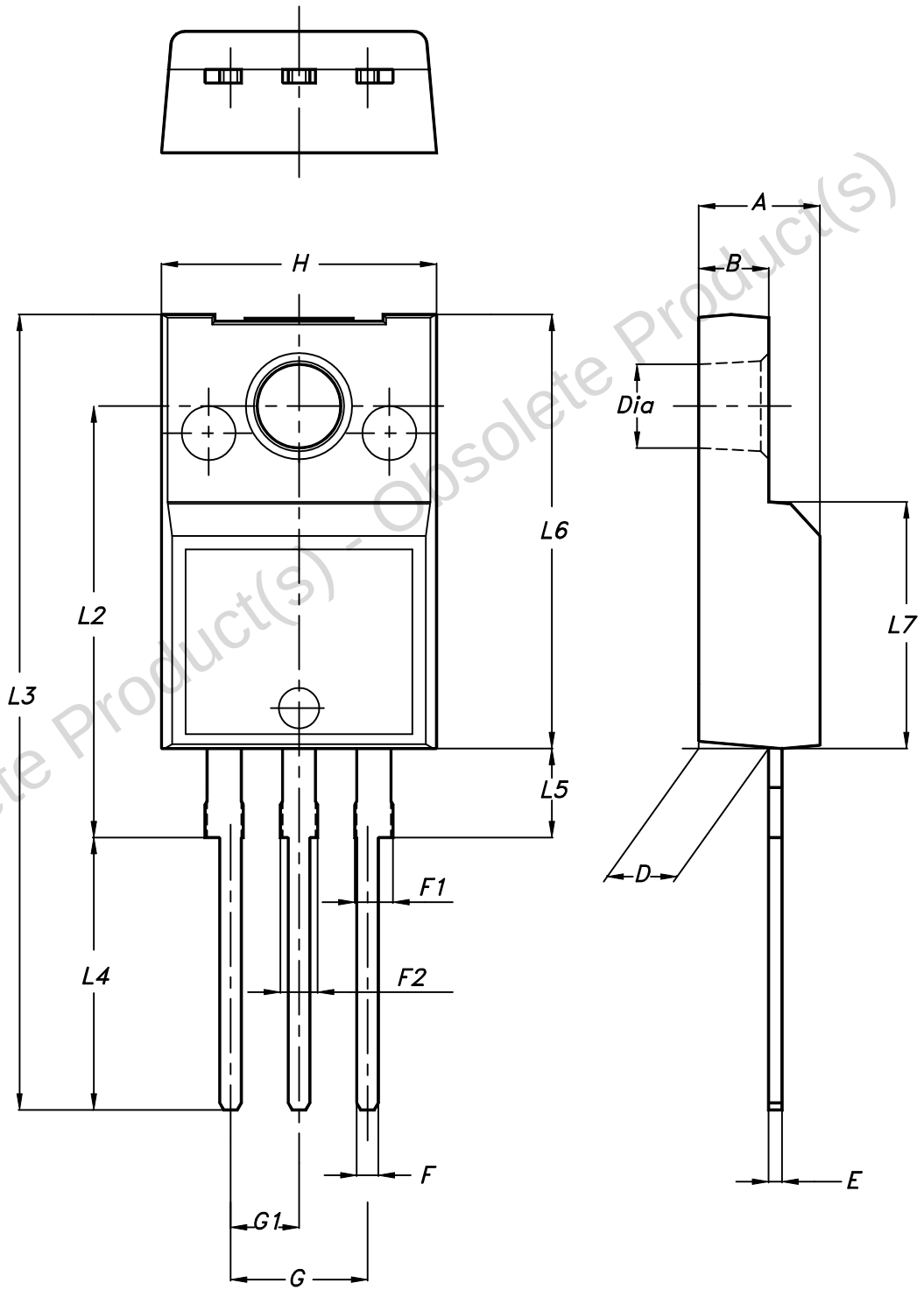


Table 7. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 8. **Document revision history**

Date	Version	Changes
10-Jan-2019	1	First release. This part number was previously included in datasheet DS0668.

Contents