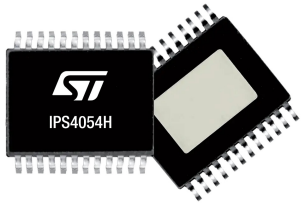
IPS4054H

Datasheet

Quad channel high-side switch with current sense



Product status link

IPS4054H

Product label

SUSTAINABLE TECHNOLOGY

Features

- $R_{ON(Max.)}$ (@T_J = 25 °C) = 27 mΩ
- Very low standby current
- 3.3 V CMOS compatible inputs
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- Proportional load current sense
- Very low current sense leakage
- High current sense precision for wide range currents
- Current sense disable
- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of VCC
- Designed to drive DC-13 loads according to EN 60947-5-1
- Designed to meet IEC 61131-2, IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- PowerSSO-24 package

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Suitable as LED driver
- General high-side switch applications

Description

The IPS4054H is a monolithic device made using STMicroelectronics VIPower technology, intended for driving resistive, inductive and capacitive loads with one side connected to the ground. Active VCC pin voltage clamp protects the device against low energy spikes.

The device integrates an analog current sense, which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. The sensed current of each output channel $OUTPUT_X$ is available on the correspondent current sense pin $CURRENT\ SENSE_X$.

When CS_DIS is driven high, the current sense pin is in a high impedance condition.

In case of overtemperature, fault condition is reported via the current sense pin.

Output current limitation protects the device in overload conditions. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shutdown intervention.

Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

1 Block diagram and pin description

Figure 1. Block diagram

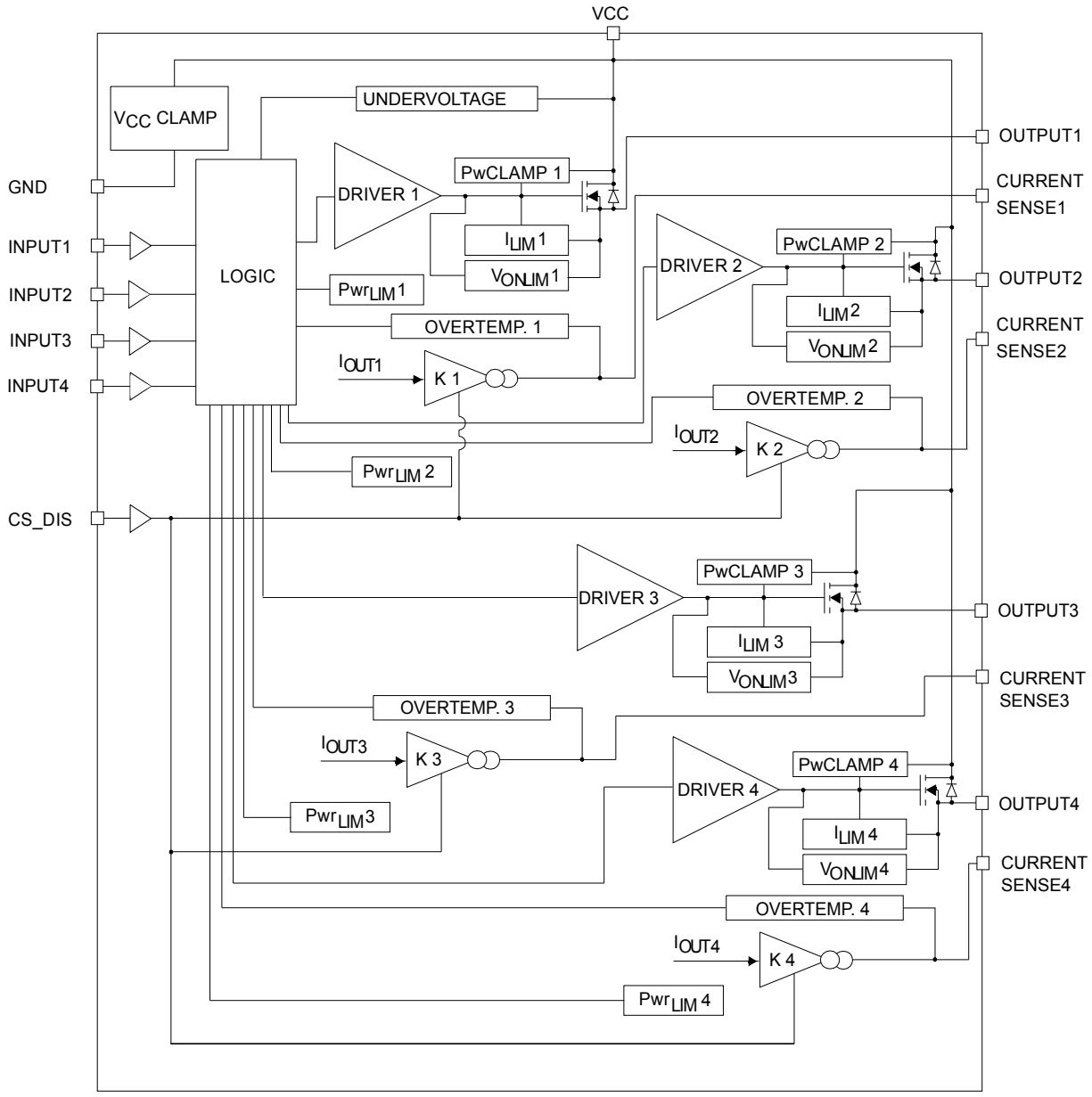


Table 1. Pin function

Pin	Name	Type	Function
1, 12, TAB	VCC	Supply	Power supply
2	GND	Supply	Ground connection
3	INPUT1	Logic input	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state for channel 1
4	CURRENT SENSE1	Analog output	Analog current sense pin for channel 1, it delivers a current proportional to the load current
5	INPUT2	Logic input	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state for channel 2
6	CURRENT SENSE2	Analog output	Analog current sense pin for channel 2, it delivers a current proportional to the load current
7	INPUT3	Logic input	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state for channel 3
8	CURRENT SENSE3	Analog output	Analog current sense pin for channel 3, it delivers a current proportional to the load current
9	INPUT4	Logic input	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state for channel 4
10	CURRENT SENSE4	Analog output	Analog current sense pin for channel 4, it delivers a current proportional to the load current
11	CS_DIS	Logic input	Active high CMOS compatible pin, to disable the current sense pin
13 to 15	OUTPUT4	Analog output	Power output channel 4
16 to 18	OUTPUT3	Analog output	Power output channel 3
19 to 21	OUTPUT2	Analog output	Power output channel 2
22 to 24	OUTPUT1	Analog output	Power output channel 1

Figure 2. Configuration diagram PowerSSO-24 (top view)

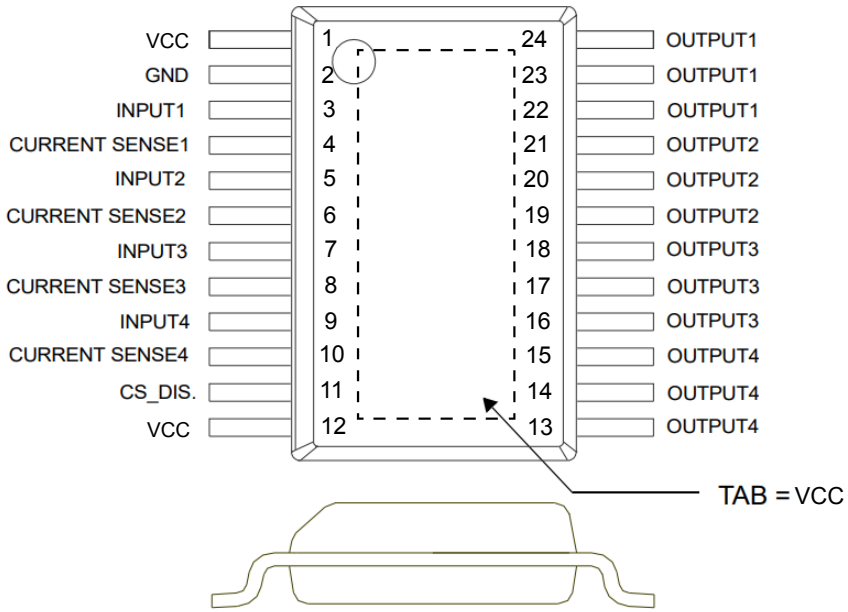


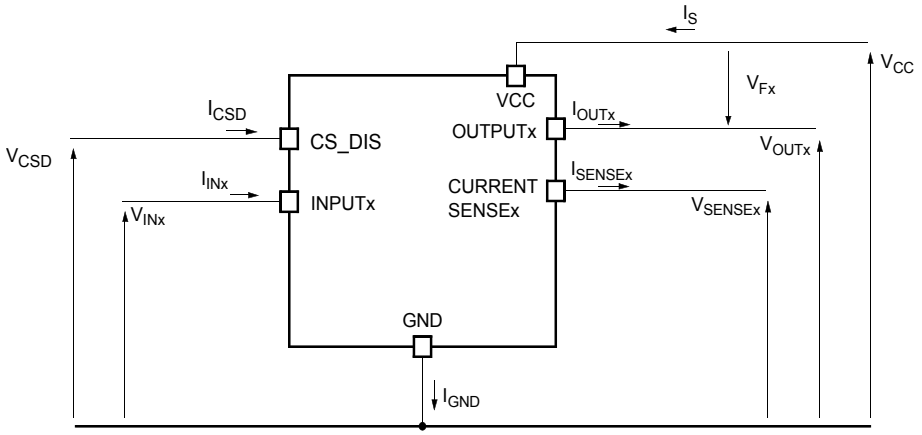
Table 2. Suggested connections for unused pins

Connection/pin	Current Sense	Output	Input	CS_DIS
Floating	Not Recommended	X	X	X
To ground	Through 1 kΩ resistor	Not Recommended	Through 10 kΩ resistor	Through 10 kΩ resistor

Note: X = don't care.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: $V_{Fx} = V_{OUTx} - V_{CC}$ during reverse polarity condition.

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC supply voltage		41	V
$-V_{CC}$	Reverse DC supply voltage		0.3	V
$-I_{GND}$	DC reverse ground pin current		200	mA
I_{OUT}	DC output current		Internally limited	A
$-I_{OUT}$	Reverse DC output current		24	A
I_{IN}	DC input current		-1 to 10	mA
I_{CSD}	DC current sense disable input current		-1 to 10	mA
$-I_{SENSEx}$	DC reverse CS pin current		200	mA
V_{SENSEx}	Current sense maximum voltage		V_{DEMAG} to V_{CC}	V
E_{MAX}	Maximum switching energy L = 0.8 mH; R_L = 0 Ω; V_{CC} = 13.5 V; Tjstart = 150 °C; I_{OUT} = I_{LIML}(Typ.)		140	mJ
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 kΩ, C = 100 pF)	$INPUT_X$	4000	V
		CURRENT $SENSE_X$	2000	
		CS_DIS	4000	
		$OUTPUT_X$	5000	
		VCC	5000	
T_J	Junction operating temperature		-40 to 150	°C
T_{STG}	Storage temperature		-55 to 150	°C

2.2 Thermal data

Table 4. **Thermal data**

Symbol	Parameter	Max. Value	Unit
R_{thJC}	Thermal resistance, junction-to-case (with one channel ON)	1.35	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	See Figure 31	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 36 V, -40 °C < T_J < 150 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5		36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance (1)	I_{OUT} = 3 A, T_J = 25 °C			27	mΩ
		I_{OUT} = 3 A, T_J = 150 °C			54	
		I_{OUT} = 3 A, T_J = 25 °C, V_{CC}=5 V			37	
V_{clamp}	Clamp voltage	I_S = 20 mA	41	46	52	V
I_{LGND}	Output current at GND disconnection	V_{CC} = V_{IN} = V_{GND} = 24 V; V_{OUT} = 0 V			0.5	mA
I_S	Supply current	Off-state, V_{CC} = 13 V, T_J = 25 °C, V_{IN} = V_{OUT} = V_{SENSE} =V_{CSD}= 0 V,		2(2)	5(2)	µA
		On-state, V_{CC} = 13 V, V_{IN} = 5 V, I_{OUT} = 0 A		8	14	mA
$I_{L(off)}$	Off-state output current (3)	V_{IN} = V_{OUT} = 0 V, V_{CC} = 13 V, T_J = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V, V_{CC} = 13 V, T_J = 125 °C	0		5	
V_F	Output - V_{CC} diode voltage (4)	-I_{OUT} = 3 A, T_J = 150 °C			0.7	V

1. *For each channel.*
2. *Power MOSFET leakage included.*
3. *For each channel.*
4. *For each channel.*

Table 6. Switching (V_{CC} = 13 V, T_J = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 4.3 Ω (see Figure 8)		40		µs
$t_{d(off)}$	Turn-off delay time	R_L = 4.3 Ω (see Figure 8)		40		µs
$(dV_{OUT}/dt)_{(on)}$	Turn-on voltage slope	R_L = 4.3 Ω	see Figure 21			V/µs
$(dV_{OUT}/dt)_{(off)}$	Turn-off voltage slope	R_L = 4.3 Ω	see Figure 22			V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 4.3 Ω (see Figure 8)		0.2		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 4.3 Ω (see Figure 8)		0.3		mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	INPUT pin low level voltage				0.9	V
I_{IL}	INPUT pin low level current	V_{IN} = 0.9 V	1			µA
V_{IH}	INPUT pin high level voltage		2.1			V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IH}	INPUT pin high level current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	INPUT pin hysteresis voltage		0.25			V
V_{ICL}	INPUT pin clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
V_{CSDL}	CS_DIS pin low level voltage				0.9	V
I_{CSDL}	CS_DIS pin low level current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	CS_DIS pin high level voltage		2.1			V
I_{CSDH}	CS_DIS pin high level current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS pin hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS pin clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		V

Table 8. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	29	42	59	A
		5 V < V_{CC} < 36 V			59	
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V, T_R < T_J < T_{TSD}		16		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset status threshold(1)		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A, V_{IN} = 0 V, L = 6 mH	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 200 mA, T_J = -40 °C to 150 °C (see Figure 9)		25		mV

1. *See Section 3.3: Thermal shutdown for details.*

Table 9. Current sense (8 V < V_{CC} < 16 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A, V_{SENSE} = 0.5 V, V_{CSD} = 0 V; T_J = -40 °C to 150 °C	1680	2910	4120	
dK_0/K_0 (1)	Current sense ratio drift	I_{OUT} = 0.5 A, V_{SENSE} = 0.5 V, V_{CSD} = 0 V; T_J = -40 °C to 150 °C	-12		12	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A, V_{SENSE} = 4 V, V_{CSD} = 0 V; T_J = -40 °C	2050	2700	3410	
		I_{OUT} = 2 A, V_{SENSE} = 4 V, V_{CSD} = 0 V; T_J = 25 °C to 150 °C	2190	2700	3210	
dK_1/K_1(1)	Current sense ratio drift	I_{OUT} = 2 A, V_{SENSE} = 4 V, V_{CSD} = 0 V; T_J = -40 °C to 150 °C	-10		10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A, V_{SENSE} = 4 V, V_{CSD} = 0 V;	2260	2690	3160	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_2	I_{OUT}/I_{SENSE}	T_J = -40 °C				
		I_{OUT} = 3 A, V_{SENSE} = 4 V, T_J = 25 °C to 150 °C	2350	2690	3030	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 3 A, V_{SENSE} = 4 V, V_{CSD} = 0 V; T_J = -40 °C to 150 °C	-7		7	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A, V_{SENSE} = 4 V, V_{CSD} = 0 V; T_J = -40 °C	2490	2700	2870	
		I_{OUT} = 10 A, V_{SENSE} = 4 V, V_{CSD} = 0 V; T_J = 25 °C to 150 °C	2590	2700	2800	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 10 A, V_{SENSE} = 4 V, V_{CSD} = 0 V; T_J = -40 °C to 150 °C	-4		4	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{CSD} = 5 V, V_{IN} = 0 V, T_J = -40 °C to 150 °C	0		1	µA
		V_{CSD} = 0 V, V_{IN} = 5 V, T_J = -40 °C to 150 °C	0		2	
		I_{OUT} = 2 A, V_{SENSE} = 0 V, V_{CSD} = 5 V, V_{IN} = 5 V, T_J = -40 °C to 150 °C	0		1	
I_{OL}	Openload on-state current detection threshold	V_{IN} = 5 V, I_{SENSE}= 5 µA	5		30	mA
V_{SENSE}	Max. analog sense output voltage	I_{OUT} = 3 A, V_{CSD} = 0 V	5			V
V_{SENSEH}	Analog sense output voltage in over temperature condition	V_{CC} = 13 V, R_{SENSE} = 3.9 kΩ		9		V
I_{SENSEH}	Analog sense output current in over temperature condition	V_{CC} = 13 V, V_{SENSE} = 5 V		8		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} <4 V, 0.5 A < I_{OUT} < 10 A, I_{SENSE} = 90% of I_{SENSE} max (see Figure 4)		50	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} <4 V, 0.5 A < I_{OUT} < 10 A, I_{SENSE} = 10% of I_{SENSE} max (see Figure 4)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} <4 V, 0.5 A < I_{OUT} < 10 A, I_{SENSE} = 90% of I_{SENSE} max (see Figure 4)		70	300	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90 % of I_{SENSE} max, I_{OUT} = 90 % of I_{OUT} max, I_{OUT} max = 2 A (see Figure 5)			200	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pins	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 10 A, I_{SENSE} = 10% of I_{SENSE} max (see Figure 4)		100	250	µs

1. *Specified by design, not tested in production.*

Figure 4. **Current sense delay characteristics**

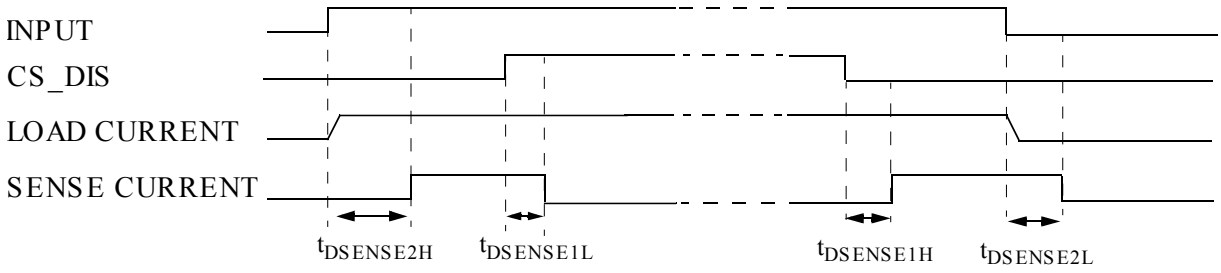


Figure 5. **Delay response time between rising edge of output current and rising edge of current sense for each channel (current sense enabled)**

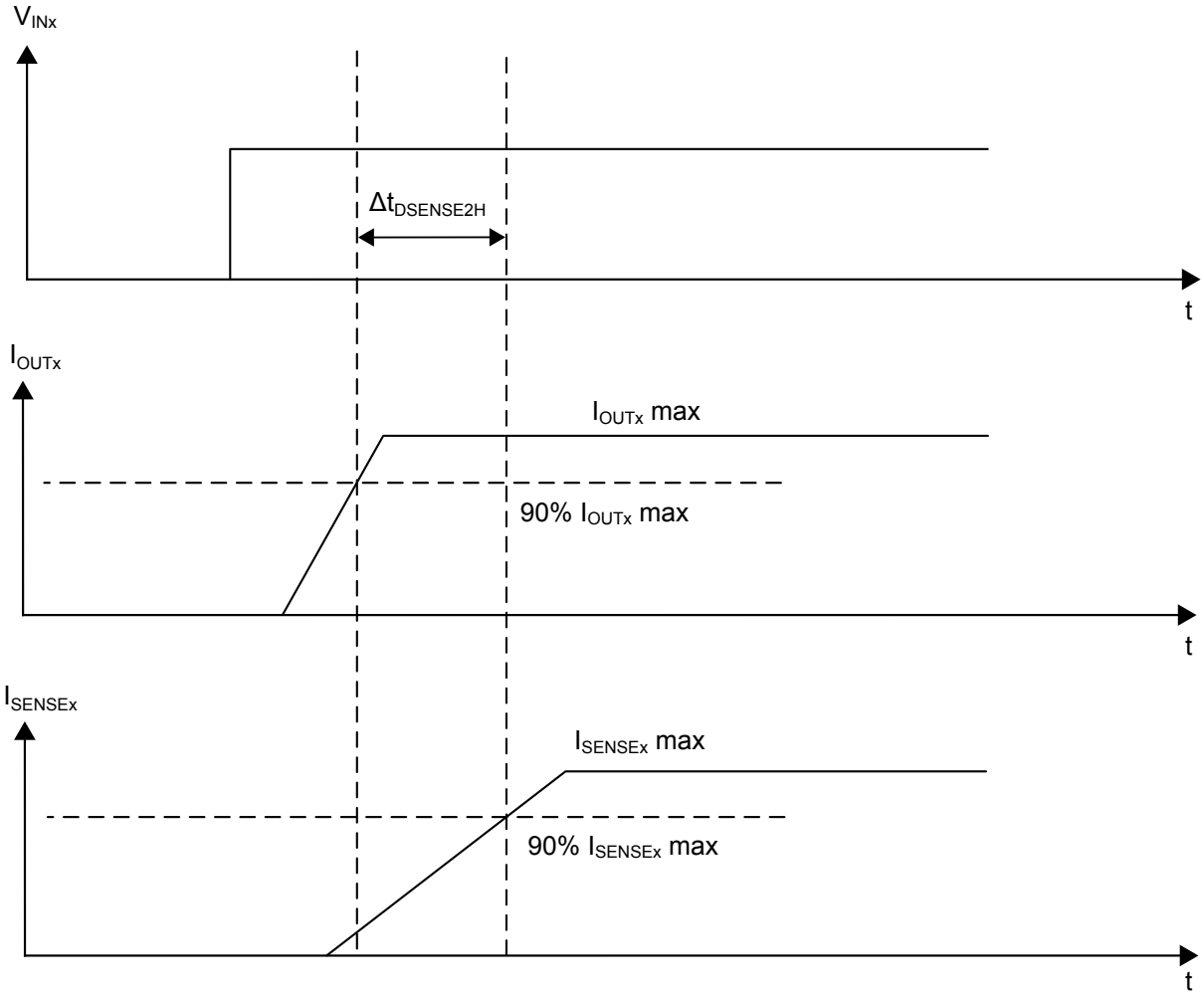


Figure 6. I_{OUT}/I_{SENSE} vs I_{OUT}

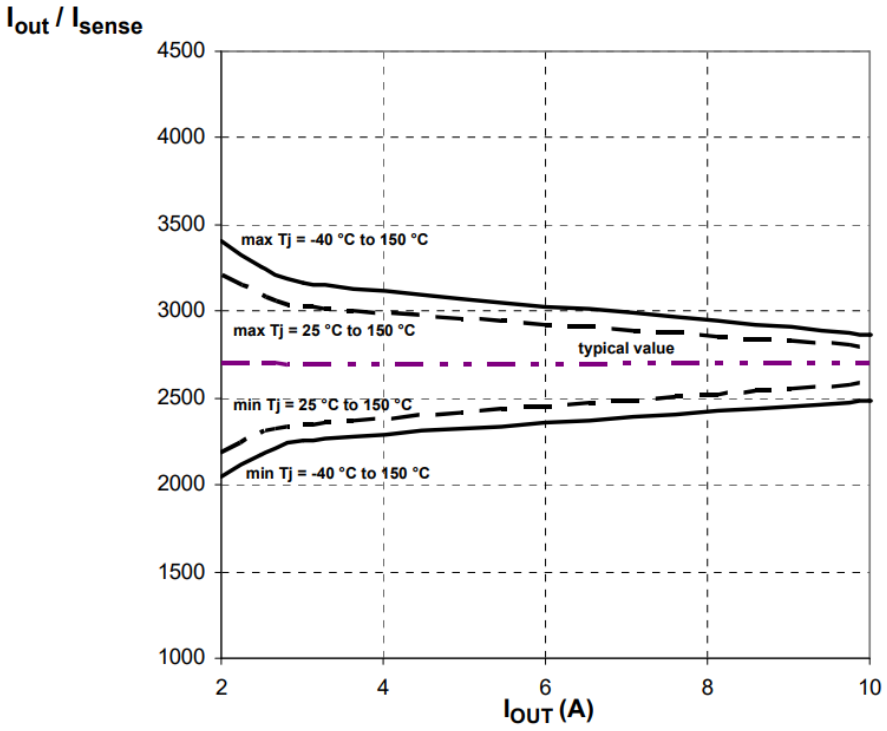


Figure 7. **Maximum current sense ratio drift vs load current**

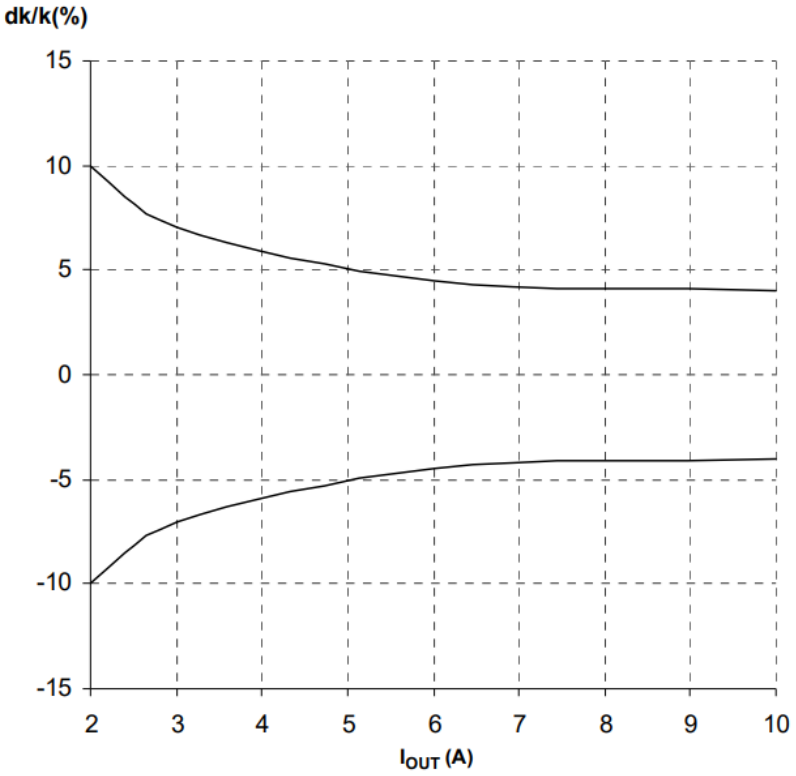


Table 10. Functional table

Device status	$INPUT_n$	$OUTPUT_n$	SENSE (V_{CSD}=0 V) (1)
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Short circuit to GND (Rsc ≤ 10 mΩ)	L	L	0
	H	L	0 if Tj < T_{TSD}
	H	L	V_{SENSEH} if Tj > T_{TSD}
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	Negative	0

1. *If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.*

Figure 8. Switching characteristics

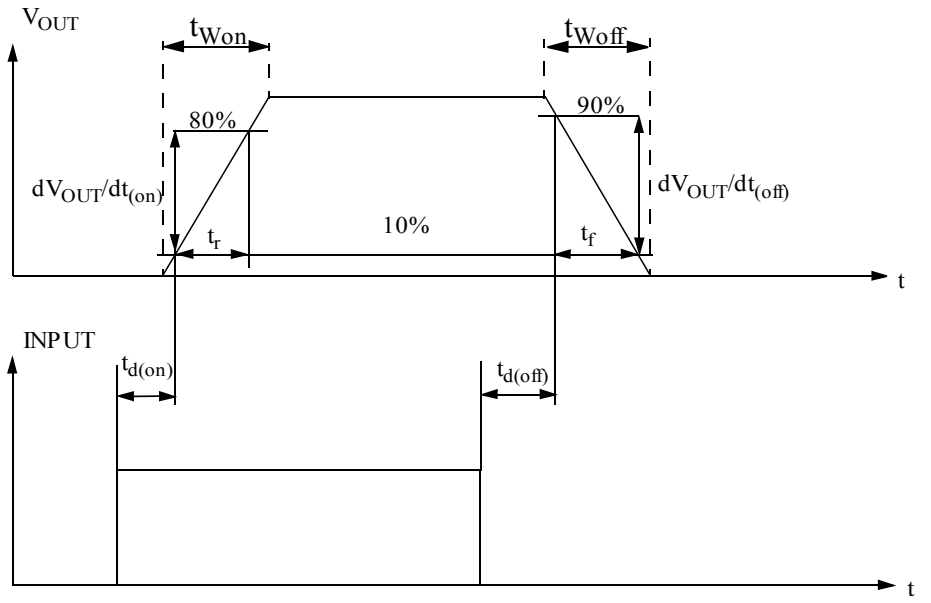


Figure 9. **Output voltage drop limitation**

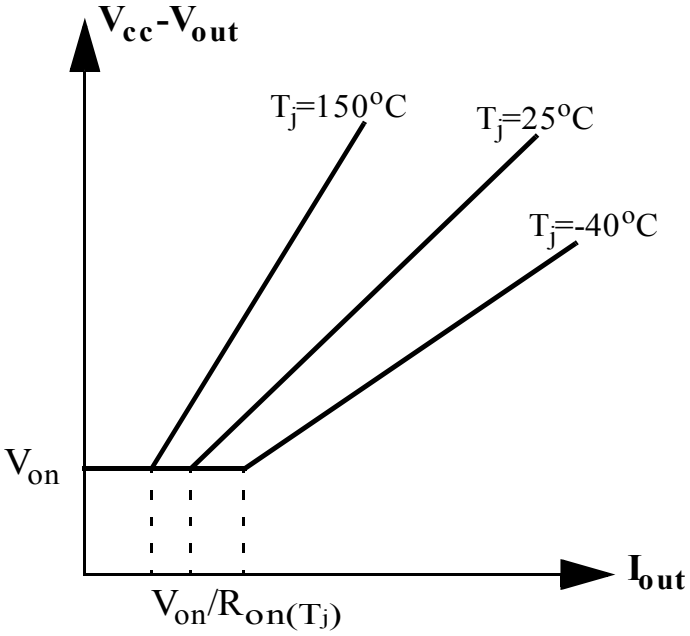
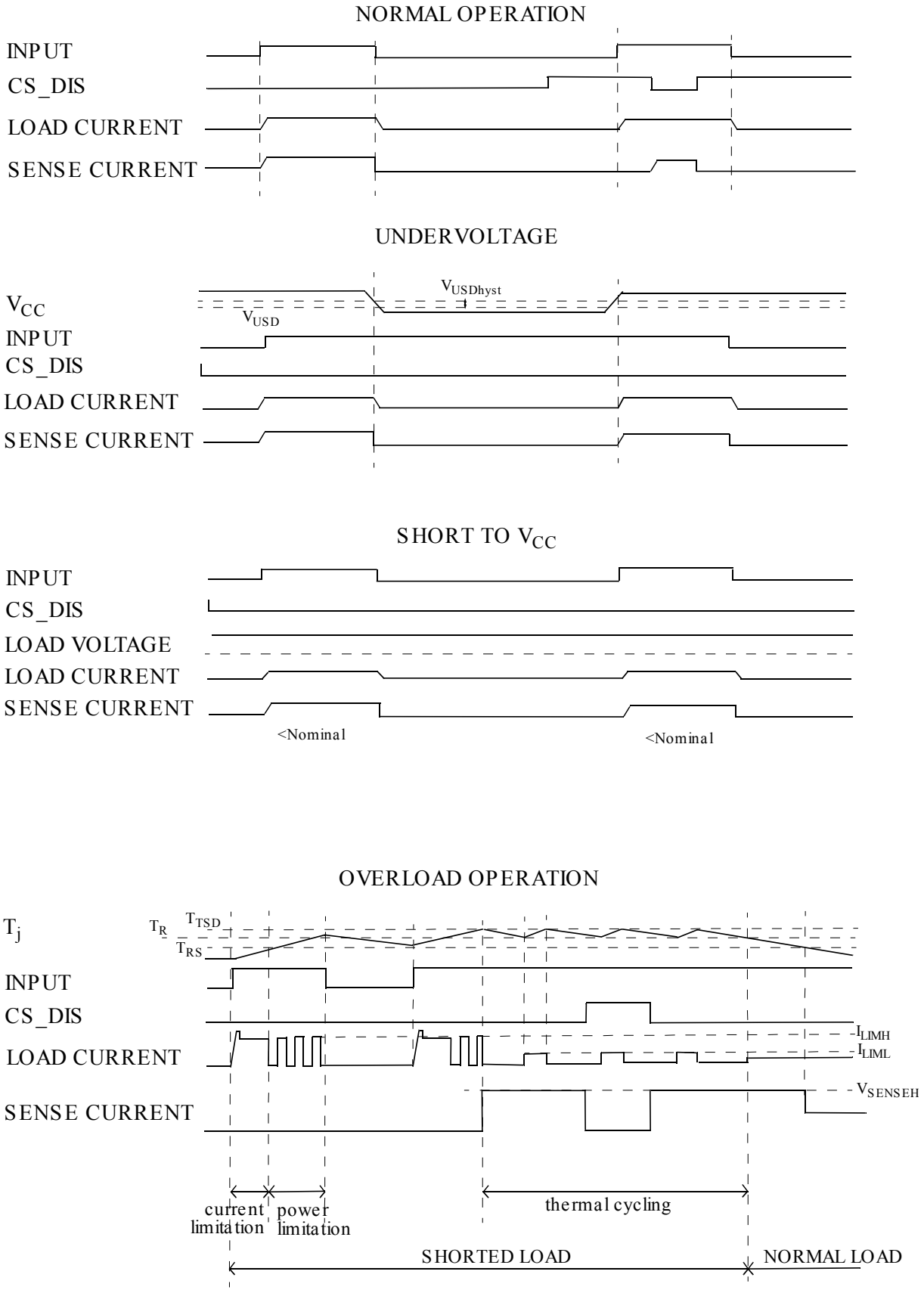


Figure 10. **Waveforms**



2.4 Electrical characteristics (curves)

Figure 11. Off-state output current

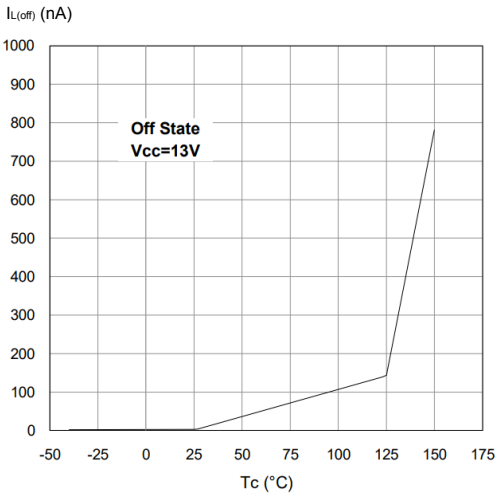


Figure 12. High level input current

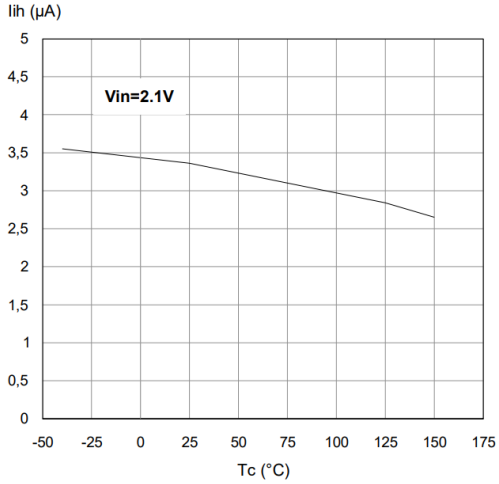


Figure 13. Input clamp voltage

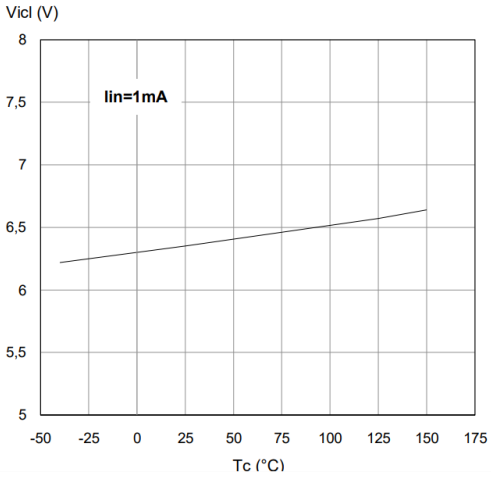


Figure 14. Input low level voltage

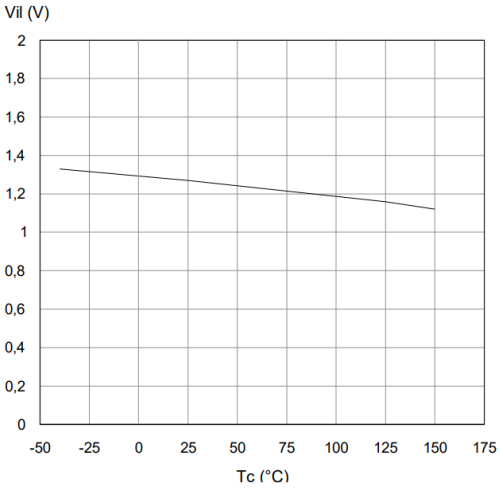


Figure 15. Input high level voltage

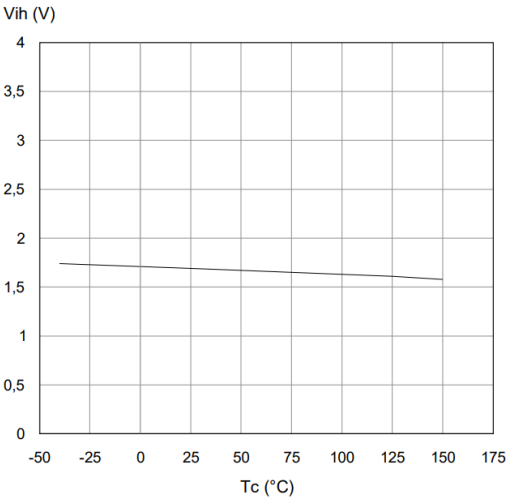


Figure 16. Input hysteresis voltage

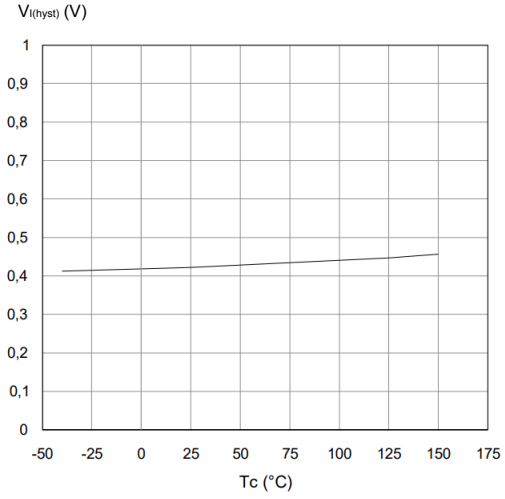


Figure 17. On-state resistance vs T_{CASE}

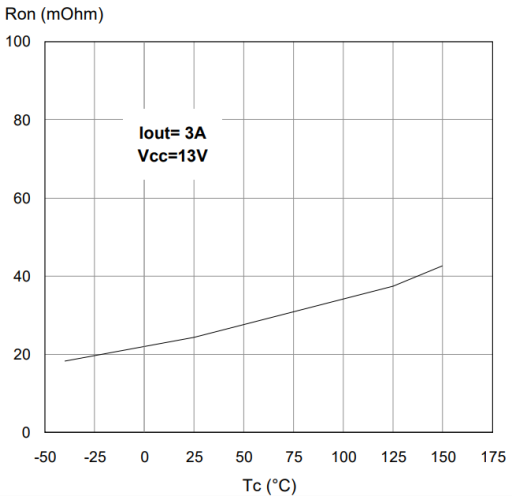


Figure 18. On-state resistance vs V_{CC}

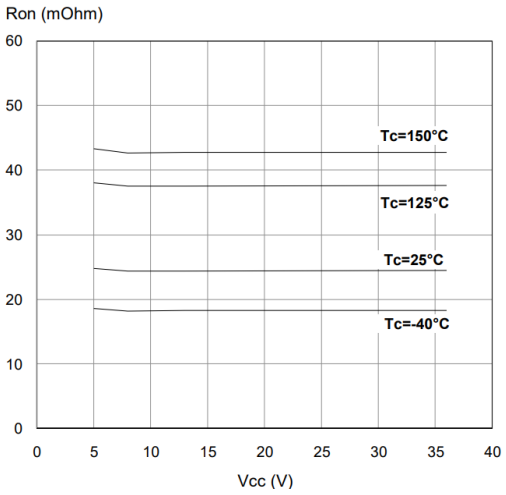


Figure 19. Undervoltage shutdown

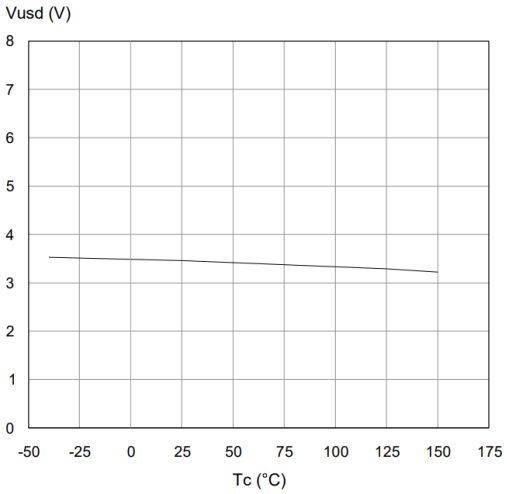


Figure 20. I_{LIMH} vs T_{CASE}

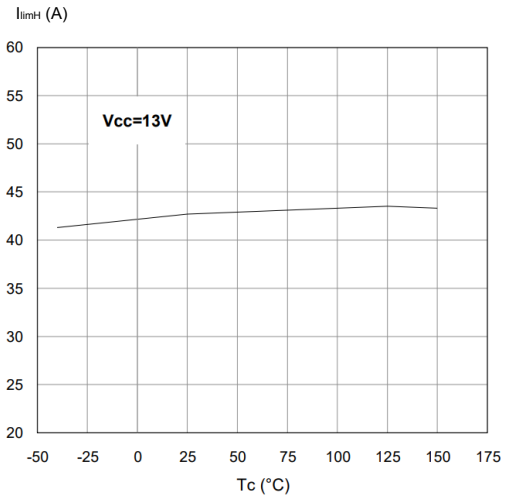


Figure 21. Turn-on voltage slope

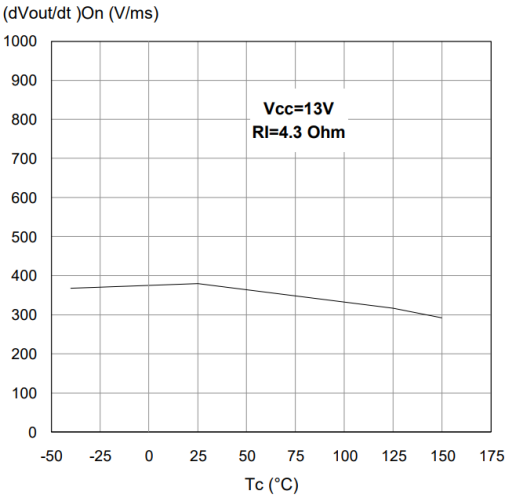


Figure 22. Turn-off voltage slope

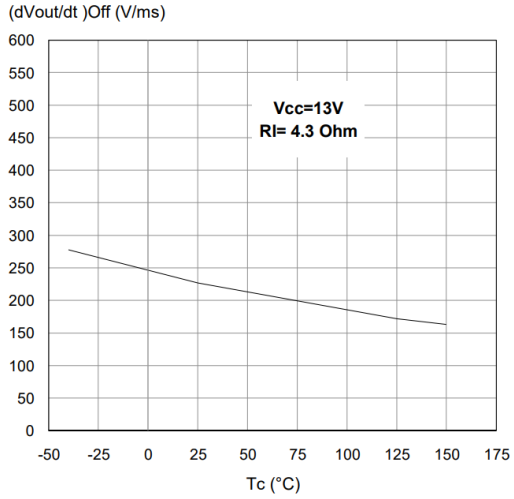


Figure 23. CS_DIS high level voltage

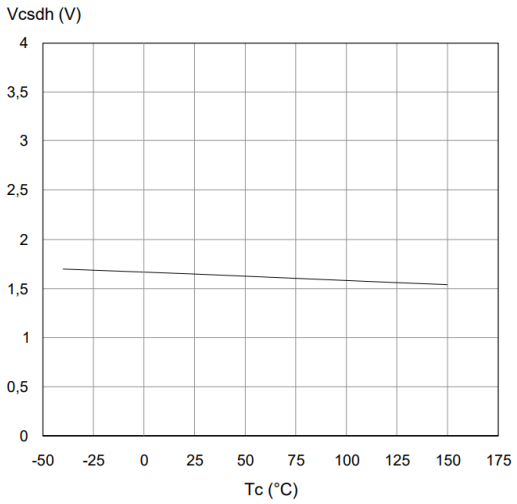


Figure 24. CS_DIS clamp voltage

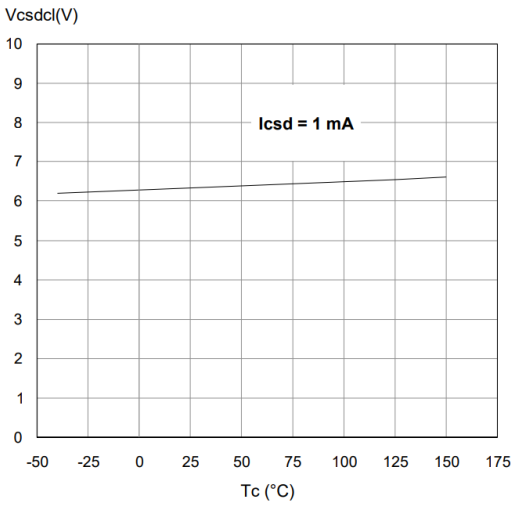
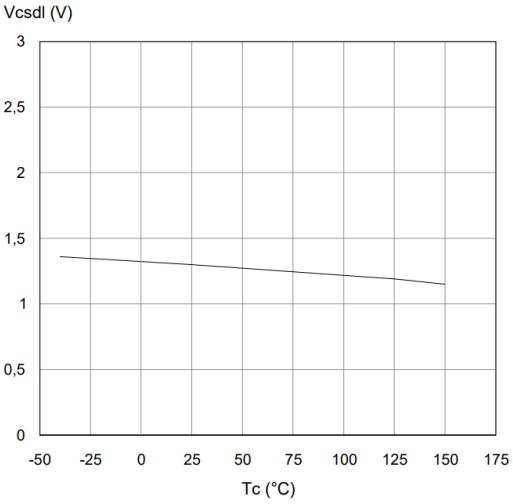


Figure 25. CS_DIS low level voltage



3 Protections

3.1 Current limitation

The device is equipped with an output current limiter in order to protect the silicon from excessive current flow. Consequently, in case of short-circuit or overload, the output current is clamped to a safety level, I_{LIMH}; in case the device enters thermal cycling a lower current limitation level, I_{LIML}, is triggered.

3.2 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing through the direct measurement of the spatial temperature gradient on the device surface.

If a faulty load event occurs, the drain current is limited to I_{LIMH} and the extreme power dissipation will cause a large thermal gradient on the device surface.

When the gradient temperature exceeds a safety threshold, output MOSFET is automatically turned off.

The device starts cool down and when the temperature decreases, the channel will be switched on again, limiting at I_{LIMH}.

The protection prevents fast thermal transient effects.

3.3 Thermal shutdown

If the device junction temperature exceeds the T_{TSD} threshold, the affected output is turned off and the device enters thermal cycling operation. During thermal cycling, the current is limited to I_{LIML} and a fault condition is indicated on CS_n pin than rises to the V_{SENSEH} value.

The output remains off until the junction temperature falls below the thermal reset temperature, T_R. The driver then automatically restarts and continues to limit the current at I_{LIML} until the thermal shutdown condition is reached again. The thermal cycling process repeats until the overload condition is removed.

When the temperature decreases under T_{RS}, the fault condition is removed.

T_{RS} is lower than T_R to ensure a stable fault indication during a faulty load condition.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device (see also Section 4).

4 Active clamp

Active clamp is also known as **Fast Demagnetization of inductive loads** or **Fast Current Decay**. When a high-side driver turns off an inductance, an undervoltage on the output is detected (see Figure 26).

The OUT pin is pulled down to V_{DEMAG}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at ~V_{DEMAG} until the load energy has been dissipated. The energy is dissipated in both IC internal switch and load resistance.

Figure 26. Active clamp typical waveforms

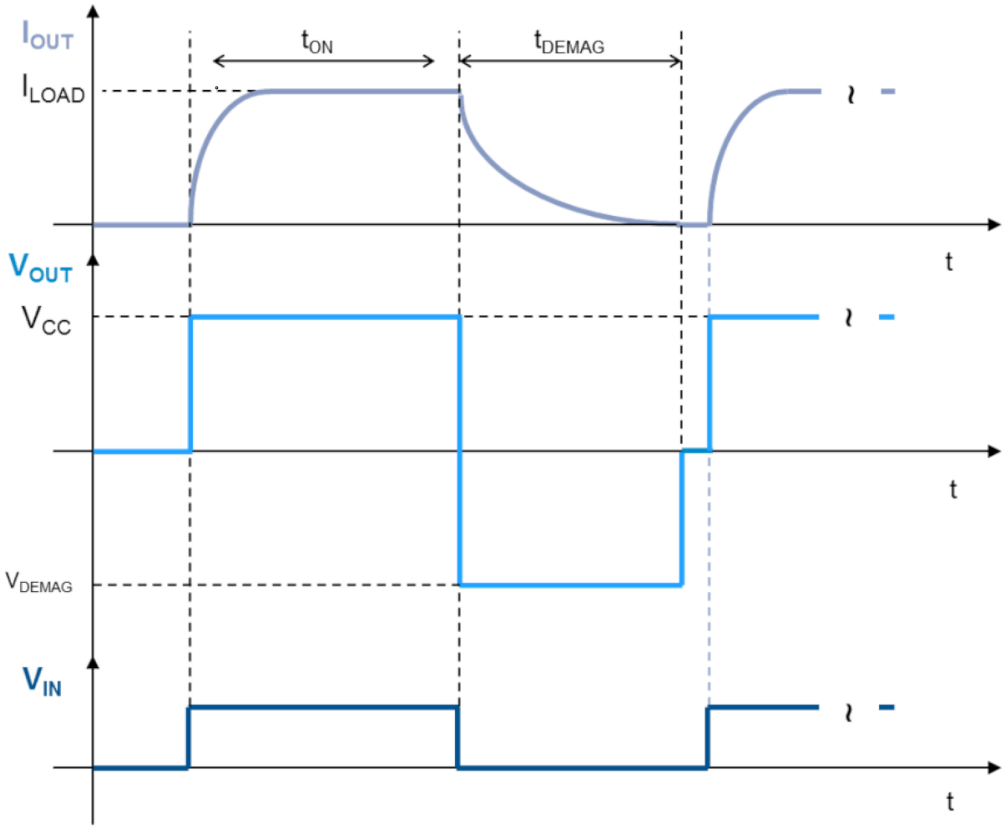
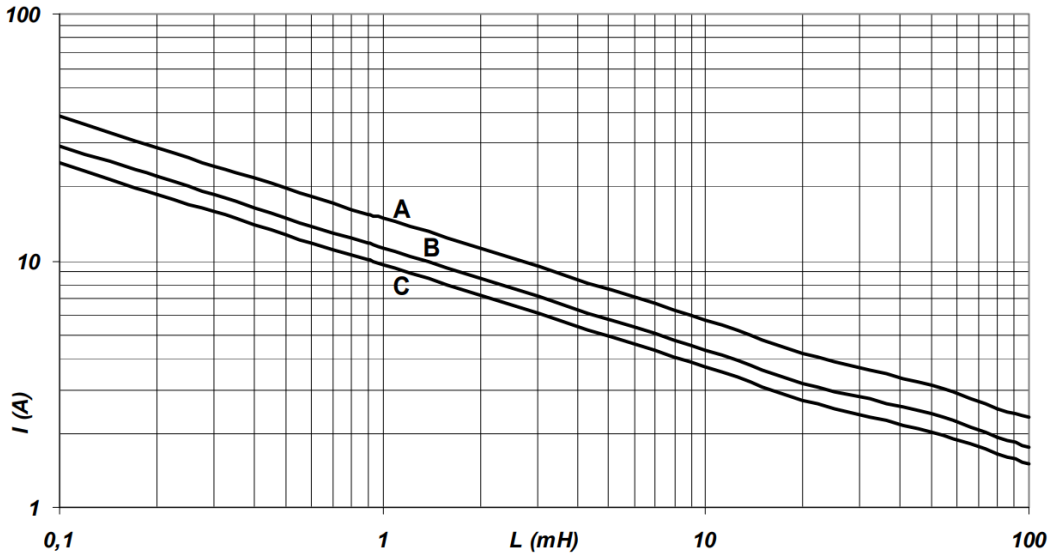


Figure 27. Maximum turn off current versus inductance for each channel (V_{CC} = 13 V)

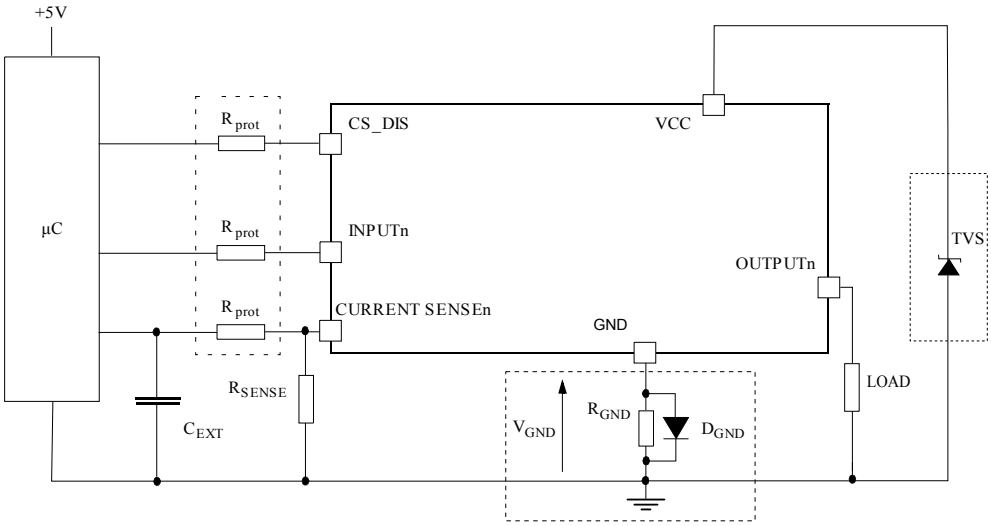


A: Tjstart = 150°C single pulse
B: Tjstart = 100°C repetitive pulse
C: Tjstart = 125°C repetitive pulse

Note: Values are generated with R_L = 0 Ω. In case of repetitive pulses, Tjstart (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Application information

Figure 28. **Application schematic**



5.1 GND protection network against reverse polarity

5.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This solution can be used with any load type.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max.})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

Where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ V: during reverse polarity) is:

$P_D = (-V_{CC})^2 / R_{GND}$

This resistor can be shared among several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max.}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max.} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation results in a large resistor value or requires several devices to share the same resistor, ST recommends implementing solution 2 (see below).

5.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel with D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared among several different HSDs. Also in this case, the presence of the ground network produces a shift (~600 mV) in the input threshold and in the status output values, if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

5.2 Vcc overshoot protection

To protect the device from supply rail overshoot, a TVS is inserted between VCC and GND.

It will be chosen to protect the circuit but not interferes with its normal operations.

For this reason, the TVS must be selected with appropriate V_{BR} and V_{CL} values for the maximum operating voltage of the application.

5.3 MCU I/Os protection

If a ground protection network is used and a negative transient is present on the VCC line, the control pins are pulled negative. ST recommends placing a resistor (Rprot) in series to protect the microcontroller I/O pins from latch-up.

The value of these resistors is a compromise between the leakage current of the microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation: R_{prot} range calculation

$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -100 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

5 kΩ ≤ R_{prot} ≤ 180 kΩ.

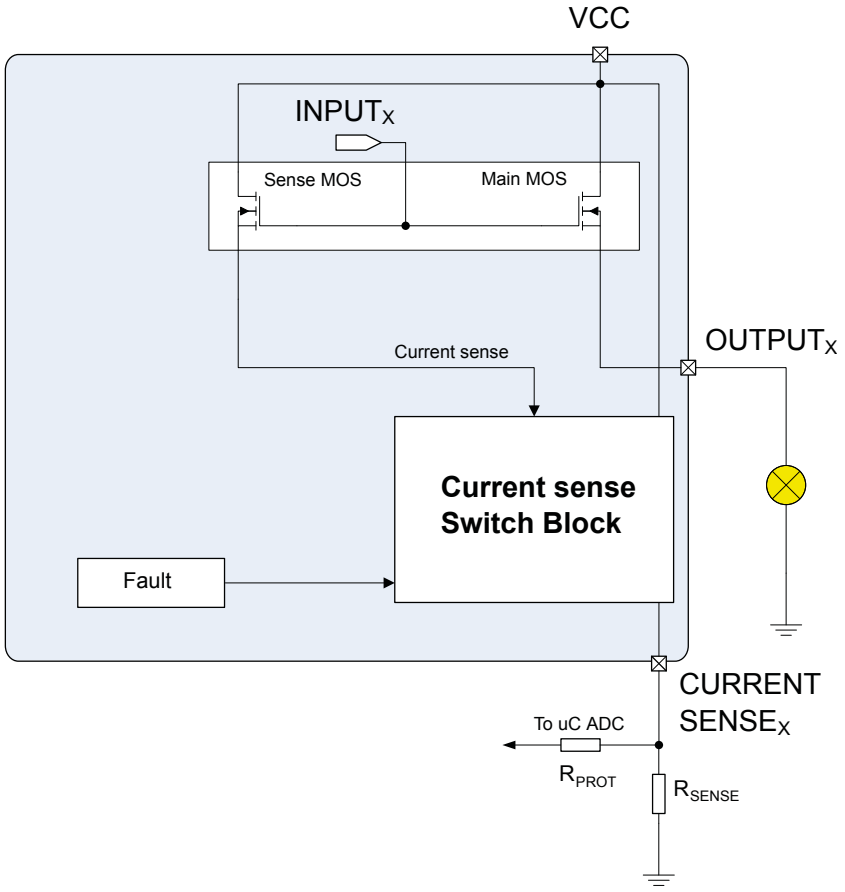
Recommended value: R_{prot} = 10 kΩ, C_{EXT}=10nF.

5.4 Analog current sense

Diagnostic information on device and load status are provided by the analog output pins (CS1, CS2).

5.4.1 Principle of current sense signal generation

Figure 29. Current sense block diagram



Current sense

The output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted into a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations.

Current provided by CS_n: $I_{SENSE} = I_{OUT} / K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT} / K$

Where:

- V_{SENSE} is the voltage measurable on the R_{SENSE} resistor
- I_{SENSE} is the current provided from CS_n pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of over-temperature, $T_J > T_{TSD}$, the fault is indicated by the CS pin, which is switched to a “current limited” voltage source, V_{SENSEH}.

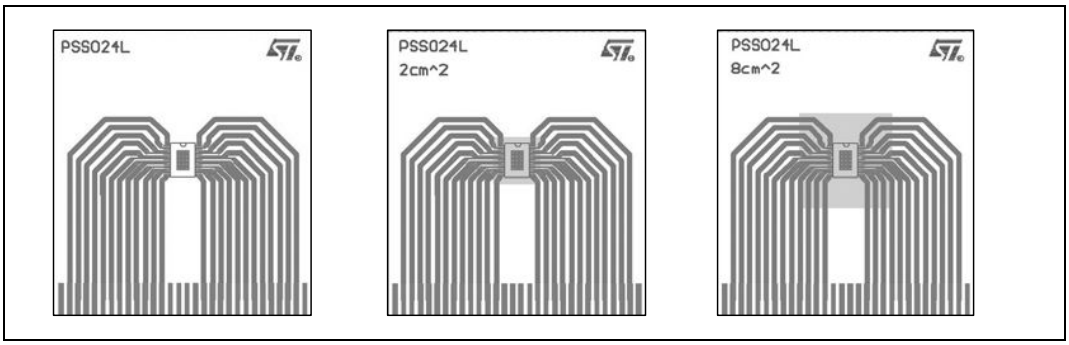
In any case, the current sourced by the CS_n pin in this condition is limited to I_{SENSEH}

The failure indication disappears when the junction temperature drops below the thermal reset status threshold T_{RS} (see also Table 10 and Figure 10).

6 Package and PCB thermal data

6.1 PowerSSO-24 thermal data

Figure 30. **PowerSSO-24 PCB**



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77 mm x 86 mm, PCB thickness=1.6mm, Cu thickness=70 µm (front and back side), Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 31. **R_{thJA} vs PCB copper area in open box free air condition (one channel ON)**

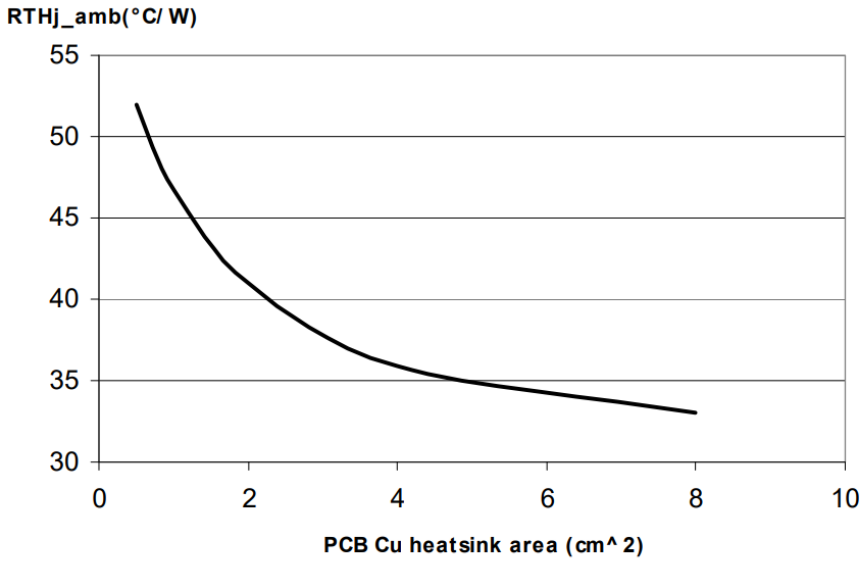


Figure 32. **PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)**

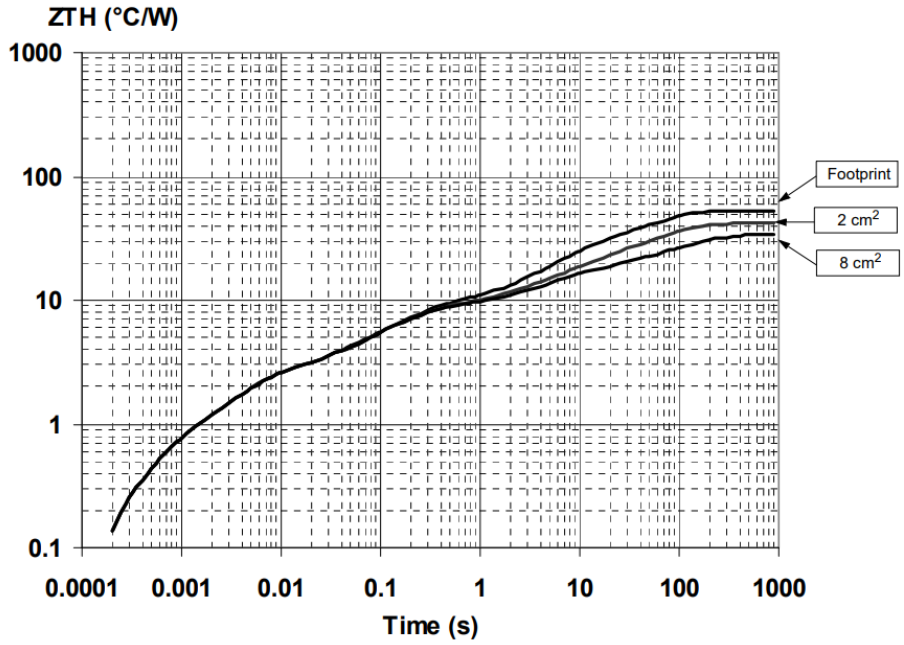
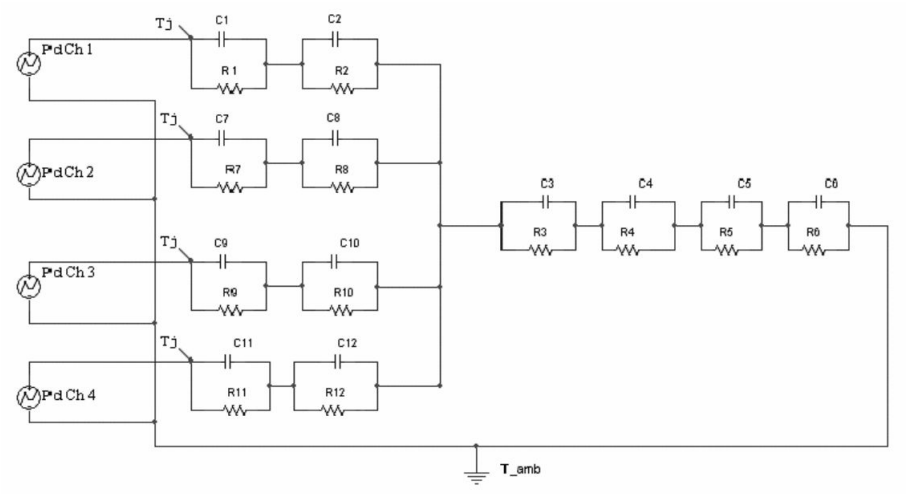


Figure 33. **Thermal fitting model of a quad channel HSD in PowerSSO-24**



The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation: pulse calculation formula

$Z_{th\delta} = R_{th} \cdot \delta + Z_{THtp} (1 - \delta)$

where $\delta = t_P / T$

Table 11. **Thermal parameters**

Area / island (cm^2)	Footprint	2	8
R1 = R7 = R9 = R11 (°C/W)	0.28		
R2 = R8 = R10 = R12 (°C/W)	0.9		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 = C7 = C9 = C11 (W.s/°C)	0.001		
C2 = C8 = C10 = C12 (W.s/°C)	0.003		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-24 package information

Figure 34. PowerSSO-24 package dimensions

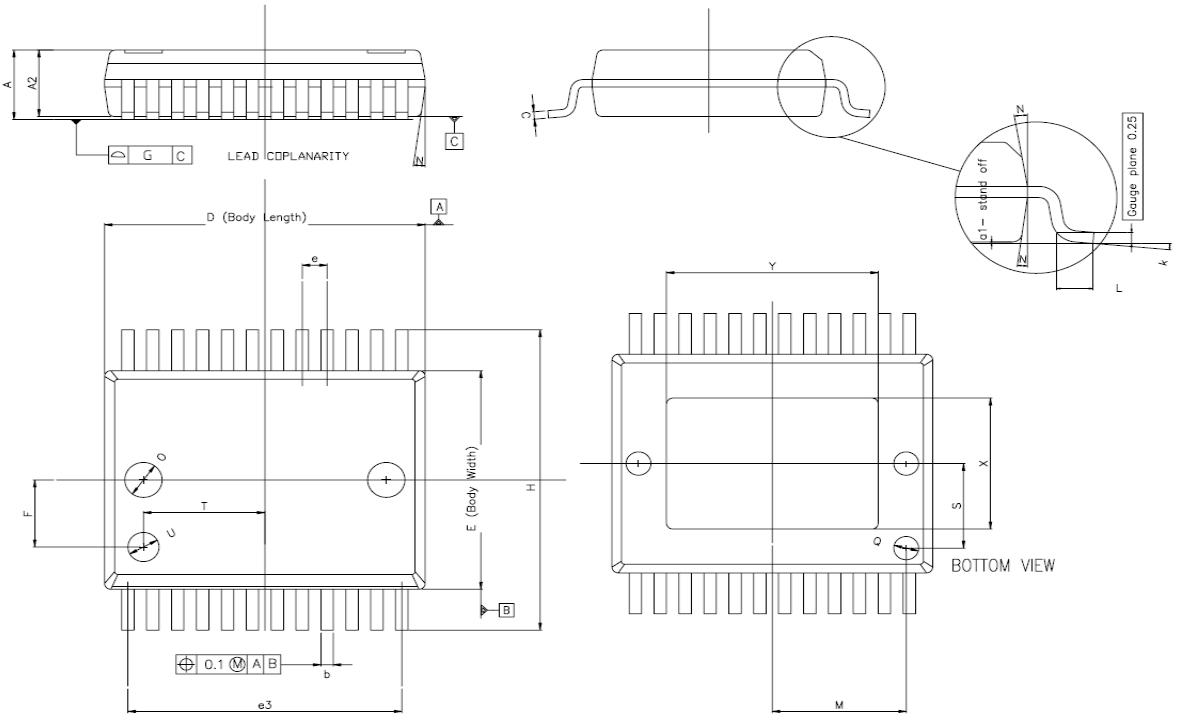
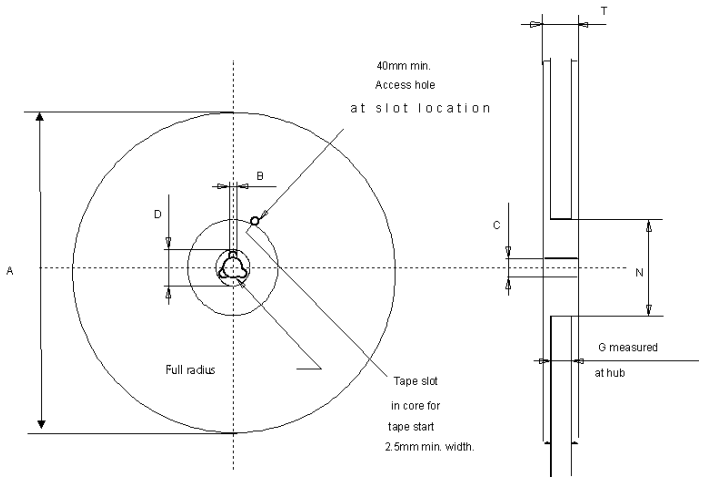


Table 12. **PowerSSO-24 mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.1
b	0.33		0.51
c	0.23		0.32
D	10.1		10.5
E	7.4		7.6
e		0.8	
e3		8.8	
F		2.3	
G			0.1
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
N			10°
X	4.1		4.7
Y	6.5		7.1

7.2 PowerSSO-24 packing information

Figure 35. **PowerSSO-24 tape and reel shipment**



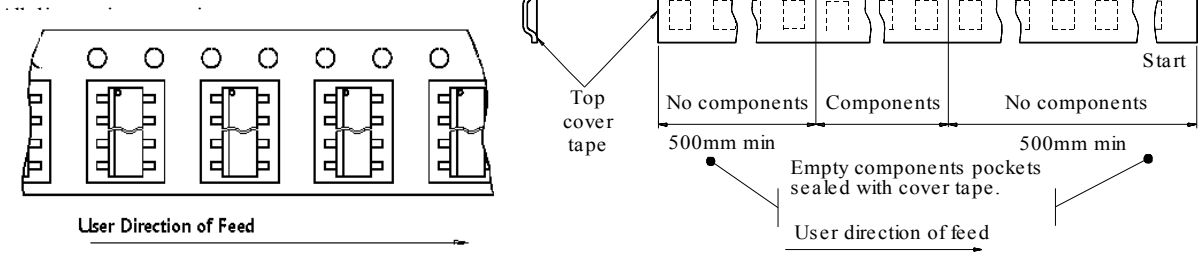
REEL DIMENSIONS

Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2



8 Ordering information

Table 13. **Ordering information**

Part number	Package	Packing
IPS4054HK	PowerSSO-24	Tape and Reel

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
31-Aug-2026	1	Initial release.

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