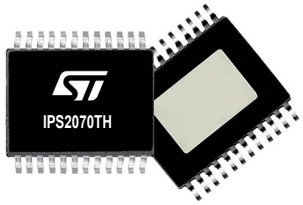
IPS2070TH

Datasheet

Dual channel high-side driver with analog current sense



Product status link

IPS2070TH

Product label

SUSTAINABLE TECHNOLOGY

Features

- $R_{ON(Typ.)}$ (@T_J = 25 °C) = 35 mΩ
- Very low standby current
- 3.3 V CMOS compatible inputs
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- Proportional load current sense
- Very low current sense leakage
- High current sense precision for wide range currents
- Off-state open-load detection
- Output short to VCC detection
- Overload and short to ground latch-off
- Thermal shutdown latch-off
- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Fault reset standby pin (FR_STBY)
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of VCC
- Designed to drive DC-13 loads according to EN 60947-5-1
- Designed to meet IEC 61131-2, IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- PowerSSO-24 package

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- General high-side switch applications

Description

The IPS2070TH is a monolithic device made using STMicroelectronics VIPower technology, intended for driving resistive, inductive or capacitive loads with one side connected to the ground. Active VCC pin voltage clamp protects the device against low energy spikes.

The device integrates an analog current sense, which delivers a current proportional to the load current. The sensed current of each output channel (1 and 2) is available on the correspondent current sense pin (CS1 and CS2).

Fault conditions such as overload, overtemperature, or short to VCC are reported via the current sense pins. Output current limitation protects the device in overload conditions. The FR_STBY pin enables special thermal protection and power-saving management, allowing latch-off, auto-restart, and low-current standby operation.

1 Block diagram and pin description

Figure 1. Block diagram

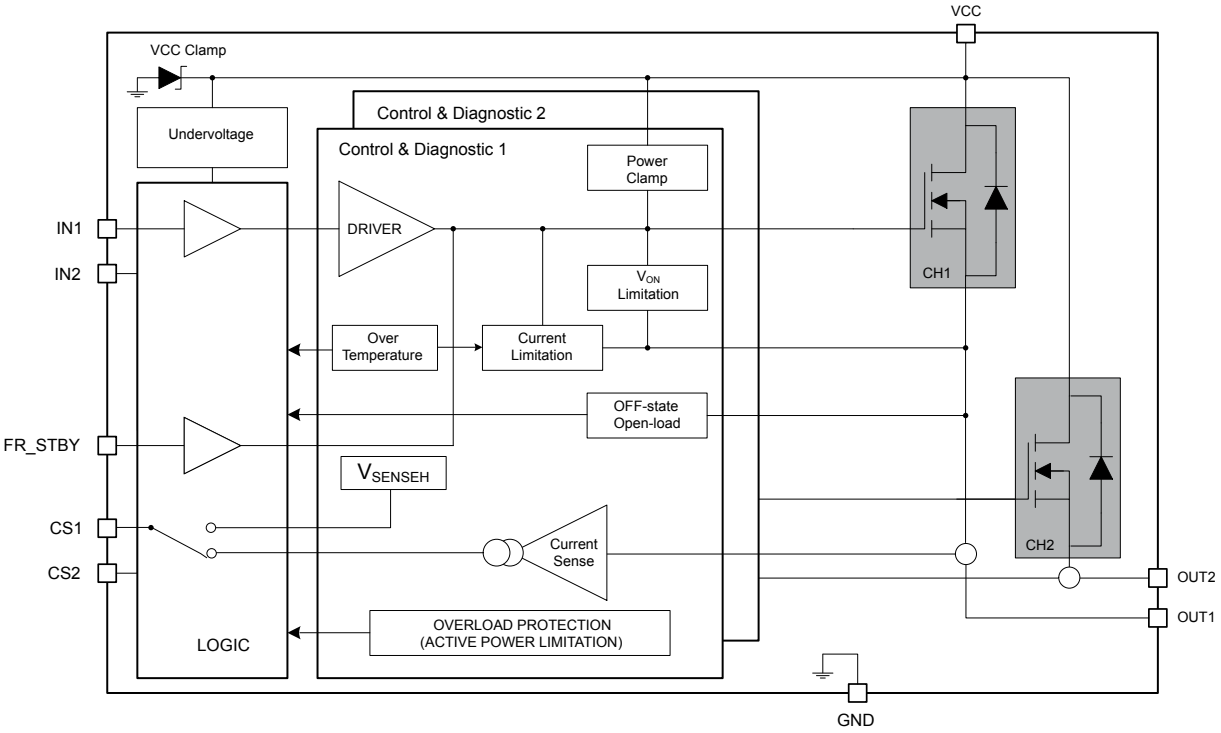
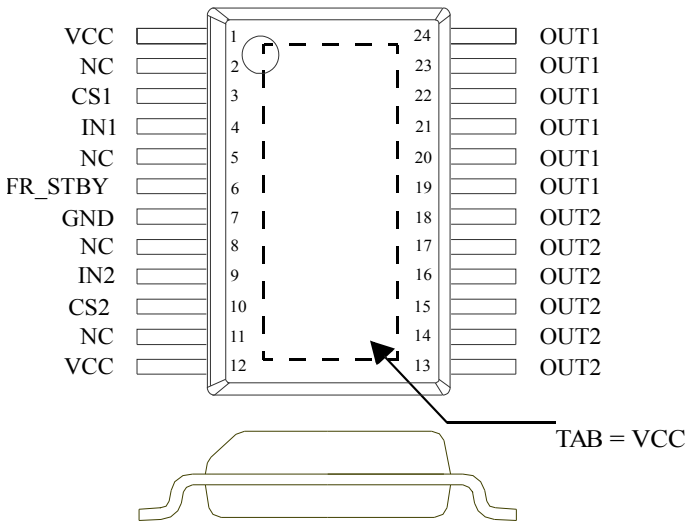


Table 1. Pin function

Pin	Name	Type	Function
1, 12, TAB	V_{CC}	Supply	Power supply
2, 5, 8, 11	NC	-	Not connected
3	CS1	Analog output	Analog current sense pin for channel 1, it delivers a current proportional to the load current
4	IN1	Logic input	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state for channel 1
6	FR_STBY	Logic input	In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_STBY pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_STBY pin are low
7	GND	Supply	Ground connection
9	IN2	Logic input	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state for channel 2
10	CS2	Analog output	Analog current sense pin for channel 2, it delivers a current proportional to the load current
13 to 18	OUT1	Analog output	Power output channel 1
19 to 24	OUT2	Analog output	Power output channel 2

Figure 2. Configuration diagram PowerSSO-24 (top view)



PowerSSO-24

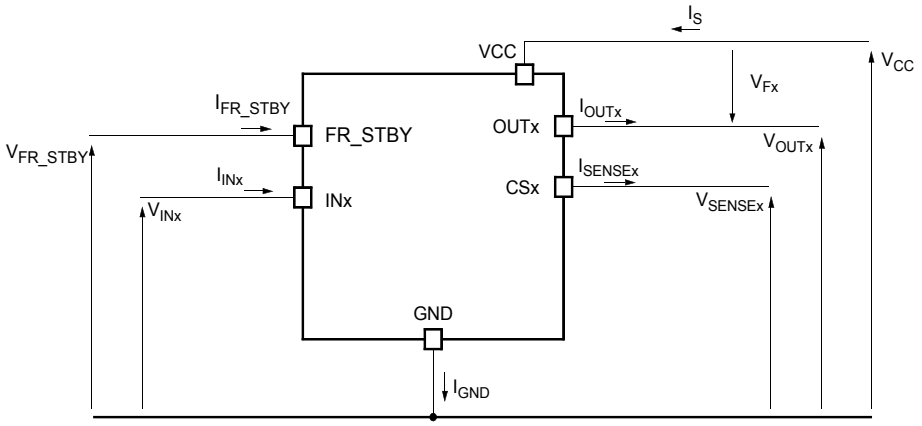
Table 2. Suggested connections for unused and not connected pins

Connection/pin	Current Sense	NC	Output	Input	FR_STBY
Floating	Not recommended	X	X	X	X
To ground	Through 10 kΩ resistor	X	Not recommended	Through 10 kΩ resistor	Through 10 kΩ resistor

Note: X = don't care.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: V_{Fx} = V_{OUTx} - VCC during reverse polarity condition (x = 1, 2).

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC supply voltage		56	V
$-V_{CC}$	Reverse DC supply voltage		0.3	V
$-I_{GND}$	DC reverse ground pin current		200	mA
I_{OUT}	DC output current		Internally limited	A
$-I_{OUTx}$	Reverse DC output current		40	A
I_{INx}	DC input current		-1 to 10	mA
I_{FR_STBY}	Fault reset standby DC input current		-1 to 1.5	mA
$-I_{SENSEx}$	DC reverse CS pin current		200	mA
V_{SENSEx}	Current sense maximum voltage		V_{DEMAG} to V_{CC}	V
E_{MAX}	Maximum switching energy L = 2.3 mH; V_{CC} = 32 V; T_{Jstart} = 150 °C; I_{OUT} = $I_{limL\ (typ.)}$		250	mJ
L_{smax}	Maximum stray inductance in short circuit condition R_L = 300 mΩ, V_{CC} = 32 V, T_{Jstart} = 150 °C, I_{OUT} = $I_{limH\ (max.)}$		40	µH
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 kΩ, C = 100 pF)	IN1, 2	4000	V
		CS1, 2	2000	
		FR_STBY	4000	
		OUT1, 2	5000	
		VCC	5000	
T_J	Junction operating temperature		-40 to 150	°C
T_{STG}	Storage temperature		-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case (with one channel ON)	2	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	See Figure 33	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 36 V, -40 °C < T_J < 150 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		8		36	V
V_{USD}	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance (1)	I_{OUT} = 3 A, T_J = 25 °C		35		mΩ
		I_{OUT} = 3 A, T_J = 150 °C			70	
V_{clamp}	Clamp voltage	I_S = 20 mA	58	64	70	V
I_{LGND}	Output current at GND disconnection	V_{CC} = V_{IN} = V_{GND} = 24 V; V_{OUT} = 0 V			0.5	mA
I_S	Supply current	Off-state, V_{CC} = 24 V, T_J = 25 °C, V_{IN} = V_{OUT} = V_{SENSE} = 0 V, V_{FR_STBY} = 0 V		2(2)	5(2)	µA
		On-state, V_{CC} = 24 V, V_{IN} = 5 V, I_{OUT} = 0 A		4.2	6	mA
$I_{L(off)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V, V_{CC} = 24 V, T_J = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V, V_{CC} = 24 V, T_J = 125 °C	0		5	
V_F	Output - V_{CC} diode voltage	-I_{OUT} = 3 A, T_J = 150 °C			0.7	V

1. *For each channel.*
2. *Power MOSFET leakage included.*

Table 6. Switching (V_{CC} = 24 V, T_J = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 8 Ω		46		µs
$t_{d(off)}$	Turn-off delay time	R_L = 8 Ω		54		µs
$(dV_{OUT}/dt)_{(on)}$	Turn-on voltage slope	R_L = 8 Ω		0.55		V/µs
$(dV_{OUT}/dt)_{(off)}$	Turn-off voltage slope	R_L = 8 Ω		0.46		V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 8 Ω		1		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 8 Ω		0.65		mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
$V_{FR\_STBY\_L}$	FR_STBY pin low level voltage				0.9	V
$I_{FR\_STBY\_L}$	FR_STBY pin low level current	V_{FR_STBY} = 0.9 V	1			µA
$V_{FR\_STBY\_H}$	FR_STBY pin high level voltage		2.1			V
$I_{FR\_STBY\_H}$	FR_STBY pin high level current	V_{FR_STBY} = 2.1 V			10	µA
$V_{FR\_STBY(hyst)}$	FR_STBY pin hysteresis voltage		0.25			V
$V_{FR\_STBY\_CL}$	FR_STBY pin clamp voltage	I_{FR_STBY} = 15 mA (t < 10 ms)	11		15	V
		I_{FR_STBY} = -1 mA		-0.7		V
t_{reset}	Overload latch-off reset time	See Figure 1	2		24	µs
t_{stby}	Standby delay	See Figure 2	120		1200	µs

Table 8. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC} = 24 V	30	42	55	A
		5 V < V_{CC} < 36 V			55	
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 24 V, T_R < T_J < T_{TSD}		10.5		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset status threshold(1)		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 3 A, V_{IN} = 0 V, L = 6 mH	V_{CC} - 58	V_{CC} - 64	V_{CC} - 70	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 150 mA, T_J = -40 °C to 150 °C		25		mV

1. See *Section 3.1.3: Thermal shutdown* for details.

Table 9. Current sense (8 V < V_{CC} < 36 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1 A, V_{SENSE} = 2 V, T_J = -40 °C	1952	2960	4150	
		I_{OUT} = 1 A, V_{SENSE} = 2 V, T_J = 25 °C to 150 °C	2080		3840	
dK_1/K_1(1)	Current sense ratio drift	I_{OUT} = 1 A, V_{SENSE} = 2 V, T_J = -40 °C to 150 °C	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A, V_{SENSE} = 4 V, T_J = -40 °C	2940	2930	3440	
		I_{OUT} = 3 A, V_{SENSE} = 4 V, T_J = 25 °C to 150 °C	2585		3265	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 3 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-10		10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 12 A, V_{SENSE} = 4 V, T_J = -40 °C	2770	2900	3125	
		I_{OUT} = 12 A, V_{SENSE} = 4 V, T_J = 25 °C to 150 °C	2755		3045	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 12 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-5		5	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{IN} = 0 V, T_J = -40 °C to 150 °C	0		1	µA
		I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{IN} = 5 V, T_J = -40 °C to 150 °C	0		2	
V_{SENSE}	Max. analog sense output voltage	I_{OUT} = 12 A, R_{SENSE} = 3.9 kΩ	5			V
V_{SENSEH}	Analog sense output voltage in fault condition (2)	V_{CC} = 24 V, R_{SENSE} = 3.9 kΩ	7.5	8.5	9.5	V
I_{SENSEH}	Analog sense output current in fault condition (2)	V_{CC} = 24 V, V_{SENSE} = 5 V	4.9	9	12	mA
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pins	V_{SENSE} < 4 V, 0.2 A < I_{OUT} < 12 A, I_{SENSE} = 90% of I_{SENSE} max, (see Figure 4)		200	400	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90 % of I_{SENSE} max, I_{OUT} = 90 % of I_{OUT} max, I_{OUT} max = 3 A (see Figure 7)			250	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pins	V_{SENSE} < 4 V, 0.2 A < I_{OUT} < 12 A, I_{SENSE} = 10% of I_{SENSE} max I_{OUT} = 90% of I_{OUT} max (see Figure 4)		5	20	µs

1. *Specified by design, not tested in production.*
2. *Fault condition includes: power limitation, overtemperature and open-load in off-state condition.*

Table 10. Open-load detection (V_{FR_STBY} = 5 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0 V, 8 V < V_{CC} < 36 V	2		4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	(see Figure 31)	180		1800	µs
$I_{L(off2)}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0 V, V_{SENSE} = 0 V, V_{OUT} rising from 0 V to 4 V,	-120		0	µA
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{OUT} = 4 V, V_{IN} = 0 V, V_{SENSE} = 90 % of V_{SENSEH}, R_{SENSE} = 3.9 kΩ			20	µs
t_{DFRSTK_ON}	Output short circuit to V_{CC} detection delay at FR_STBY activation	Input1,2 = low (see Figure 6)			50	µs

Figure 4. Current sense delay characteristics

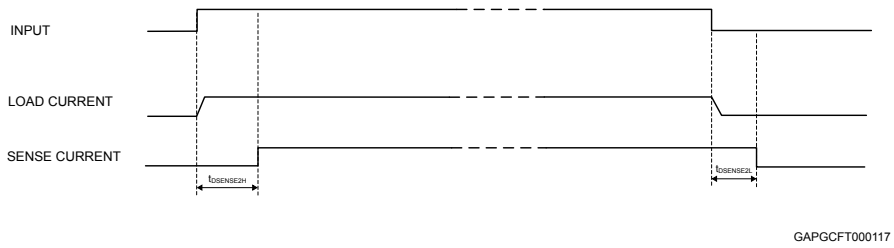


Figure 5. Switching characteristics

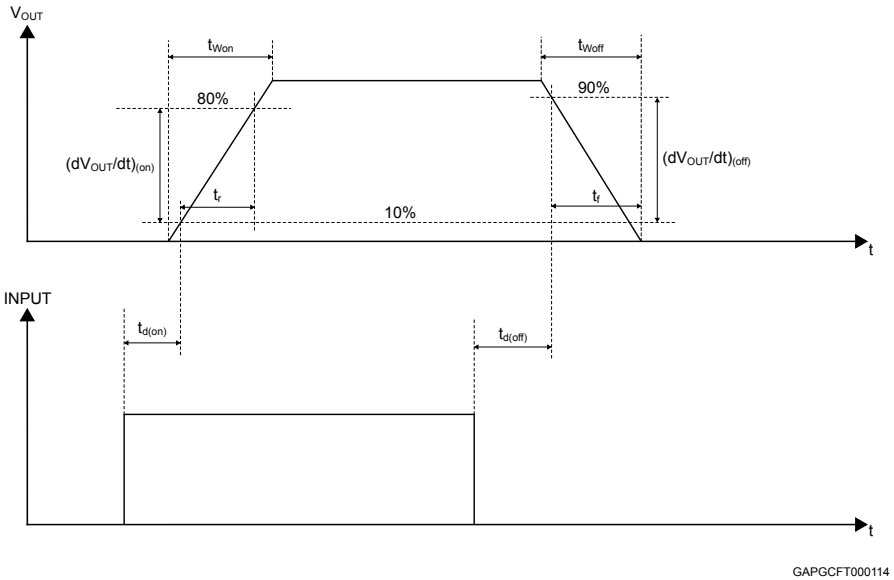


Figure 6. Output stuck to V_{CC} detection delay time at FR_STBY activation

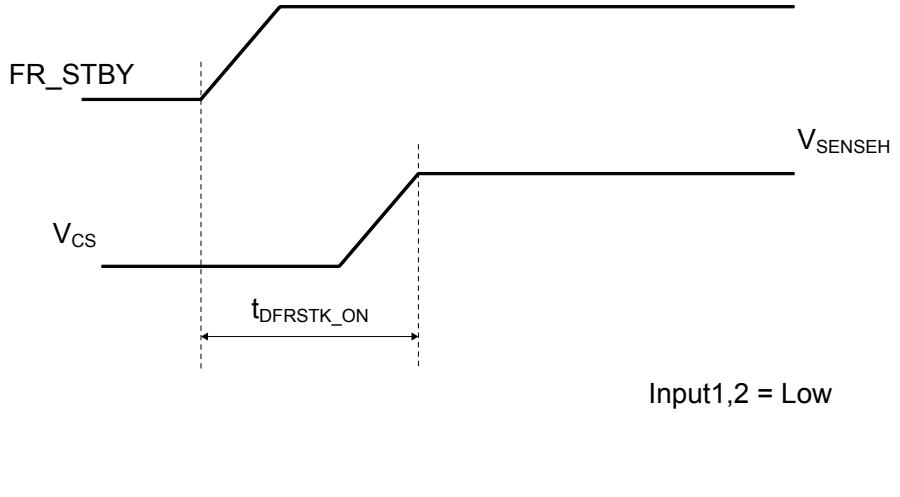


Figure 7. Delay response time between rising edge of output current and rising edge of current sense for each channel

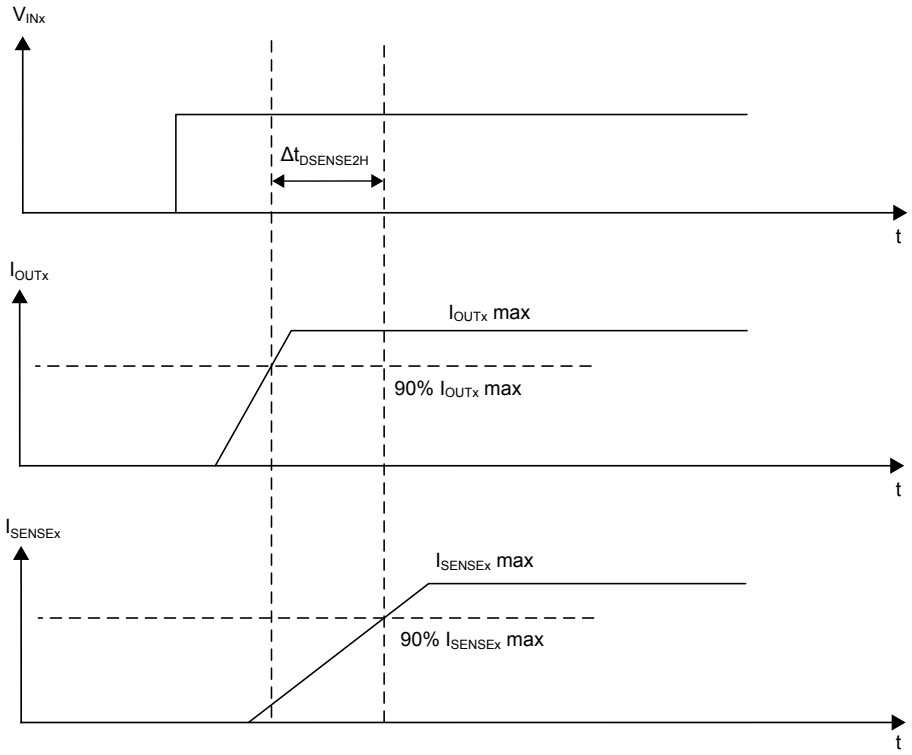
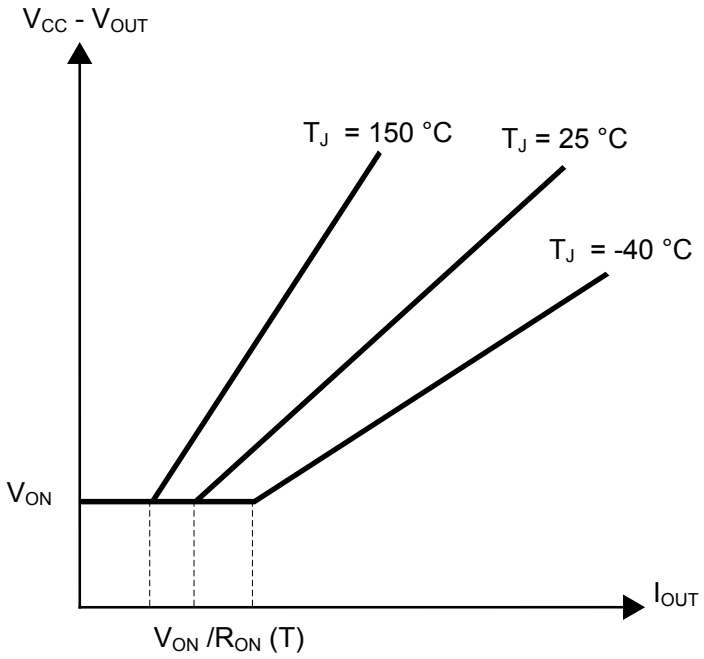


Figure 8. **Output voltage drop limitation**



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2.4 Electrical characteristics (curves)

Figure 9. Off-state output current

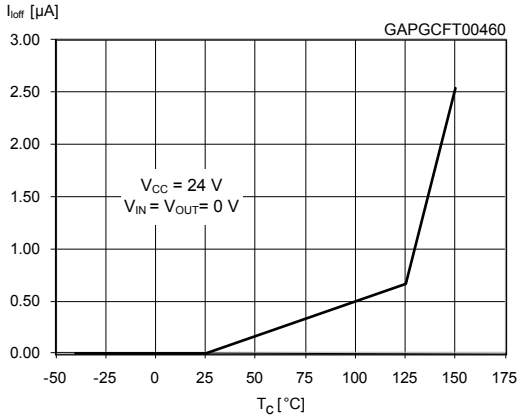


Figure 10. High level input current

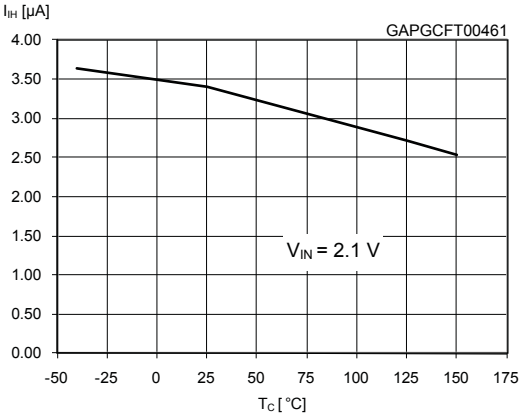


Figure 11. Input clamp voltage

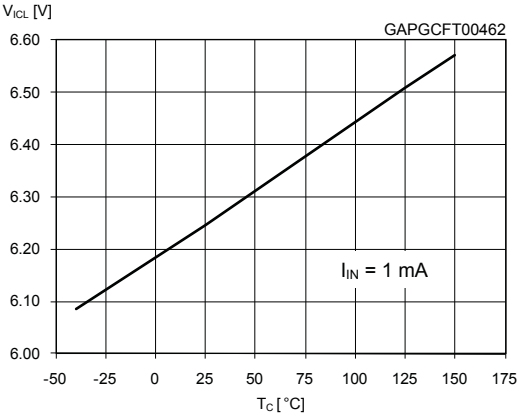


Figure 12. High level input voltage

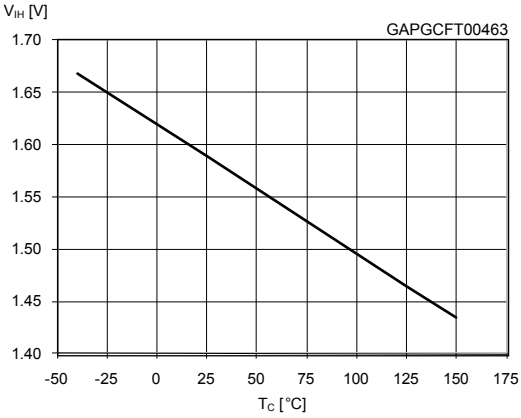


Figure 13. Low level input voltage

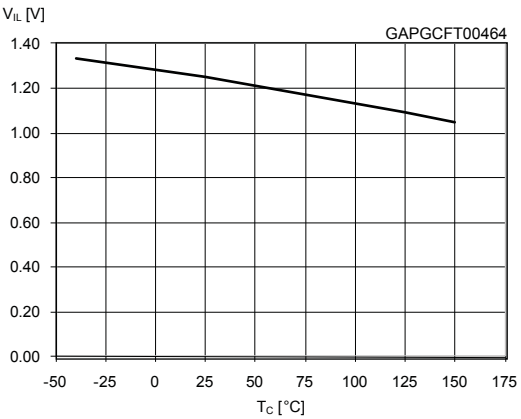


Figure 14. Input hysteresis voltage

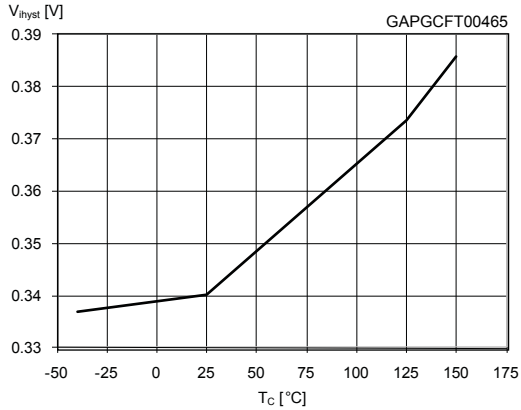


Figure 15. On-state resistance vs T_C

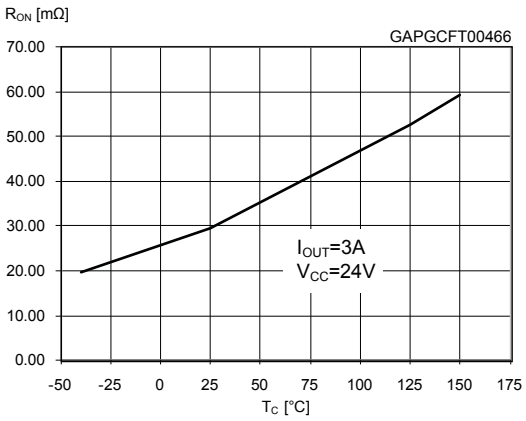


Figure 16. On-state resistance vs V_{CC}

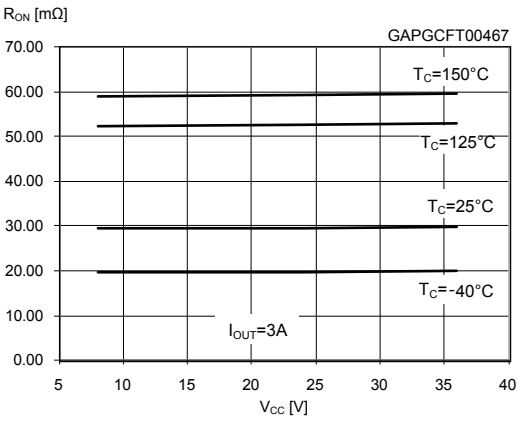


Figure 17. Turn-on voltage slope

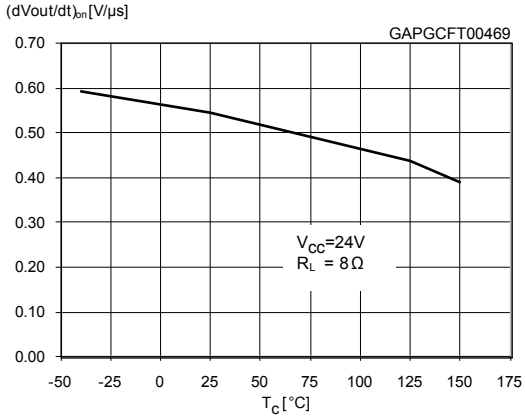


Figure 18. Turn-off voltage slope

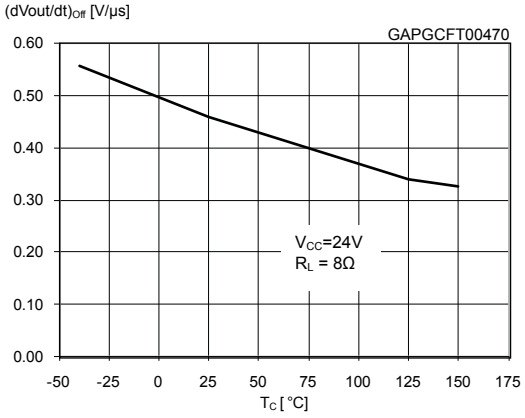
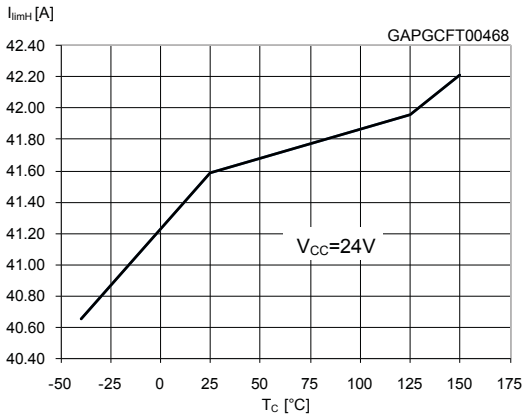


Figure 19. I_{LIMH} vs T_C



3 Protections

3.1 Thermal protections

To reduce the effects of excessive power dissipation and consequent thermal stress, the device implements a sophisticated overload/short circuit management.

3.1.1 Current limitation

The device is equipped with an output current limiter in order to protect the silicon from excessive current flow. Consequently, in case of short-circuit or overload, the output current is clamped to a safety level, I_{limH}; in case the device enters thermal cycling a lower current limitation level, I_{limL}, is triggered.

3.1.2 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing through the direct measurement of the spatial temperature gradient on the device surface.

When the gradient temperature exceeds a safety threshold, output MOSFET is automatically turned off and the CS pin indicates a thermal intervention bringing the voltage on the CSx pin to the V_{SENSEH} value.

The device starts cool down and, based on the FR_STBY pin status, the output MOSFET switches on and cycles with a thermal hysteresis, limiting at I_{limH}, according to the maximum instantaneous power which can be handled (FR_STBY = Low) or remain off (FR_STBY = High); (see also Section 4).

The protection prevents fast thermal transient effects.

Following figures show the mechanism previously described.

Figure 20. Power limitation on a shorted load (FR_STBY = Low)

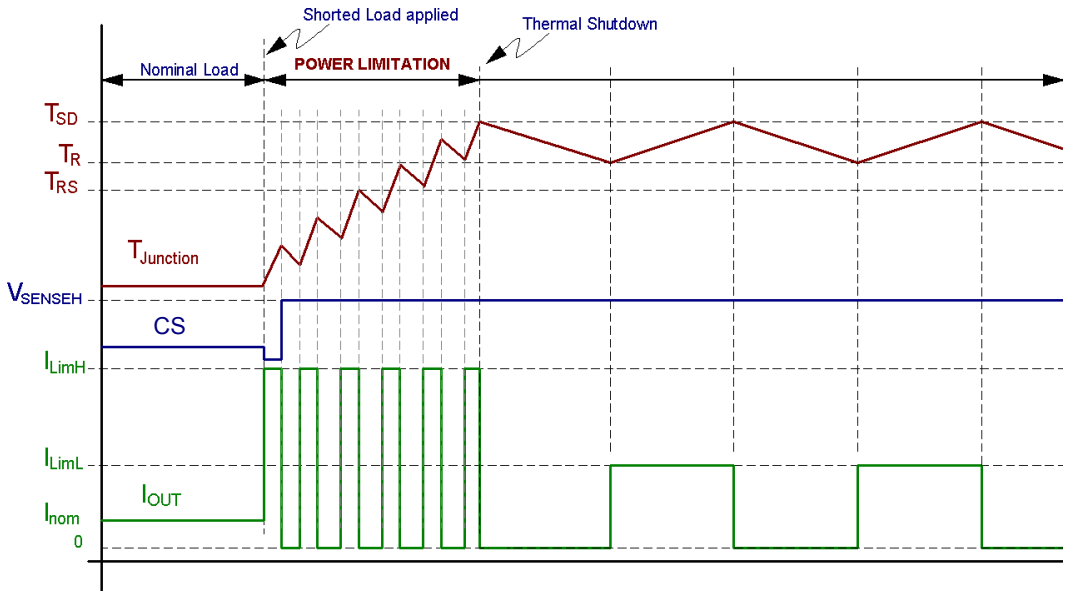
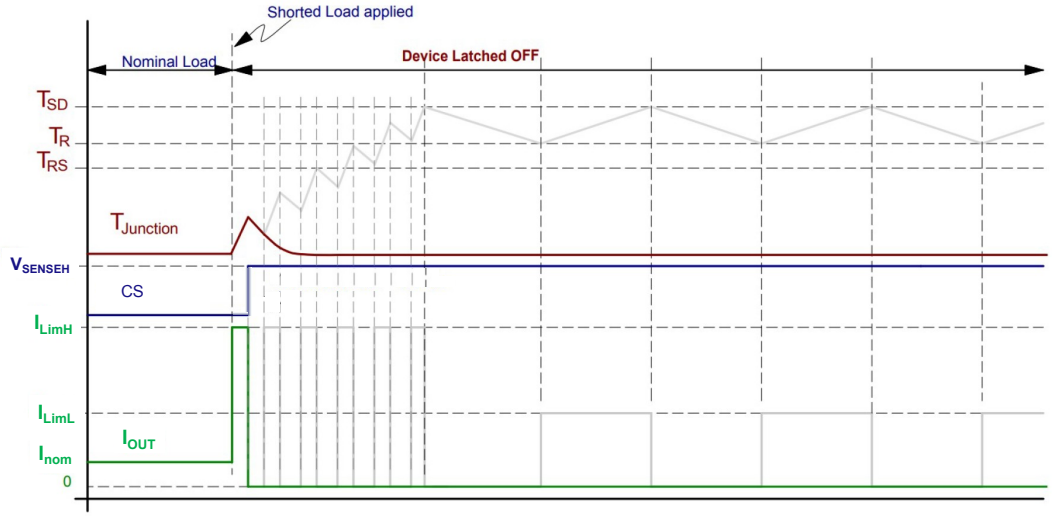


Figure 21. **Power limitation with latch (FR_STBY = High)**



3.1.3 Thermal shutdown

If the device junction temperature exceeds the T_{TSD} threshold, the affected output is turned off.

Based on the FR_STBY pin status, the device enters thermal cycling operation (FR_STBY = Low) or remains off (FR_STBY = High) (see also Section 4).

In the first case, the current is limited to I_{limL} and a fault condition is indicated on CSx, unless already asserted due to power limitation.

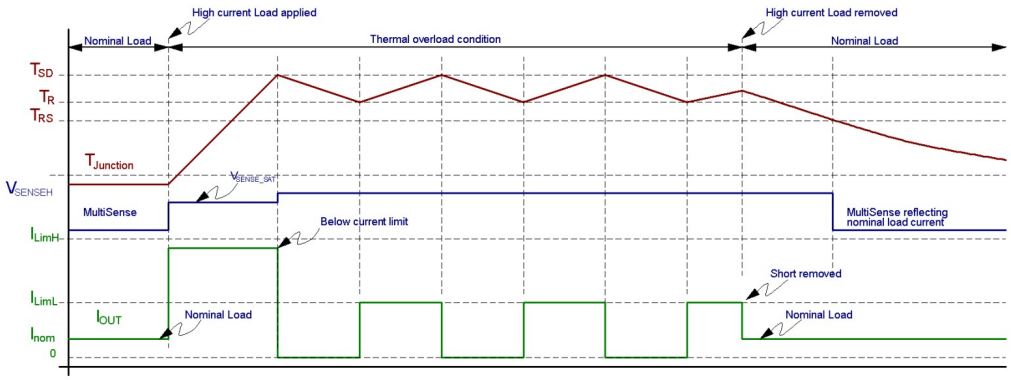
The output remains off until the junction temperature falls below the thermal reset temperature, T_R . The driver then automatically restarts and continues to limit the current at I_{limL} until the thermal shutdown condition is reached again. The thermal cycling process repeats until the overload condition is removed.

When the temperature decreases under T_{RS}, the fault condition is removed.

T_{RS} is lower than T_R to ensure a stable fault indication during a faulty load condition.

The following figure shows the thermal shutdown response.

Figure 22. **Thermal shutdown response (no power limitation) (FR_STBY = Low)**



3.2 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device (see also Section 5).

4 Reset and standby mechanism description

The IPS2070TH features a special thermal protection and power saving mechanism controlled by the FR_STBY pin. In the event of an overload, when the FR_STBY pin is high (default state), the device turns off the affected channel and does not attempt to turn it back on, even if the temperature drops or the load returns to normal; the device enters **latch-off mode**.

At the same time, the voltage on the CS_x pin rises to the V_{SENSEH} value.

Recovery from an overload and reactivation of the outputs are managed through the FR_STBY pin: applying a low pulse for a minimum specified time (t_{reset}) resets the latch-off condition (fault reset) and triggers a new attempt to activate the channel, as shown in Figure 23.

If the FR_STBY pin remains low after the reset pulse, the device enters **auto-restart mode**. On the contrary, if FR_STBY is set high, the device remains inactive (see Figure 25).

When FR_STBY is kept low together with IN1 and IN2, the device enters **standby mode**, allowing minimum current consumption, I_S(off-state) (see Figure 24).

Figure 25 shows the device's behavior under overload conditions as a function of the possible combinations of the FR_STBY and IN_X signals.

The possible device mode and related pins status/values are summarized in Table 11.

Figure 23. t_{reset} definition

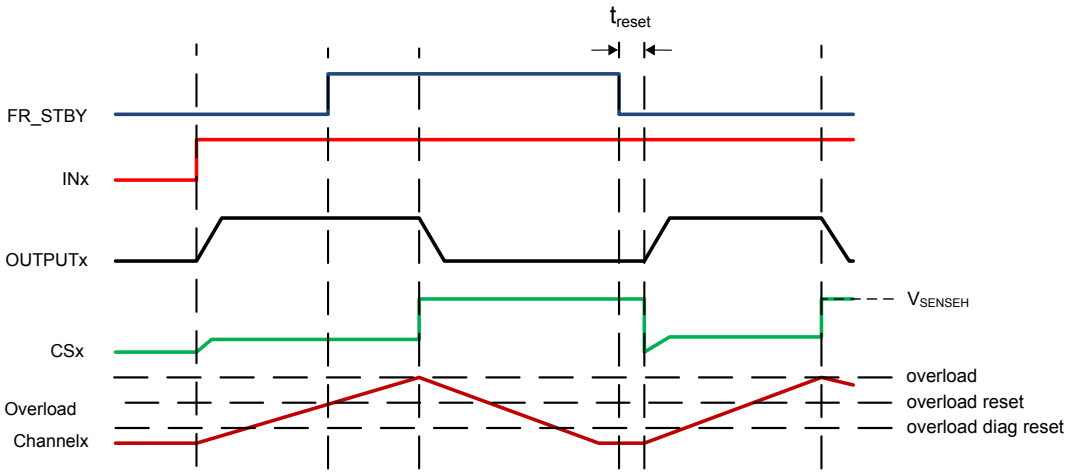


Figure 24. t_{stby} definition

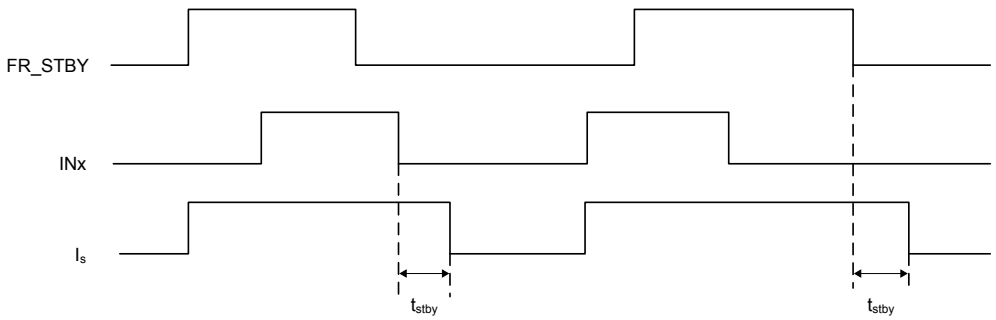
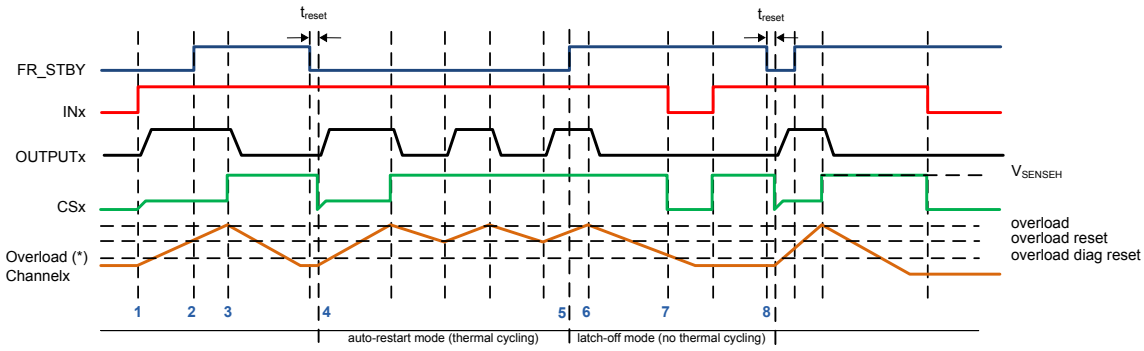


Figure 25. Device behavior in overload condition



1: OUTPUTx and CSx controlled by INx
2: FR_STBY from '0' to '1' → no action on CSx pin
3: Overload latch-off. INn high → CSx high
4: FR_STBY low AND Temp channel x < overload_reset → overload latch reset after t_reset
4 to **5**: FR_STBY low AND INx high → thermal cycling, CSx high
5: FR_STBY high → latch-off reset disabled
6 to **7**: Overload event and FR_STBY high → latch-off, no thermal cycling
7 to **8**: Overload diagnostic disabled/enabled by the input
8: Overload latch-off reset by FR_STBY

(*) Overload = thermal shutdown or power limitation

Table 11. Functional table

Device status	FR_STBY	IN_X	OUT_X	CS_X
Standby	L	L	L	0
Normal operation	X	L	L	0
	X	H	H	Nominal
Overload	X	L	L	0
	X	H	H	> Nominal
Overtemperature/short to ground	X	L	L	0
	L	H	Cycling	V_{SENSEH}
	H	H	Latched	V_{SENSEH}
Undervoltage	X	X	L	0
Short to V_{CC}	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	< Nominal
Open-load off-state (with pull-up)	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	0
Negative output voltage clamp	X	L	Negative	0

5 Active clamp

Active clamp is also known as **Fast Demagnetization of inductive loads** or **Fast Current Decay**. When a high-side driver turns off an inductance, an undervoltage on the output is detected (see Figure 26).

The OUT pin is pulled down to V_{DEMAG}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at ~V_{DEMAG} until the load energy has been dissipated. The energy is dissipated in both IC internal switch and load resistance.

Figure 26. Active clamp typical waveforms

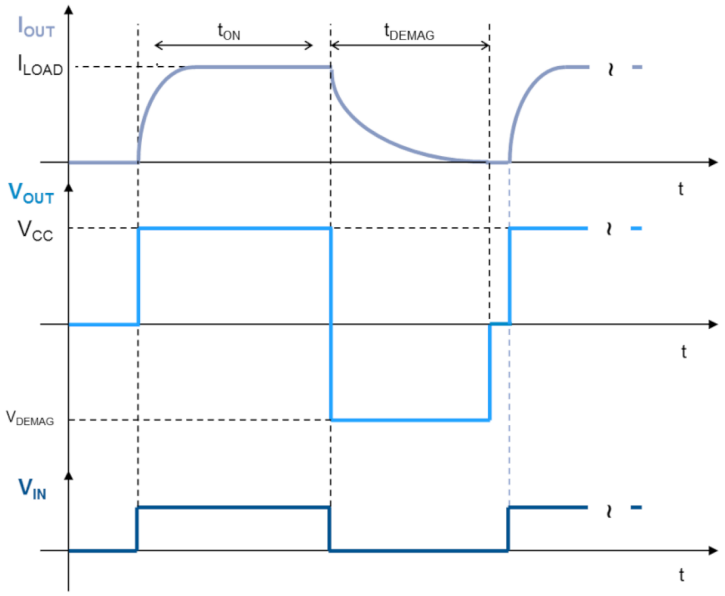
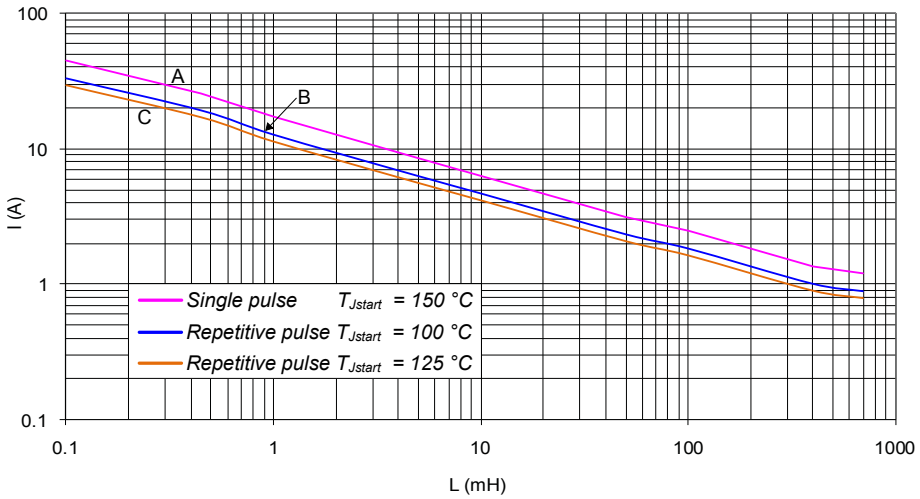


Figure 27. Maximum turn off current versus inductance for each channel



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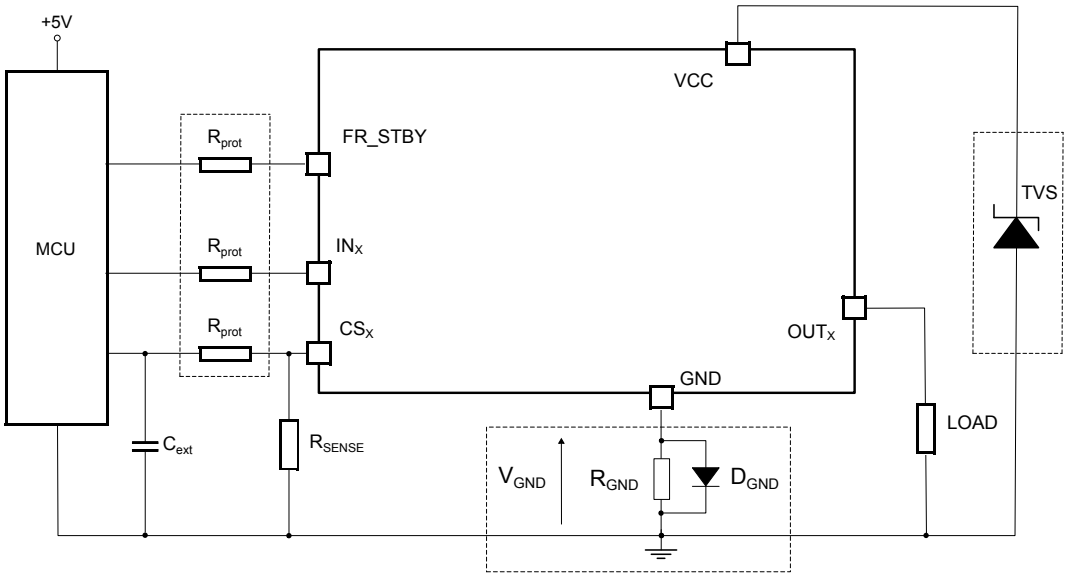
Note: Values are generated with R_L = 0 Ω. In case of repetitive pulses, T_{Jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

How to read the plot: referring to case B (single pulse T_{jstart}) to get a 1 A turn off current, a 400 mH inductance is needed.

6 Application information

Figure 28. **Application schematic**



6.1 GND protection network against reverse polarity

6.1.1 Solution 1: resistor in the ground line (RGND only)

This solution can be used with any load type.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max.})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

Where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ V: during reverse polarity) is:

$P_D = (-V_{CC})^2 / R_{GND}$

This resistor can be shared among several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max.}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max.} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation results in a large resistor value or requires several devices to share the same resistor, ST recommends implementing solution 2 (see below).

6.1.2 Solution 2: diode (DGND) in the ground line

A resistor (R_{GND} = 4.7 kΩ) should be inserted in parallel with D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared among several different HSDs. Also in this case, the presence of the ground network produces a shift (≈ 600 mV) in the input threshold and in the status output values, if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

6.2 Vcc overshoot protection

To protect the device from supply rail overshoot, a TVS is inserted between VCC and GND.

It will be chosen to protect the circuit but not interferes with its normal operations.

For this reason, the TVS must be selected with appropriate V_{BR} and V_{CL} values for the maximum operating voltage of the application.

6.3 MCU I/Os protection

If a ground protection network is used and a negative transient is present on the VCC line, the control pins are pulled negative. ST recommends placing a resistor (Rprot) in series to protect the microcontroller I/O pins from latch-up.

The value of these resistors is a compromise between the leakage current of the microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation: R_{prot} range calculation

$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -600 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

30 kΩ ≤ R_{prot} ≤ 180 kΩ.

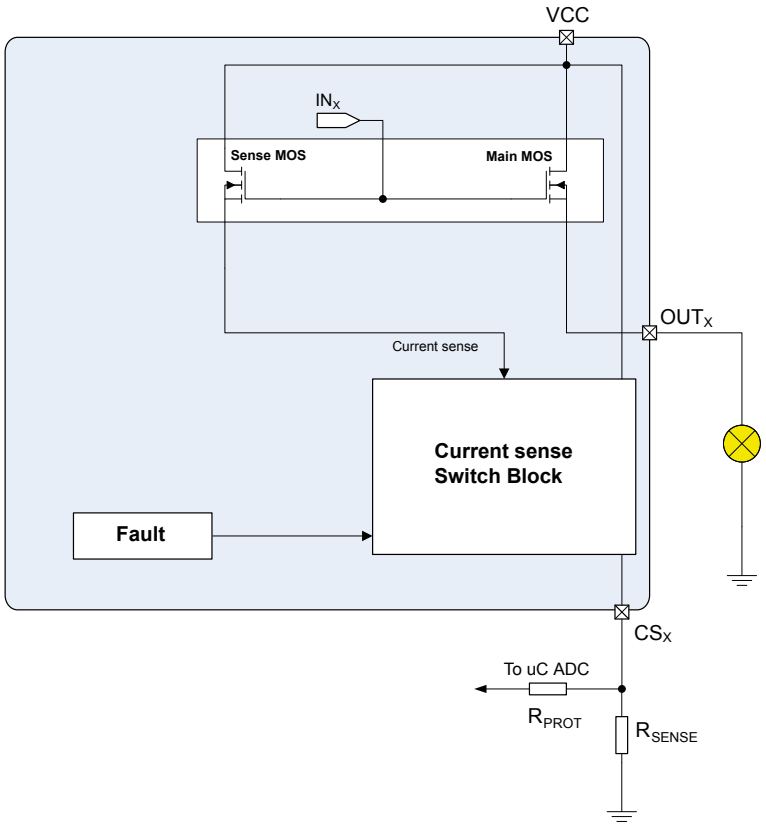
Recommended value: R_{prot} = 60 kΩ.

6.4 Analog current sense

Diagnostic information on device and load status are provided by the analog output pins (CS1, CS2).

6.4.1 Principle of current sense signal generation

Figure 29. Current sense block diagram



Current sense

The output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted into a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations.

Current provided by CS_X: $I_{SENSE} = I_{OUT} / K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT} / K$

Where:

- V_{SENSE} is the voltage measurable on the R_{SENSE} resistor
- I_{SENSE} is the current provided from CS_X pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/over-temperature, the fault is indicated by the CS pin, which is switched to a “current limited” voltage source, V_{SENSEH}.

In any case, the current sourced by the CS_X pin in this condition is limited to I_{SENSEH}.

6.4.2 Short to VCC and OFF-state open-load detection

Short to VCC

A short circuit between VCC and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off-state mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} (see Figure 30).

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

$R_{PU} < (V_{PU} - 4) / I_{L(off2)min}$

Figure 30. **Application schematic for open-load detection in off-state**

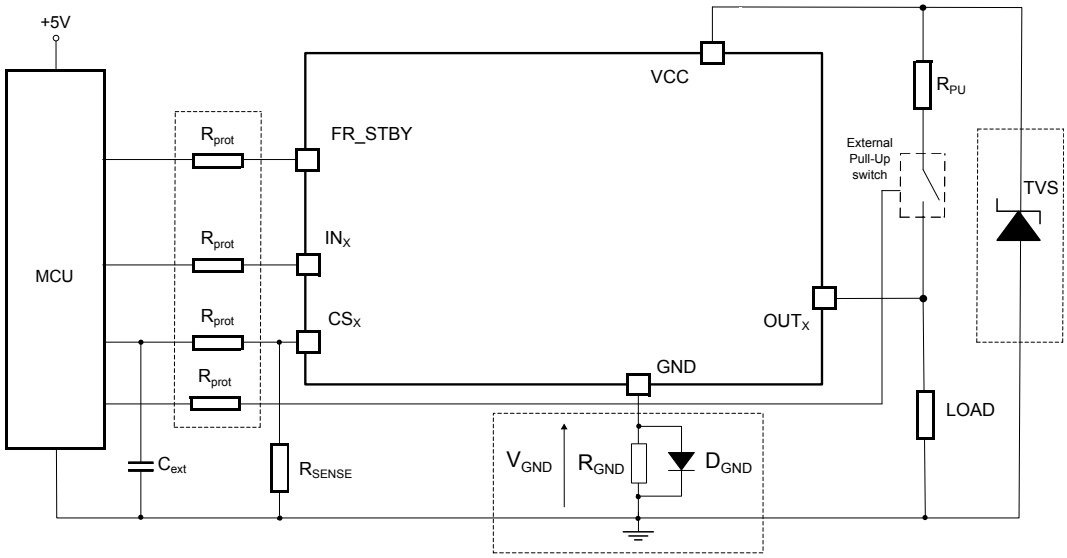
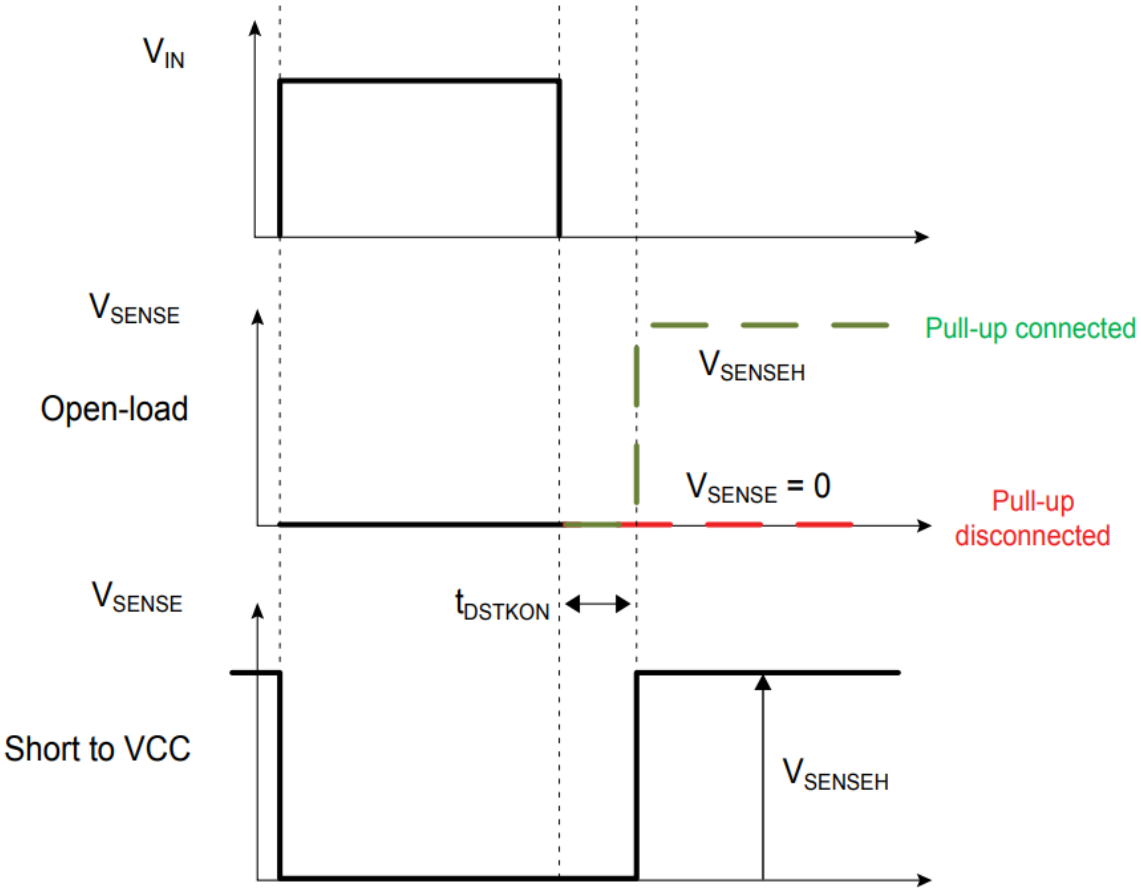


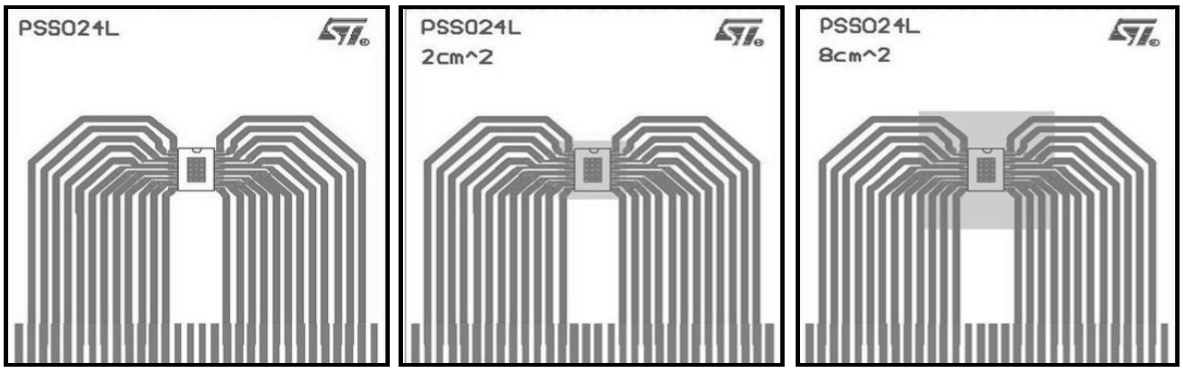
Figure 31. **Open-load / short to VCC condition**



7 Package and PCB thermal data

7.1 PowerSSO-24 thermal data

Figure 32. **PowerSSO-24 PCB**



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Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 µm (front and back side), copper areas: from minimum pad lay-out to 8 cm^2).

Figure 33. **R_{thJA} vs PCB copper area in open box free air condition (one channel ON)**

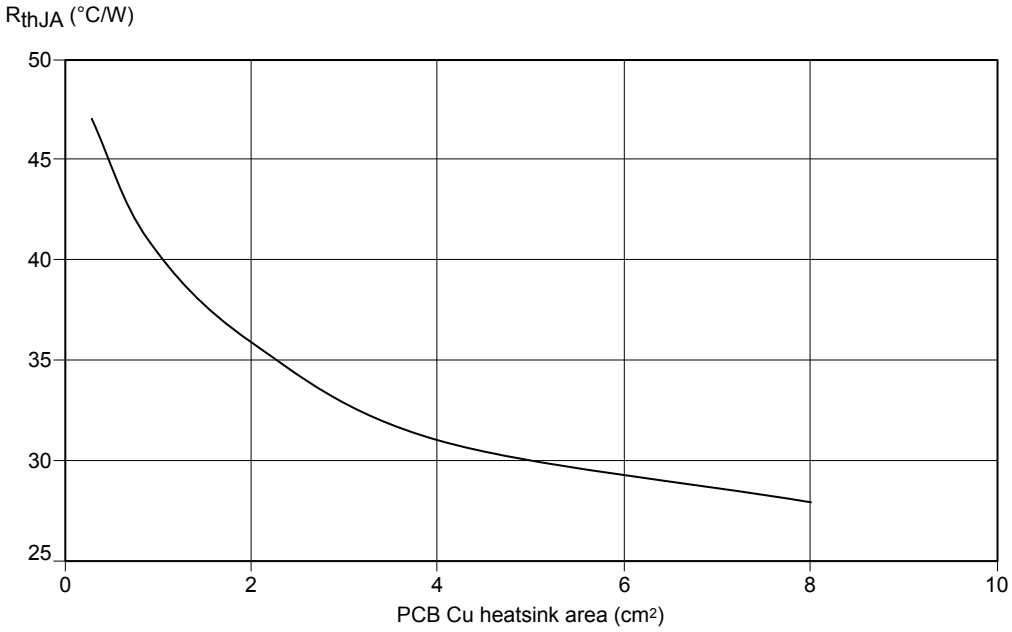

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Figure 34. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

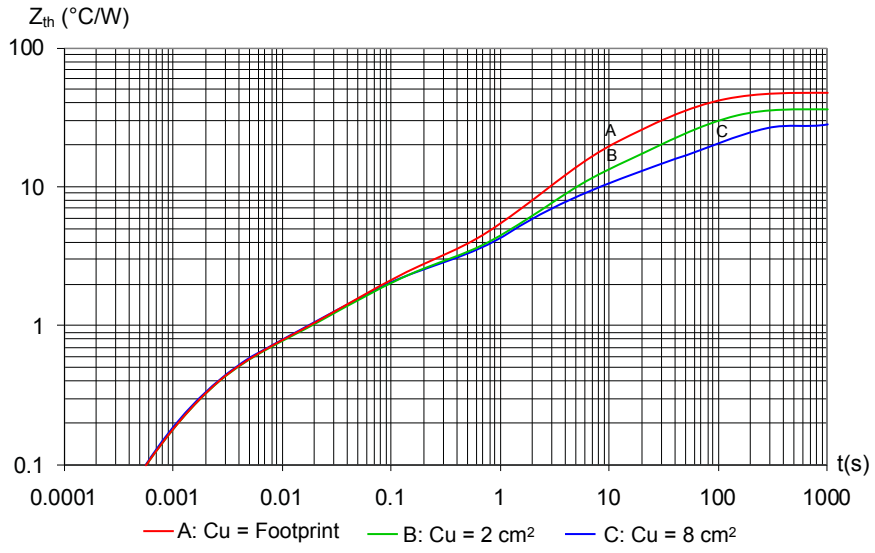

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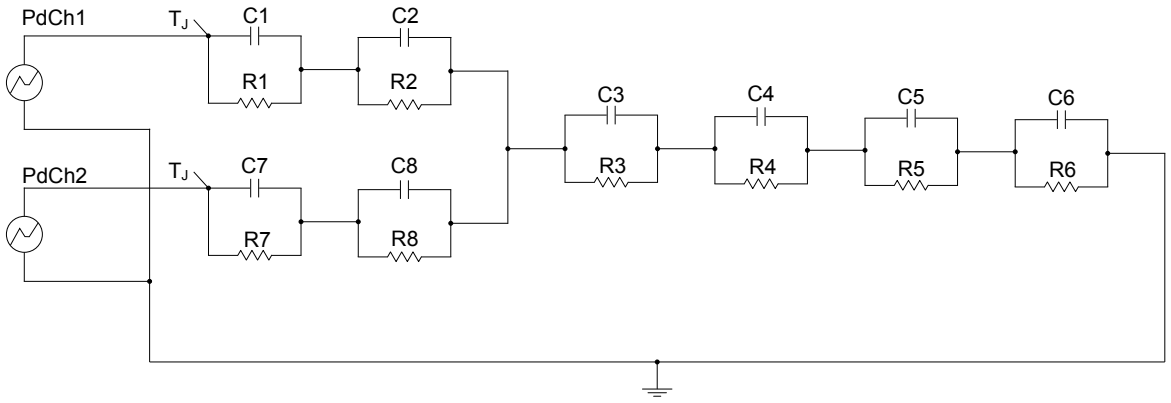
Figure 35. Thermal fitting model of a double channel HSD in PowerSSO-24



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The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation: pulse calculation formula

$Z_{th\delta} = R_{th} \cdot \delta + Z_{thtp} (1 - \delta)$

where $\delta = t_P/T$

Table 12. **Thermal parameters**

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	0.5		
R2 (°C/W)	0.75		
R3 (°C/W)	1		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
R7 (°C/W)	0.5		
R8 (°C/W)	0.75		
C1 (W.s/°C)	0.005		
C2 (W.s/°C)	0.05		
C3 (W.s/°C)	0.1		
C4 (W.s/°C)	0.5		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17
C7 (W.s/°C)	0.005		
C8 (W.s/°C)	0.05		

8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 PowerSSO-24 package information

Figure 36. PowerSSO-24 package dimensions

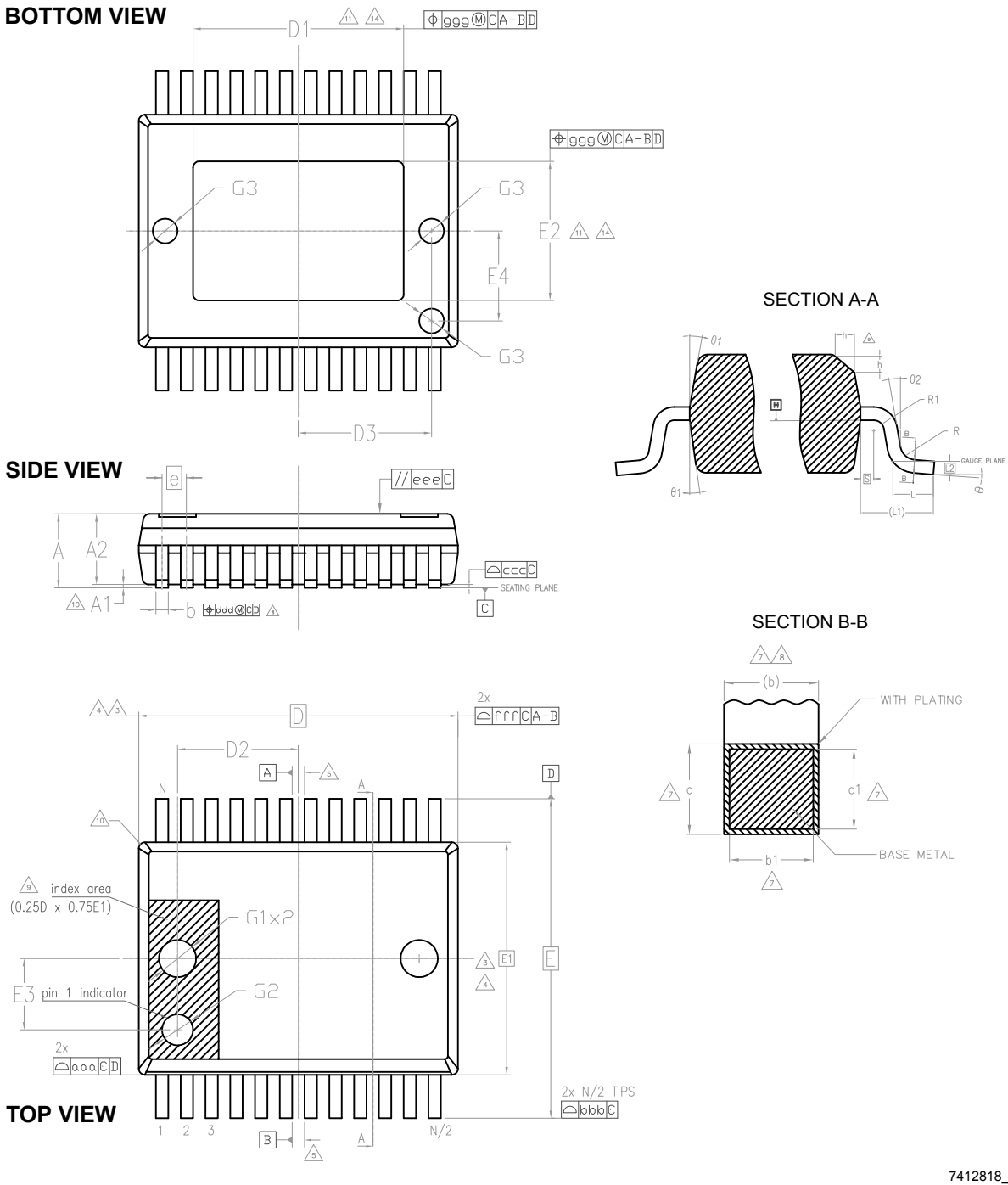

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Table 13. **PowerSSO-24 mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
θ	0°		8°
θ1	5°		10°
θ2	0°		
A			2.45
A1	0.00		0.10
A2	2.15		2.35
b	0.33		0.51
b1	0.28	0.40	0.48
c	0.23		0.32
c1	0.20	0.20	0.30
D		10.30 BSC	
D1	6.50		7.10
D2		3.65	
D3		4.30	
e		0.80 BSC	
E		10.30 BSC	
E1		7.50 BSC	
E2	4.10		4.70
E3		2.30	
E4		2.90	
G1		1.20	
G2		1.00	
G3		0.80	
h	0.30		0.40
L	0.55	0.70	0.85
L1		1.40 REF	
L2		0.25 BSC	
N		24	
R	0.30		
R1	0.20		
S	0.25		

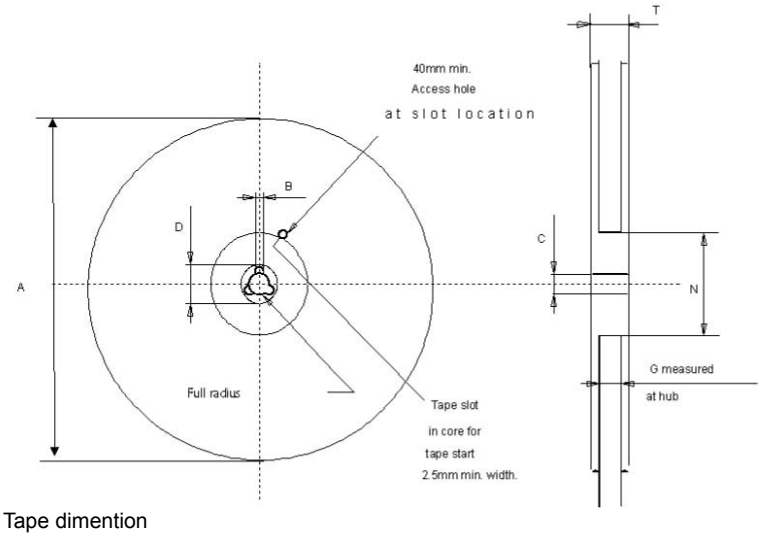
Table 14. **PowerSSO-24 tolerance of form and position**

Symbol	Millimeters
aaa	0.20
bbb	0.20
ccc	0.10
ddd	0.20
eee	0.10

Symbol	Millimeters
fff	0.20
ggg	0.15

8.2 PowerSSO-24 packing information

Figure 37. PowerSSO-24 tape and reel shipment



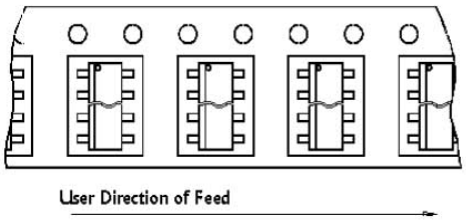
Reel dimensions

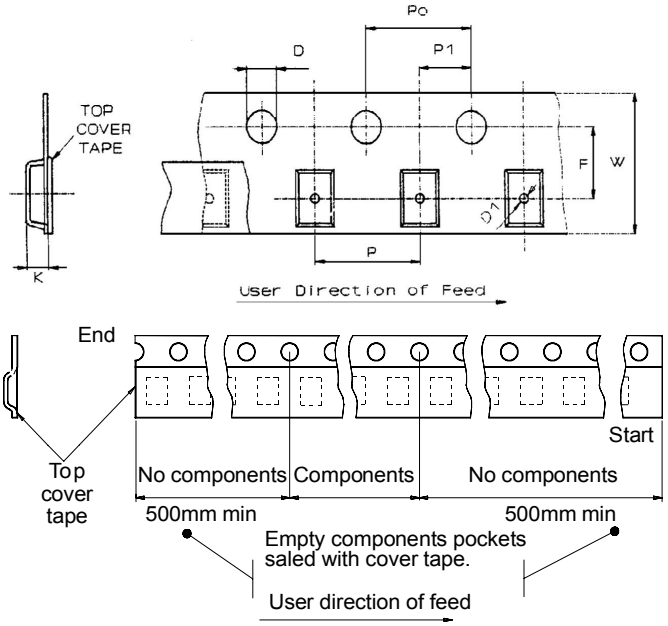
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2/-0)	24.4
N (min)	100
T (max)	30.4

Tape dimention
According to Electronic Industries Association
(EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape hole spacing	P0 (±0.1)	4
Component spacing	P	12
Hole diameter	D (±0.05)	1.55
Hole diameter	D1 (min)	1.5
Hole position	F (±0.1)	11.5
Compartment depth	K(max)	2.85
Hole spacing	P1 (±0.1)	2

All dimensions are in mm.





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9 Ordering information

Table 15. **Ordering information**

Part number	Package	Packing
IPS2070THK	PowerSSO-24	Tape and reel

Revision history

Table 16. **Document revision history**

Date	Revision	Changes
28-Aug-2026	1	Initial release.
17-Sep-2026	2	Changed Vcc AMR in Table 3; some minor changes.

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