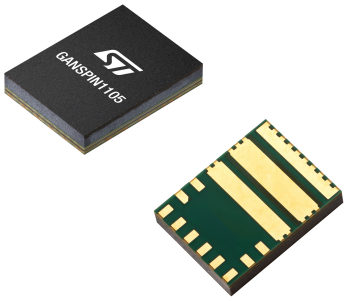
GANSPIN1105

Datasheet

100 V GaN high-power density half-bridge motor driver



LGA 5 x 6.5 x 1.12 mm

Product status link
GANSPIN1105

Features

- 5.5 mΩ half-bridge GaN FETs
- Embedded gate driver with dynamic bootstrap switch
- 100 V transient, 80 V continuous operating voltage
- Switching performance:
  - Switching frequency up to 5 MHz
  - 20 ns propagation delay
  - 1 ns delay matching
- Independent high-side and low-side driving signal with interlocking
- Smart shoot-through protection
- Adjustable turn-on timings
- UVLO, OVLO, and thermal shutdown
- Integrated VCC/Bootstrap capacitors

Applications

- Robotics
- Factory automation
- E-bikes
- Drones
- Power tools

Description

The GANSPIN1105 is a 100 V, 29 A, GaN half-bridge for compact, high-efficiency motor control applications. In a 5x6.5 mm LGA package, it integrates two GaN FETs, a gate driver, and supply capacitors. It offers a compact and efficient GaN power solution.

The GANSPIN1105 provides two independent logic inputs for the control of the high-side and low-side GaN FETs. The externally available outputs of the gate driver allow adjusting the switching speed for the best EMI and efficiency trade-off.

The GANSPIN1105 Smart shoot-through protection circuit, in combination with the interlocking, guarantees no simultaneous high-side and low-side conduction even at near zero dead time.

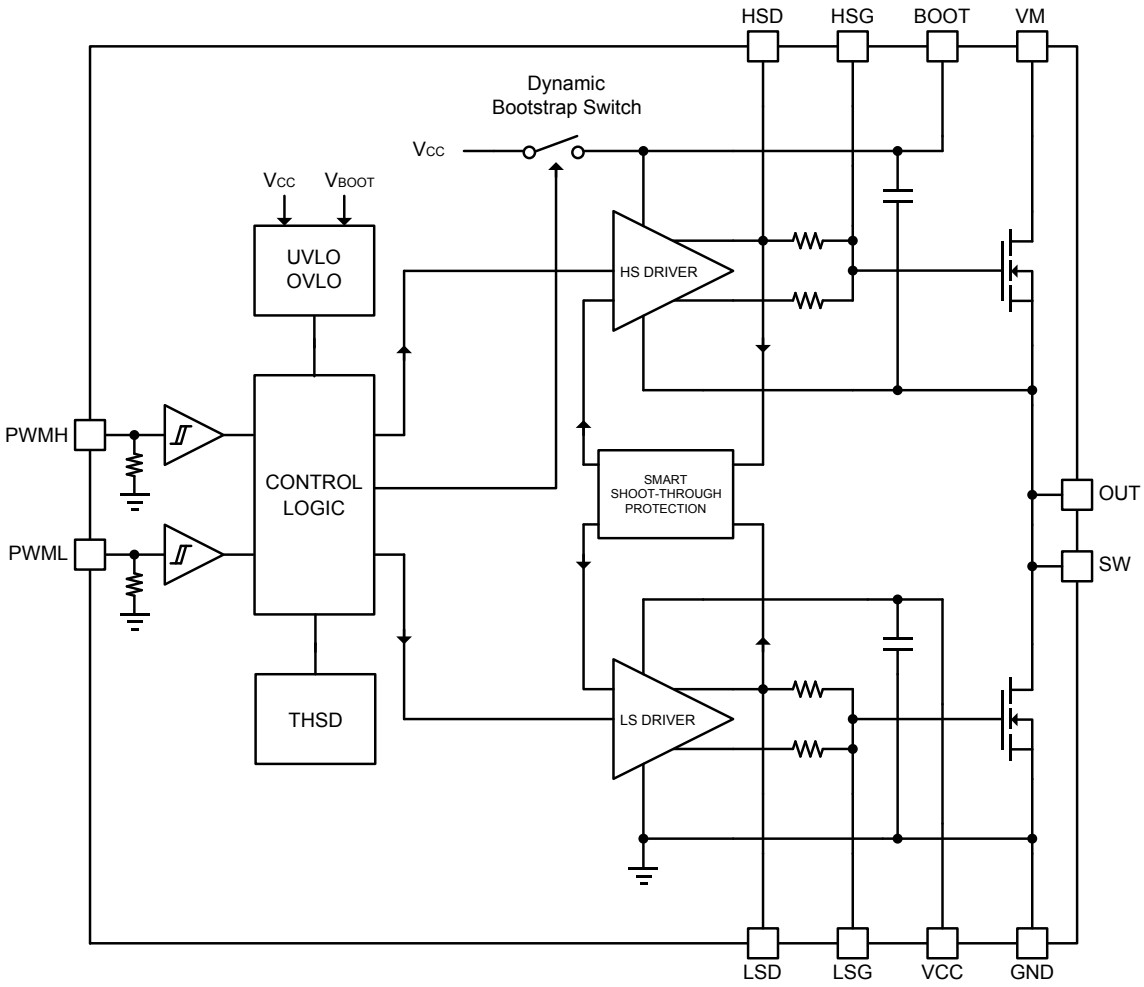
The dynamic bootstrap switch prevents overcharging of the bootstrap capacitor, ensuring stable gate drive voltage in all conditions.

A full set of protections, including UVLO and OVLO for both VCC and BOOT, and thermal shutdown, makes the device suitable for demanding applications.

Fast propagation delay, accurate delay matching, and high dV/dt immunity make the GANSPIN1105 suitable for motor control applications requiring power density and efficiency.

1 Block diagram

Figure 1. **Block diagram**



2 Device ratings

2.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 1 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.
All voltages are referred to GND.

Table 1. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
V_M	Motor supply voltage		-0.3 to 100	V
V_{CC}	Gate driver supply voltage		-0.3 to 6	V
V_{BOOT}	Bootstrap supply voltage		-0.3 to 105	V
V_{BOOT} - V_{OUT}	Bootstrap to switching node voltage		-0.3 to 6	V
V_{OUT}	Switching node voltage		-5 to 100	V
V_{HSG}, V_{HSD}	High side gate and driver voltage		V_{OUT}-0.3 to V_{BOOT}+0.3	V
V_{LSG}, V_{LSD}	Low side gate and driver voltage		-0.3 to 6	V
V_{PWMx}	PWM control inputs voltage		-0.3 to 6	V
I_{OUT}	Output current (1)	Continuous	29	A
		Pulsed (t_{pulse}≤ 100 µs)	125	A
Tj	Junction temperature		-40 to 150	°C
T_{stg}	Storage temperature		-40 to 150	°C

1. *Actual range could be limited by the heat dissipation performance of the application*

2.2 Recommended operating conditions

All voltages are referred to GND.

Table 2. Recommended operating conditions

Symbol	Parameter	Test Conditions	Value	Unit
V_M	Motor supply voltage		0 to 80	V
V_{CC}	Gate driver supply voltage		4.5 to 5.5	V
V_{BOOT}	Bootstrap supply voltage		V_{OUT}+4.5 to V_{OUT}+5.5	V
V_{OUT}	Switching node voltage		-4 to 80	V
V_{PWMx}	PWM control inputs voltage		0 to 5.5	V
SW	Switching node slew-rate		≤ 50	V/ns
Tj	Operating junction temperature		-40 to 125	°C

2.3 Thermal data

In accordance with the JESD51 and JESD51-1 standards, the thermal characteristics of the package are simulated.

Table 3. Thermal data GANSPIN1105

Symbol	Parameter	Test conditions	Value	Unit
R_{thJA}	Thermal resistance, junction to ambient		61.3	°C/W
$R_{thJC(TOP)}$	Thermal resistance, junction to case top		19.3	°C/W
$R_{thJ\ C(BOT)}$	Thermal resistance, junction to case bottom		4.3	°C/W

2.4 Electrical sensitivity characteristics

Table 4. ESD ratings

Symbol	Parameter	Test Conditions	Value	Unit
HBM	Human Body Model	JESD22-A114	1000	V
CDM	Charged Device Model	JESD22-C101F	1000	V

3 Electrical characteristics

Testing conditions: T_J = 25°C, VCC = BOOT = 5 V, OUT = GND = 0 V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Supply						
I_{CCq}	VCC quiescent current	PWML = PWMH = 0 V		35	60	µA
I_{CC}	VCC current consumption	f_{PWM} = 1 MHz		20	30	mA
I_{BOOTq}	BOOT quiescent current	PWML = PWMH = 0 V		40	70	µA
I_{BOOT}	BOOT current consumption	f_{PWM} = 1 MHz		20	30	mA
V_{CCOV}	VCC OVLO threshold	VCC voltage rising	5.7	6	6.3	V
$V_{CCOVHyst}$	VCC OVLO hysteresis			0.25		V
V_{CCUV}	VCC UVLO threshold	VCC voltage rising	3.9	4.1	4.3	V
$V_{CCUVHyst}$	VCC UVLO hysteresis			0.3		V
V_{BOOTUV}	BOOT UVLO threshold	BOOT voltage rising		3.6		V
$V_{BOOTUVHyst}$	BOOT UVLO hysteresis			0.5		V
$C_{VCC(int)}$	Integrated bypass capacitance	(1)		200		nF
Logic inputs						
V_{IL}	Logic low input voltage				0.8	V
V_{IH}	Logic high input voltage		2.2			V
$V_{I,Hyst}$	Logic input hysteresis			0.6		V
R_{PD}	Logic input pull-down resistance			200		kΩ
Bootstrap						
$R_{BOOT(ON)}$	Bootstrap switch on resistance			4		Ω
$C_{BOOT(int)}$	Integrated bootstrap capacitance	(1)		200		nF
Thermal shutdown						
T_{THSD}	Thermal shutdown temperature threshold			165		°C
$T_{THSDHyst}$	Thermal shutdown hysteresis			20		°C
Gate driver						
I_{SINK}	Peak sink current	HSG = BOOT for HS, LSG = VCC for LS		4.3		A
I_{SOURCE}	Peak source current	HSD = OUT for HS, LSD = GND for LS		1.7		A
$R_{NMOS(ON)}$	NMOS on resistance (pull-down)	I_{SINK} = 10 mA		0.2	1	Ω
R_{PMOS}	PMOS on resistance (pull-up)	I_{SOURCE} = 10 mA		1	2	Ω
GaN FETs						
I_{DSS}	Drain-Source leakage current	V_{DS} = 80 V		0.5	14	µA
$R_{DS(ON)}$	Drain-Source on resistance	I_D = 25 A		5.5	7.0	mΩ
V_{SD}	Source-Drain forward voltage	I_S = 0.5 A		1.4		V

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{OSS}	Output capacitance	V_{DS} = 50 V (1)		220		pF
C_{RSS}	Reverse transfer capacitance	V_{DS} = 50 V (1)		3.5		pF
$C_{OSS(ER)}$	Energy related output capacitance	V_{DS} = 0 to 50 V (1)		340		pF
$C_{RSS(TR)}$	Time related reverse transfer capacitance	V_{DS} = 0 to 50 V (1)		500		pF
Q_{OSS}	Output charge	V_{DS} = 0 to 50 V (1)		25		nC
Timings						
$t_{PWM(min)}$	Minimum pulse charging the output	(1)		10		ns
$t_{HSD(min)}$ $t_{LSD(min)}$	Minimum gate driver output pulse	(1)		12		ns
t_{RHS} t_{RLS}	HSG and LSG rise time	From 0.5 V to 4.5 V (1)		10		ns
t_{FHS} t_{FLS}	HSG and LSG fall time	From 4.5 V to 0.5 V (1)		3		ns
t_{DT}	Dead time	LSG off to HSD on, HSG off to LSD on (1)		1		ns
$t_{DHS(OFF)}$	HS turn-off propagation delay	PWMH falling to HSG falling (1)		20		ns
$t_{DHS(ON)}$	HS turn-on propagation delay	PWMH rising to HSD rising (1)		20		ns
$t_{DLS(OFF)}$	LS turn-off propagation delay	PWML falling to LSG falling (1)		20		ns
$t_{DLS(ON)}$	LS turn-on propagation delay	PWML rising to LSD rising (1)		20		ns
$MT_{(HS-LS)}$	Delay matching between HSG off and LSD on	(1)		1		ns
$MT_{(LS-HS)}$	Delay matching between LSG off and HSD on	(1)		1		ns

1. *Not 100% tested. Guaranteed by design*

3.1 Characteristics and timing graphs

Figure 2. Timing diagram

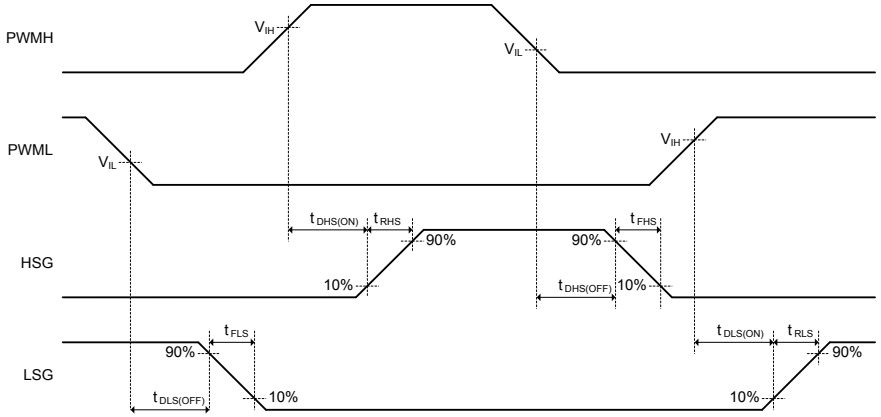


Figure 3. Pulsed Drain current vs. Drain voltage at 25°C

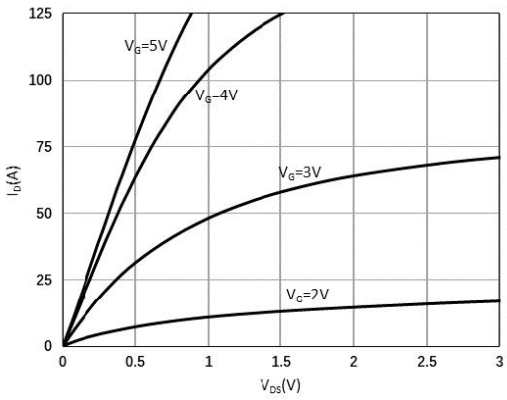


Figure 4. Pulsed Drain current vs. Drain voltage at 125°C

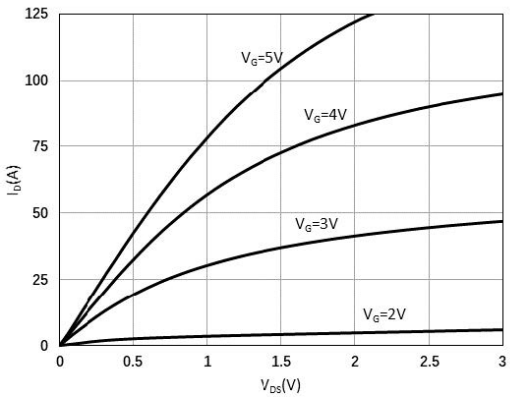


Figure 5. Source-Drain reverse conduction at 25°C

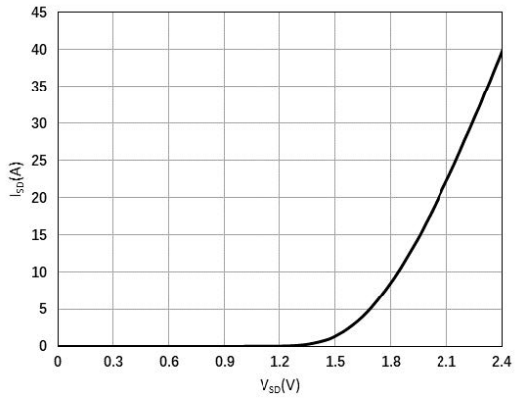


Figure 6. Source-Drain reverse conduction at 125°C

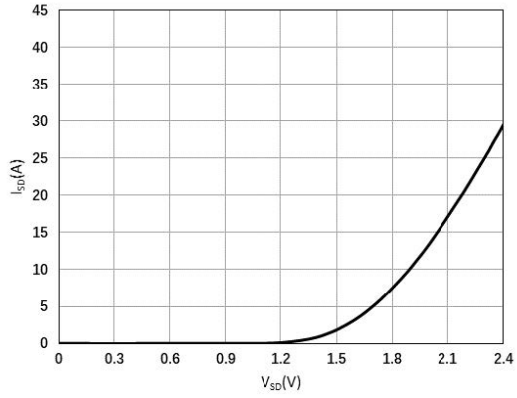


Figure 7. Normalized $R_{DS(ON)}$ vs. temperature

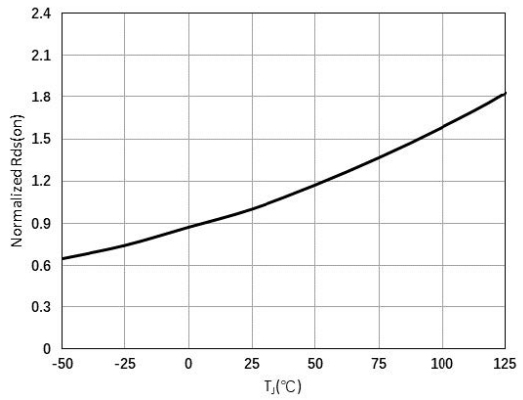


Figure 8. Output capacitance vs. Drain voltage

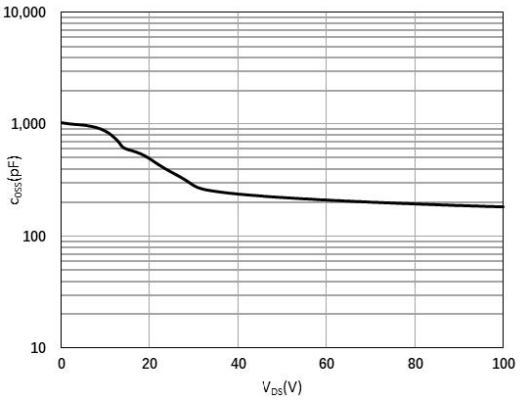


Figure 9. Output cap. stored energy vs. drain voltage

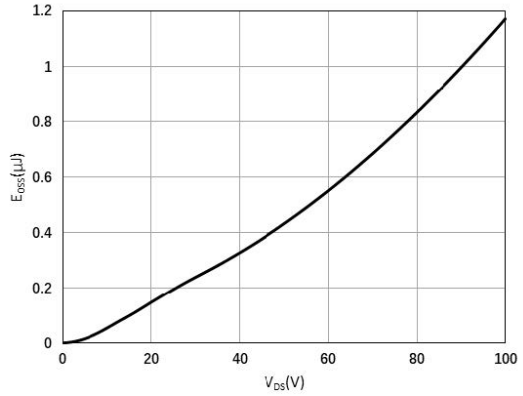


Figure 10. Output charge vs. Drain voltage

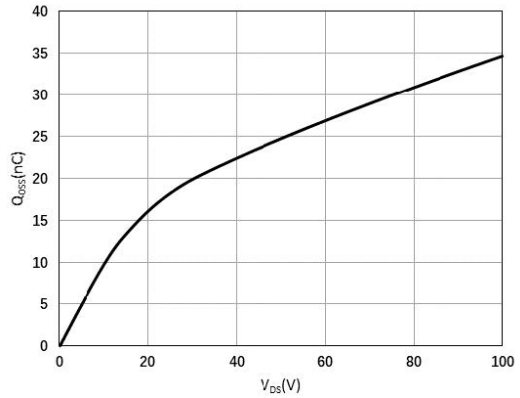


Figure 11. HSG turn-on and LSG turn-off with 10 Ω ext. resistor

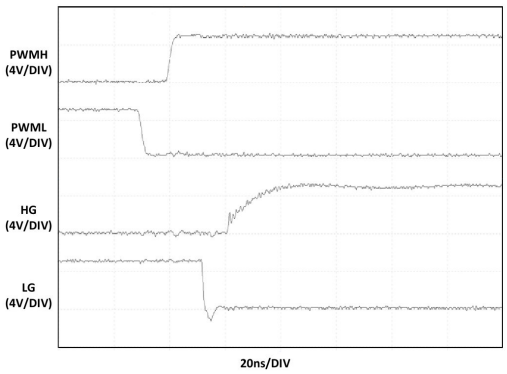


Figure 12. HSG turn-off and LSG turn-on with 10 Ω ext. resistor

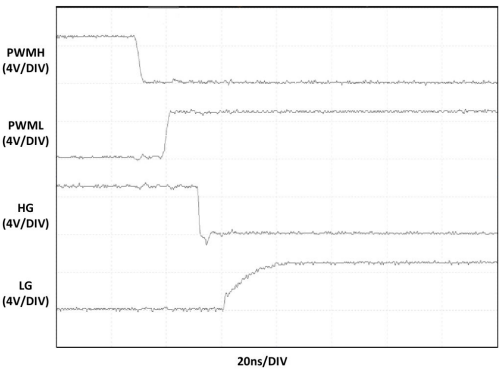


Figure 13. OUT rising (V_M = 48 V, I_{OUT} = 10 A)

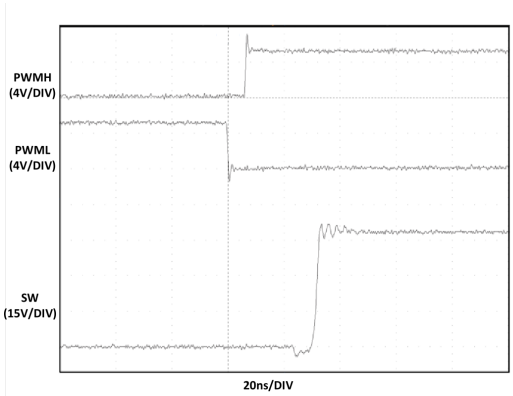


Figure 14. OUT falling (V_M = 48 V, I_{OUT} = 10 A)

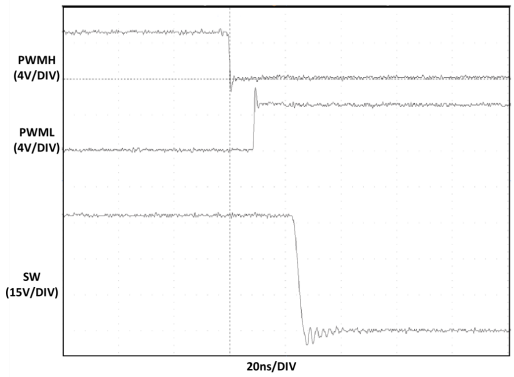


Figure 15. I_{CCq} vs. temperature

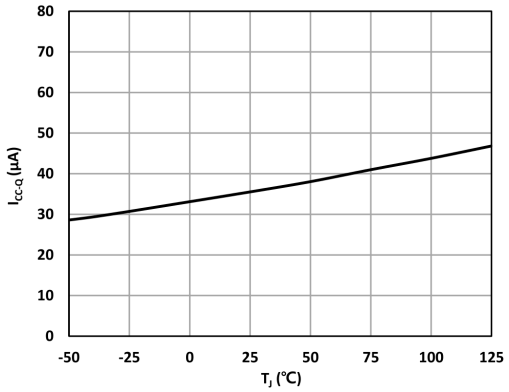


Figure 16. I_{BOOTq} vs. temperature

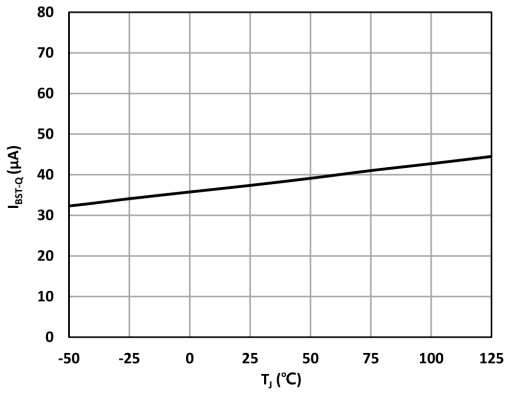


Figure 17. VCC OVLO thresholds vs. temperature

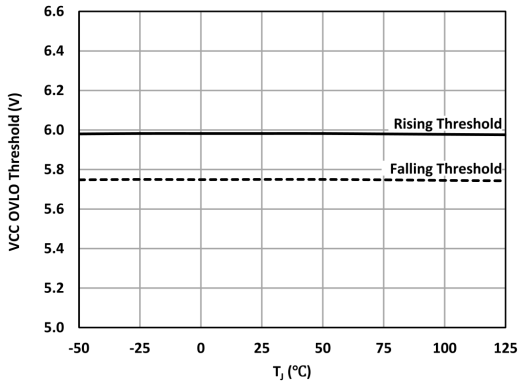


Figure 18. VCC UVLO thresholds vs. temperature

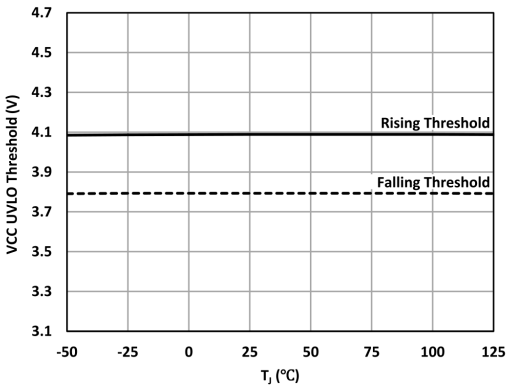


Figure 19. **BOOT UVLO thresholds vs. temperature**

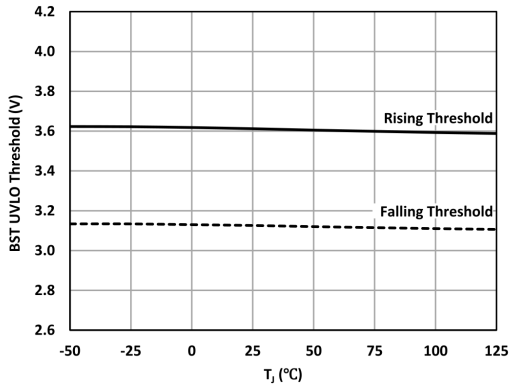


Figure 20. **PWM input threshold vs. temperature**

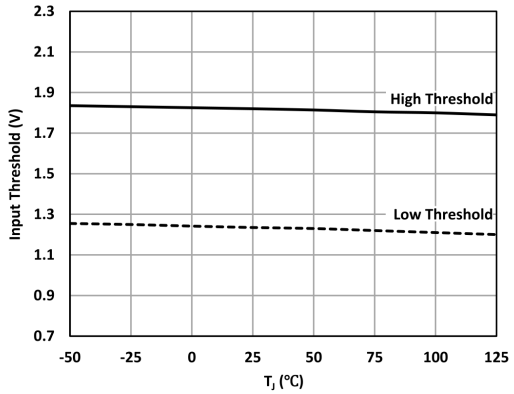


Figure 21. **Bootstrap switch voltage drop vs. current**

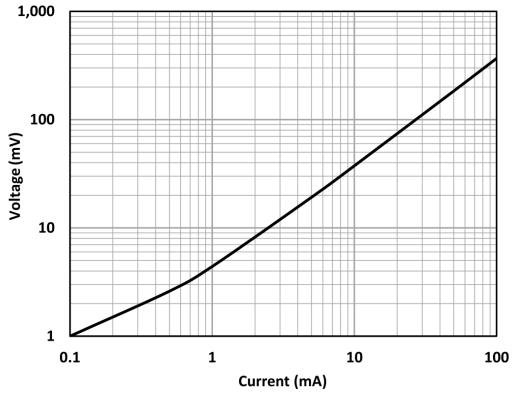


Figure 22. **Output pull-down/pull-up resistance vs. temperature**

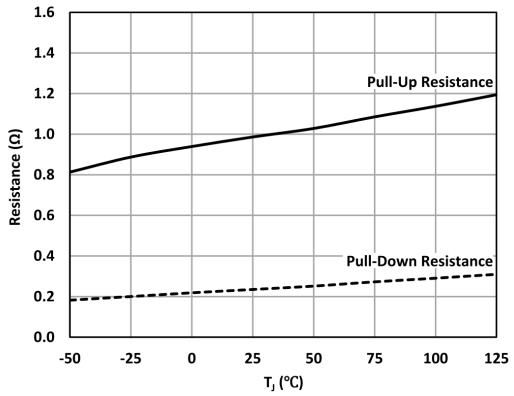


Figure 23. **Low-side propagation delay vs. temperature**

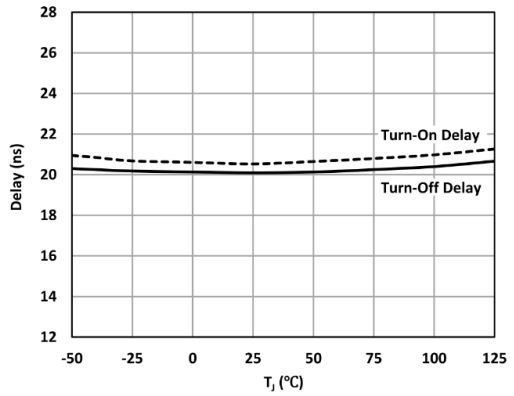
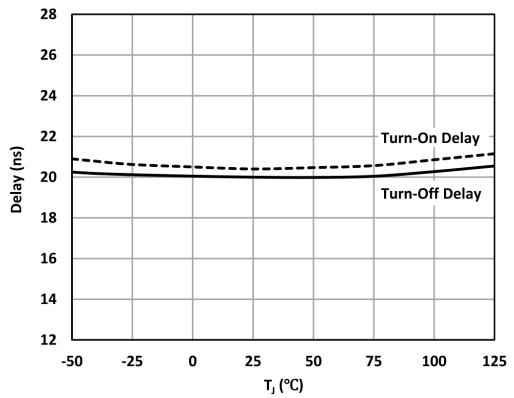


Figure 24. **High-side propagation delay vs. temperature**



4 Pin description

Figure 25. **Pinout**

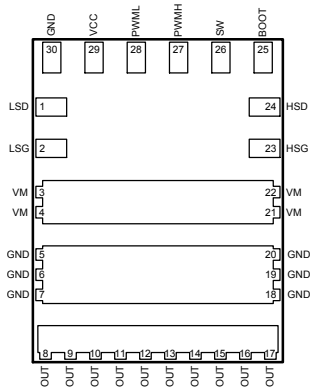


Table 6. **Pin list**

Pin N.	Name	Type	Description
1	LSD	Analog	Low-side gate driver source output. Adding a resistor between LSD and LSG adjusts the turn-on time of the low-side GaN FET.
2	LSG	Analog	Low-side GaN FET gate. Adding a resistor between LSD and LSG adjusts the turn-on time of the low-side GaN FET.
3, 4, 21, 22	VM	Analog	Motor supply voltage and high-side GaN FET drain. All pins are internally shorted.
5, 6, 7, 18, 19, 20, 30	GND	Ground	Ground voltage and low-side GaN FET source. All pins are internally shorted.
8, 9, 10, 11, 12, 13, 14, 15, 16, 17	OUT	Analog	Half-bridge switching node: high-side GaN FET source and low-side GaN FET drain. All pins are internally shorted.
23	HSG	Analog	High-side GaN FET gate. Adding a resistor between HSD and HSG adjusts the turn-on time of the high-side GaN FET.
24	HSD	Analog	High-side gate driver source output. Adding a resistor between HSD and HSG adjusts the turn-on time of the high-side GaN FET.
25	BOOT	Supply	High-side gate driver supply. A total of 200 nF ceramic capacitance is integrated between BOOT and OUT. Additional external bootstrap capacitor is optional.
26	SW	Analog	Switching node monitoring pin internally connected to OUT pins.
27	PWMH	Digital input	High-side control signal.
28	PWML	Digital input	Low-side control signal.
29	VCC	Supply	Gate driver supply voltage. A total of 200 nF ceramic capacitance is integrated between VCC and GND. Additional external bypass capacitor is optional.

5 Device description

The GANSPIN1105 is a 100 V half-bridge module offering an easy-to-use GaN power stage for the design of compact and efficient motor driving applications.

It integrates, in a compact 5×6.5 mm LGA package, two high-performance enhancement-mode gallium nitride (GaN) FETs, a gate driver, gate resistors, and VCC and BOOT supply capacitors (see Figure 26).

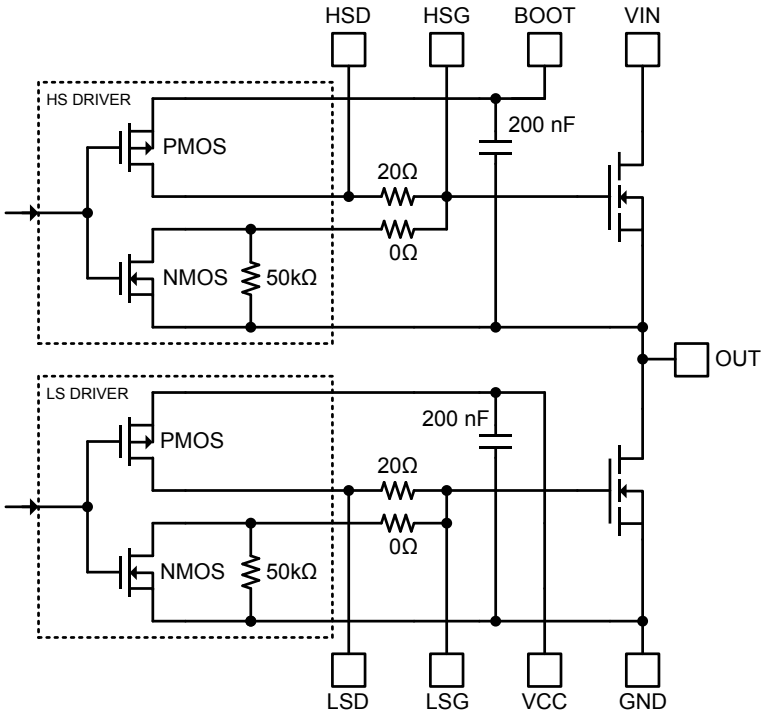
GANSPIN1105 features split gate driver outputs for independent control of the turn-on and turn-off timings of both high-side and low-side GaN FETs. The two fully independent control inputs with interlocking function allow maximum flexibility and the Smart shoot-through protection ensures that the high-side and low-side GaN FETs do not conduct simultaneously.

Thanks to the fast propagation delay (20 ns typical) and the excellent delay matching (1 ns typical) between the high-side and low-side driver channels, the GANSPIN1105 can easily operate at PWM frequencies up to 5 MHz.

The high-side gate driver supply voltage is generated by an embedded dynamic bootstrap switch that prevents overcharging during reverse conduction.

Additionally, a complete set of protections is provided, including independent VCC and BOOT undervoltage lockout (UVLO), VCC overvoltage lockout (OVLO), and thermal shutdown.

Figure 26. Simplified circuit diagram of the power stage



5.1 Control signals

The PWMH and PWML TTL-compatible inputs control the turn-on and the turn-off of the high-side and low-side GaN FETs respectively.

Both inputs include a 10 ns (typical) input deglitch filter to remove spurious pulses from a PWM input. A narrow input pulse exceeding this deglitch delay time is extended to a minimum output pulse of 12 ns (typical) to ensure proper gate turn-on and turn-off transients.

GANSPIN1105 features an interlocking function that prevents shoot-through conditions. When both input pins, PWMH and PWML, are high, the internal logic turns off both output pins, as indicated in Table 7.

Both input pins have an internal pull-down resistor of 200 kΩ and withstand input voltages up to 5.5 V regardless of VCC voltage.

Table 7. Truth table

PWML	PWMH	LS gate driver	HS gate driver	Out
0	0	Sink	Sink	High impedance (Both GaN FETs off)
1	1	Sink	Sink	High impedance - Interlocking (Both GaN FETs off)
1	0	Source	Sink	Connected to GND (Low side GaN FET on, High side GaN FET off)
0	1	Sink	Source	Connected to VM (Low side GaN FET off, High side GaN FET on)

5.2 Smart shoot-through protection

The smart shoot-through protection circuit monitors the true gate voltage of GaN FETs through the split outputs of the gate driver.

It enables the immediate turn-on of the GaN FET after a complete turn-off of the opposite one, avoiding simultaneous conduction (shoot-through or cross-conduction) in any situation.

The turn-off detection condition is detected with extremely fast timing (1 ns typical), making possible a near-zero dead time delay that boosts efficiency and enables high-frequency operation.

5.3 VCC UVLO and OVLO protections

The GANSPIN1105 features UVLO and OVLO for VCC.

When the VCC voltage falls below its UVLO threshold (V_{CCUV}) or exceeds above its OVLO threshold (V_{CCOV}), the embedded gate driver turns off both the high-side and low-side GaN FETs whatever the PWMH and PWML inputs.

5.4 BOOT supply and dynamic bootstrap switch

The GANSPIN1105 integrates a low-resistance dynamic bootstrap switch to generate the high-side supply voltage (BOOT).

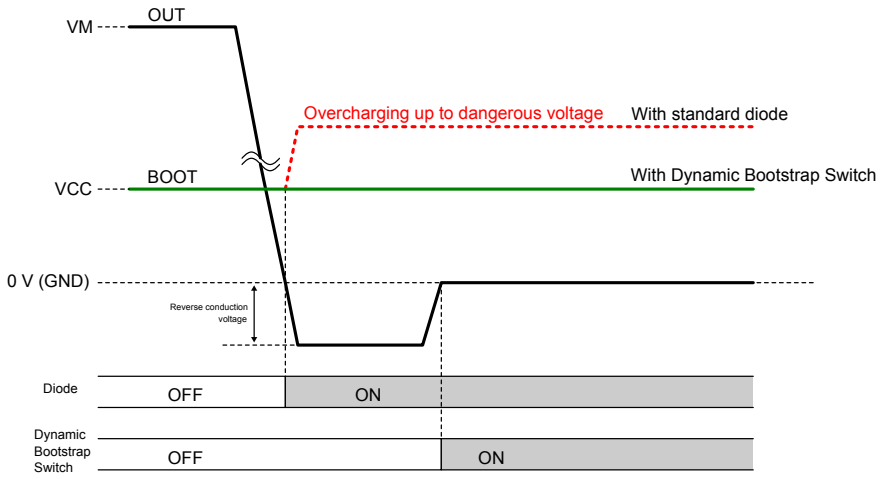
Unlike silicon-based MOSFETs, GaN FETs enter reverse conduction when the gate voltage is 0 V and a drain current is present (see Figure 21), which results in a negative drain voltage of a few volts. This condition usually occurs during the dead time and allows recirculation of the output current.

If the half-bridge sources the current, the low-side GaN FET enters the reverse conduction region, and the reference voltage of the BOOT supply is forced below ground. This condition can overcharge the bootstrap capacitor and can permanently damage the gate driver or violate the gate's AMR of high-side GaN FET.

The dynamic bootstrap switch of the GANSPIN1105 turns on to charge the bootstrap capacitor only when the low-side power switch turns on and the OUT node is shorted to GND. In all other conditions, it turns off to avoid overcharging.

Thanks to this solution GANSPIN1105 guarantees a stable BOOT voltage close to VCC, achieving a matched performance between the high-side and low-side drivers.

Figure 27. Dynamic bootstrap switch operation



5.5 Thermal shutdown

The GANSPIN1105 provides thermal shutdown protection. If the internal junction temperature exceeds the shutdown threshold (T_{THSD}), both the high-side and low-side GaN FETs turn off ignoring the control inputs.

Normal operation is restored as soon as the temperature drops by $T_{THSDHyst}$.

6 Application examples

6.1 Layout and design guidelines

Thanks to the high-performance GaN FET technology, GANSPIN1105 supports high-frequency operation.

Taking advantage of this characteristic implies high voltage (dV/dt) and current (dI/dt) slew rates in the power stage. These slew rates can cause voltage and current spikes when the gate-drive and power-stage loops are not properly managed.

The GANSPIN1105 is a compact module with optimized internal layout and component selection to minimize the gate driving loop and power stage loop parasitics.

However, to minimize parasitics at PCB level requires specific layout strategies:

1. The optional resistor between the HSD/LSD and HSG/LSG pins, which adjusts the turn-on speed of the GaN FETs, must be placed as close as possible to the GANSPIN1105. Use small footprint resistors with low equivalent inductance.
2. The optional VCC decoupling capacitor must be placed as close as possible to the GANSPIN1105, connecting the ground on pin 30. Use ceramic capacitors with low ESR and equivalent inductance.
3. Use planes for the supply (VM) and ground (GND) of the power stage to minimize power losses and parasitics. Place the decoupling capacitors as close as possible to the GANSPIN1105. Ceramic capacitors with low ESR and equivalent inductance are preferred.

Thanks to its optimized pinout, the GANSPIN1105 can achieve good performance even with a two-layers PCB layout.

However, the best results are obtained using four layers or more.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 LGA 5x6.5 mm, 1.12 mm height

Figure 28. Mechanical description - LGA package

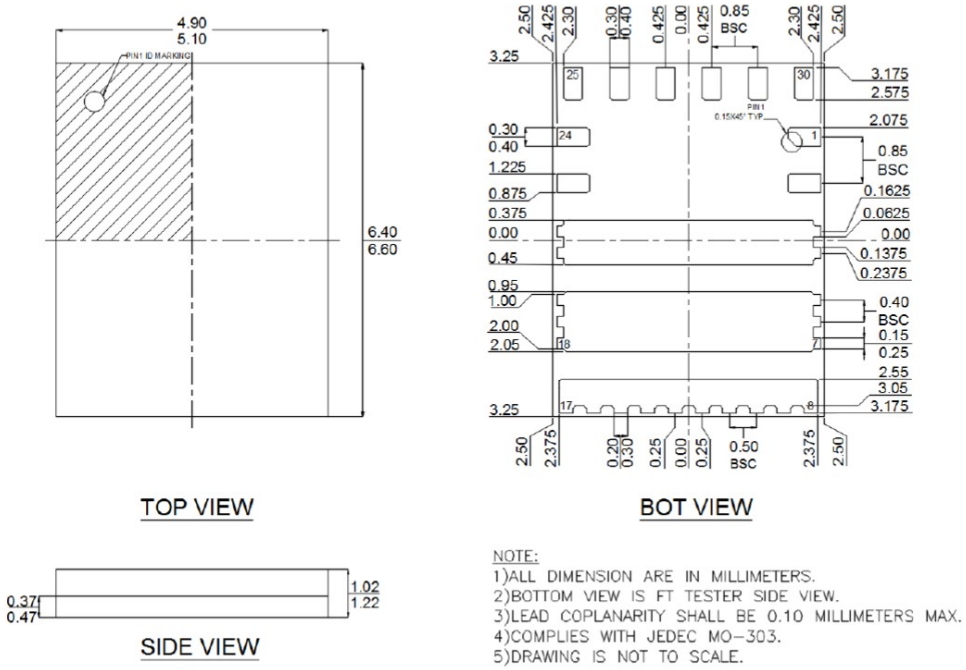
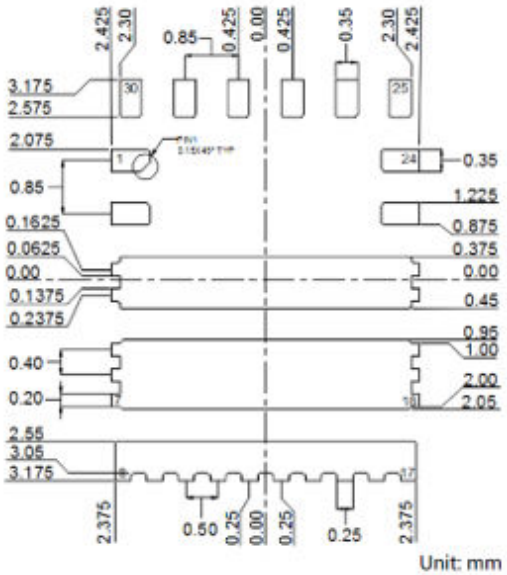


Figure 29. Recommended footprint - LGA package



8 Ordering information

Table 8. **Ordering information**

Order code	Package	Package marking	Packing
GANSPIN1105	LGA 5x6.5 mm, 1.12 mm height		Tape and reel

Revision history

Table 9. **Document revision history**

Date	Version	Changes
04-Nov-2026	1	Initial release.

Contents

1 Block diagram 2
2 Device ratings 3
2.1 Absolute maximum ratings 3
2.2 Recommended operating conditions 3
2.3 Thermal data 4
2.4 Electrical sensitivity characteristics 4
3 Electrical characteristics 5
3.1 Characteristics and timing graphs 7
4 Pin description 11
5 Device description 12
5.1 Control signals 13
5.2 Smart shoot-through protection 13
5.3 VCC UVLO and OVLO protections 13
5.4 BOOT supply and dynamic bootstrap switch 14
5.5 Thermal shutdown 14
6 Application examples 15
6.1 Layout and design guidelines 15
7 Package information 16
7.1 LGA 5x6.5 mm, 1.12 mm height 16
8 Ordering information 17
Revision history 18
List of tables 20
List of figures 21

List of tables

Table 1. Absolute maximum ratings . . . 3
Table 2. Recommended operating conditions . . . 3
Table 3. Thermal data GANSPIN1105 . . . 4
Table 4. ESD ratings . . . 4
Table 5. Electrical characteristics . . . 5
Table 6. Pin list . . . 11
Table 7. Truth table . . . 13
Table 8. Ordering information . . . 17
Table 9. Document revision history . . . 18

List of figures

Figure 1. Block diagram . . . 2
Figure 2. Timing diagram . . . 7
Figure 3. Pulsed Drain current vs. Drain voltage at 25°C . . . 7
Figure 4. Pulsed Drain current vs. Drain voltage at 125°C . . . 7
Figure 5. Source-Drain reverse conduction at 25°C . . . 7
Figure 6. Source-Drain reverse conduction at 125°C . . . 7
Figure 7. Normalized $R_{DS(ON)}$ vs. temperature . . . 8
Figure 8. Output capacitance vs. Drain voltage . . . 8
Figure 9. Output cap. stored energy vs. drain voltage . . . 8
Figure 10. Output charge vs. Drain voltage . . . 8
Figure 11. HSG turn-on and LSG turn-off with 10 Ω ext. resistor . . . 8
Figure 12. HSG turn-off and LSG turn-on with 10 Ω ext. resistor . . . 8
Figure 13. OUT rising (V_M = 48 V, I_{OUT} = 10 A) . . . 9
Figure 14. OUT falling (V_M = 48 V, I_{OUT} = 10 A) . . . 9
Figure 15. I_{CCq} vs. temperature . . . 9
Figure 16. I_{BOOTq} vs. temperature . . . 9
Figure 17. VCC OVLO thresholds vs. temperature . . . 9
Figure 18. VCC UVLO thresholds vs. temperature . . . 9
Figure 19. BOOT UVLO thresholds vs. temperature . . . 10
Figure 20. PWM input threshold vs. temperature . . . 10
Figure 21. Bootstrap switch voltage drop vs. current . . . 10
Figure 22. Output pull-down/pull-up resistance vs. temperature . . . 10
Figure 23. Low-side propagation delay vs. temperature . . . 10
Figure 24. High-side propagation delay vs. temperature . . . 10
Figure 25. Pinout . . . 11
Figure 26. Simplified circuit diagram of the power stage . . . 12
Figure 27. Dynamic bootstrap switch operation . . . 14
Figure 28. Mechanical description - LGA package . . . 16
Figure 29. Recommended footprint - LGA package . . . 16

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved