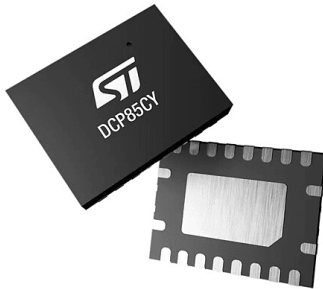


Wide 5.5 V to 85 V input voltage range synchronous buck controller

Features



Maturity status link

[DCP85CY](#)

- AEC-Q100 Grade 1 qualified 
- Wide 5.5 V to 85 V input voltage range
- Adjustable output voltage from 0.8 V to 60 V
- 100 kHz - 1 MHz switching frequency range
- 40 ns minimum on-time for extreme duty ratio
- Low dropout operation during line transient
- Adjustable soft-start or input voltage tracking
- Pulse skipping or forced PWM operation at light load
- Synchronization
- Adjustable precision enables
- Power-good open collector output validates V_{OUT}
- 7.5 V gate drivers for standard V_{TH} MOSFETs
- Constant current protection with hiccup mode
- Precision or lossless programmable current sensing
- Input voltage undervoltage lockout
- Internal voltage monitoring
- Thermal protection
- Operating junction temperature range: -40 °C to 150 °C

Applications

- Unregulated 24 V and 48 V input voltage Automotive bus
- Conversion from high-voltage battery to 12 V and 5 V rail

Description

The **DCP85CY** is a synchronous buck controller that features a wide input voltage range of 5.5 V to 85 V. It supports an extreme voltage conversion ratio across a switching frequency range of 100 kHz to 1 MHz, thanks to a 40 ns minimum conduction time.

The diode emulation (DEM) mode implements pulse-skipping operation, which maximizes efficiency at light load and provides controlled output voltage ripple. Forced pulse-width modulation (FPWM) maintains a constant switching frequency across the load range and minimizes output voltage ripple.

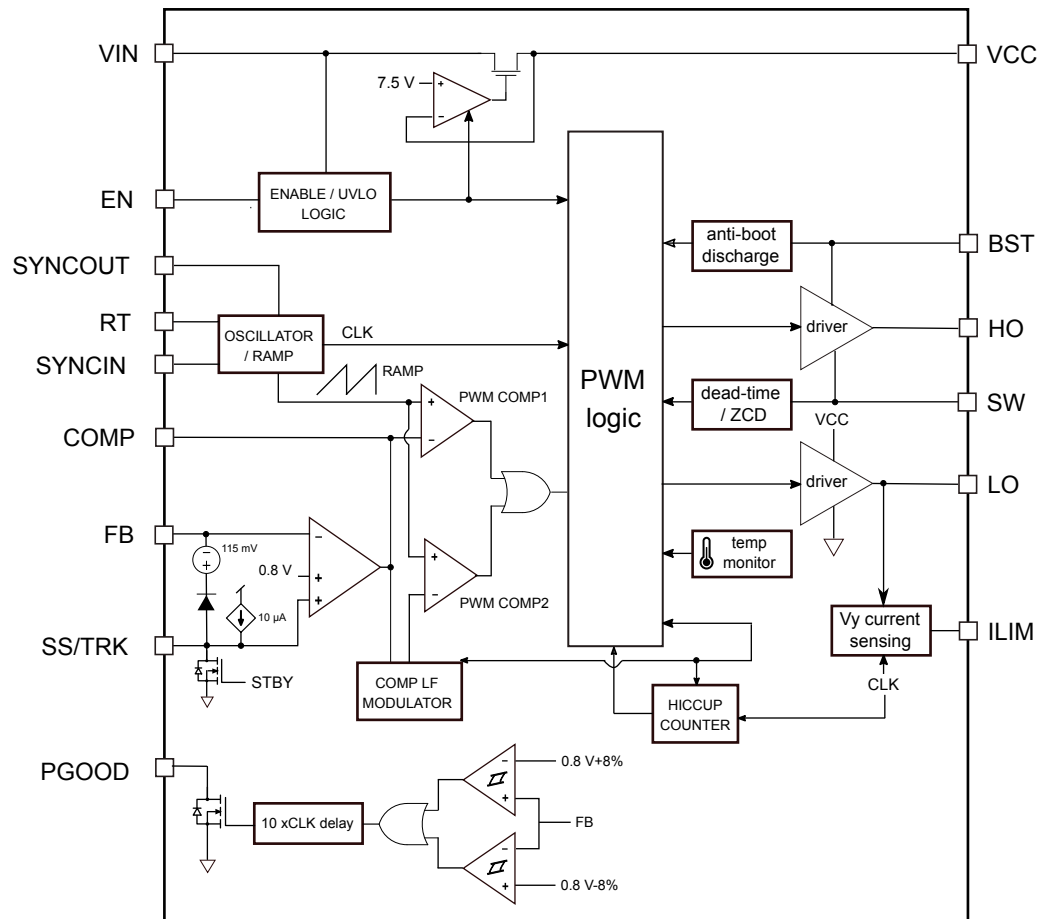
The power-good open-collector output validates the regulated output voltage for monitoring. It also supports output voltage sequencing for digital integrated circuits (ICs) during power-up. An embedded gate driver minimizes the number of external components and is designed for standard threshold-voltage (V_{TH}) MOSFETs.

Embedded protection functions, including output overcurrent, input undervoltage lockout (UVLO), internal voltage monitoring, and thermal shutdown, ensure controlled and safe operation in critical telecom, networking, and Automotive applications.

The device is available in a QFN 20 leads 3.5 x 4.5 mm package with wettable flanks.

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. QFN pin connection (top view)

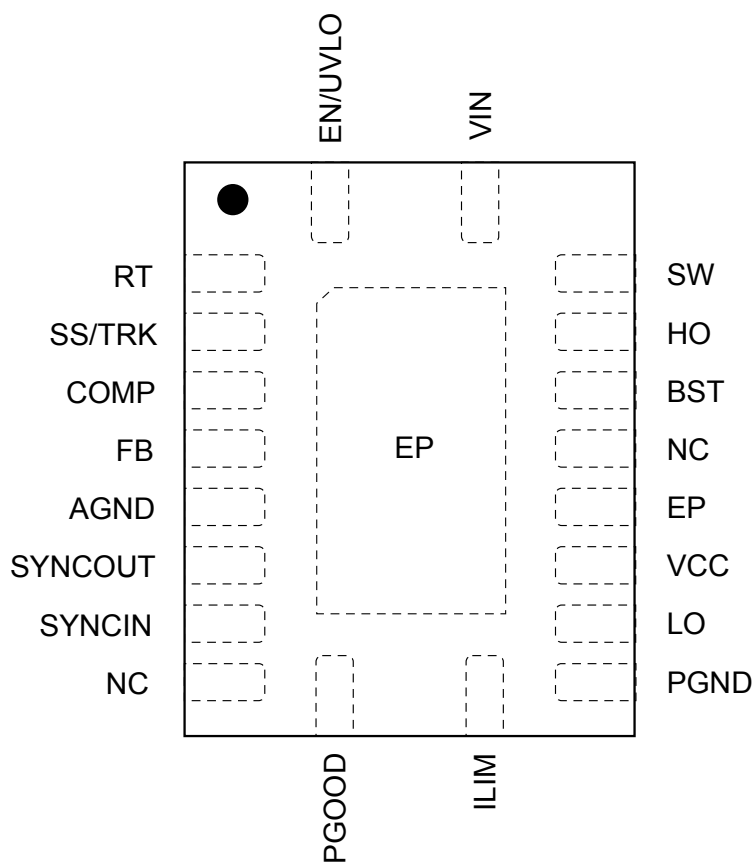


Table 1. Pin description

QFN pin	Name	Function
1	EN/UVLO	The central tap of a resistor divider connected to this pin helps to design the enable and undervoltage lockout thresholds referred to the input voltage. - VEN/UVLO < 0.4 V typ.: the device is in shutdown mode 0.4 V typ. < VEN/UVLO < 1.2 V typ.: device in standby - VCC regulator active - SS/TRK pin in low-impedance - VEN/UVLO > 1.2 V typ.: SS/TRK pin released and the device ready to start - 10 μA current flows to the external resistor divider to design the enable hysteresis.
2	RT	A pull-down resistor to AGND programs the oscillator frequency (100 kHz – 1 MHz) and adjust the internal ramp for constant PWM gain.
3	SS/TRK	The pin circuitry features a current generator (10 μ A typ.) to charge an external capacitor and program the soft-start time. Otherwise, it implements voltage tracking if connected to an auxiliary voltage source. In the soft-start phase, the SS/TRK voltage is the error amplifier reference, and then the internal reference becomes active after the start-up phase ends. The pin is clamped at 115 mV above the FB voltage for controlled recovery from an overcurrent event, or clamped to ground during standby operation or an internal fault.
4	COMP	Output of the internal error amplifier. Connect the compensation network between COMP and the FB.
5	FB	Inverting input of the internal error amplifier. Connect the compensation network between COMP and the FB.
6	AGND	Analog ground
7	SYNCOUT	Synchronization output implements an 180° phase shifted signal referred to the high-side gate driving signal. It always has a duty cycle of 50% at the switching frequency of the device (set by RT resistor or externally) and an amplitude of 3.3 V (typ.).
8	SYNCIN	Synchronization input and DEM / FPWM selection. The device always implements DEM during soft start to support pre-charged output capacitor at device startup. Low logic level selects DEM, high logic level or synchronization clock input enables forced PWM. The device features a smooth transition from DEM to FPWM thanks to the embedded dedicated circuitry.
9	NC	Not internally connected
10	PGOOD	Power-good output. The collector is driven in low-impedance when the FB voltage is outside the regulation window.
11	ILIM	Valley current limit adjustment and current-sense comparator input. A series resistor programs valley current threshold for accurate sensing across external sensing resistor or lossless sensing directly on the drain of the low-side MOSFET.
12	PGND	Power ground
13	LO	Low-side MOSFET gate-drive output. An optional series resistor can be connected to adjust switching times for EMI compatibility.
14	VCC	Output of the internal 7.5 V linear regulator that powers the embedded voltage gate driver. Connect a high-quality MLCC capacitor (470 nF $\leq$ C _{VCC} $\leq$ 2 μ F) to power ground. An external voltage source higher than internal regulator output can be connected (VEN/UVLO > 0.4 V) to increase MOSFET driving capability in terms of gate-driver VTH overdriving or output current capability required at high switching frequency.
15	EP	Pin internally connected to the exposed pad and electrically isolated. Connect to the PGND plane.
16	NC	Not internally connected
17	BST	Bootstrap supply for the high-side gate driver. Connect an external diode between VCC and BOOT and a capacitor (100 nF typ.) between the BOOT and SW pins.
18	HO	High-side MOSFET gate-drive output. An optional series resistor can be connected to adjust switching times for EMI compatibility.
19	SW	Switching node. Connect to the source of the HS MOSFET, the drain of the LS MOSFET and the bootstrap capacitor terminal.
20	VIN	Voltage input for the internal circuitry and VCC linear regulator.
E.P.	EP	Exposed pad. Connect to the PGND plane.

2.1 **Wettable flanks**

The quad-flat no-lead (QFN) package selected for this device enables fully automated optical inspection (AOI). The wettable flanks make this inspection possible because their specific design improve soldering precision. This operation is typically performed after assembly of the part on to the printed board circuit to check whether the package is soldered correctly. The inspection is required to meet high safety and reliability requirements while reducing manufacturing time and cost.

3 Typical application circuit

Figure 3. Typical application

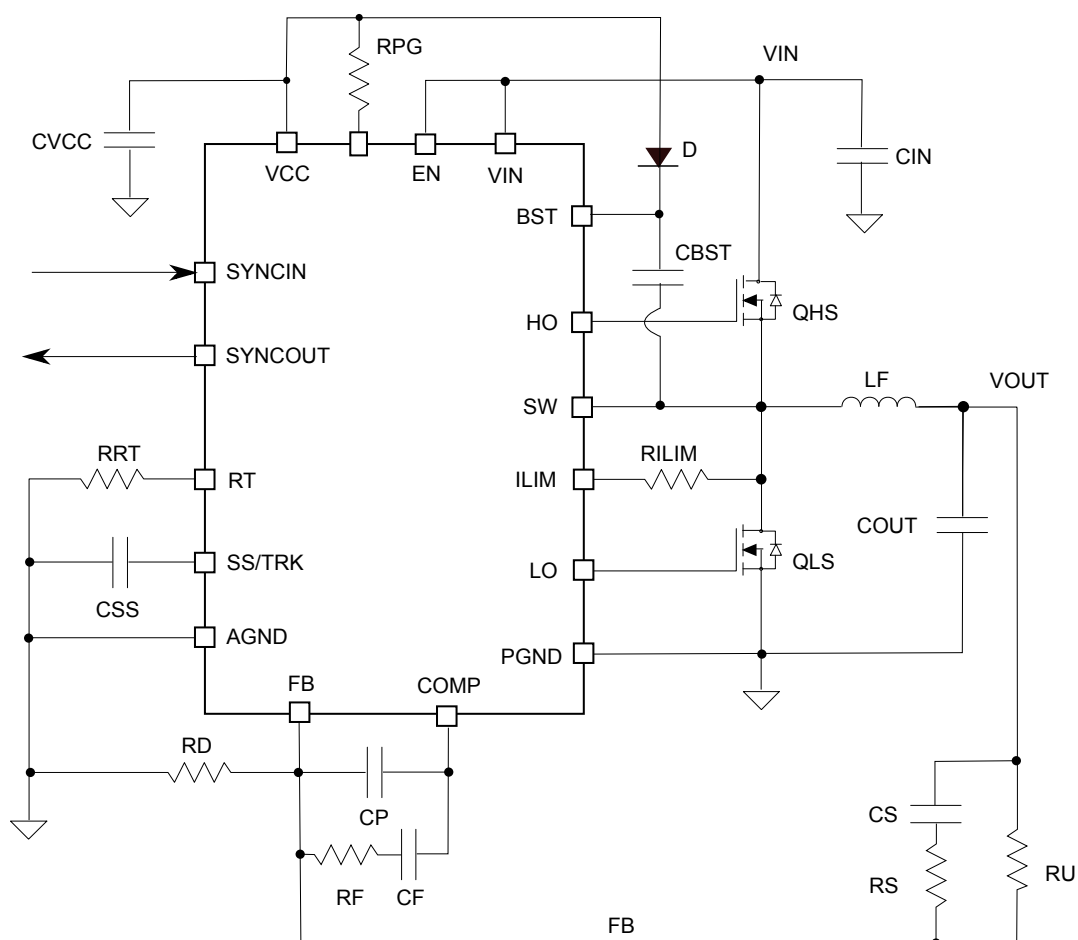


Table 2. Schematic application components description

Symbol	Description
CIN	Input capacitor
CBST	Bootstrap capacitor
COUT	Output capacitor
CC	Compensation capacitor
CP	Compensation capacitor
RF	Compensation resistor
CS	Feed-forward capacitor
RS	Feed-forward resistor
RU	High-side feedback resistor
RD	Low-side feedback resistor
CSS	Soft-start capacitor
RRT	Frequency adjust resistor
RLIM	Current limit resistor

Symbol	Description
LF	Buck inductor
Q1	High-side MOSFET
Q2	Low-side MOSFET
D	Bootstrap diode

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	Input voltage	-0.3	100	V
SW	Switching node	-1	100	V
	Switching node (20 ns transient)	-5	100	V
ILIM	Current limit pin	-1	100	V
EN/UVLO	Enable pin and undervoltage lockout	-0.3	100	V
VCC	VCC pin	-0.3	14	V
FB, SS/TRK, RT	Analog pins	-0.3	4.6	V
SYNCIN	Synchronization input	-0.3	14	V
BST	Bootstrap pin	-0.3	100	V
BST to SW	Bootstrap to SW voltage difference	-0.3	13	V
LO	20 ns transient	-3		V
PGOOD	Power-good	-0.3	14	V
TJ	Operating junction temperature	-40	150	°C
TSTG	Storage temperature range	-40	150	°C

Note: Stressing the device above the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R _{thJA}	Thermal resistance junction-ambient ⁽¹⁾	30	°C/W

1. FR4 board with 1 sq-in pad, 1 oz Cu.

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM AEC Q100-102 HBM ESD Class Level 2	±2	kV
		CMD (corner pins) AEC Q100-011 Class Level C4A	±750	V
		CDM AEC Q100-011 Class Level C4B	±500	V

Table 6. Recommended operating conditions

Symbol	Parameter	Value	Unit
V _{IN}	Input voltage	5.5 to 85	V
EN/UVLO	Analog pins	0 to V _{IN}	V
PGOOD	Power-good	0 to 13	V
I _{SYNCOU}	SYNCOU pin sink and source currents	-1 to 1	mA
I _{PGOOD}	PGOOD sink current	2	mA
T _{OP}	Operating junction temperature range	- 40 to 150	°C

5 Electrical characteristics

$V_{EN/UVLO} = 1.5\text{ V}$, $V_{IN} = 48\text{ V}$; $R_{RT} = 24.9\text{ k}\Omega$; typical values are at $T_J = 25\text{ }^{\circ}\text{C}$; minimum and maximum values are at $-40\text{ }^{\circ}\text{C} \leq T_J \leq 150\text{ }^{\circ}\text{C}$, unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Input supply						
V_{IN}	Operating input voltage		5.5		85	V
I_Q	Quiescent current	Not switching, $V_{SS/TRK} = 0\text{ V}$		2.25	2.5	mA
		$V_{EN/UVLO} = 1\text{ V}$		2.1	2.4	mA
I_{Q-SDN}	Shutdown input current	$V_{EN/UVLO} = 0\text{ V}$, $V_{VCC} < 1\text{ V}$		8.5	40	μA
VCC regulator						
V_{VCC}	Internal regulator voltage	$V_{SS/TRK} = 0\text{ V}$, $9\text{ V} \leq V_{VIN} \leq 85\text{ V}$, $I_{VCC} = 10\text{ mA}$	7.3	7.5	7.7	V
$V_{VCC-LDO}$	VIN to VCC dropout voltage	$V_{VIN} = 6\text{ V}$, $V_{SS/TRK} = 0\text{ V}$, $I_{VCC} = 20\text{ mA}$; $T_J = 25\text{ }^{\circ}\text{C}$		0.4	0.72	V
I_{SC-LDO}	VCC short-circuit current	$V_{SS/TRK} = 0\text{ V}$, $V_{VCC} = 0\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$	40	50	70	mA
V_{VCC-UV}	VCC undervoltage threshold	V_{VCC} rising	4.78	4.93	5.2	V
$V_{VCC-UVH}$	VCC undervoltage hysteresis	V_{VCC} falling		0.26		V
$V_{VCC-EXT}^{(1)}$	Minimum external bias supply voltage	Voltage required to disable V_{CC} regulator	8			V
I_{VCC}	External VCC input current, not switching	$V_{SS/TRK} = 0$, $V_{VCC} = 13\text{ V}$			2.5	mA
Enable and input UVLO						
V_{SDN}	Shut down to standby threshold	$V_{EN/UVLO}$ rising		0.42		V
$V_{SDN-HYS}$	Shutdown threshold hysteresis	$V_{EN/UVLO}$ falling		50		mV
V_{EN}	Standby to operating threshold	$V_{EN/UVLO}$ rising	1.16	1.2	1.25	V
I_{EN-HYS}	Standby to operating hysteresis current	$V_{EN/UVLO} = 1.5\text{ V}$	8	10	11	μA
Error amplifier						
V_{REF}	FB reference voltage	FB connected to COMP	788	800	812	mV
$I_{FB-BIAS}$	FB input bias current	$V_{FB} = 0.8\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$	-0.1		0.1	μA
$V_{COMP-OH}$	COMP output high voltage	$V_{FB} = 0\text{ V}$, COMP sourcing 1 mA		3.3		V
$V_{COMP-OL}$	COMP output low voltage	COMP sinking 1 mA; $T_J = 25\text{ }^{\circ}\text{C}$			0.3	V
$AVOL^{(1)}$	DC gain			94		dB
$GBW^{(1)}$	Unity gain bandwidth			6.5		MHz
Soft-start and voltage tracking						
I_{SS}	SS/TRK capacitor charging current	$V_{SS/TRK} = 0\text{ V}$	7.5	10	12	μA
R_{SS}	SS/TRK discharge FET resistance	$V_{EN/UVLO} = 1\text{ V}$, $V_{SS/TRK} = 0.1\text{ V}$		12		Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SS-FB}	SS/TRK to FB offset	T _J = 25 °C	-15		15	mV
V _{SS-CLAMP}	SS/TRK clamp voltage	V _{SS/TRK} – V _{FB,VFB} = 0.8 V		115		mV
Power-good						
PG _{UTH}	FB upper threshold for PGOOD high to low	% of V _{REF} , V _{FB} rising	106	108	110	%
PG _{LTH}	FB lower threshold for PGOOD high to low	% of V _{REF} , V _{FB} falling	90	92	94	%
PG _{HYS_U}	PGOOD upper threshold hysteresis	% of V _{REF}		3		%
PG _{HYS_L}	PGOOD lower threshold hysteresis	% of V _{REF}		2		%
T _{PG-RISE} ⁽¹⁾	PGOOD rising filter	FB to PGOOD rising edge		10/FSW		μs
T _{PG-FALL} ⁽¹⁾	PGOOD falling filter	FB to PGOOD falling edge		10/FSW		μs
V _{PG-OL}	PGOOD low-state output voltage	V _{FB} = 0.9 V, I _{PGOOD} = 2 mA			150	mV
I _{PG-OH}	PGOOD high-state leakage current	V _{FB} = 0.8 V, V _{PGOOD} = 13 V; T _J = 25 °C			100	nA
Oscillator						
F _{SW}	Oscillator frequency	R _{RT} = 100 kΩ		115		kHz
		R _{RT} = 25 kΩ	375	400	425	
		R _{RT} = 11 kΩ		800		
Synchronization input / output						
F _{SYNC}	SYNCIN external clock frequency (> 120 kHz < 1 MHz)	% of nominal frequency set by R _{RT}	-15		+50	%
V _{SYNC-IH}	Minimum SYNCIN input logic high		2			V
V _{SYNC-IL}	Maximum SYNCIN input logic low				0.8	V
R _{SYNCIN}	SYNCIN input resistance	V _{SYNCIN} = 3 V		20		kΩ
T _{SYNCl-PW}	SYNCIN input minimum pulse-width	Minimum high-state or low-state duration; T _J = 25°C	50			ns
V _{SYNCO-OH}	SYNCOOUT high-state output voltage	I _{SYNCOOUT} = –1 mA (sourcing)	3			V
V _{SYNCO-OL}	SYNCOOUT low-state output voltage	I _{SYNCOOUT} = 1 mA (sinking)			0.4	V
T _{SYNCOOUT}	Delay from HO rising to SYNCOOUT leading edge	V _{SYNCIN} = 0 V, T _S = 1 / F _{SW} , F _{SW} set by R _{RT}		TS/2 - 140		ns
T _{SYNCIN}	Delay from SYNCIN leading edge to HO rising	50% to 50%, R _T = 11 kΩ, V _{IN} = 85 V		190		ns
Bootstrap and BST UVLO						
I _{Q-BST}	BST to SW quiescent current, not switching	V _{SS} / T _{RK} = 0 V, V _{SW} = 48 V, V _{BST} = 54 V, V _{EN} = 1.1 V		300	500	μA
V _{BST-UV}	BST to SW undervoltage detection	V _{BST} – V _{SW} falling		3.4		V
V _{BST-HYS}	BST to SW undervoltage hysteresis	V _{BST} – V _{SW} rising		0.42		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PWM Control						
$T_{ON(MIN)}$	Minimum controllable on-time	$V_{BST} - V_{SW} = 7\text{ V}$, HO 50% to 50%		40	60	ns
$T_{OFF(MIN)}$	Minimum off-time	$V_{BST} - V_{SW} = 7\text{ V}$, HO 50% to 50%		180	250	ns
DC_{MAX}	Maximum duty cycle	$F_{SW} = 100\text{ kHz}$, $5.5\text{ V} \leq V_{VIN} \leq 60\text{ V}$	98	99		%
		$F_{SW} = 400\text{ kHz}$, $5.5\text{ V} \leq V_{VIN} \leq 60\text{ V}$	90	94		%
$V_{RAMP(min)}$	Ramp valley voltage (COMP at 0% duty cycle)			300		mV
k_{FF}	PWM feed-forward gain (V_{IN} / V_{RAMP})	$5.5\text{ V} \leq V_{VIN} \leq 85\text{ V}$		30		V/V
Overcurrent protection (OCP)						
I_{RS}	ILIM source current, R_{SENSE}	25 °C	90	100	110	μA
		-40 °C to 150 °C	80	100	110	
$I_{RDS(on)}$	ILIM source current, $R_{DS(on)}$ mode	SW voltage detected at I_{LIM} , $T_J = 25\text{ °C}$	180	200	220	μA
$I_{RSTC}^{(1)}$	I_{LIM} current temperature compensation	R_{DS-ON} mode		4500		ppm/°C
		R_{SENSE} mode		0		
$V_{ILIM-TH}$	I_{LIM} comparator threshold at ILIM		-9	-2	4.5	mV
Short-circuit protection (SCP)						
$V_{CLAMP-OS}$	Clamp offset voltage – no current limiting	CLAMP to COMP steady-state offset voltage; -40 ≤ T_J ≤ +125 °C		$0.2 + V_{VIN}/150$		V
$V_{CLAMP-MIN}$	Minimum clamp voltage	CLAMP voltage with continuous current limiting; -40 ≤ T_J ≤ +125 °C		$0.3 + V_{VIN}/300$		V
Hiccup mode						
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated		128		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS/TRK release		8192		cycles
Diode emulation						
V_{ZCD-SS}	Zero-cross detect (ZCD) soft-start ramp	ZCD threshold measured at SW pin 50 clock cycles after first HO pulse		0		mV
$V_{ZCD-DIS}$	Zero-cross detect disable threshold (CCM)	ZCD threshold measured at SW pin 1000 clock cycles after first HO pulse		200		mV
V_{DEM-TH}	Diode emulation zero-cross threshold	Measure dat SW with V_{SW} rising	-7	-2	4	mV
Gate drivers						
R_{HO-UP}	HO high-state resistance, HO to BST	$V_{BST} - V_{SW} = 7\text{ V}$, $I_{HO} = -100\text{ mA}$		1.5		Ω
$R_{HO-DOWN}$	$R_{HO-DOWN}$ HO low-state resistance, HO to SW	$V_{BST} - V_{SW} = 7\text{ V}$, $I_{HO} = 100\text{ mA}$		0.9		Ω
R_{LO-UP}	LO high-state resistance, LO to VCC	$V_{BST} - V_{SW} = 7\text{ V}$, $I_{LO} = -100\text{ mA}$		1.5		Ω
$R_{LO-DOWN}$	LO low-state resistance, LO to PGND	$V_{BST} - V_{SW} = 7\text{ V}$, $I_{LO} = 100\text{ mA}$		0.9		Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{HOH}, I_{LOH}^{(1)}$	HO, LO source current	$V_{BST} - V_{SW} = 7\text{ V}$, HO = SW, LO = AGND		2.3		A
$I_{HOL}, I_{LOL}^{(1)}$	HO, LO sink current	$V_{BST} - V_{SW} = 7\text{ V}$, HO = BST, LO = VCC		3.5		A
T_{HO-TR}, T_{LO-TR}	HO, LO rise times	$V_{BST} - V_{SW} = 7\text{ V}$, $C_{LOAD} = 1\text{ nF}$, 20% to 80%		7		ns
T_{HO-TF}, T_{LO-TF}	HO, LO fall times	$V_{BST} - V_{SW} = 7\text{ V}$, $C_{LOAD} = 1\text{ nF}$, 80% to 20%		4		ns
$T_{HO-DT}^{(1)}$	HO turn-on deadtime	$V_{BST} - V_{SW} = 7\text{ V}$, LO off to HO on, 50% to 50%		14		ns
$T_{LO-DT}^{(1)}$	LO turn-on deadtime	$V_{BST} - V_{SW} = 7\text{ V}$, HO off to LO on, 50% to 50%		14		ns
Thermal protection						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD-HYS}	Thermal shutdown hysteresis			20		°C

1. Specified by design – not tested in production.

6 Typical performance characteristics

Efficiency curves, temperature behavior of electrical characteristics, V_{IN} and V_{CC} dependencies. $V_{IN} = 48\text{ V}$, $R_{RT} = 46.4\text{ k}\Omega$, SYNCIN tied to VCC and EN/UVLO tied to VIN, unless otherwise specified.

Figure 4. Efficiency ($V_{OUT} = 5\text{ V}$), CCM

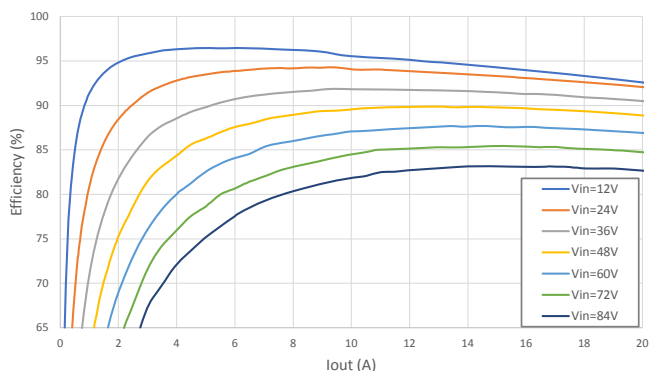


Figure 5. Efficiency ($V_{OUT} = 12\text{ V}$), CCM

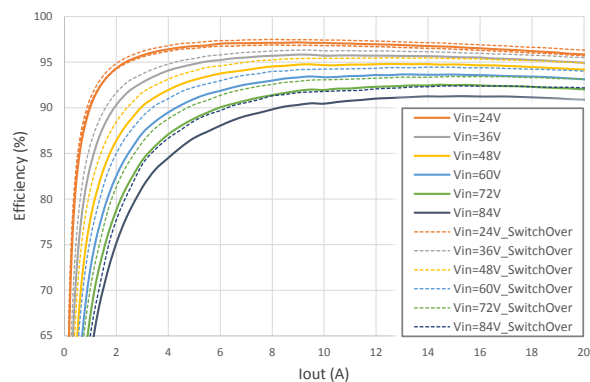


Figure 6. Efficiency ($V_{OUT} = 12\text{ V}$), DCM

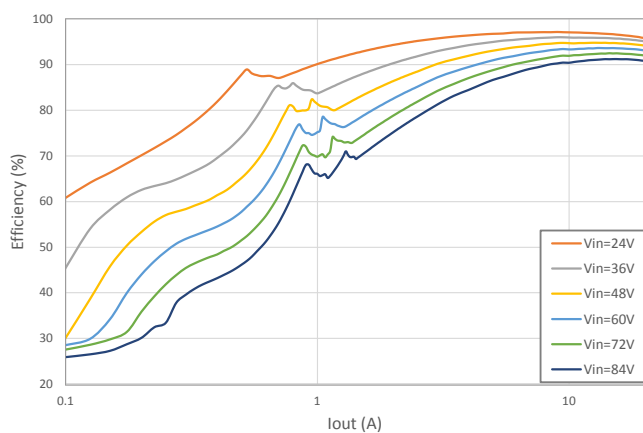


Figure 7. Shut down current (Enable = GND)

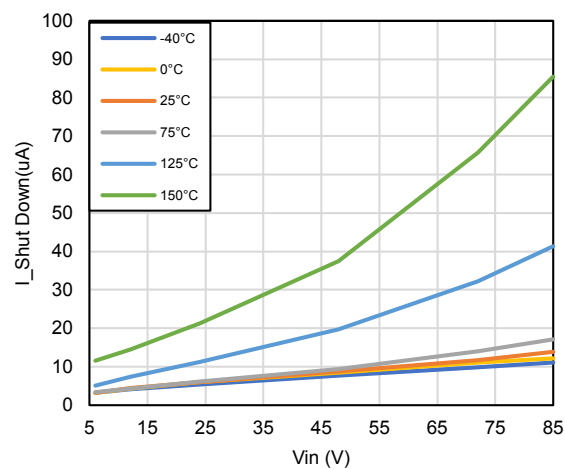


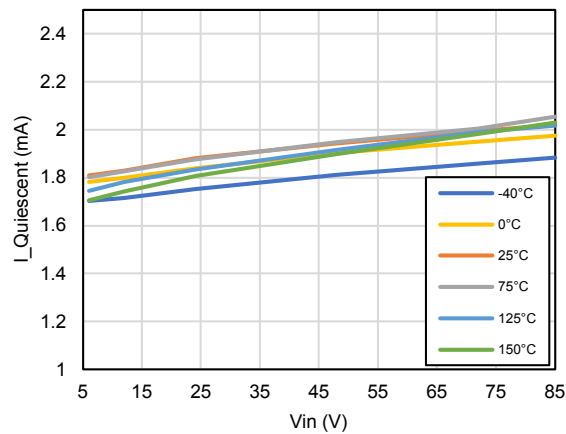
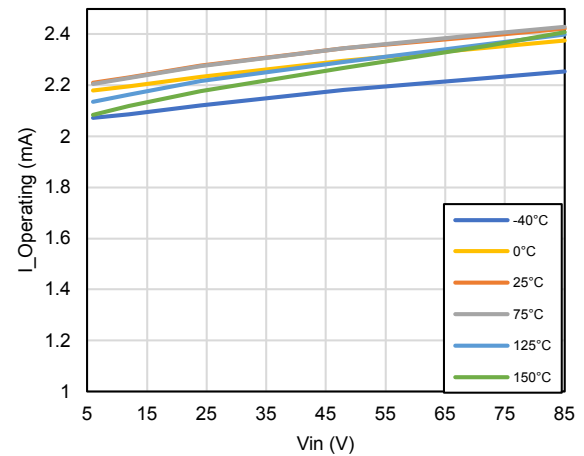
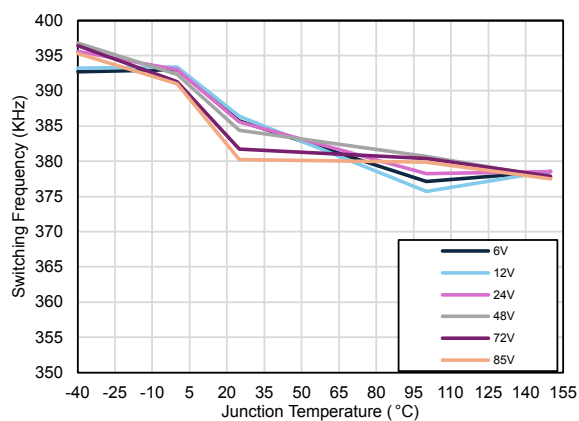
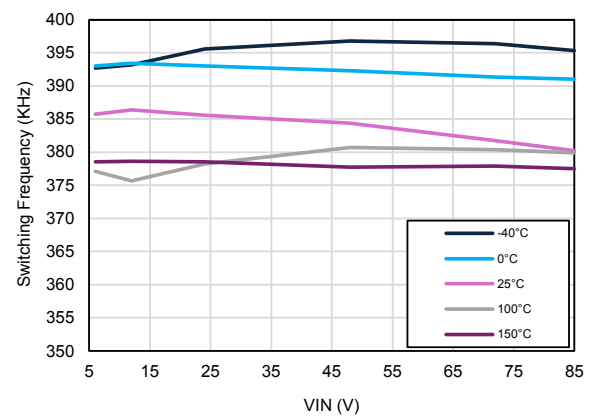
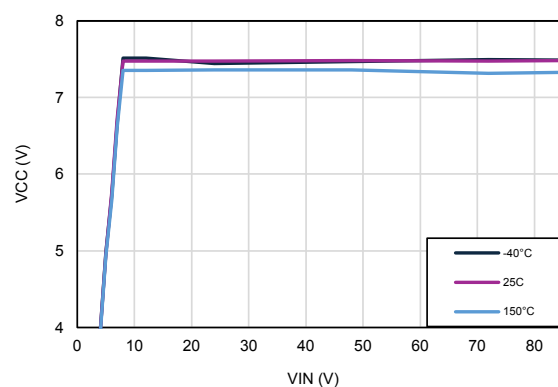
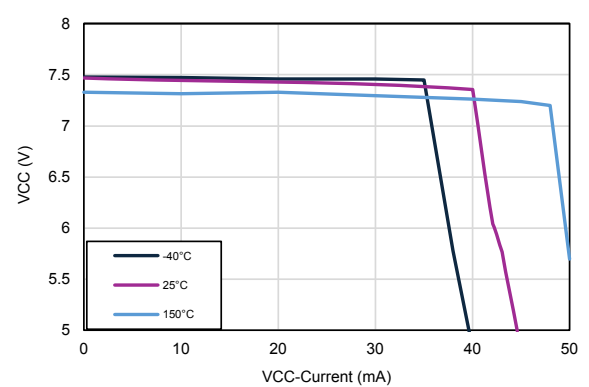
Figure 8. Quiescent current - Enable = 1 V

Figure 9. Operating (Enable = 1.5 V- SS/TRK = GND)

Figure 10. Oscillator frequency (°C)

Figure 11. Oscillator frequency (VIN)

Figure 12. VCC voltage - SS/TRK = GND, EN = 1.5 V

Figure 13. VCC voltage - SS/TRK = GND - VIN = 48 V


Figure 14. VCC voltage - SS/TRK = GND - VIN = 6 V

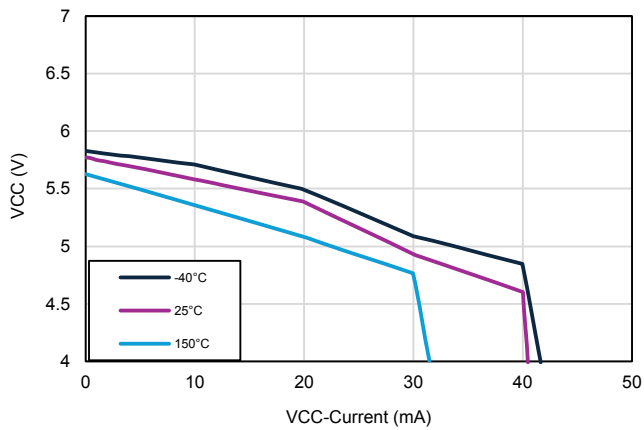


Figure 15. FB reference voltage

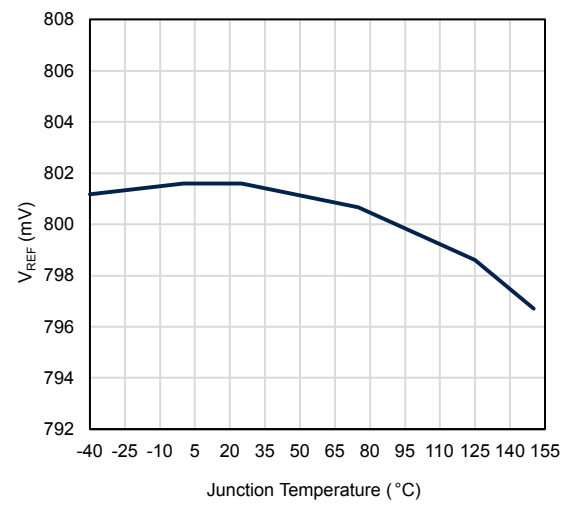


Figure 16. Minimum on-time / Minimum off-time

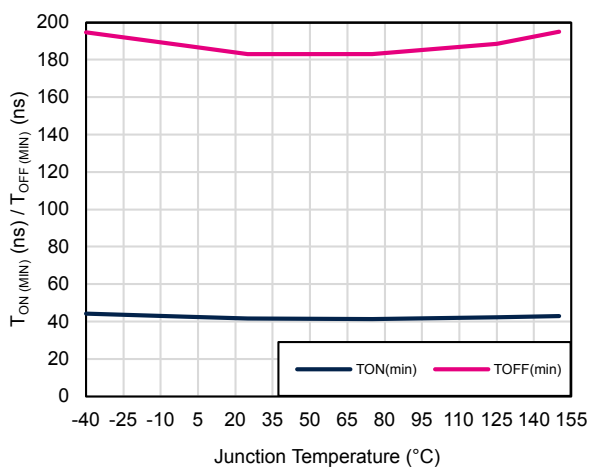


Figure 17. OCP current source

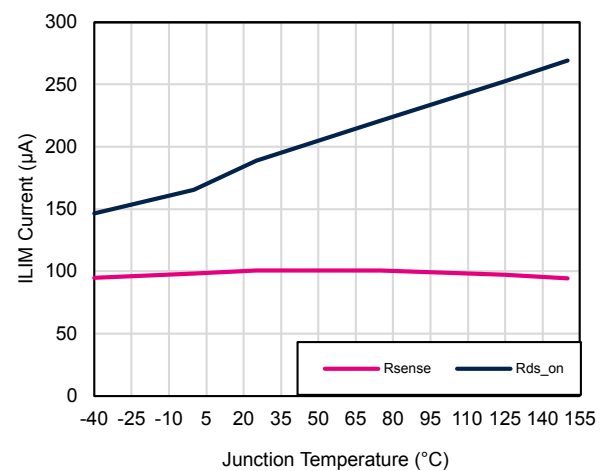


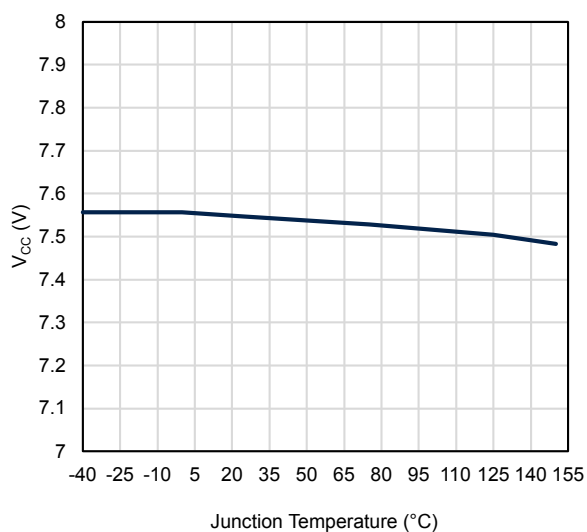
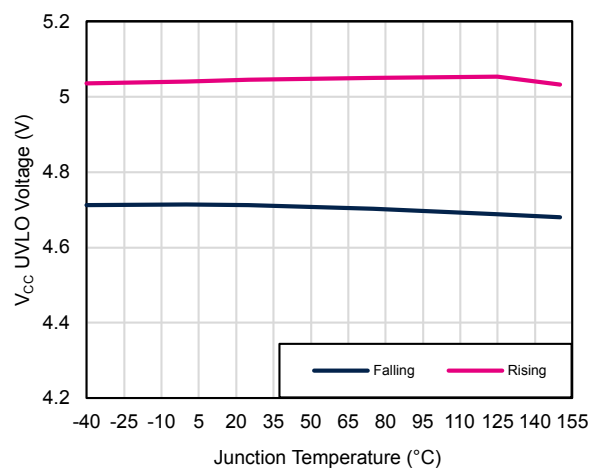
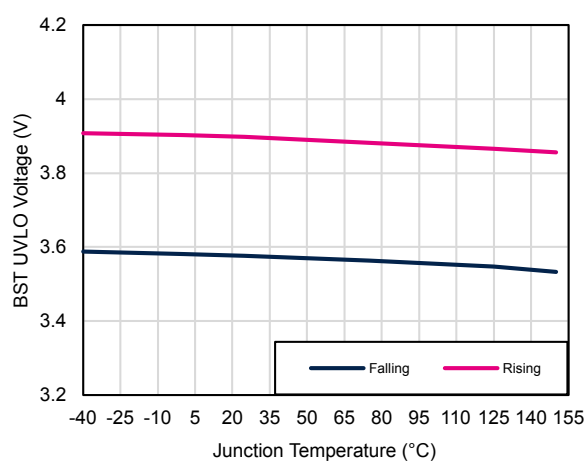
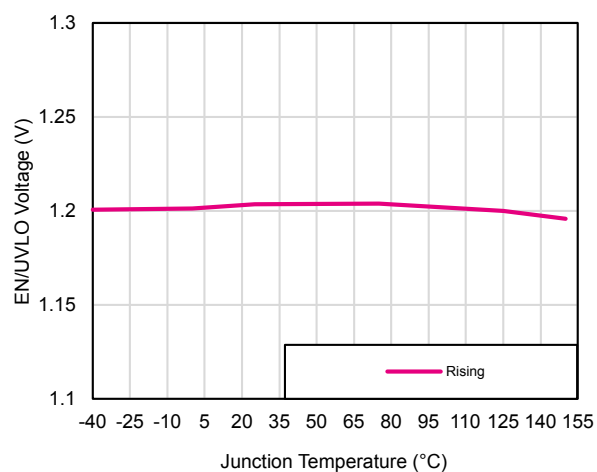
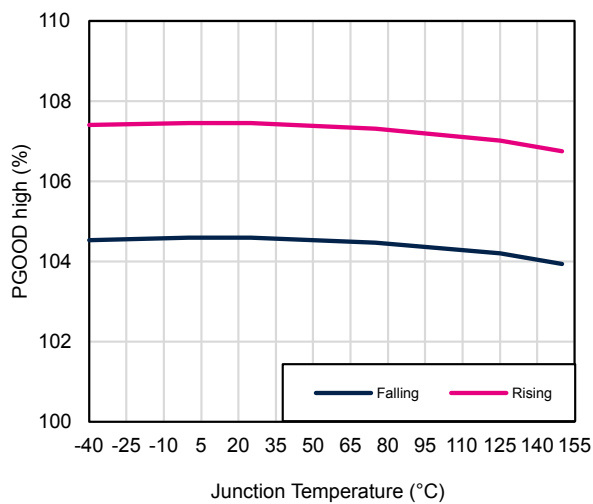
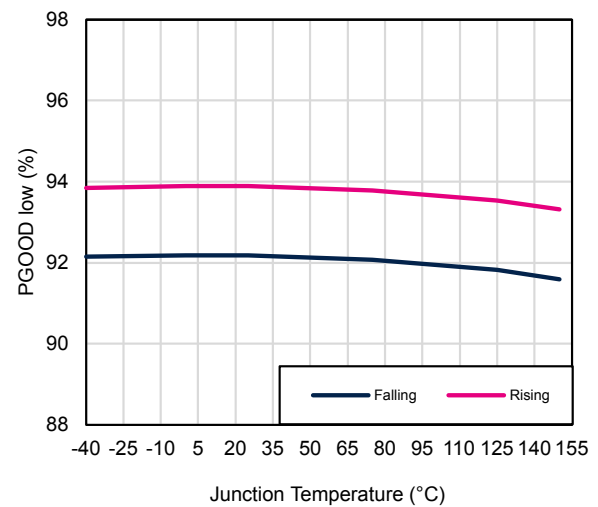
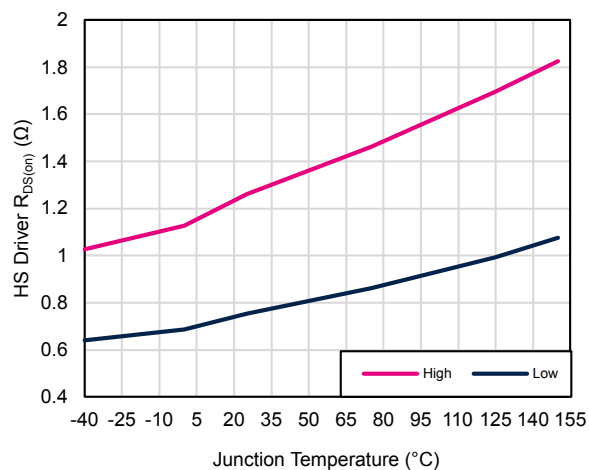
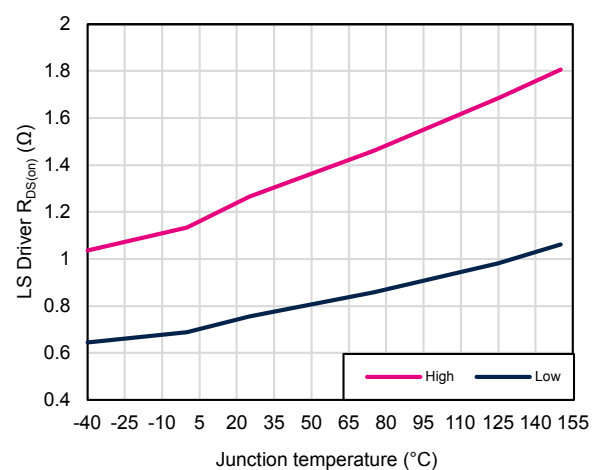
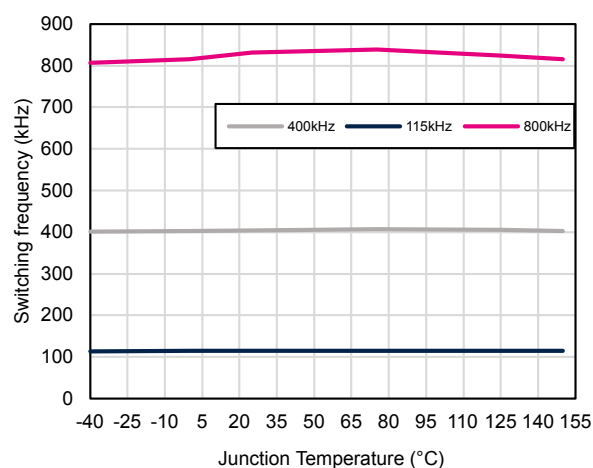
Figure 18. Internal V_{CC} regulator voltage

Figure 19. V_{CC} UVLO thresholds

Figure 20. BST to SW UVLO thresholds

Figure 21. EN/UVLO thresholds


Figure 22. PGOOD upper threshold

Figure 23. PGOOD lower thresholds

Figure 24. High-side gate driver resistance

Figure 25. Low-side gate driver resistance

Figure 26. Oscillator frequency


7 Functional description

The DCP85CY is a buck controller that is based on a constant-frequency, voltage-mode architecture. The output voltage, V_{OUT} , sensed through the feedback pin (FB), is compared with an internal 0.8 V reference, generating an error signal on the COMP pin. The comparison between the COMP voltage level and the internal programmable sawtooth ramp controls the activation time of the external power switches.

The main internal blocks are shown in the block diagram in Figure 1 and can be summarized as follows:

- A voltage regulator that supplies the internal circuitry and provides a fixed internal reference. This block also implements undervoltage lockout (UVLO) circuitry, which monitors the input and internal voltages.
- Embedded external N-channel MOSFET drivers and bootstrap capacitor circuitry to supply the high-side driver.
- Embedded circuitry that generates the sawtooth ramp to modulate the duty cycle based on the internal programmable oscillator or the input synchronization signal. Input voltage feed-forward is implemented to improve line transient response.
- A voltage-mode error amplifier.
- PWM comparators and the associated analog and digital circuitry are required to drive the internal MOSFET drivers.
- Soft-start circuitry to limit inrush current during start-up, and a reference clamp.
- An adjustable sensorless or precise valley current-limit sensing block, together with hiccup circuitry to handle overload and short-circuit conditions.
- Thermal shutdown circuitry to prevent thermal runaway.
- Output voltage monitoring circuitry that releases the PGOOD signal when the sensed output voltage is above 87% of the target value.

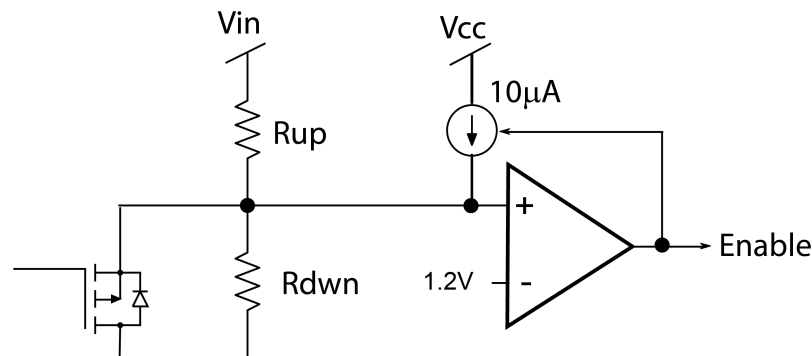
7.1 Precision enable

The EN/UVLO pin multiplexes the inherent functions described below:

- $V_{EN} / UVLO < 0.4$: the device is in shutdown mode.
- $0.4V < V_{EN} / UVLO < 1.2V$: device in standby mode, with the V_{CC} regulator active but device operation inhibited, and the SS / TRK pin in low impedance.
- $V_{EN} / UVLO > 1.2V$: SS / TRK pin released, and the device starts operating. An internal 10 μA current flows to the external resistor divider to set the enable to UVLO hysteresis.

The central tap of a resistor divider connected to the EN/UVLO pin from V_{IN} sets the enable and undervoltage lockout thresholds referred to the input voltage as shown in the figure below:

Figure 27. EN/ UVLO resistor divider



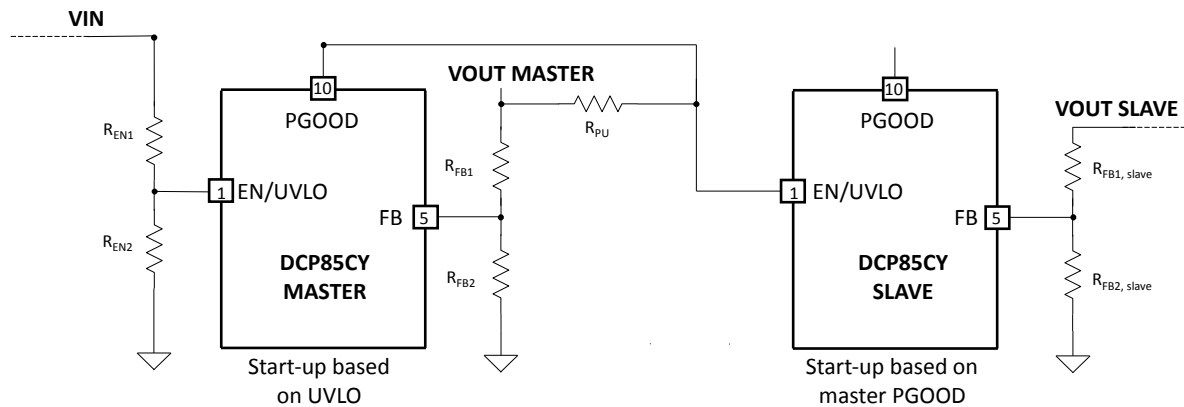
$$R_{UP} = \frac{VIN_{ON} - VIN_{OFF}}{10\mu A} \quad R_{DWN} = R_{UP} \cdot \frac{1.2}{VIN_{ON} - 1.2} \quad (1)$$

Where VIN_{ON} and VIN_{OFF} represent the desired turn-on and turn-off thresholds.

7.2 Power-good indicator

The PGOOD pin behaves as a flag pin and indicates when the output voltage is regulated within an acceptable range. Use this output signal to enable the start-up of subsequent converters, for output monitoring, or for fault protection. Figure 28 shows the typical implementation of a master-slave sequencing with a connection from PGOOD to EN/UVLO. The pin is an open-drain and must be pulled up to a DC voltage that does not exceed 14 V AMR. A resistor divider can be used to adjust the voltage from a higher voltage, as long as the pullup resistance ranges from 10 kΩ to 100 kΩ.

Figure 28. Master slave



The PGOOD signal is driven by an internal switch that depends on the FB voltage, which is directly related to the regulated output voltage. When FB is within the typical window from 92% to 108% of the reference voltage V_{REF} , the switch turns off and the pull-up resistor drives PGOOD high. This state indicates good regulation of the output voltage. If the FB voltage is above or below that interval, the internal switch turns on, pulling PGOOD low, which indicates that V_{OUT} is not regulated.

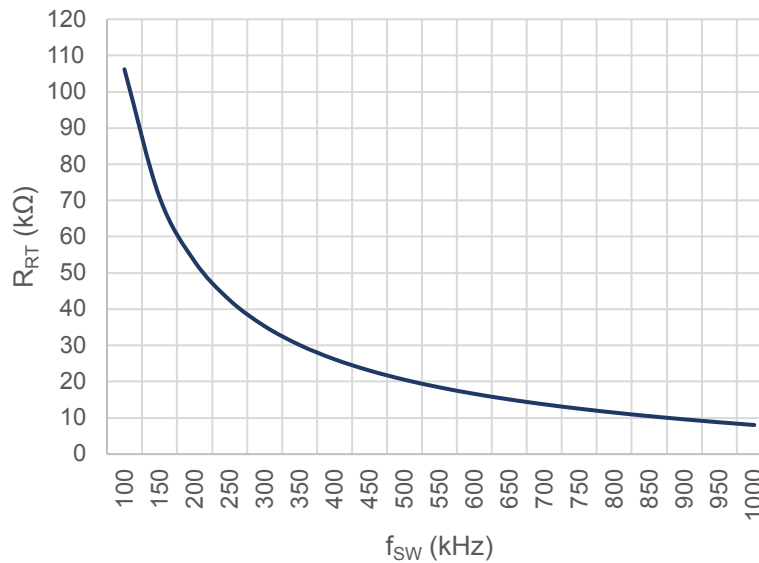
7.3 Oscillator and synchronization

The DCP85CY enables two options to set the switching frequency f_{SW} and gives the designer more flexibility. Connect an external resistor between the R_T pin and ground to set the desired frequency or use the SYNCIN pin to synchronize the device with an external clock signal.

The programmable internal oscillator frequency depends on the external resistor R_{RT} connected between the R_T pin and GND. The resulting switching frequency ranges from 100 kHz to 1 MHz. The resistance is calculated according to the formula given in Equation 1:

$$R_{RT}[k\Omega] = \frac{10500}{f_{SW}[kHz]} + 0.004 \cdot (400 - f_{SW}[kHz]) \quad (2)$$

The relationship between the switching frequency and the R_{RT} resistor is shown in Figure 5, and some commercial resistance values are reported for simplicity.

Figure 29. R_{RT} resistor value for f_{SW} programming


The switching frequency can also be adjusted by synchronizing the device to an external clock signal applied to the SYNCIN pin that satisfies the following requirements:

- Clock frequency range: 120 kHz to 1 MHz.
- Clock frequency: -15% to +50% of the oscillator frequency programmed by RRT.
- Clock maximum amplitude: 13 V.
- Clock minimum pulse: 50 ns.

The device operates in phase with the synchronization signal. After synchronization, if the SYNCIN signal is removed, the device requires a power cycle to guarantee the f_{SW} set by the resistor on the RT pin.

The device generates a synchronization signal available at the SYNCOUT pin that has a 180° phase shift referred to the rising edge of the high-side gate driving signal. Synchronized operation is easily accomplished by connecting the SYNCOUT of the master to the SYNCIN of the slave device to reduce the RMS current of the input filter and increase EMI performance. If more than two devices are synchronized, the phase shift remains fixed and all slaves have a common 180° phase shift relative to the master.

For two DCP85CY devices that operate in synchronization and regulate the same output voltage (i.e.: operating with the same duty cycle), the input filter RMS current is minimized and is calculated as:

$$I_{RMS} = \begin{cases} \frac{I_{OUT}}{2} \cdot \sqrt{2D \cdot (1 - 2D)} & \text{if } D < 0.5 \\ \frac{I_{OUT}}{2} \cdot \sqrt{(2D - 1) \cdot (2 - 2D)} & \text{if } D > 0.5 \end{cases} \quad (3)$$

7.4 Internal sawtooth ramp feed-forward

The DCP85CY features an internal sawtooth-ramp feed-forward that maintains a constant PWM gain across the input voltage and a programmable switching frequency range. This solution also improves the response to input-voltage transients. In fact, to maintain constant modulator gain, an increase in input voltage is accompanied by an increase in ramp voltage amplitude. The constant gain of the PWM controller, evaluated in Equation 4, simplifies the compensation-loop design because it is independent of input-voltage changes.

$$G_{PWM} = \frac{V_{OUT}}{V_{COMP}} = \frac{V_{IN}}{\Delta V_{RAMP}} = \frac{V_{IN}}{V_{IN}/K} = K \quad \text{where } K = 30 \quad (4)$$

Figure 30. Internal sawtooth ramp feed-forward - voltage feed forward

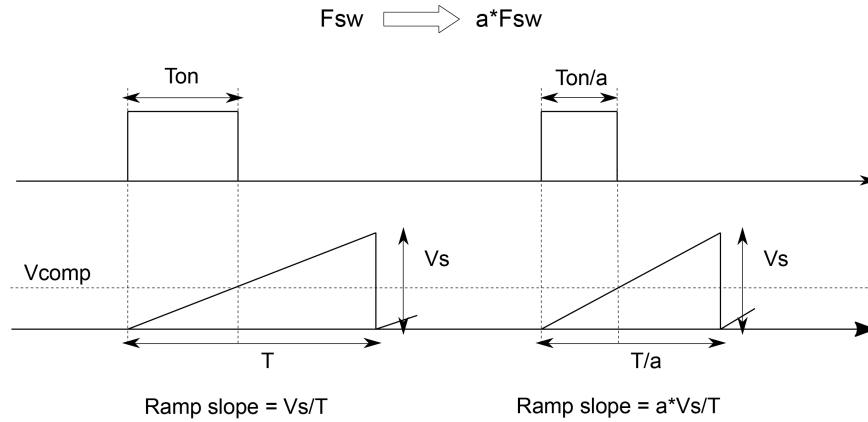
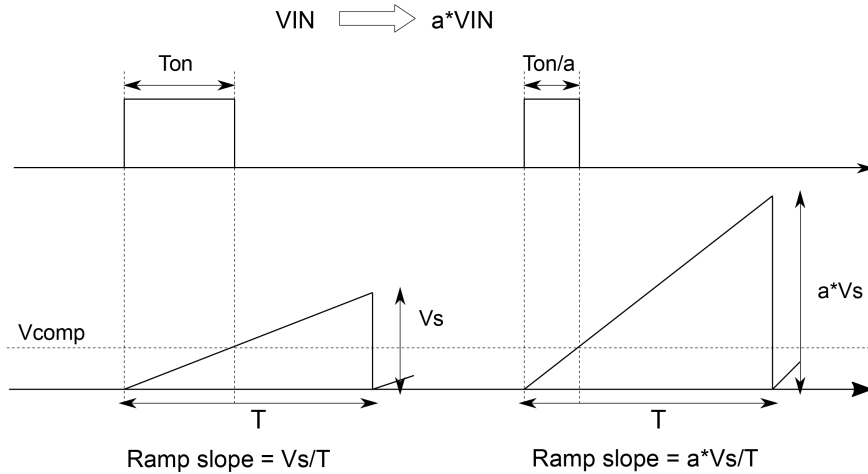


Figure 31. Internal sawtooth ramp feed-forward - f_{sw} adjusted by external resistor



7.5 Soft-start and tracking

The soft-start (SS) feature minimizes the inrush current, prevents an overcurrent condition, reduces stress on the power components during power-up, and makes the DC output voltage increase monotonically to the level that requires the feedback resistor.

When the EN/UVLO pin voltage exceeds the 1.2 V rising threshold, the soft-start phase begins.

Figure 33 shows a typical operating principle. The time required to reach the target output is determined by the external soft-start capacitor C_{SS} . This feature makes the soft-start of the DCP85CY programmable.

An internal 10 μ A current source charges the capacitor to ramp the SS/TRK pin voltage up to the internal reference voltage of 0.8 V. Once it exceeds the threshold, the internal error amplifier drives the non-inverting input and the soft-start ends. The time t_{SS} for ramping the output voltage to the set value is calculated in Equation 5.

$$t_{SS} = \frac{C_{SS} \cdot V_{REF}}{I_{SS}} \quad (5)$$

By inverting this equation and substituting the fixed internal value, the external soft-start capacitor C_{SS} is sized once the user set the soft-start time t_{SS} . For simplicity, Equation 6 shows this relationship, where C_{SS} is in nF and t_{SS} in ms.

$$C_{SS} = 12.5 \cdot t_{SS} \quad (6)$$

Internally, the SS/TRK voltage is clamped dynamically to 115 mV above the FB pin voltage to implement a partial soft-start, depending on the actual FB voltage, to recover from an abrupt load removal in an overcurrent event. Figure 32 shows the internal and external components that are used during the soft-start of the DCP85CY.

Figure 32. Soft-start block diagram

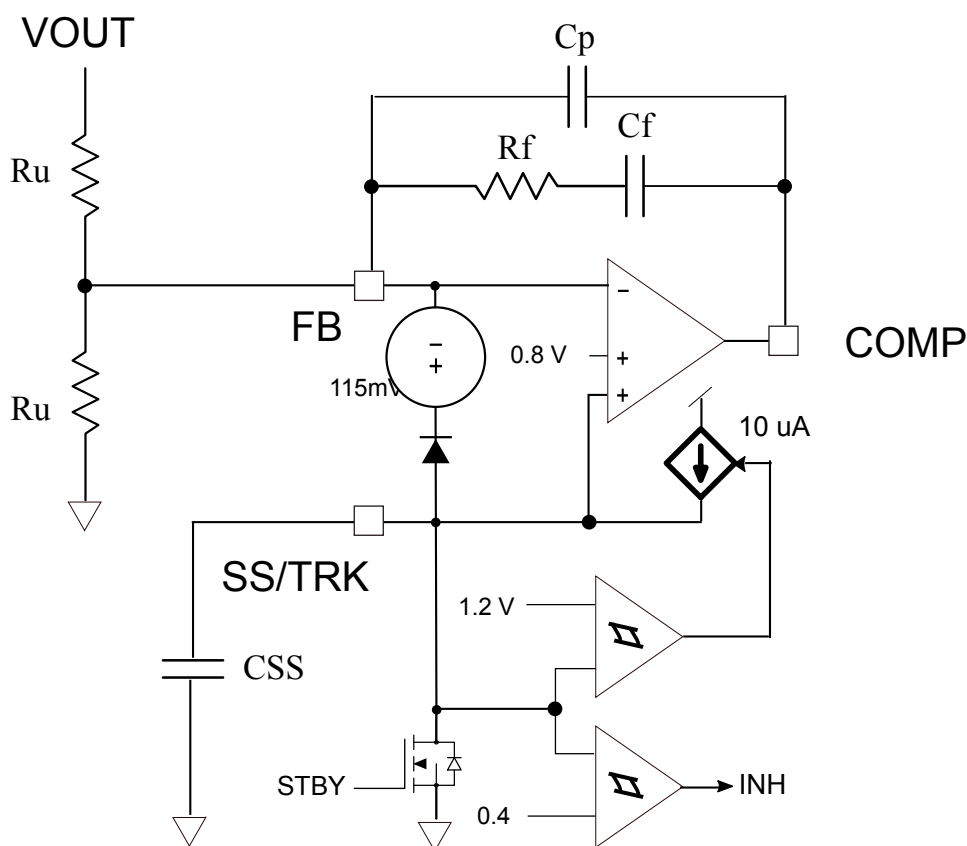
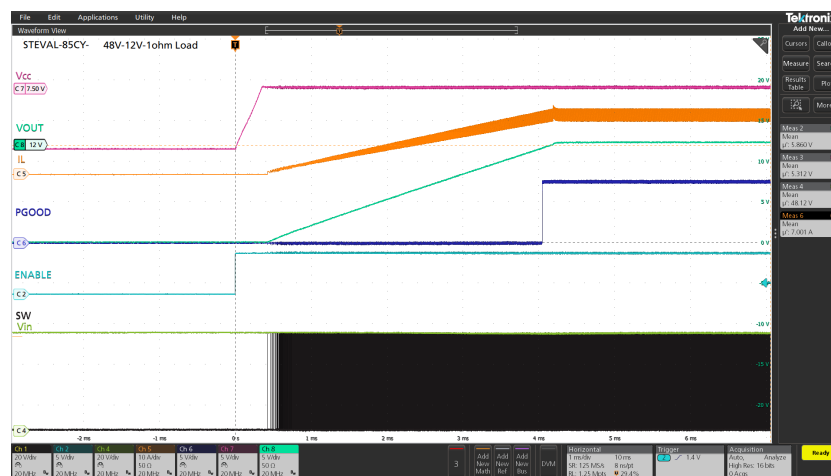


Figure 33. Soft-start phase



7.5.1 Tracking

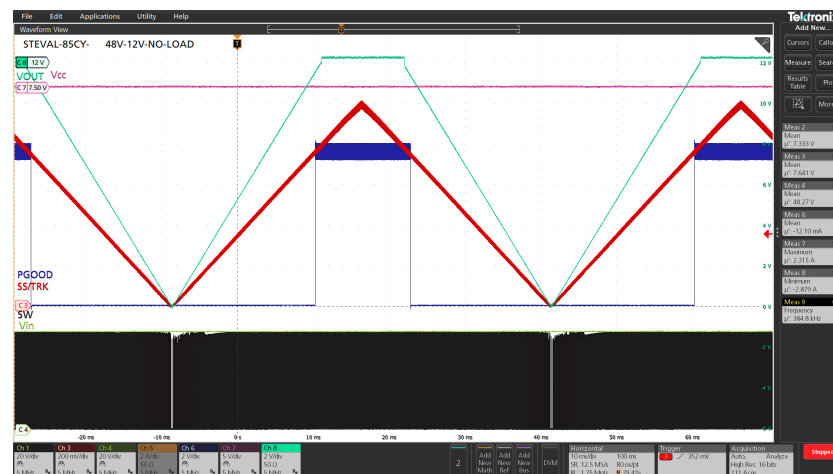
Apply an external voltage to the SS/TRK pin to deactivate the standard soft-start procedure and enable a master-slave power-supply tracking, useful for multiple power rails suitable for digital ICs.

A simple voltage divider from the master output voltage is required to set up this feature. Tracking can be coincident or ratiometric, depending on the resistor value.

As in the normal soft-start procedure, the slave output voltage is regulated when the SS/TRK reaches the internal voltage threshold of 0.8 V. A soft-start capacitor can be used to prevent overcurrent and to control how fast the slave voltage ramps up.

In [Figure 34](#), the output voltage ramps up when SS/TRK is below the reference voltage. Once the signal exceeds the threshold, the slave regulates the output voltage at the target value, 5 V in this example, and the PGOOD signal goes high. If the tracking voltage goes below the reference voltage, the output voltage decreases consistently.

Figure 34. Typical voltage tracking waveforms

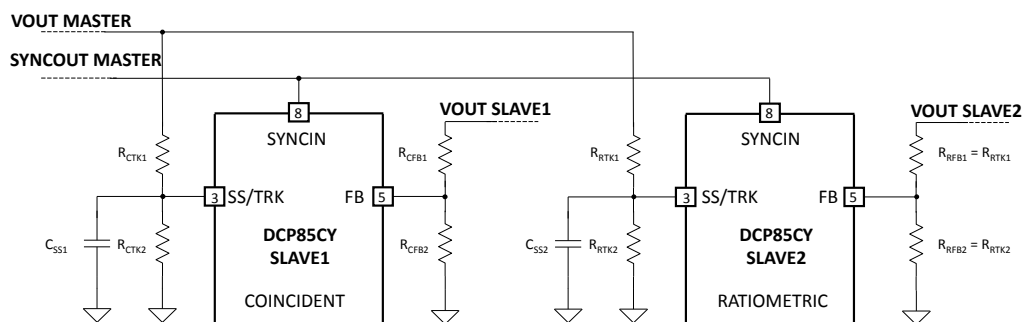


Tracking is normally implemented in coincident or ratiometric configurations, as shown in [Figure 35](#).

With ratiometric tracking, during the start-up, the slave's output voltage is only a fraction of the master's given by the voltage divider. On the other hand, coincident tracking means that the output voltage ramp rates for the master and slave channels are the same up to the slave output's regulated setpoint.

Coincident tracking is obtained connecting a voltage divider from the master's output to SS/TRK pin, identical to the voltage divider used to set the slave's output voltage. Ratiometric tracking gives more freedom to the designer, provided that the input voltage at SS/TRK pin is higher than the internal reference. As a rule of thumb, the SS/TRK must be at least 100 mV higher than the threshold to avoid output voltage inaccuracy.

Figure 35. Schematic to implement input voltage tracking



7.6 Error amplifier

The error amplifier (EA) provides the error signal for comparison with the sawtooth to perform pulse width modulation. Its non-inverting input is internally connected to a 0.8 V voltage reference, while the inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device, the error amplifier is a voltage-mode operational amplifier with high DC gain and low output impedance.

The uncompensated error amplifier characteristics are as follows:

Table 8. Error amplifier characteristics

Characteristic	Value
Non-inverting input voltage reference voltage	800 mV
Low frequency gain (A0)	95 dB
GBWP	6.5 MHz
Output voltage swing	0.3 to 3.3 V
Source / sink current capability	20 / 45 mA

In continuous conduction mode (CCM), the transfer function of the power stage has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different compensation network topologies can be used depending on the ESR value of the output capacitor.

If the zero from the output capacitor helps compensate for the double pole of the LC filter, a type II compensation network can be used. Otherwise, a type III compensation network must be used (see Section 8 for details on the compensation network design).

In any case, the loop compensation method is to introduce zeros to obtain a safe phase margin.

7.7 Embedded gate driver supply

The embedded gate-driver power supply is the output of the internal LDO regulator. Its value is 7.5 V, and it is available on the VCC pin. For proper operation, connect a multi-layer ceramic capacitor (MLCC) with a value between 47 nF and 2.2 µF. For high-current applications, the DCP85CY uses gate drivers with sufficiently low impedance to perform effectively when high output current is required.

The VCC regulator provides the gate voltage for direct low-side and floating high-side driving, through bootstrap capacitor charge refresh. This capacitor is charged from the VCC through an external diode when the low-side MOSFET conducts. This charge powers the high-side gate-driver. Connect a capacitor of 100 nF or more between BST and SW, as close as possible.

Select external MOSFETs so that the total driving current consumption is lower than the VCC regulator output current capability at the programmed switching frequency.

$$I_{DRV} = (Q_{GHS} + Q_{GLS}) \cdot f_{SW} \leq I_{VCC, limit} = 40 \text{ mA (minimum)} \quad (7)$$

The typical regulator dropout voltage is 250 mV @ $V_{IN} = 6 \text{ V}$, $I_{VCC} = 20 \text{ mA}$. Therefore, the VCC voltage drops to input voltage if the input voltage is lower than 7.75 V. Be aware that the VCC drop to low input voltage can increase the “not logic level MOSFET” $R_{DS(on)}$, affect the nominal programmed OCP threshold and increase switching and conduction losses. For an operation at low input voltage, select “logic level MOSFET” with a guaranteed maximum $V_{TH} = 4.5 \text{ V}$.

7.8 Switchover

The internal LDO regulator dissipates power to provide the VCC voltage and it increases the higher the input voltage is. In some applications, the DCP85CY shows a useful function to increase power efficiency by turning off the LDO regulator. In fact, the internal circuitry is not active if a different voltage source drives the VCC pin higher than the regulated LDO. This voltage can be an external power rail, or the regulated output voltage and it has to be connected to VCC through a series diode. Figure 36 and Figure 37 show the two alternatives to implement this feature. During the soft-start of the device, the VCC voltage is provided by the LDO regulator and is set to 7.5 V. Once the output voltage overcomes this value, the internal voltage ramps to the output voltage level. It is mandatory not to exceed the AMR of a VCC pin, then the external voltage must be between 8 V and 13 V. Note that a series resistor can be added before the diode if the external voltage is greater than 13 V, sized considering an I_{VCC} current of 40 mA.

The switchover function enables a generally higher efficiency conversion also at light load. A VCC higher than typical 7.5 V implies better $R_{DS(on)}$ and therefore efficiency gain at high load.

While implementing this function, it is necessary for the external power supply at VCC pin to be provided/removed when V_{IN} is applied to the DCP85CY, to prevent damage and to assure the correct working principle of the device.

Figure 36. VCC power from VOUT

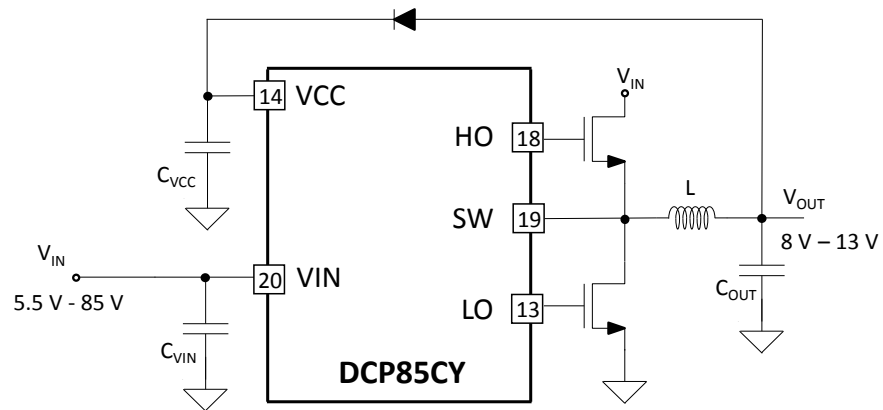
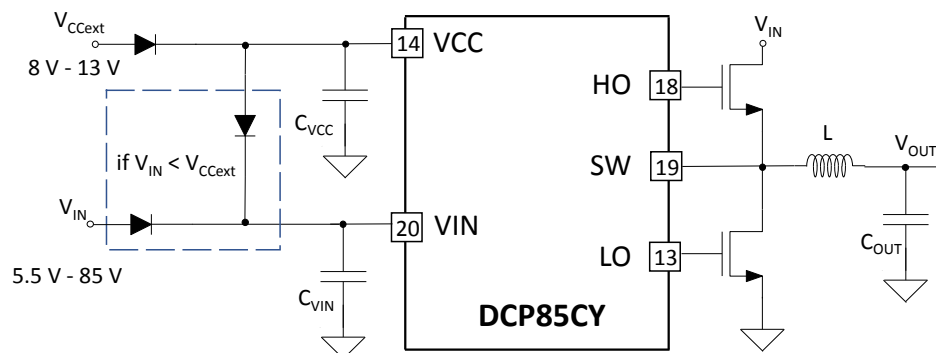
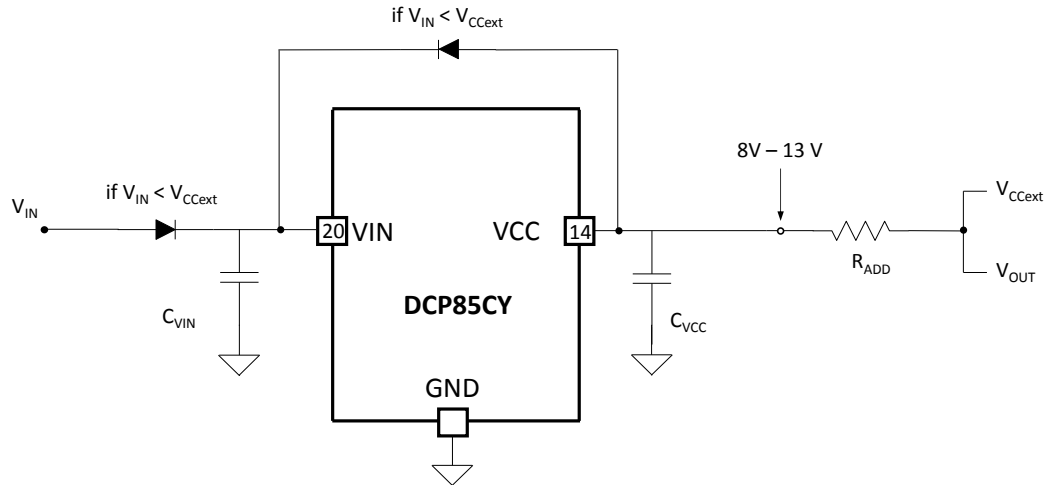


Figure 37. VCC power from external VCC



If the application requires an input voltage V_{IN} lower than the external voltage V_{CCext} , add a series diode from V_{IN} to the VIN pin to prevent reverse current flowing from the VCC to the VIN pin. A Schottky diode between these pins is also recommended to prevent parasitic effects inside the device.

Figure 38. VCC power circuits with a Schottky diode

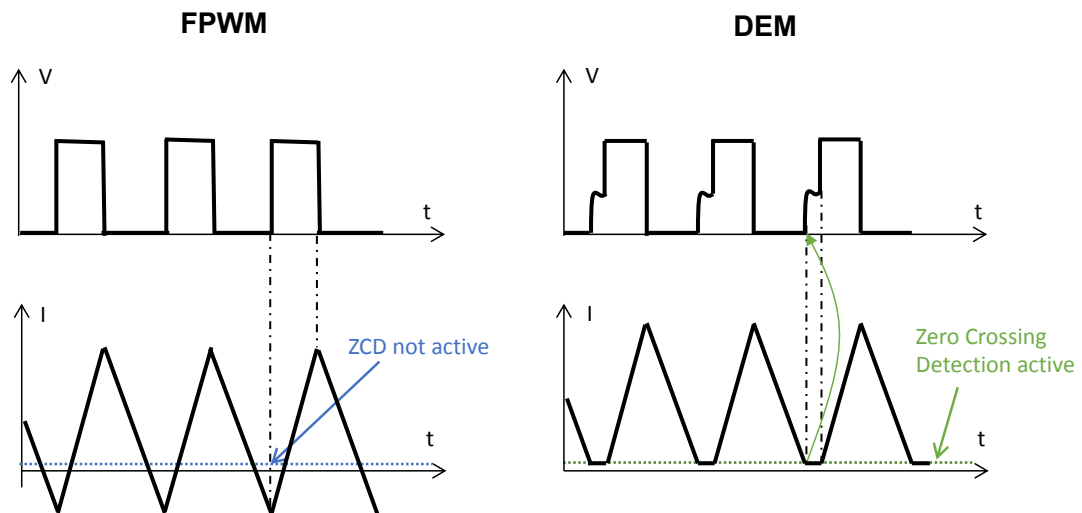


7.9 Light-load operation

The device always implements diode emulation (DEM) during soft-start to support a precharged output capacitor at start-up.

The state of the SYNCIN pin at power-up determines the light-load operation: low logic level selects DEM, high logic level, or detected synchronization clock signal enables the forced PWM mode, so-called "FPWM". In detail, the DEM to FPWM transition is implemented by smoothly ramping the zero current detecting threshold (ZCD) from 0 V to 200 mV over 1000 clock cycles, starting with the first PWM pulse from the loop.

Figure 39. DEM vs. FPWM management in light-load condition



The DEM mode operates in DCM and pulse-skipping at light load. It maximizes the efficiency in these operation conditions and minimizes conversion losses while controlled output voltage ripple.

The forced PWM (FPWM) over the load range makes the switching frequency constant and minimizes the output voltage ripple, suggested for low-noise applications like sensors or analog circuitry supply.

Figure 40. DEM to FPWM smooth transition in 1000 clk at power-up

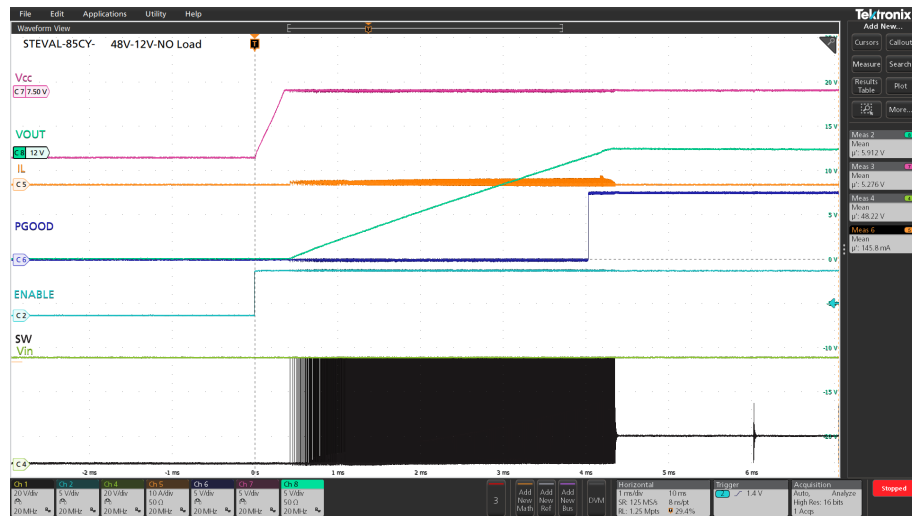


Figure 41. DEM output voltage ripple at zero load

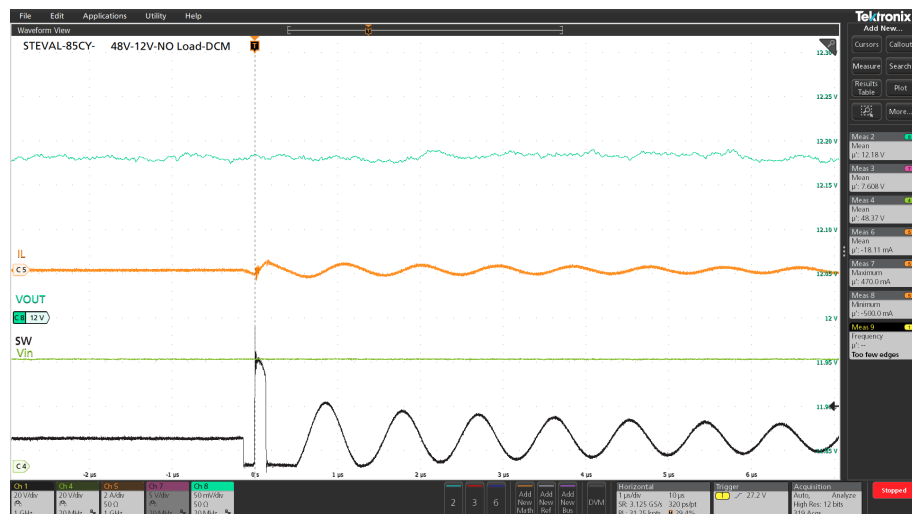
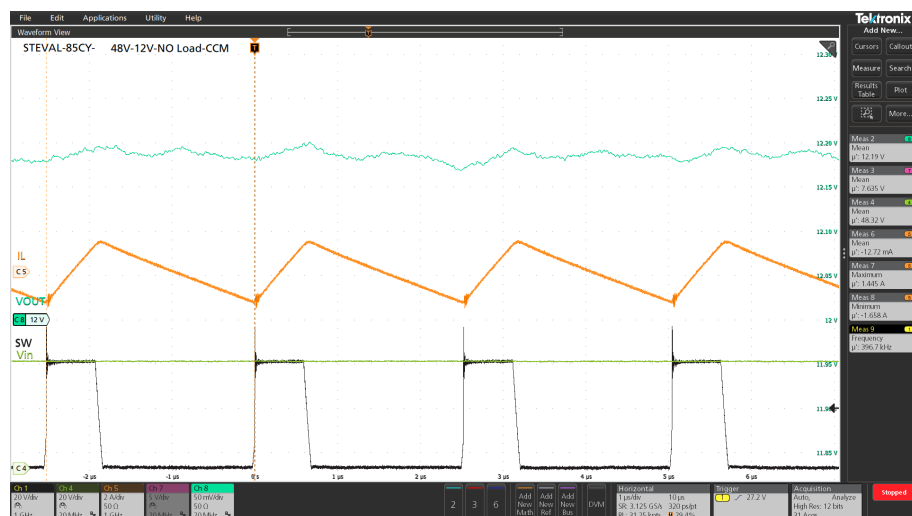


Figure 42. FPWM output voltage ripple at zero load



7.10 Overcurrent protection

The DCP85CY implements improved pulse-by-pulse valley current sensing through a dedicated control logic for an effective current protection over the duty cycle range. The device supports programmable valley current monitoring through two different designs, as shown in Figure 43. Monitoring can be performed across an optional sensing resistor for the best sensing accuracy (OCP precise) or across the on-state $R_{DS(on)}$ of the low-side MOSFET to minimize the conduction losses (OCP lossless).

The valley current threshold is easily programmed with the series resistor R_{ILIM} connected from the $ILIM$ pin to the selected sensing element (see Figure 43). When the LO gate signal is driven high by the PWM controller, an internal generator sources a constant current out of the $ILIM$ pin, causing a voltage V_{ILIM} on the pin, as reported in Equation 8.

$$V_{ILIM}(t) = (R_{ILIM} + R_X) \cdot I_{ILIM} - R_X \cdot I_{VALLEY}(t) \approx R_{ILIM} \cdot I_{ILIM} - R_X \cdot I_{VALLEY}(t) \quad (8)$$

Where R_X can be the low-side $R_{DS(on)}$ or the shunt resistor R_{SENSE} . An internal comparator monitors the pin voltage and keeps the LO signal high until it drops to $V_{ILIM\ TH}$ threshold ($\approx -2\ mV$). The current source amplitude I_{ILIM} is set by the device at the start-up and both levels are compensated with the 4500 ppm/°C thermal coefficient. Equation 9 reports the differences.

$$I_{ILIM} = \begin{cases} 200\ \mu A & , \quad @ \ T_J = 300K, \text{ if } OCP \text{ lossless.} \\ 100\ \mu A & , \quad @ \ T_J = 300K, \text{ if } OCP \text{ precise.} \end{cases} \quad (9)$$

Both levels compensated with the 4500 ppm/°C thermal coefficient.

As a consequence, assuming $V_{ILIM} \approx 0$, the R_{ILIM} value can be calculated as:

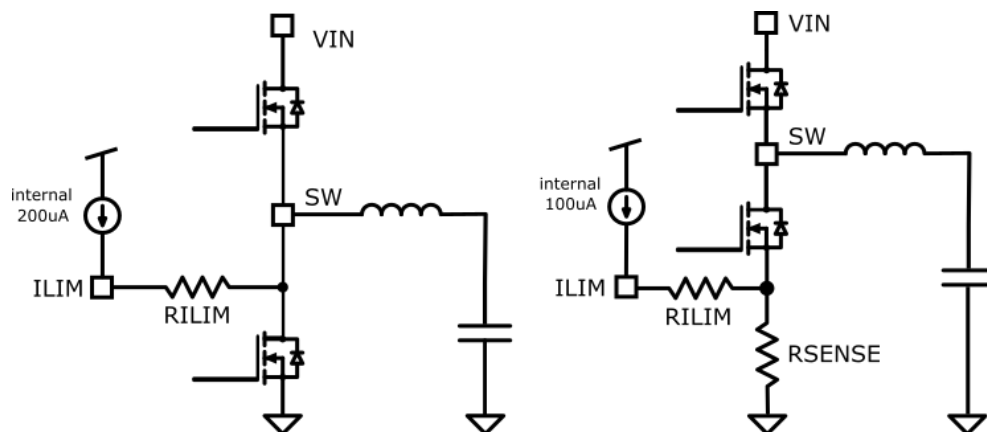
$$R_{ILIM} = \frac{R_X \cdot I_{VALLEY,MAX}}{I_{ILIM}} = \frac{R_X}{I_{ILIM}} \left(I_{OUT,MAX} - \frac{\Delta I_L}{2} \right) \quad (10)$$

Where the sensed inductor current $I_{VALLEY,MAX}$ can be expressed in terms of DC output current $I_{OUT,MAX}$, and the inductor current ripple ΔI_L for simplicity.

In case of OCP lossless current sensing, the $ILIM$ pin is subjected to a large voltage swing and therefore a capacitor from $ILIM$ to PGND must be designed to allow proper circuitry operation. Choose C_{ILIM} so that the time constant with R_{ILIM} is $\sim 5\ ns$.

Overcurrent protection (OCP), current sensing is often used at lower output current levels to avoid reducing power-conversion efficiency. For-high current applications, this method is generally not recommended unless overcurrent protection setpoint stability and precision are essential requirements.

Figure 43. R_{ILIM} resistor connection to define lossless and precise OCP setting



The current protection circuitry features constant current protection to handle an exceptional dynamic load request that can persist for a maximum 128 clock cycles. During this time window, the device limits the DC output current accordingly with valley current threshold programmed value with the RILIM resistor, as shown in Figure 44.

If the overcurrent event lasts longer, the hiccup protection is triggered to limit the stress of the external power components during a continuous short-circuit event. Switching activity is prevented for 8192 clock cycles and the SS capacitor is discharged for a new soft-start cycle, as shown in Figure 45.

Figure 44. Constant current in a persistent short-circuit

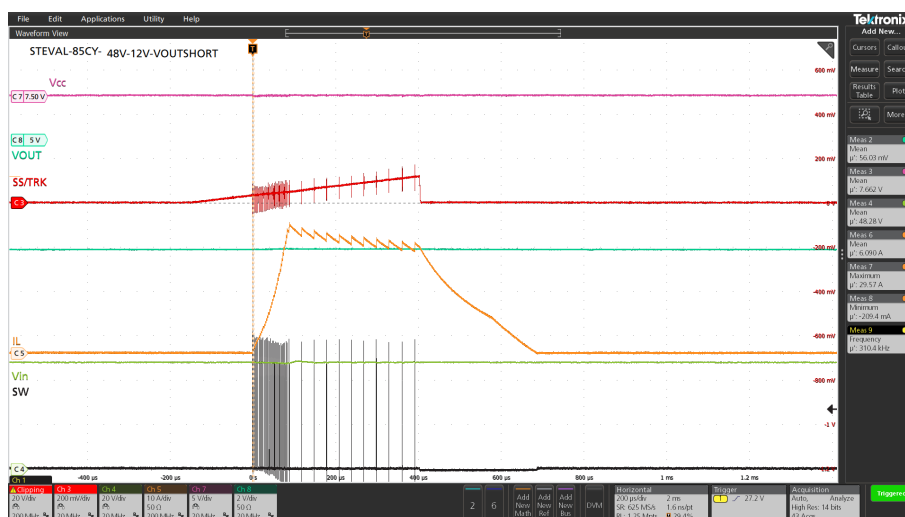
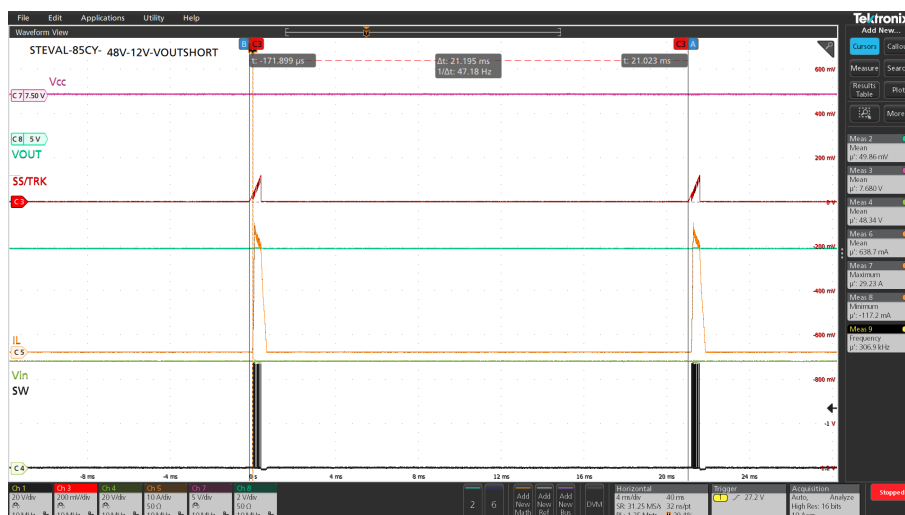


Figure 45. Hiccup in a persistent short-circuit

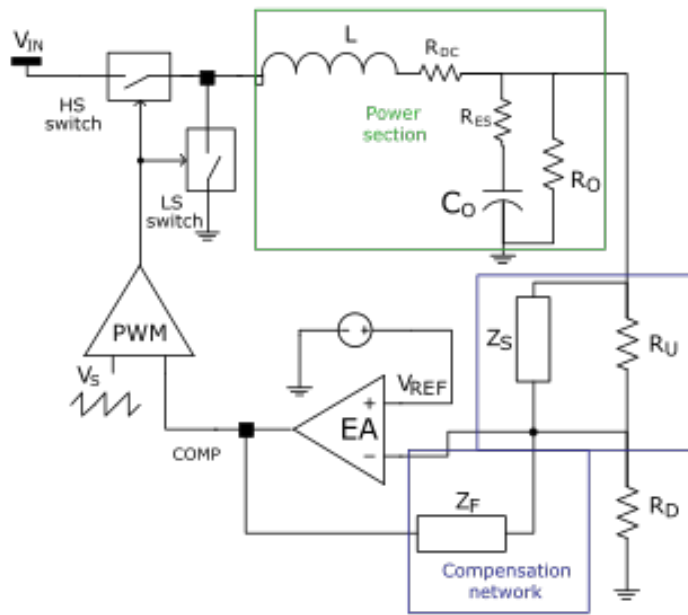


8 Closing the loop

8.1 Total transfer function

The compensation network ensures stability and good dynamic performance over the application conditions. The DCP85CY loop uses voltage mode control. The embedded wide-bandwidth operational amplifier can be considered ideal for compensator calculations because its frequency response is much higher than the designed system bandwidth.

Figure 46. Voltage mode control loop



The transfer function of the PWM modulator from the error amplifier output (COMP pin) to the LX pin has an almost constant gain because voltage feed-forward generates a sawtooth with an amplitude V_S directly proportional to the input voltage.

$$G_{PWM0} = \frac{V_{IN}}{V_S} = K_{FF} = 30 \quad (11)$$

The transfer function of the power section (that is, the L-C filters and the output load) is:

$$G_{LC}(s) = \frac{R_O \parallel (R_{ES} + \frac{1}{s \cdot C_O})}{R_O \parallel (R_{ES} + \frac{1}{s \cdot C_O}) + s \cdot L + R_{DC}} \quad (12)$$

given L , R_{DC} , C_O , R_{ES} and R_O as defined in Figure 36 and Figure 37.

For convenience, the GLC can be written as:

$$G_{LC}(s) = G_{LC0} \cdot \frac{1 + \frac{s}{2 \cdot f_{ZESR}}}{1 + \frac{s}{2 \cdot Q \cdot f_{LC}} + \left(\frac{s}{2 \cdot f_{LC}}\right)^2} \text{ where } G_{LC0} = \frac{R_O}{R_O + R_{DC}} \approx 1 \quad (13)$$

$$f_{ZESR} = \frac{1}{2\pi \cdot C_O \cdot R_{ES}} \quad f_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_O} \cdot \sqrt{\frac{R_O + R_{ES}}{R_O + R_{DC}}}} \approx \frac{1}{2\pi \cdot \sqrt{L \cdot C_O}} \quad (14)$$

$$Q = \frac{\sqrt{L \cdot C_O} \cdot \sqrt{R_O + R_{DC}} \sqrt{R_O + R_{ES}}}{L + C_O \cdot (R_O \cdot R_{DC} + R_O \cdot R_{ES} + R_{ES} \cdot R_{DC})} \approx \frac{\sqrt{L \cdot C_O} \cdot R_O}{L} = \sqrt{\frac{C_O}{L}} \cdot R_O \quad (15)$$

Assuming the inductor and output capacitor parasitic resistance, R_{DC} and R_{ES} , negligible compared to R_O .
The total closed loop gain is:

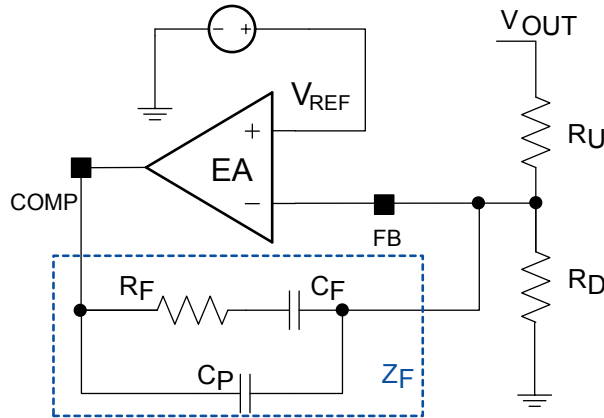
$$G_{LOOP}(s) = G_{PWM0} \cdot G_{LC}(s) \cdot G_{COMP}(s) \quad (16)$$

The implemented compensation networks represented with $G_{COMP}(s)$ terms depend on the characteristics of the selected output capacitor as explained in the following chapters.

8.2 Type II compensation network

If the equivalent series resistance (ESR) of the output capacitor introduces a zero at a frequency within the desired bandwidth (that is: $2\pi \cdot R_{ES} \cdot C_O > 1 / BW$), this zero help to stabilize the loop. Electrolytic capacitors show non-negligible ESR ($> 30 \text{ m}\Omega$ typically), so with this type of output capacitor, the type II network combined with the ESR zero stabilize the loop.

Figure 47. Type II compensation network



The type II compensation network transfer function, from V_{OUT} to COMP, is computed in the equation below:

$$G_{COMP II}(s) = -\frac{Z_F(s)}{R_U} = -1 \cdot \frac{1 + \frac{s}{2 \cdot f_{Z1}}}{\frac{s}{2 \cdot f_{P0}} \cdot \left(1 + \frac{s}{2 \cdot f_{P1HF}}\right)} \quad (17)$$

$$f_{Z1} = \frac{1}{2 \cdot R_F \cdot C_F} \quad f_{P0} = \frac{1}{2 \cdot (C_F + C_P) \cdot R_U} \quad f_{P1HF} = \frac{1}{2 \cdot R_F \cdot C_F \parallel C_P} \quad (18)$$

The following suggestions can be followed for quite a common compensation strategy, assuming that $C_P \ll C_F$. $G_{LOOP}(s)$ in case of a type II compensation network and electrolytic output capacitors can be written as follows at $s = 2\pi \cdot f_{BW}$ to derive the R_F / R_U ratio as fixed:

$$G_{LOOP II}(s = 2 \cdot f_{BW}) \cong K_{FF} \cdot \frac{f_{LC}^2}{f_{ZESR}} \cdot \frac{R_F}{R_U} \cdot \frac{1}{f_{BW}} = 1 \quad (19)$$

After choosing the regulator bandwidth (typically $f_{BW} < 0.2 \cdot f_{SW}$) and a value for R_U , usually between $10 \text{ k}\Omega$ and $100 \text{ k}\Omega$ in order to achieve C_F and C_P values not comparable to parasitic capacitance of the board, the required R_F value is calculated as follows from the previous equation:

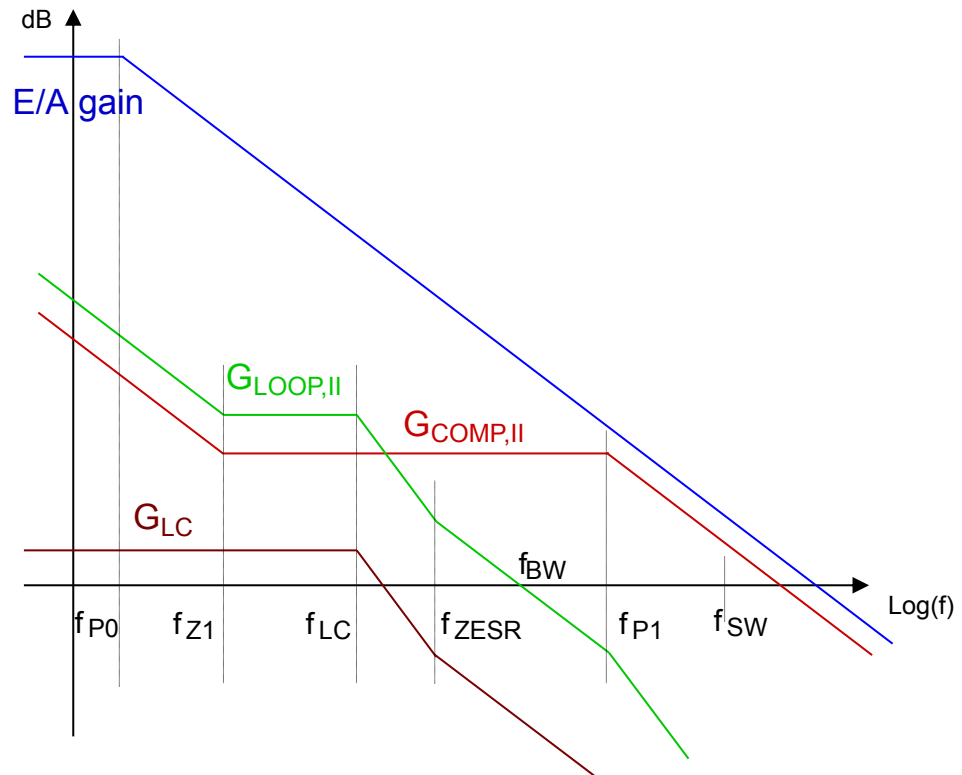
$$R_F = \frac{f_{ZESR} \cdot f_{BW}}{K_{FF} \cdot f_{LC}^2} \cdot R_U \quad (20)$$

Select C_F in order to place f_{Z1} below f_{LC} (typically $0.1 \cdot f_{LC}$) and C_P to place f_{P1HF} at $0.5 \cdot f_{SW}$

$$C_F = \frac{1}{2 \cdot R_F \cdot 0.1 \cdot f_{LC}} \quad C_P = \frac{1}{2 \cdot R_F \cdot 0.5 \cdot f_{SW}} \quad (21)$$

The resulting control loop and other transfer function gains are shown in the figure below.

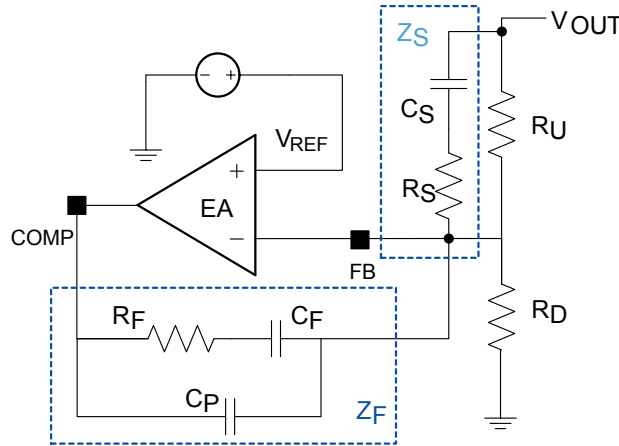
Figure 48. Type II compensation - Bode plot



8.3 Type III compensation network

If f_{ZESR} is higher than the target loop bandwidth, as is usually the case if the output filter is based on MLCC ceramic capacitors, a type III compensation network is recommended, in order to increase the bandwidth and system performance.

Figure 49. Type III compensation network



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The type III compensation network transfer function, from V_{OUT} to COMP, is computed in the equation below:

$$G_{COMPIII}(s) = -\frac{Z_F(s)}{R_U \parallel Z_F(s)} = -1 \cdot \frac{\left(1 + \frac{s}{2 \cdot f_{Z1}}\right) \cdot \left(1 + \frac{s}{2 \cdot f_{Z2}}\right)}{\frac{s}{2 \cdot f_{P0}} \cdot \left(1 + \frac{s}{2 \cdot f_{P1HF}}\right) \cdot \left(1 + \frac{s}{2 \cdot f_{P2HF}}\right)} \quad (22)$$

In addition to the singularities of $G_{COMPII}(s)$ shown in the previous chapter, one more zero and HF pole are present:

$$f_{Z2} = \frac{1}{2\pi \cdot (R_U + R_S) \cdot C_S} \quad f_{P2HF} = \frac{1}{2\pi \cdot R_S \cdot C_S} \quad (23)$$

The following suggestions can be followed for quite a common compensation strategy, assuming that $C_P \ll C_F$ and $R_S \ll R_U$.

In the case of a type III compensation network and electrolytic output capacitors, $G_{LOOP}(s)$ can be written as follows at $s = 2\pi \cdot f_{BW}$ to derive the R_F / R_U ratio as fixed:

$$G_{LOOPIII}(s = 2 \cdot f_{BW}) \cong K_{FF} \cdot \frac{f_{LC}}{f_{BW}} \cdot \frac{R_F}{R_U} = 1 \quad (24)$$

After choosing the regulator bandwidth (typically $f_{BW} < 0.2 \cdot f_{SW}$) and a value for R_U , usually between 10 kΩ and 100 kΩ to ensure that C_F and C_P are sufficiently larger than the board parasitic capacitances, the required value of R_F can be calculated from the previous equation as follows:

$$R_F = \frac{f_{BW}}{K_{FF} \cdot f_{LC}} \cdot R_U \quad (25)$$

Select C_F in order to place f_{Z1} below f_{LC} (typically $0.8 \cdot f_{LC}$) and C_P to place f_{P1HF} at $0.5 \cdot f_{SW}$.

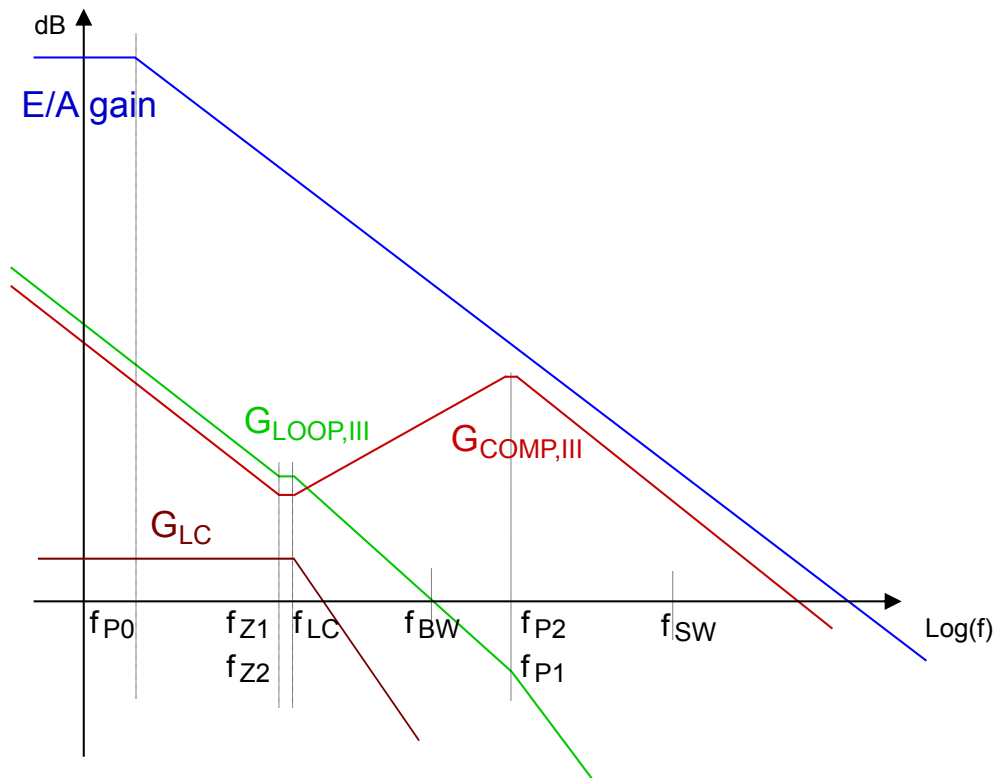
$$C_F = \frac{1}{2 \cdot R_F \cdot 0.1 \cdot f_{LC}} \quad C_P = \frac{1}{2 \cdot R_F \cdot 0.5 \cdot f_{SW}} \quad (26)$$

Select C_S in order to place f_{Z2} at $0.8 \cdot f_{LC}$ and R_S to place F_{P2HF} at $0.5 \cdot f_{SW}$.

$$C_S = \frac{1}{2 \cdot R_U \cdot f_{LC}} \quad R_S = \frac{1}{2 \cdot C_S \cdot 0.5 \cdot f_{SW}} \quad (27)$$

The resulting control loop and other transfer function gains are shown in the figure below.

Figure 50. Type III compensation - Bode plot



9 Application notes

The DCP85CY is a synchronous buck controller that is suitable for a wide range of applications because of the flexibility provided by the external components. Therefore, the power elements (inductor, input and output capacitors, power MOSFETs) and the output voltage divider must be chosen to meet the target specifications of a given application.

Achieving high efficiency at high current loads requires a MOSFET with a low $R_{DS(on)}$. The output current and switching frequency are strongly related to the inductor value. The output voltage and its ripple influence the sizing of the output capacitor and the voltage divider. A wide range of V_{IN} or high-voltage conversion ratio are of interest in the selection of the input capacitor.

To speed up the design process of the external components for a given application, use eDesignSuite, the online proprietary tool available on the STMicroelectronics website, which is a useful tool to customize any application. In the following sections, some equations used for sizing the external components are discussed to provide a better understanding of the device and its application.

9.1 Inductor selection

Typically, the inductor ripple current ΔI_L is selected between 20% and 40% of the desired output load current at the nominal input voltage. The inductor current ripple flowing into the output capacitor contributes to determining the output voltage ripple. Based on the inductor current ripple equation, the required inductance value can be calculated as shown in Equation 28.

$$L_F = \frac{V_{IN} - V_{OUT}}{\Delta I_L \cdot F_{SW}} \cdot \frac{V_{OUT}}{V_{IN}} \quad (28)$$

When selecting the inductor, it is important to verify in the corresponding datasheet that its saturation current rating is higher than the peak inductor current expected in the target application. To minimize power losses, especially in high-current applications, the inductor DC resistance (DCR) must also be taken into account. In general, a lower DCR reduces conduction losses and minimizes its impact on system stability.

Once the inductor has been selected, the peak current flowing through it can be calculated using Equation 29. Note that, for a given operating condition, decreasing the inductance value increases the inductor current ripple and, consequently, the peak current. Conversely, a higher inductance value reduces the current ripple and allows a higher average output current to be delivered before reaching the current-limit threshold.

$$I_{L,peak} = \frac{\Delta I_{L,real}}{2} \quad (29)$$

9.2 Output capacitor selection

The output capacitor must be selected by considering two main aspects. First, it must filter the inductor ripple current to ensure that the output voltage ripple meets the application requirements. Second, it must provide sufficient charge to maintain the output voltage within the specified limits during load transients. The output voltage ripple, ΔV_{OUT} , can be calculated using Equation 30.

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \cdot C_{OUT} \cdot F_{SW}} + ESR \cdot \Delta I_L \quad (30)$$

Where ESR is the equivalent series resistance of the output capacitor. Ceramic capacitors (MLCC) are typically preferred to minimize the output voltage ripple due to their very low ESR. Electrolytic capacitors, on the other hand, can provide higher capacitance values at a relatively low cost and within a compact PCB area, making them suitable for supporting the output voltage during load transients. Assuming to select MLCC capacitors, the resistive contribution given by ESR is negligible and the minimum output capacitor is given by Equation 31. To further reduce the total parasitic resistance, it is possible to design output capacitors in parallel, which will of course increase the final cost.

$$C_{OUT, ripple} > \frac{\Delta I_{L,max}}{8 \cdot \Delta V_{OUT} \cdot f_{SW}} \quad (31)$$

When a load transient ΔI_{OUT} occurs, the output capacitor must provide or absorb the transient current to limit the resulting output voltage deviation until the control loop responds and restores the regulated output voltage. The recovery time is mainly determined by the control-loop bandwidth (BW) and the overall system stability. To meet the required transient-response specifications, C_{OUT} must also satisfy the condition provided in Equation 32.

$$C_{OUT, dynamic} > \frac{\Delta I_{OUT}}{8 \cdot V_{undershoot} \cdot BW} \quad (32)$$

9.3 Input capacitor selection

As a general rule, the input capacitor voltage rate must be higher than the maximum input voltage expected in the application. High-voltage ripple may seriously affect electronics components and increase conducted and radiated EMI. Input capacitors are needed to prevent undesired events and to stabilize the voltage in case of a line transient event. To minimize parasitic effects, input capacitors are typically placed as close as possible to the high side drain MOSFET and to the V_{IN} pin of the device. The peak to peak across the input capacitor is given in Equation 33.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D(1-D)}{C_{IN} \cdot f_{SW}} + I_{OUT} \cdot ESR \quad (33)$$

Combine dielectric capacitors with multilayer ceramic capacitors to get low impedance over a wide temperature range and good line transient response, being cost-effective in the application. In general, a bulk capacitor with an adequate ripple-current rating, combined with ceramic capacitors for high-frequency decoupling, is sufficient. When multiple low-ESR ceramic capacitors are connected in parallel, their equivalent ESR contribution can generally be considered negligible. Under this assumption, the required input capacitance C_{IN} can be calculated as shown in Equation 34.

$$C_{IN} > \frac{I_{OUT} \cdot D(1-D)}{\Delta V_{IN} \cdot f_{SW}} \quad (34)$$

Power MOSFETs

In a DC-DC converter, the selection of the external power MOSFETs has a significant impact on the overall converter performance and efficiency. For high-current applications, MOSFETs with low $R_{DS(on)}$ should be selected to minimize conduction losses. In high-switching-frequency applications, MOSFETs with low parasitic capacitances and low gate charge should be preferred to reduce switching and gate-drive losses.

In commercially available power MOSFETs $R_{DS(on)}$ and gate charge generally involve a trade-off: devices with lower $R_{DS(on)}$ often exhibit higher gate charge, and vice versa. Therefore, the MOSFET selection should be optimized according to the operating conditions and performance requirements of the target application.

For the high-side MOSFET, the main contributions to power dissipation are conduction losses during the duty-cycle interval (D), switching losses during the turn-on and turn-off transitions, and gate-drive losses. Therefore, an appropriate trade-off between $R_{DS(on)}$ and gate charge is required to achieve the target efficiency and performance. As a first-order approximation, the losses associated with the MOSFET output capacitance and body-diode reverse recovery can be neglected.

For the low-side MOSFET, the main contributions to power dissipation are conduction losses while carrying the inductor current during the 1-D interval, gate-drive losses, and body-diode conduction losses during the dead times. Switching losses are generally lower than those of the high-side MOSFET, since the switching-node voltage can approach zero before the low-side MOSFET turns on, depending on the operating conditions and dead-time interval.

In high step-down-ratio applications, the low-side MOSFET conducts the output current for most of the switching period. Therefore, selecting a MOSFET with low $R_{DS(on)}$ is particularly important to minimize conduction losses and improve overall converter efficiency.

Table 9. Main MOSFETs contribution to power losses

Power losses contributes	Formula	High-side	Low-Side
Conduction	$P_{cond} = D \cdot \left(I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)}$	x	x
Switching	$P_{sw} = \frac{1}{2} \cdot V_{IN} \cdot f_{sw} \cdot I_{OUT} \cdot (t_{rise} + t_{falling})$	x	-
Gate driving	$P_{gate} = V_{CC} \cdot f_{sw} \cdot Q_G$	x	x
Body diode	$P_{bd} = V \cdot f_{sw} \cdot I_{OUT} \cdot (t_{dead1} + t_{dead2})$	-	x

Additional parameters must be considered when selecting the external power MOSFETs. The drain-to-source voltage rating V_{DS} must be higher than the maximum input voltage expected in the application, with sufficient margin to account for switching-node voltage overshoots and transients. For applications operating up to the maximum supported input voltage, MOSFETs with a voltage rating of at least 85 V are recommended to ensure adequate design margin.

In addition, considering $V_{CC} = 7.5$ V under standard operating conditions, the relevant MOSFET parameters, particularly $R_{DS(on)}$ should be evaluated at a gate-to-source voltage V_{GS} close to the actual gate-drive voltage.

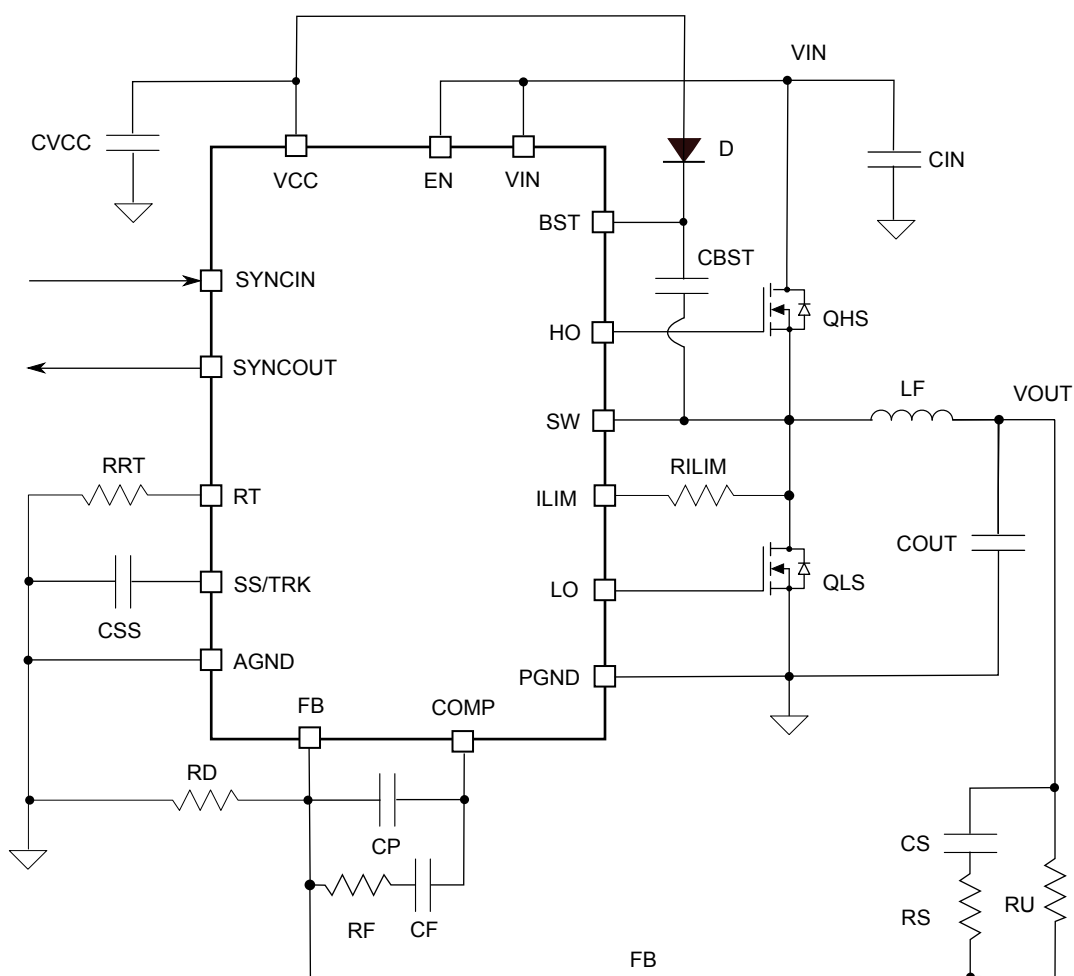
The gate-charge characteristics must also be considered. In particular, the Miller plateau voltage, as shown in the Q_G versus V_{GS} characteristic, should be compatible with the available gate-drive voltage. A Miller plateau in the 2 V to 5 V range ensures sufficient gate-drive margin for proper MOSFET turn-on with a 7.5 V gate-drive supply.

9.4 Output voltage divider

The internal reference voltage of the error amplifier is 800 mV. The output voltage divider must be designed to obtain the required output voltage V_{OUT} . Select R_U within a range of 10 k Ω to 100 k Ω and then calculate R_D following the Equation 35.

$$R_D = \frac{R_U}{\frac{v_{OUT}}{0.8} - 1} \quad (35)$$

Figure 51. DCP85CY application schematic



9.5 PCB layout

PCB design is a crucial factor for the final application of EMC and for proper device operation in a buck converter topology, which is critical for inherent high dv/dt pulsed current paths. The scenario gets even more complex for a controller with external MOSFETs because of additional gate-driving paths that are usually internally optimized in a monolithic device.

Figure 52. Pulsed current paths in buck topology

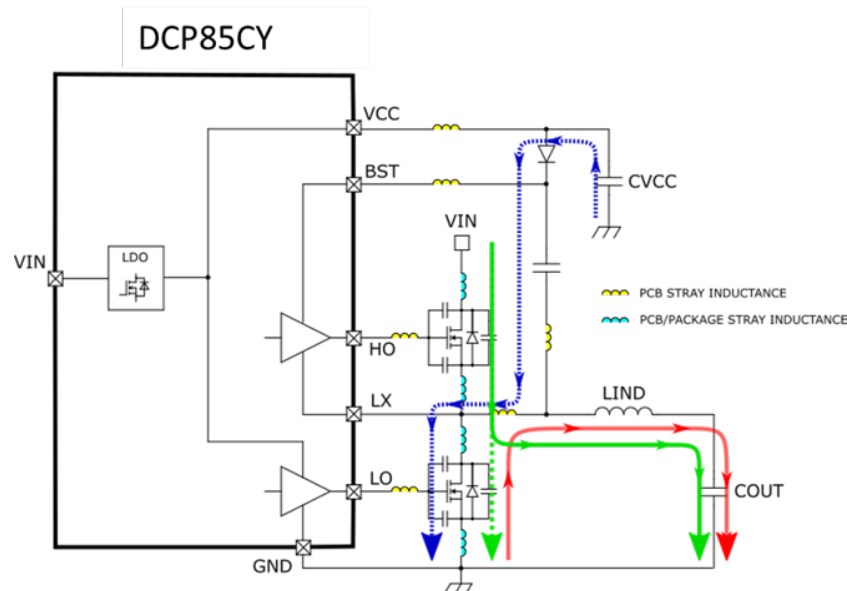


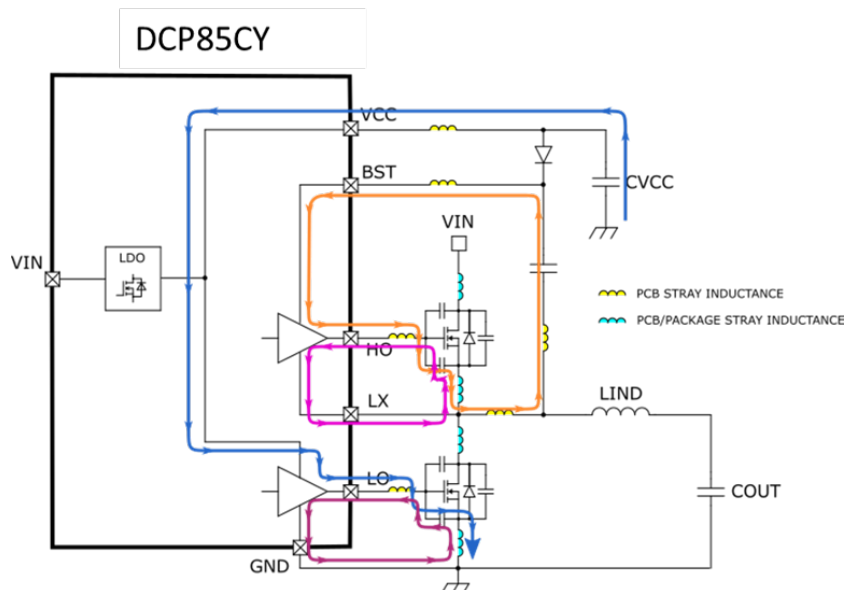
Figure 52 shows the current paths in a buck topology. During TON, when the HS ("high-side Switch") is closed, an impulsive current, shown by green-dotted trace, flows from VIN to the LS ("low-side switch") diode to recover the majority gate charge in spatial zone; that is the Q_{rr} for the diode reverse recovery operation from forward biasing. This pulsed current level can be much higher than the load current: the amount of gate charge depends on the diode p-n junction, and the peak current is limited only by parasitic elements. When the diode is reverse biased, the LX node rises and the HS current becomes the inductor current, including the output current ripple, as shown by the green trace.

Unlike the HS turn-off (red trace), the inductor current flows through the LS body diode during the dead time and then through the LS when the anticross-conduction circuitry enables it. At the same time, the blue dotted trace current flows from VCC to the grounded LX node, restores the HS gate charge spent during TON on the bootstrap capacitor and compensates for the HS driver current consumption.

The specified switched currents may generate voltage spikes due to inductive parasitic components in the printed circuit board (PCB) traces and package bonding wires of the external power components.

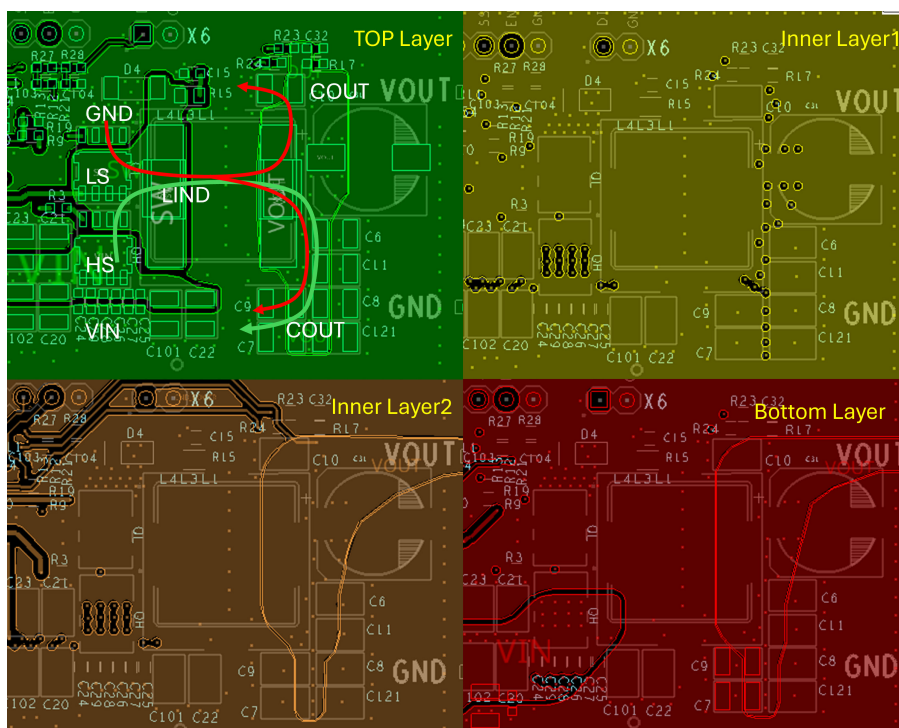
In addition to the previous description, which applies to a monolithic device with embedded power elements, a controller with external MOSFETs, such as the DCP85CY, has additional gate-drive loops for the external MOSFETs, as shown in Figure 53.

Figure 53. High-frequency gate-driving loops



The orange and blue traces represent the turn-on paths for the HS and LS respectively, while the purple and dark red traces represent the turn-off paths of the external MOSFETs. All these loops operate at the switching frequency and at high dv/dt , with current capability limited by the driver internal MOSFETs (a few Ω).

Figure 54. Board layout example



Consequently, as anticipated at the beginning of the section, the placement of the external power components (C_{IN} , C_{BOOT} , C_{VCC} , diode, and both power elements) and the connection wire to minimize inductive parasitic components are critical for device operation and EMC reduction. Figure 54 shows an example of an optimized board layout in terms of component placing and wire trace design that keeps the mentioned critical loops on the layer 1, preventing PCB via insertion in critical high-frequency loops.

10 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 QFN20 (3.5 x 4.5 mm) package information

Figure 55. QFN20 (3.5 x 4.5 mm) package outline

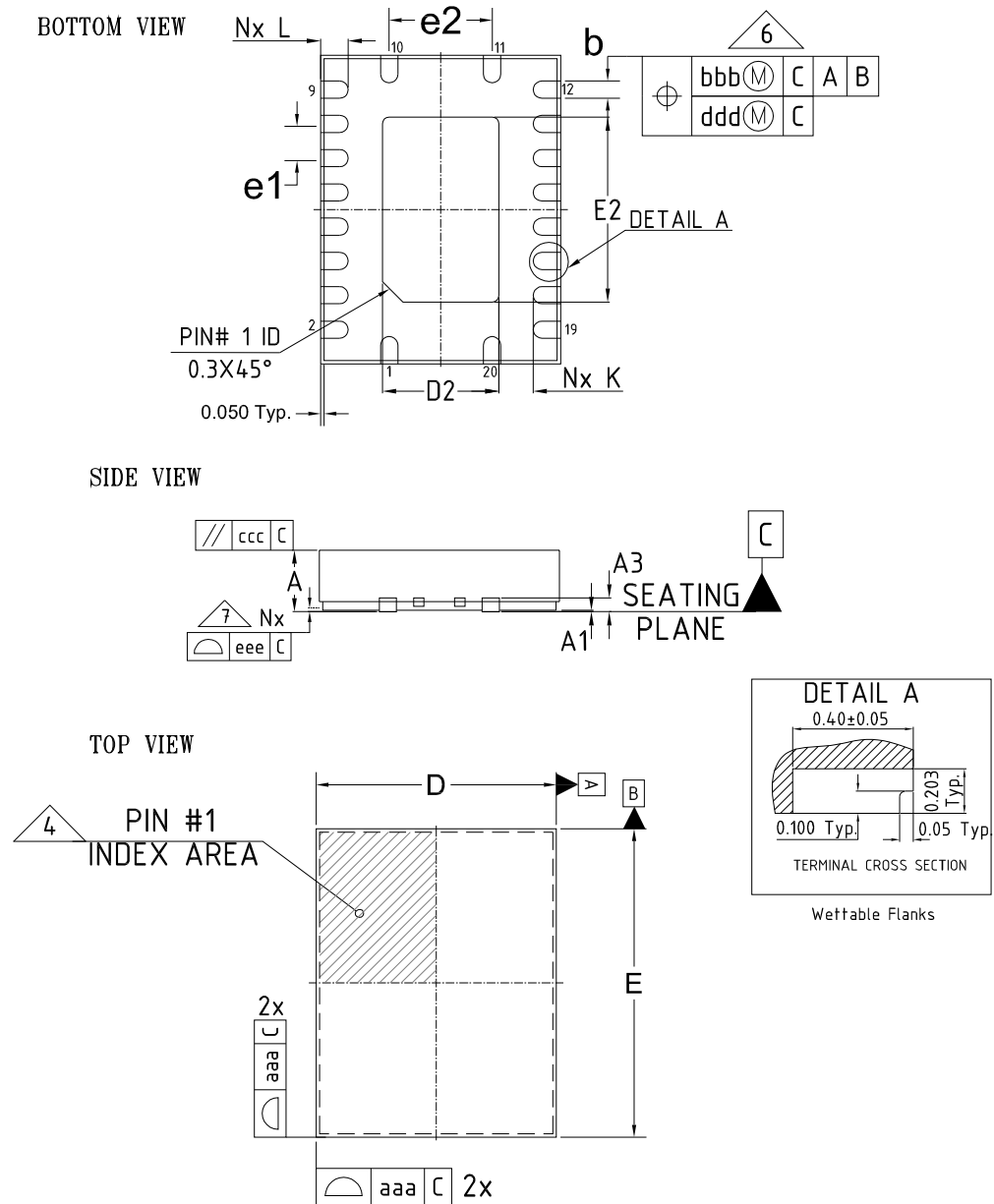
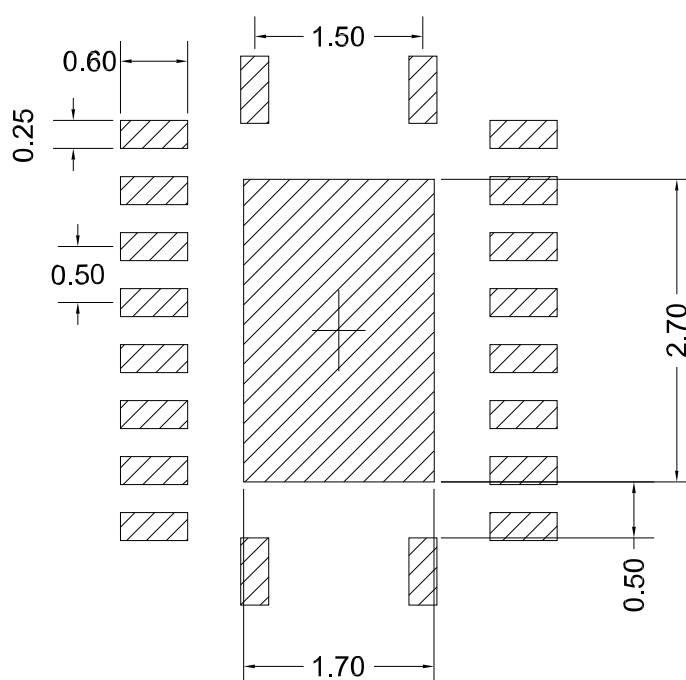


Table 10. QFN20 (3.5 x 4.5 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.203 Ref.		
b	0.20	0.25	0.30
D	3.50 BSC		
E	4.50 BSC		
e1	0.50 BSC		
e2	1.50 BSC		
D2	1.60	1.70	1.80
E2	2.60	2.70	2.80
K	0.20	-	-
L	0.30	0.40	0.50
N	20		
ND	2		
NE	8		
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Figure 56. QFN20 (3.5 x 4.5 mm) recommended footprint



10.2 QFN20 (3.5 x 4.5 mm) packing information

Figure 57. QFN20 (3.5 x 4.5 mm) tape drawing

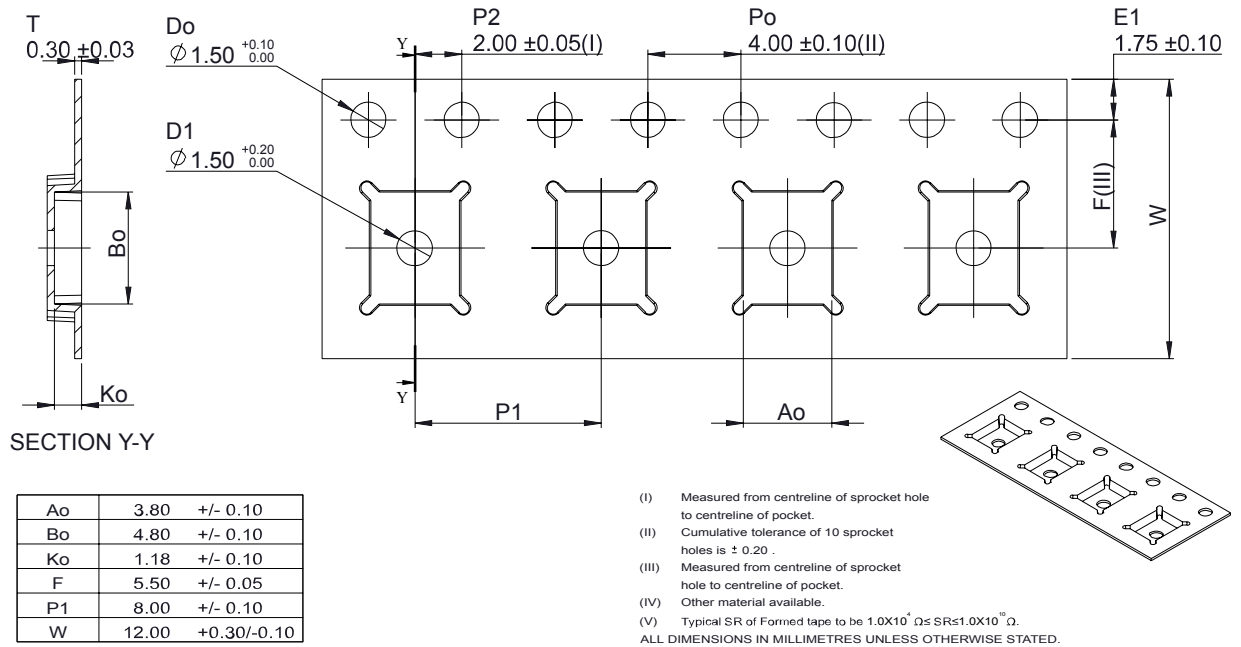


Figure 58. QFN20 (3.5 x 4.5 mm) tape oriented

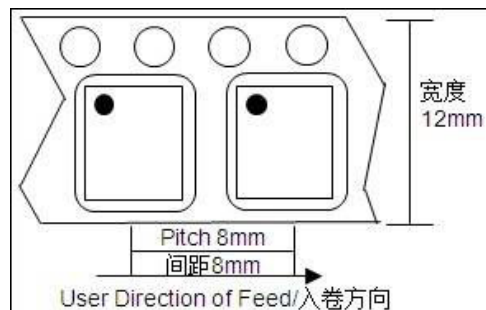
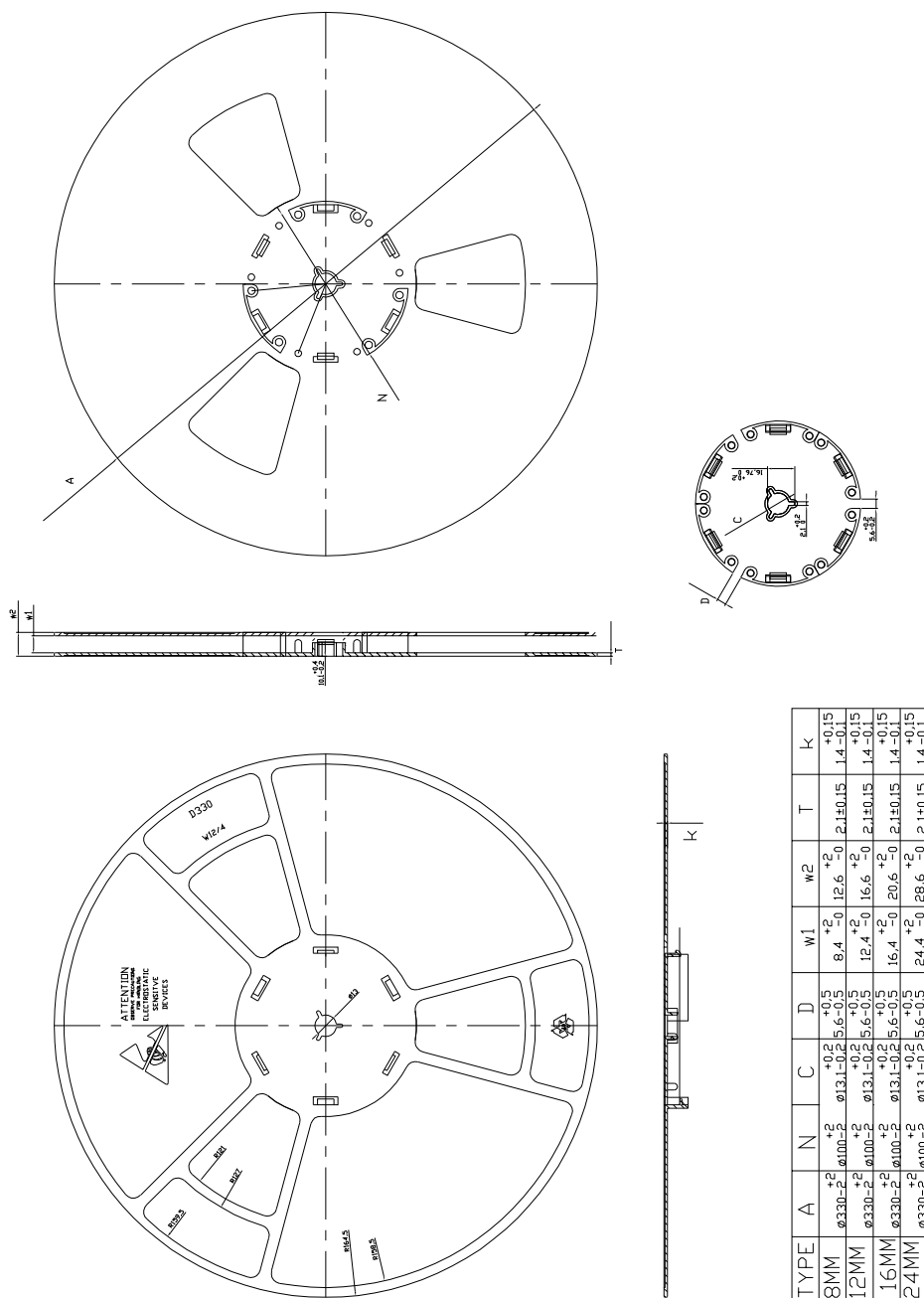


Figure 59. QFN20 (3.5 x 4.5 mm) reel dimensions



11 Ordering information

Table 11. Order codes

Order code	Package	V _{OUT}	Grade	Marking
DCP85CPURY	QFN20 (3.5 x 4.5 mm)	ADJ	Automotive	85CY

Revision history

Table 12. Document revision history

Date	Revision	Changes
20-Oct-2026	1	Initial release.

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