

36 V, up to 3 W synchronous iso-buck converter for isolated applications



Maturity status link

[DCP3601I](#)

Features

- Designed for iso-buck topology
- 3.3 V to 36 V input operating voltage range
- Primary output voltage regulation / no optocoupler required
- 1.5 A source / sink peak primary current capability
- Peak current mode control architecture in forced PWM operation
- 150 ns blanking time
- 500 kHz fixed switching frequency
- Synchronous rectification
- Internal compensation network
- Overvoltage protection
- Thermal shutdown
- Precision enable
- Frequency dithering
- Available in SOT23-6L package

Applications

- Isolated IGBT/SiC MOSFET gate driver supply
- Photovoltaic inverter
- Electric traction systems
- Charging stations

Description

The **DCP3601I** is a device specifically designed for an isolated buck topology. The extended input range from 3.3 V to 36 V makes the device suitable for a wide range of industrial applications.

The primary output voltage can be accurately adjusted, whereas the isolated secondary output is derived by using a given transformer ratio. No optocoupler is required. The primary sink capability up to -1.5 A (even during soft-start) allows a proper energy transfer to the secondary side as well as enabling a tracked soft-start of the secondary output. The control loop is based on a peak current mode architecture and the device operates in forced PWM. The 150 ns blanking time filters oscillations, generated by the transformer leakage inductance.

The **DCP3601I** operates at a fixed switching frequency of 500 kHz and embeds protections against overcurrent, overvoltage and overtemperature events. The compact SOT23-6L package and the internal compensation of the **DCP3601I** help minimize design complexity and size.

1 Pin connections

Figure 1. Pin configuration (top view)

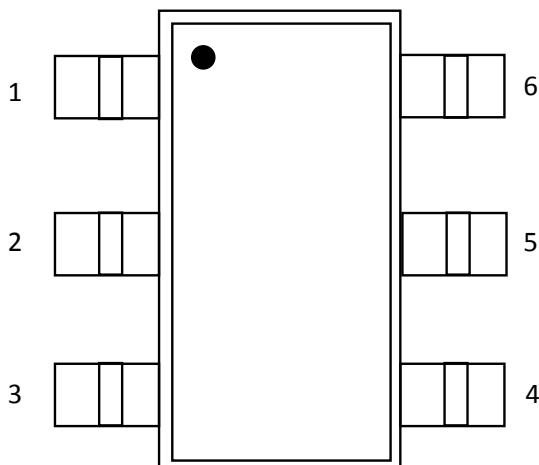
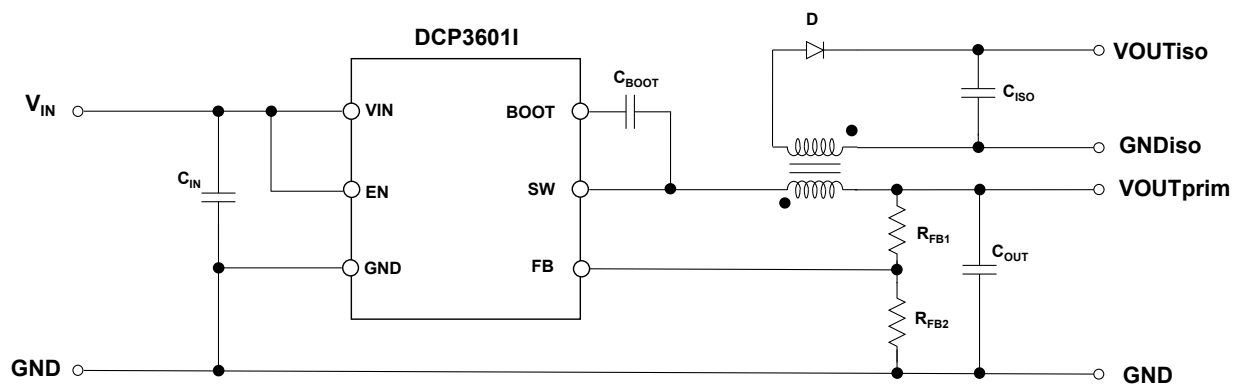


Table 1. Pin description

Name	Pin	Description
BOOT	1	Bootstrap. Connect a capacitor between SW and BOOT to form a floating supply across the high-side switch driver. A 100 nF low ESR ceramic capacitor is recommended.
GND	2	System ground. GND is the reference ground of the regulated output voltage. Therefore, care must be taken during PCB layout. Use wide PCB traces to make the connection.
FB	3	Feedback. An external resistor divider from the output to GND tapped to FB sets the output voltage. It is recommended to place the resistor divider as close as possible to the FB pin.
EN	4	Enable. Precision enable pin. If the EN voltage is below 0.95 V, the converter is in shutdown mode with all functions disabled (cannot be left floating).
VIN	5	Input voltage. VIN supplies power for the internal MOSFET, regulator, and the embedded analog circuitry. Input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
SW	6	Switch output. Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.

2 Application schematic

Figure 2. DCP3601I application schematic



3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{IN}	Power supply voltage	-0.3	38	V
V_{EN}	Enable input voltage	-0.3	$V_{IN} + 0.3$	V
V_{FB}	Feedback pin voltage	-0.3	1.5	V
$V_{BOOT-SW}$	Boot to SW differential voltage	-0.3	5.5	V
SW	Switching node voltage DC	-0.3	$V_{IN} + 0.3$	V
T_J	Operating junction temperature	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Thermal data

Symbol	Parameter	SOT23-6L	Unit
R_{thJA}	Thermal resistance junction-to-ambient	160	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106	
$R_{\theta JB}$	Junction-to-board thermal resistance	55	
Ψ_{JT}	Junction-to-top characterization parameter	29	
Ψ_{JB}	Junction-to-board characterization parameter	61	

Note: These values were calculated in accordance with JESD specification and simulated on a 4-layer JEDEC board.

Table 4. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input supply voltage	3.3		36	V
V_{EN}	Enable supply voltage			V_{IN}	V

1. The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.

Table 5. ESD ratings

Symbol	Parameter	Value	Unit
V_{ESD}	Human Body Model (HBM)	±2000	V
	Charged Device Model (CDM)	±500	

4 Electrical characteristics

$T_J = 25\text{ °C}$, $V_{IN} = 24\text{ V}$, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{FB}	Feedback voltage	$T_J = 25\text{ °C}$	0.833	0.850	0.867	V
I_Q	Quiescent current	$V_{EN} = 3.3\text{ V}$, $V_{FB} = 0.95\text{ V}$ (No switching)		1.3		mA
I_{SD}	Shutdown current	$V_{EN} = 0\text{ V}$		4	8	μA
I_{VY_SINK}	Reverse current limit ⁽¹⁾		1.3	1.5	1.7	A
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.85		3.2	V
		V_{IN} falling	2.6		2.95	V
V_{EN}	Enable threshold	V_{EN} rising	1.14	1.24	1.34	V
		V_{EN} falling	1.1	1.2	1.3	V
I_{LKG_EN}	Enable input leakage current	$V_{EN} = 3.3\text{ V}$		5		nA
$R_{DS_ON_HS}$	High-side MOSFET on-resistance	$I_{SW} = 0.1\text{ A}$		0.50	0.60	Ω
$R_{DS_ON_LS}$	Low-side MOSFET on-resistance	$I_{SW} = 0.1\text{ A}$		0.26	0.40	
I_{LIM_HS}	High-side MOSFET switch current limit ⁽¹⁾	$V_{IN} = 24\text{ V}$	1.37	1.55	1.70	A
I_{LIM_LS}	Low-side MOSFET switch current limit ⁽¹⁾	$V_{IN} = 24\text{ V}$	0.9	1.1	1.3	A
t_{ON_MIN}	Minimum switch-on time	on SW pin	300	330	360	ns
t_{OFF_MIN}	Minimum switch-off time	on SW pin		145		ns
t_{SS}	Internal soft-start time	from 10% to 90% of V_{FB}		1.4		ms
f_{SW}	Switching frequency		440	500	560	kHz
T_{SD}	Thermal shutdown threshold			175		$^{\circ}\text{C}$
T_{SD_REC}	Thermal recovery threshold			155		$^{\circ}\text{C}$
V_{OVP}	Overvoltage threshold (V_{OVP}/V_{FB})			120		%
V_{OVP_HYST}	Overvoltage hysteresis			4		%

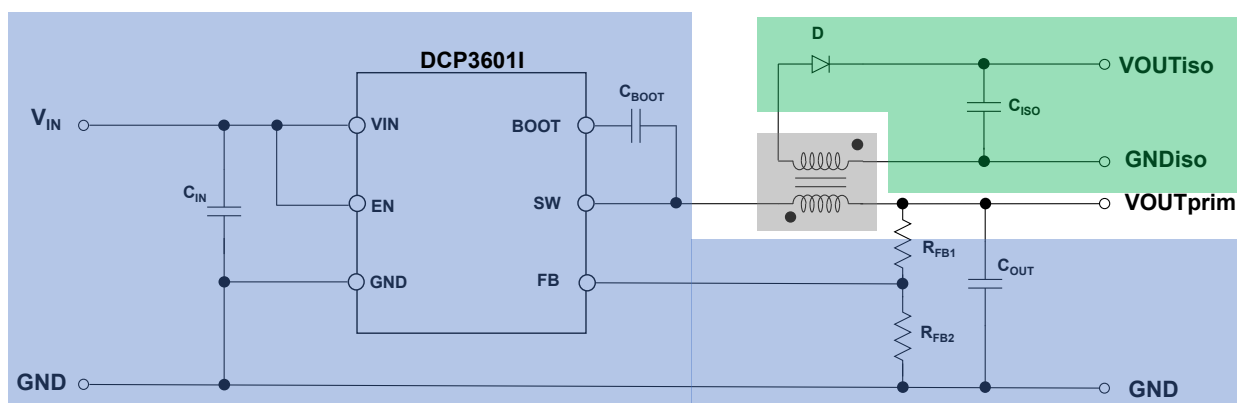
1. Parameter tested in a static condition during the testing phase. The parameter value may change under a dynamic application condition.

5 Functional description

The iso-buck topology based on the DCP3601I consists of:

- The primary side, the regulation loop of the peak current mode architecture regulates the primary voltage (blue area in the image below).
- A two-windings transformer (in gray).
- The secondary side, which generates the isolated output voltage (in green) given the selected transformer ratio.

Figure 3. Iso-buck general schematic



5.1 Primary side

The primary side of the DCP3601I is based on a “peak current mode” architecture with constant frequency control.

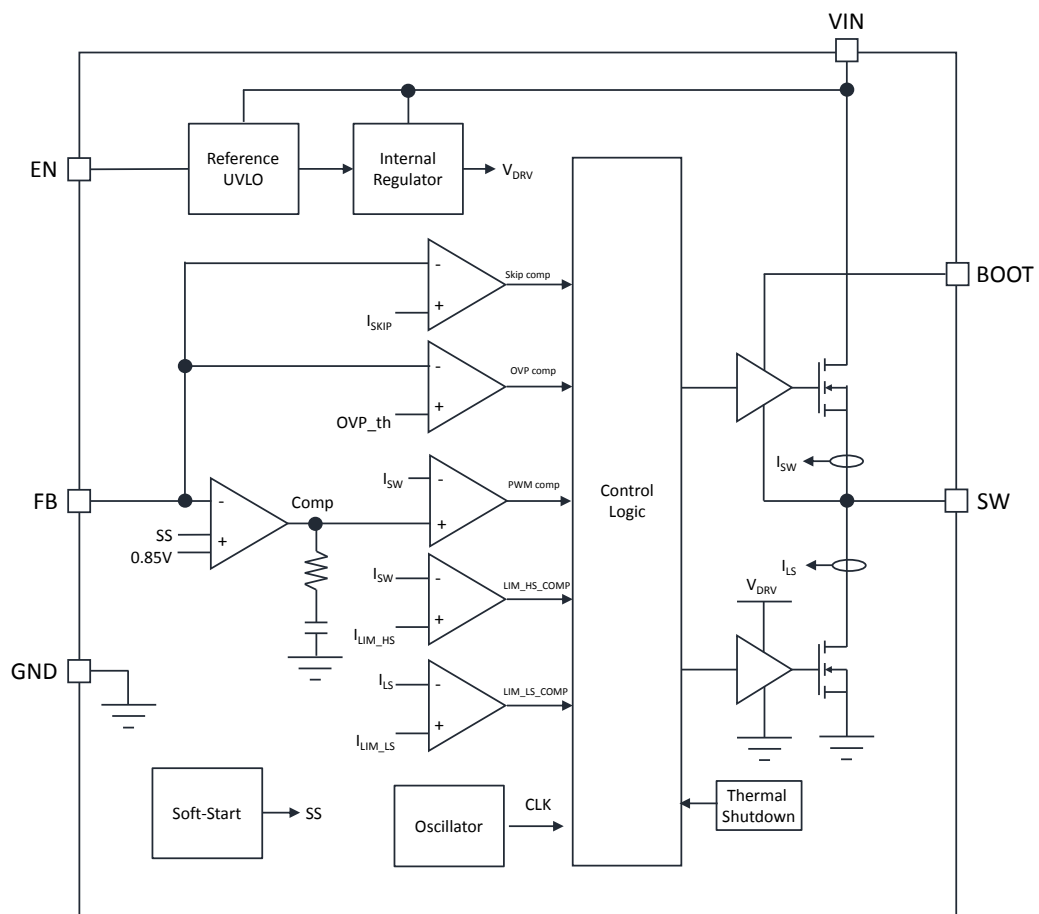
Therefore, the intersection between the error amplifier output and the sensed current in the primary winding of the transformer generates the PWM control signal to drive the power switch.

The device operates in forced PWM mode with a switching frequency of 500 kHz.

The main internal blocks shown in the block diagram (see Figure 4) are:

- Embedded power elements
- A fully integrated saw tooth oscillator with the ramp for the slope compensation avoiding subharmonic instability
- The transconductance error amplifier with integrated compensation network
- The high-side current sense amplifier to sense the inductor current
- A “pulse width modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start blocks to ramp the error amplifier reference voltage and so decrease the inrush current at power-up. The EN pin inhibits the device when driven low
- The EN pin switches the device on and off
- The current limitation circuit to implement the constant current protection, sensing pulse-by-pulse the high-side / low-side switch current
- A circuit to implement the thermal protection function
- Dithering
- The OVP circuitry to discharge the output capacitor in case of overvoltage event

Figure 4. DCP3601I primary side block diagram



5.1.1 Enable

The EN pin controls the ON/OFF operation of the buck converter. If the voltage is less than 0.95 V, it shuts down the device, while a voltage of greater than 1.36 V is required to start the converter. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the DCP3601I is to connect the EN to VIN. This allows self-startup when VIN is within the operating range.

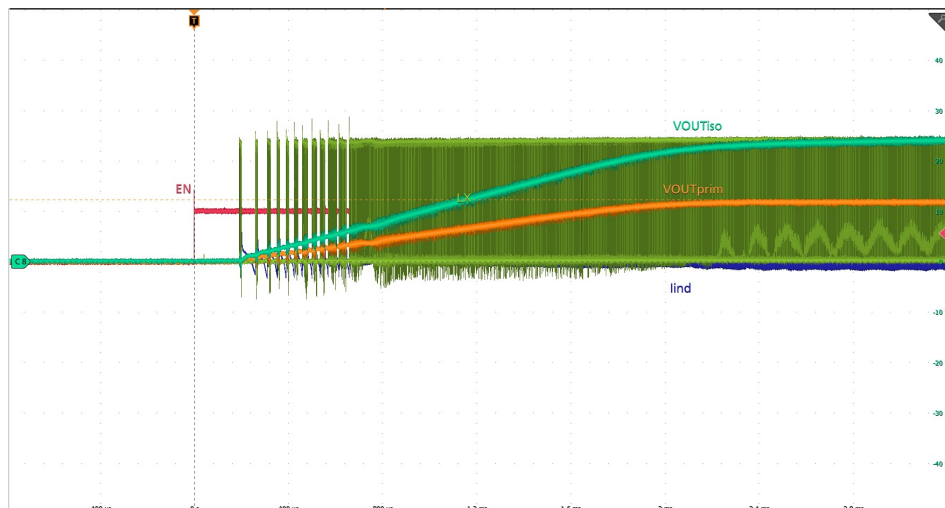
5.1.2 Soft-start

The soft-start (SS) limits the inrush current surge and makes the output voltage of the primary output increase monotonically. The device implements the soft-start phase by ramping the internal reference with very small steps. Once the SS ends, the error amplifier reference is switched to the internal value coming directly from the bandgap cell. During normal operation, a new soft-start cycle takes place in case of:

1. Thermal shutdown event
2. UVLO event
3. EN pin rising over the VEN threshold

The secondary output voltage tracks the primary output voltage rise, obviously with a different slope due to the turn ratio of the selected transformer.

Figure 5. Soft-start



5.1.3 Dithering

To reduce the cost impact of the input filter for EMI reduction, the DCP3601I implements the dithering function by default.

The internal dithering circuit changes the switching frequency in a range of $\pm 10\%$.

$$\Delta f_{SW} = 0.1 \cdot f_{SW} \quad (1)$$

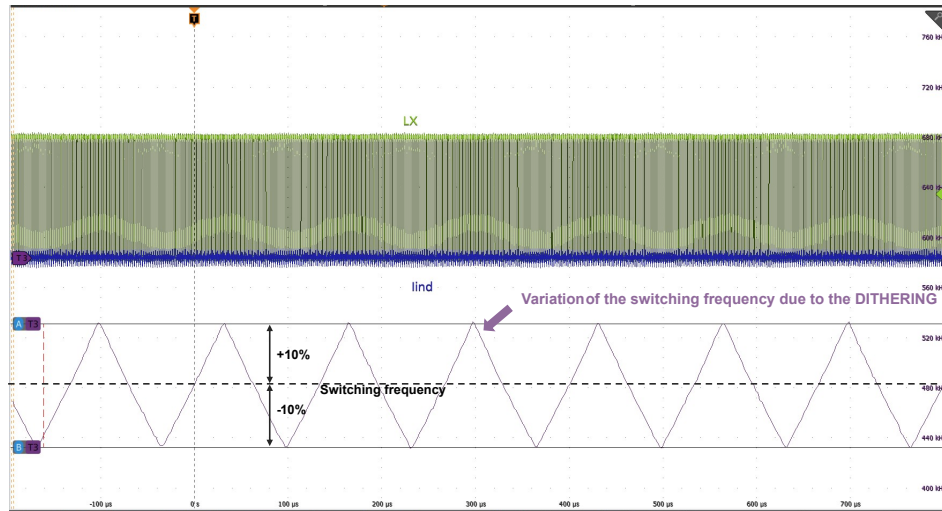
The device updates the frequency every clock period by fixed steps:

- Ramps up in 63 steps from minimum to maximum f_{SW}
- Ramps down in 63 steps from maximum to minimum f_{SW}

The modulation shape is almost triangular (see Figure 6) with a frequency of:

$$f_{DITHERING} = \frac{f_{SW}}{126} \quad (2)$$

Figure 6. Effect of the dithering on the switching frequency



5.2 Transformer

The transformer is the key component for the iso-buck, ensuring the desired isolation as well as allowing the energy transfer to the secondary side, hence generating the secondary isolated output voltage.

More details about the transformer selection are provided in the dedicated section (see [Section 9.2](#)).

5.3 Secondary side

The secondary side includes an LC filter (secondary winding of the transformer and secondary output capacitor) and the rectifying element (Schottky diode).

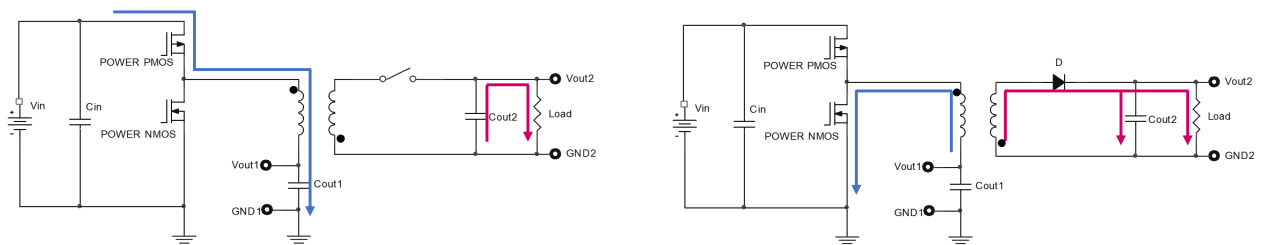
5.3.1 Iso-buck operating principle

The diagram below describes the operating principle of the iso-buck converter.

When the high-side MOSFET is turned on, the current flows through the primary winding of the transformer and charges the primary output capacitor. Considering the dot convention of the transformer, the voltage at the anode of the Schottky diode is negative, hence the diode is reverse biased and no current flows in the secondary winding. The load connected to the secondary output is supplied by COUT2.

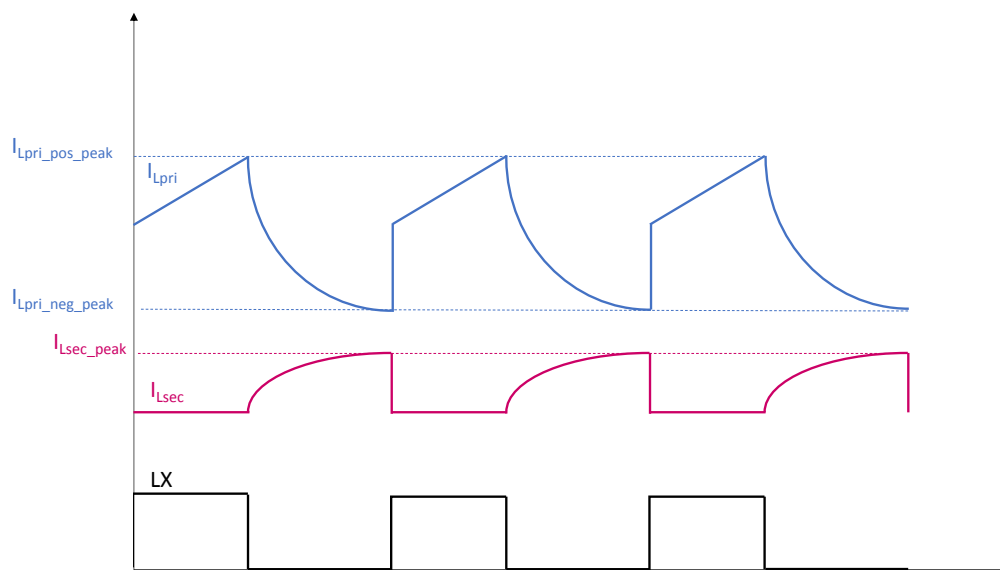
When the low-side MOSFET is turned on, the voltage applied at the transformer winding inverts its polarity. As a consequence, the Schottky diode is now forward biased and allows the current to flow from the secondary winding to COUT and the load. Under this condition, the energy transfer from primary to secondary side occurs.

Figure 7. Iso-buck basic operating principle



The waveforms in [Figure 15](#) reproduce the trend of the current in the two windings according to the switch node transitions.

Figure 8. Iso-buck primary and secondary current waveforms



6 Iso-buck performance

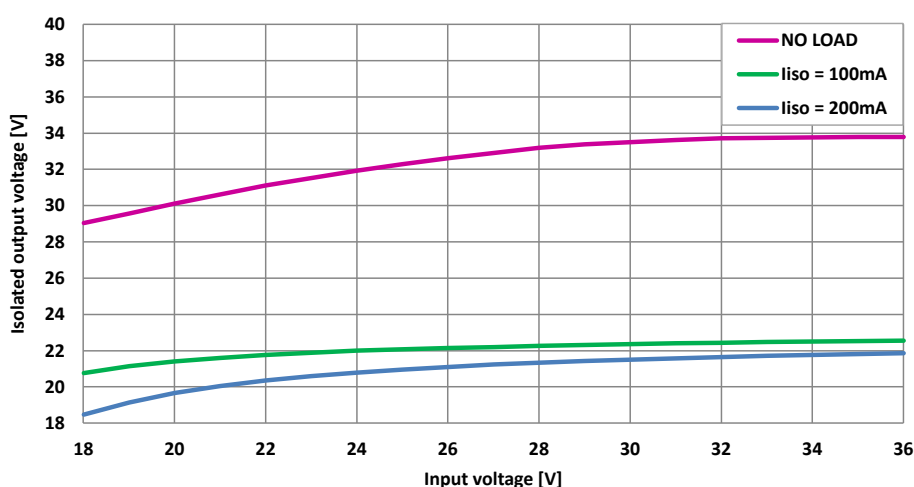
All results shown in this section come from measurements performed using the demoboard described in the dedicated section.

6.1 Secondary output line regulation

The secondary output line regulation is defined as the variation of the secondary output voltage due to the input voltage change at a specific current. The secondary output line regulation is mainly affected by the transformer and, in particular, by its leakage inductance.

Keeping the leakage inductance constant (that is, using the same transformer), a higher input voltage causes the isolated output voltage to slightly increase, as shown in Figure 9.

Figure 9. Line regulation at different isolated output currents

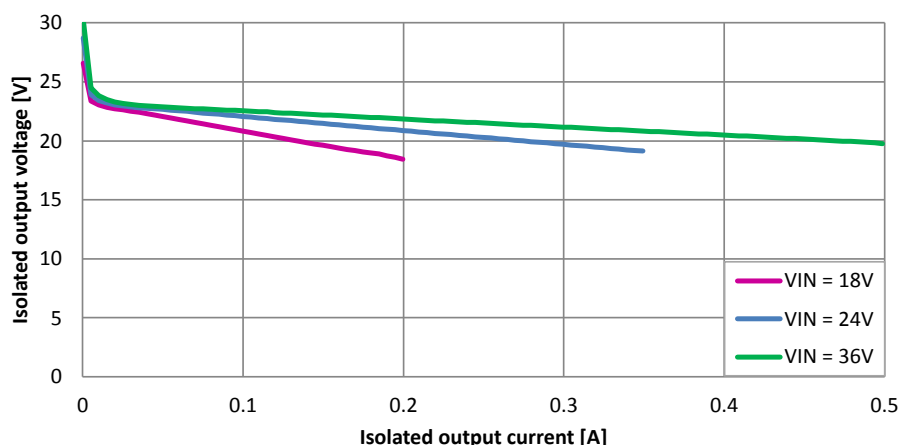


6.2 Secondary output load regulation

Since there is no regulation loop involving the secondary output, its load regulation depends, to some extent, on the primary load regulation and is affected by the leakage inductance of the transformer, the voltage drops across to the Schottky diode (diode forward voltage) and the DCR of the secondary coil, as indicated by Equation (6) in Section 8.1 (where only the last two contributions are considered). Minimizing all the mentioned parameters leads to better load regulation.

As shown in Section 6.1, the input voltage also plays a role in the isolated output regulation, as depicted below.

Figure 10. Load regulation at different input voltages

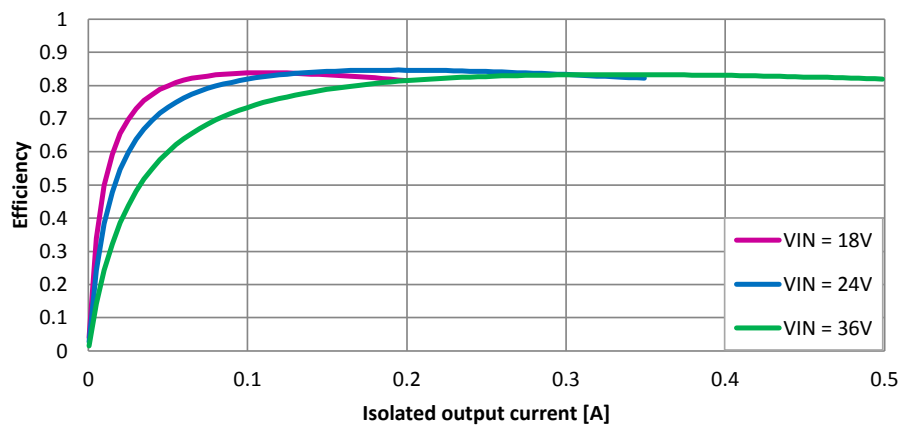


6.3 Efficiency

Figure 11 shows the efficiency referred to the secondary isolated output at different input voltages.

The effect of the input voltage on efficiency is more evident at lower currents, where the conduction losses are impacting the efficiency less, and losses affected by the input voltage (e.g. switching losses) are more significant.

Figure 11. Efficiency at different input voltages



7 Protections

The DCP3601I implements the following protections against:

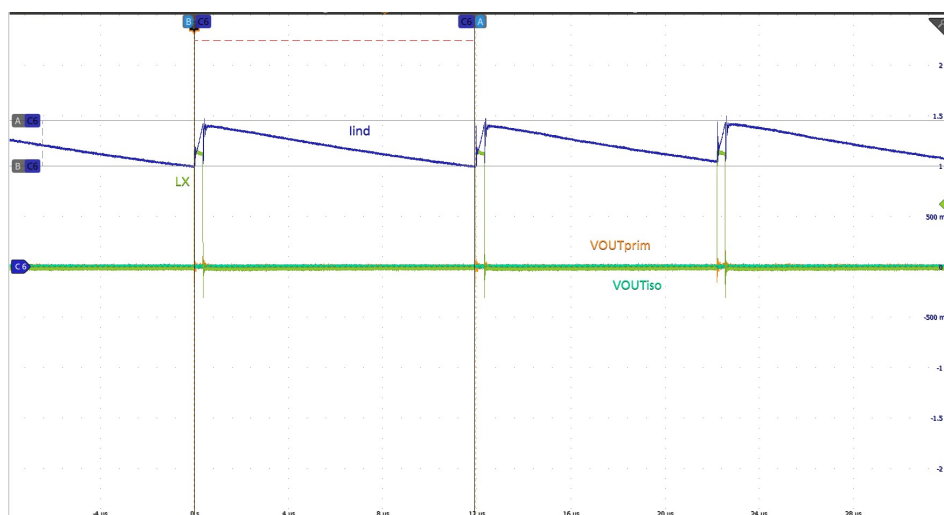
- overcurrent/short-circuit events at the primary output
- overcurrent/short-circuit events at the isolated secondary output
- primary output overvoltage
- excessive increase of the temperature (thermal shutdown)

7.1 Primary output short-circuit protection

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (please refer to [Table 7](#)) in an overcurrent condition. The DCP3601I device implements a pulse-by-pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak”, the low-side sensing “valley”. The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” (t_{ON_MIN}) because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. Therefore, the peak current protection is disabled for a masking time after the high-side switch is turned on. The masking time for the valley sensing (t_{OFF_MIN}) is activated after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, the valley current protection at extremely high duty cycles. The DCP3601I device ensures an effective overcurrent protection by sensing the current flowing in both power elements. In case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected by sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits ensure the effectiveness of the overcurrent protection even under extreme duty cycle conditions. In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. The low-side operation is able to prevent the high-side turn-on, so the device can skip pulses decreasing the switching frequency.

[Figure 12](#) shows the effect of a short-circuit on the primary side. The t_{ON} is reduced to its minimum value and the t_{OFF} is extended as much as necessary to bring the winding current below the I_{LIM_LS} (later on also named “valley current limit”). This leads to a reduction of the switching frequency.

Figure 12. Short-circuit at the primary output



7.2 Secondary output short-circuit protection

The protection against overcurrent or short-circuit events at the secondary isolated output is based on two different algorithms that can be triggered according to the application conditions, the selected transformer, and so on.

1. The primary winding current exceeds the reverse current twice within t_{OFFmin}
2. The primary winding current exceeds the valley current limit and then the reverse current limit (I_{VY_SINK} in Table 6)

In both cases, the device stops the switching activity and implements a new soft-start. The device re-starts again and, in case the overcurrent/short-circuit condition persists, the device stops the switching activity again, and so on.

Figure 13. Current protection when the current exceeds the reverse current limit twice within t_{OFF_MIN}

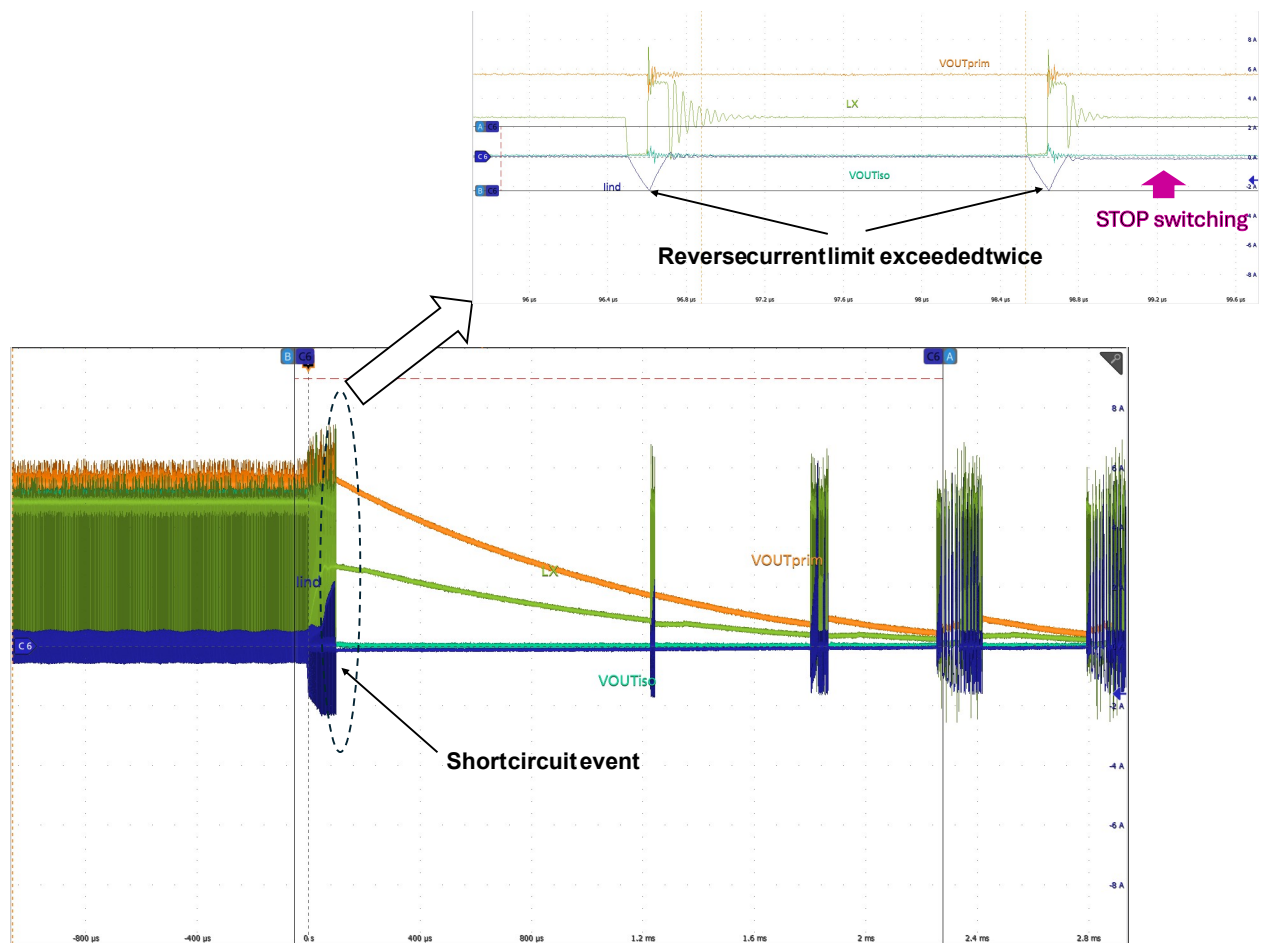
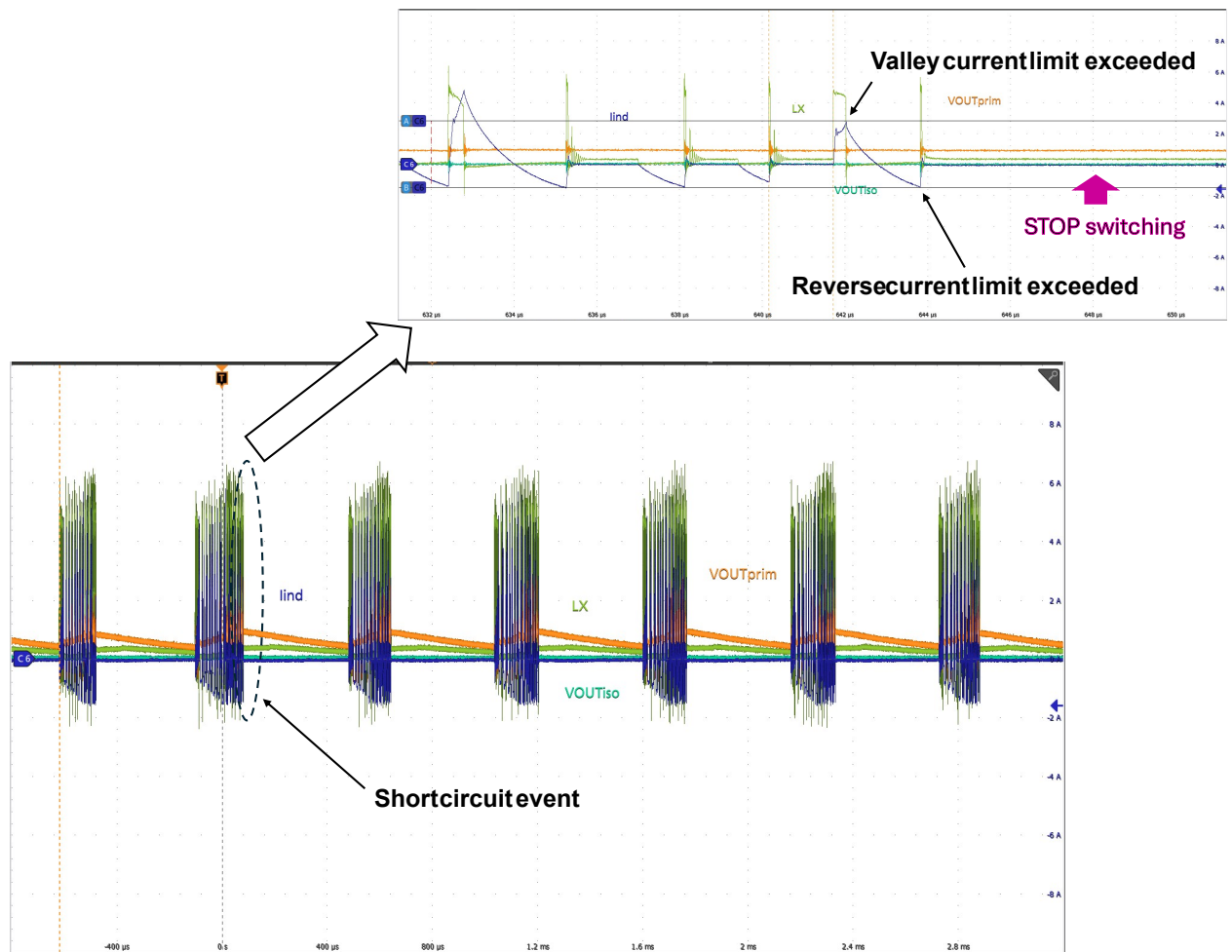
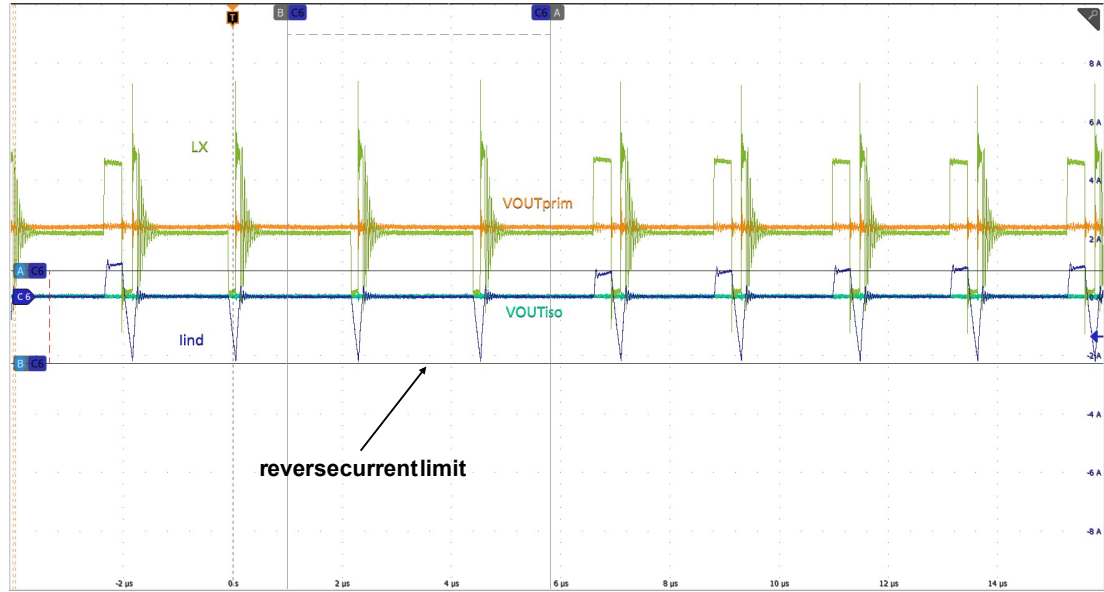


Figure 14. Current protection when the current exceeds both the valley and the reverse current limits



Before starting up again, the DCP3601I discharges the primary output voltage by sinking a current (see [Section 7.6](#)).

Depending on the device characteristics (e.g. the t_{OFF_MIN}) and the winding current slopes (linked to the application conditions and the transformer), the two algorithms mentioned above might not be triggered. Nevertheless, the DCP3601I implements a current limitation algorithm by preventing the primary negative winding from exceeding the reverse current limit cycle by cycle.

Figure 15. Current limited by the reverse current limit


7.3 Current peaks estimate

The protections described in the previous sections rely on exceeding the current peaks in the primary winding. A correct estimate of the current peaks is therefore necessary.

The positive and negative current peaks in the primary winding can be estimated using the following equations:

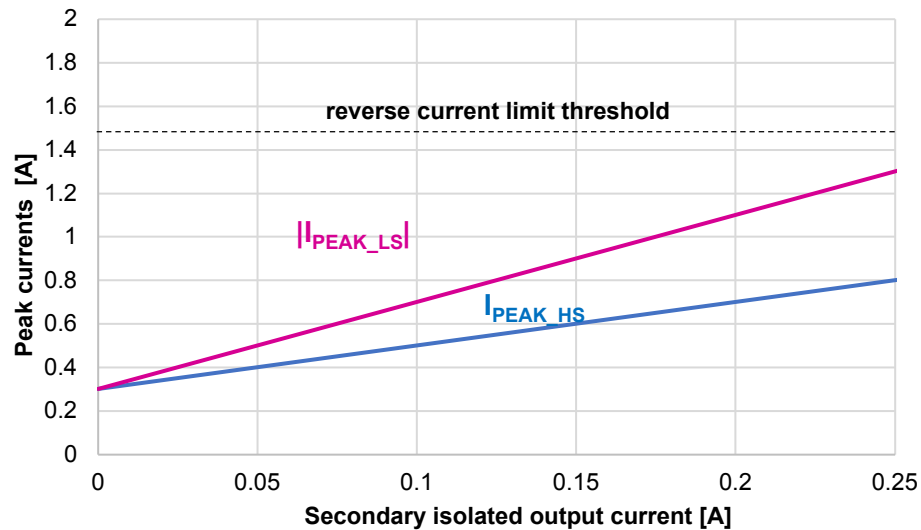
$$I_{PEAKHS} = N \cdot I_{OUT_sec} + \frac{\Delta I_L}{2} \quad (3)$$

$$I_{PEAKLS} = -N \cdot I_{OUT_sec} \cdot \left(\frac{2 \cdot D}{1-D} \right) - \frac{\Delta I_L}{2} \quad (4)$$

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \cdot V_{IN}}{V_{OUT} \cdot f_{SW} \cdot L_m} \quad (5)$$

and are also useful to determine the maximum current deliverable to the load. [Figure 16](#) shows how the current peaks (positive and negative) vary with the isolated output current and the maximum value, defined by the reverse current limit threshold.

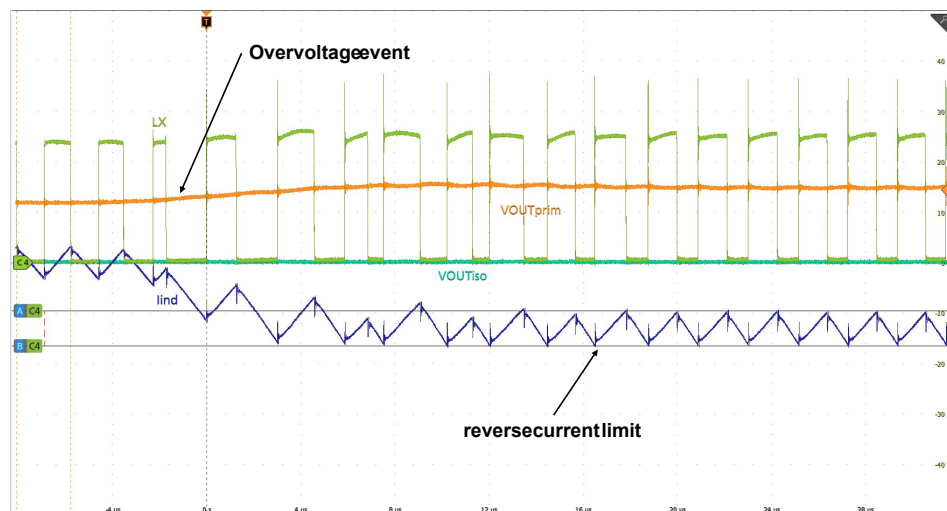
Figure 16. Current peaks in HS and LS MOSFETs depending on the isolated output current $V_{IN} = 24\text{ V}$, $V_{OUTprim} = 12\text{ V}$, $N = 2$, $f_{SW} = 500\text{ kHz}$



7.4 Primary output overvoltage protection

The overvoltage protection monitors the FB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% over the nominal value. This is a second-level protection, and it should never be triggered under normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should ensure an output voltage regulation within the overvoltage threshold even during the worst-case scenario in terms of load transitions. The protection is reliable and able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. Consequently, the output voltage regulation would be affected. The reverse current limit of the DCP3601I (refer to IVY_SINK, Table 6) implements a negative current limitation to limit the maximum reversed switch current during the overvoltage operation.

Figure 17. Overvoltage protection



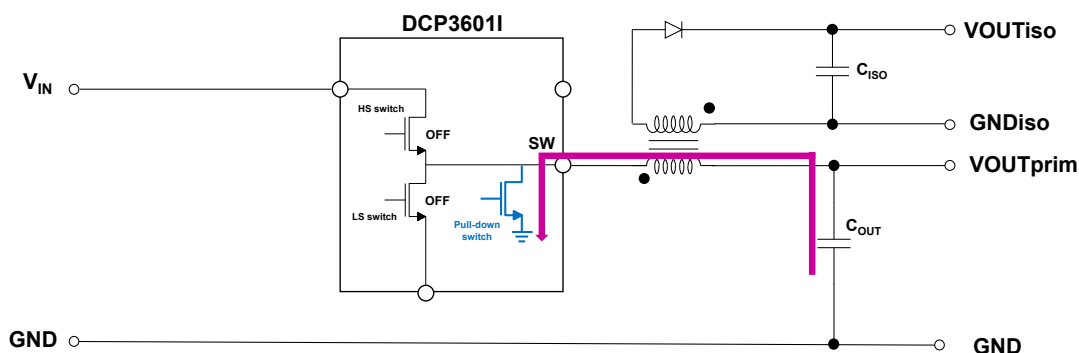
7.5 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (T_{SD} , refer to Table 7). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately $20\text{ }^{\circ}\text{C}$ prevents the device from turning ON and OFF too fast. After a thermal protection event has expired, the DCP3601I restarts with a new soft-start.

7.6 Embedded pull-down

As mentioned in the [Section 7.2](#), in case one of the two protection algorithms is triggered, the DCP3601I restarts. Since the primary output capacitor will already be charged, a new soft-start process first imposes the discharge of the output capacitor through the low-side MOSFET. Depending on the voltage present at the primary output and the capacitance value, the amount of charge to dissipate can be relevant. To prevent the low-side MOSFET from being damaged by this current, an internal pull-down switch is embedded ([Figure 18](#)).

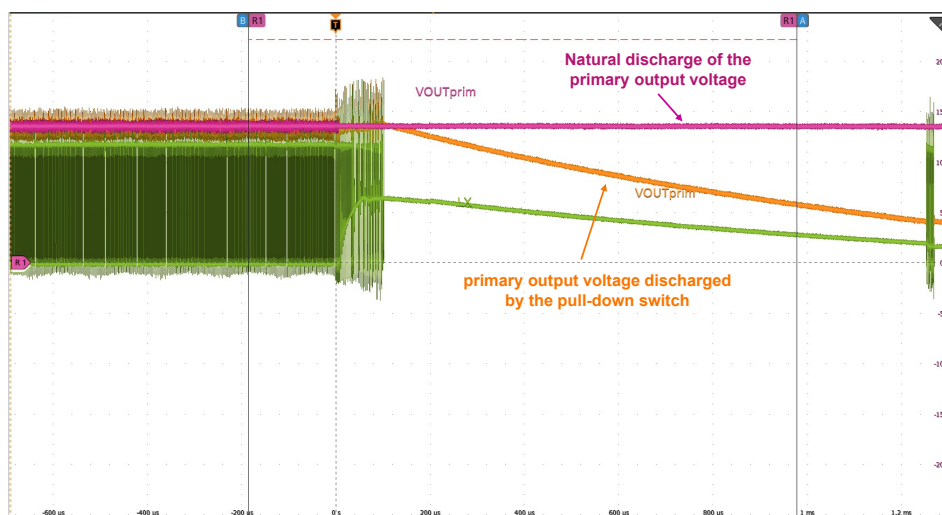
Figure 18. Pull-down mechanism



This switch acts as a current sink. It starts drawing current from the SW node (typ. 135 mA) when the device stops the switching activity due to one of the two conditions described in the [Section 7.2](#).

[Figure 17](#) compares the natural discharge of the primary output voltage if there was no pull-down switch (magenta) with the fast discharge due to the embedded pull-down switch (orange).

Figure 19. Effect of the internal discharge switch compared to a "natural" discharge



8 Application notes

8.1 Isolated output voltage adjustment

In the iso-buck converter, the secondary isolated output voltage is not included in the regulation loop. Nevertheless, a good regulation of the secondary output voltage is achieved by relying on the primary output voltage regulation, and the selection of a proper turn ratio of the transformer. Other influencing parameters are the voltage drops due to the secondary winding resistance and the Schottky diode, as well as the leakage inductance of the transformer.

This is summarized by the following equation:

$$V_{OUT_sec} = N \cdot V_{OUT_prim} \cdot \frac{L_m}{L_m + L_{LEAK}} - R_{wind_sec} \cdot I_{OUT_sec} - V_{FD1} \quad (6)$$

Where V_{OUT_prim} is the primary output voltage defined by the following equation:

$$V_{OUT_prim} = 0.85 \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \quad (7)$$

In the equation, 0.85 V represents the error amplifier reference voltage, whereas R_{FB1} and R_{FB2} are the upper and lower resistor of the output divider respectively.

A general recommendation for defining the V_{OUT_prim} is to keep the duty cycle below 70%. A higher duty cycle would limit off-time, limiting the time in which the energy transfer to the secondary side takes place.

Another restriction in the duty cycle selection derives from the minimum on-time (t_{ON_MIN}). The minimum duty cycle can be so defined:

$$D \geq D_{MIN} = t_{ON_MIN} \cdot f_{SW} \quad (8)$$

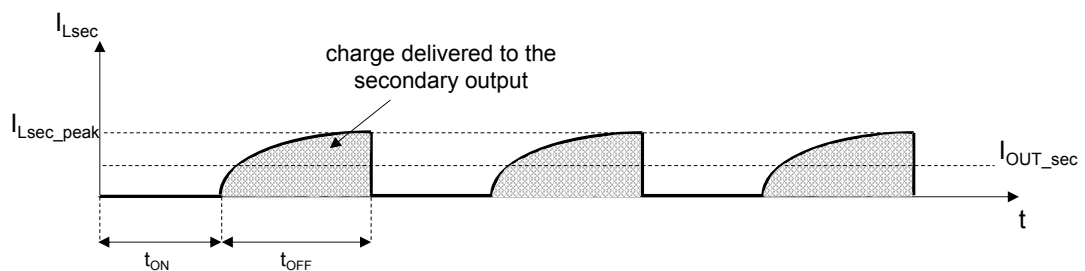
In the equation the other parameters can be described as:

- N is the turn ratio
- V_{FD1} is the forward voltage of the Schottky diode
- L_m is the magnetizing inductance of the transformer
- L_{LEAK} is the leakage inductance of the transformer.

The equation emphasizes how the selection of the transformer and, to some extent, the Schottky diode, play a crucial role in the accurate regulation of the secondary output voltage.

Another factor affecting the secondary output voltage regulation is the leakage inductance of the transformer. As described later, the leakage inductance determines the peak of the secondary winding current. This current peak defines the maximum current from the secondary isolated output by limiting the amount of charge delivered to the output. When the current demand from the secondary isolated output exceeds the maximum deliverable charge (limited by the peak current), the isolated output voltage drops.

Figure 20. Secondary output current typical waveform



The effect of the leakage on the load regulation has already been shown in [Figure 10](#).

The duty cycle can also affect the secondary output voltage to some extent. Since the energy transfer from primary to secondary only occurs during t_{OFF} , a duty cycle that is too high could reduce the achievable peak current, hence limiting the deliverable current to the secondary output. Under this condition, the secondary output could drop.

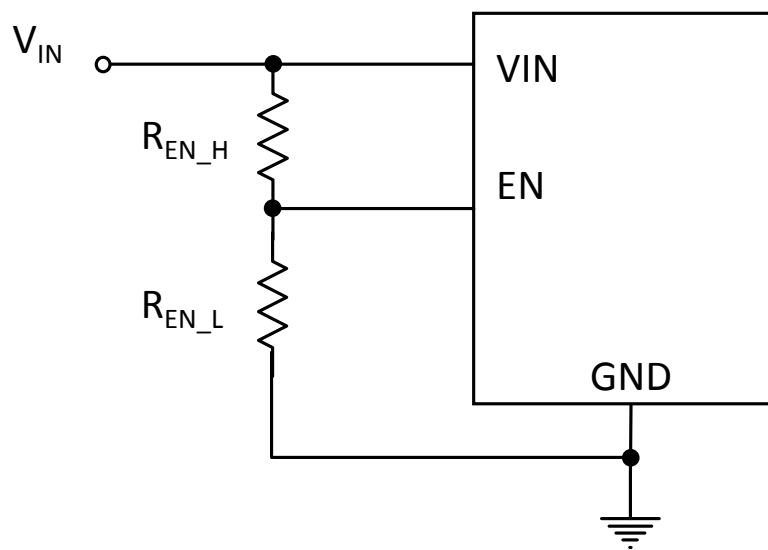
8.2 Enable resistor divider

The DCP3601I EN pin is designed with two enable threshold levels (see [Section 5.1.1](#)).

The enable thresholds are characterized by 130 mV hysteresis (typical value) to guarantee good noise immunity and a programmable start up.

The Vin start-up can be easily programmed connecting a voltage divider to the EN pin between the VIN pin and GND as show in [Figure 20](#).

Figure 21. Connection of the enable resistor divider



The enable rising threshold is equal to 1.23 V. (refer to [Table 6](#)).

The power-up threshold is adjusted according to the formula reported in equation 9:

$$V_{POWER_UP} = 1.24 \cdot \left(1 + \frac{R_{EN_H}}{R_{EN_L}} \right) \quad (9)$$

The enable falling threshold is equal to 1.1 V (refer to [Table 6](#)).

The turn-off threshold is obtained according to the formula reported in equation 10:

$$V_{POWER_DOWN} = 1.2 \cdot \left(1 + \frac{R_{EN_H}}{R_{EN_L}} \right) \quad (10)$$

If the EN pin is not used, it can be connected directly to the VIN pin. In this case, the device will start up/switch off once V_{IN} reaches/falls below $V_{IN-UVLO}$.

To maximize the overall system efficiency, it is suggested to use R_{EN_H} and R_{EN_L} between 10 kΩ and 1 MΩ.

9 Design of the external components

9.1 Input capacitor selection

The input capacitor, just like in a standard buck, should limit the input voltage ripple. Key parameters of the input capacitor are, together with its value, the maximum operating voltage and the RMS current capability.

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity, a pulsed current flows into the input capacitor and so its RMS current capability must be selected according to the application conditions. Internal losses of the input filter depend on the ESR value, so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, a lower ESR input filter has lower losses and thus contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$I_{RMS} = \left(\frac{I_{OUT_sec}}{N} \right) \cdot \sqrt{\left(1 - \frac{D}{\eta} \right) \cdot \frac{D}{\eta}} \quad (11)$$

In the ideal case of efficiency $\eta = 1$, the RMS current reaches its maximum value when $D = 0.5$.

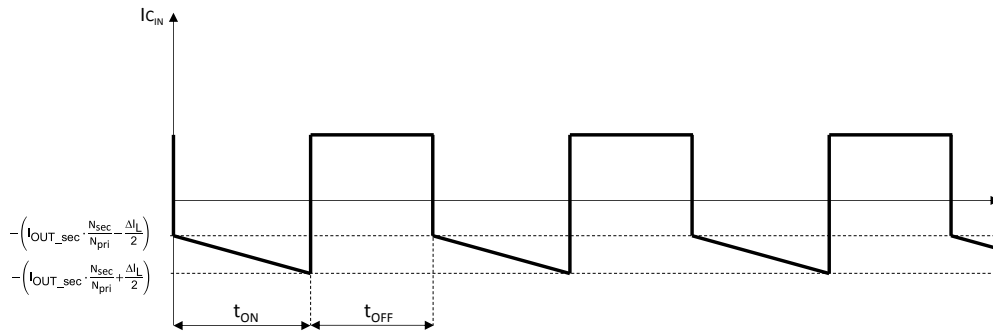
In general, the maximum and minimum duty cycles can be calculated as:

$$D_{MAX} = \frac{V_{OUT_pri} + \Delta V_{LS}}{V_{INmin} + \Delta V_{LS} - \Delta V_{HS}} \quad (12)$$

Where ΔV_{HS} and ΔV_{LS} are the voltage drop across the high-side and low-side MOSFETs respectively.

The AC component of the input current (see Figure 21) flows in the input capacitor, generating the input voltage ripple.

Figure 22. Input capacitor AC current



The peak-to-peak voltage across the input capacitor can be calculated as follows:

$$V_{PP} = \left(\frac{I_{OUT_sec} \cdot \frac{N_{sec}}{N_{pri}}}{C_{IN} \cdot f_{SW}} \right) \cdot \frac{D}{\eta} \cdot \left(1 - \frac{D}{\eta} \right) + ESR \cdot \left(I_{OUT_sec} + \frac{\Delta I_L}{2} \right) \quad (13)$$

In case of negligible ESR (e.g. in case of MLCC capacitors), the equation can be simplified. The value of the input capacitor can thus be derived:

$$C_{IN} = \frac{I_{OUT_sec} \cdot \frac{N_{sec}}{N_{pri}}}{V_{PP} \cdot f_{SW}} \cdot \frac{D}{\eta} \cdot \left(1 - \frac{D}{\eta} \right) \quad (14)$$

Considering the ideal case of $\eta = 1$, the equation above reaches its maximum value when $D = 0.5$. Therefore, the minimum input capacitance value can be defined as follows:

$$C_{IN} \geq C_{INmin} = \frac{I_{OUT_sec} \cdot \frac{N_{sec}}{N_{pri}}}{4 \cdot V_{PP} \cdot f_{SW}} \quad (15)$$

Typically, C_{IN} is dimensioned to keep the maximum peak-to-peak voltage across the input filter in the order of 5% of V_{INmax} .

9.2 Transformer selection

The transformer has two essential tasks:

- Providing the isolation between the primary and secondary side in accordance with the application requirements
- Generating the necessary secondary output voltage from the regulated primary voltage with the most suitable turn ratio

The transformer selection implies defining the following parameters:

- Isolation voltage
- Turn ratio
- Primary inductance
- Peak and RMS currents
- Windings resistance
- Leakage inductance
- Parasitic capacitances

Isolation voltage

The isolation of the transformer in terms of voltage capability (1.5 kV, 4 kV, and so on) and type (functional basic, reinforced, etc.) is mainly driven by the application. Both parameters normally affect the size of the transformer as well as other electrical characteristics (e.g. winding resistance, leakage inductance, etc.).

Turn ratio

Naming the number of turns of the primary and secondary windings N_{prim} and N_{sec} respectively, the turn ratio is defined as:

$$N = \frac{N_{sec}}{N_{prim}} \quad (16)$$

Considering the equation (17), the turn ratio must be defined so that the voltage at the secondary output is the desired one over the whole secondary output current range:

$$N \geq \frac{V_{OUT_sec} + R_{wind_sec} \cdot I_{OUT_sec} + V_{FD1}}{V_{OUT_pri}} \quad (17)$$

If no current is drawn from the primary output, the turn ratio should only be chosen to compensate the drops due to the secondary winding resistance and the Schottky diode.

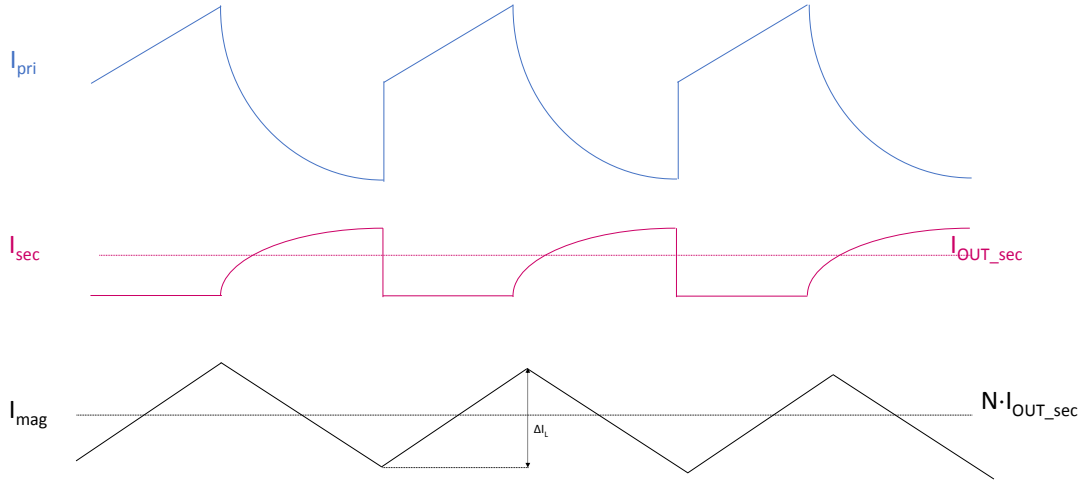
The effect of the leakage inductance on the secondary output voltage regulation (not included in the equation above) should also be taken into account. [Figure 17](#) clearly shows how the secondary output voltage can drift due to the leakage inductance.

Primary inductance SLOPE COMPENSATION

The choice of the primary inductance does not differ so much from a standard buck. The magnetizing current (see [Figure 23](#)), which combines the two winding currents, has the same shape as the buck inductor current and can be defined as:

$$I_{\text{mag}} = N \cdot I_{\text{sec}} \quad (18)$$

Figure 23. Primary winding current (blue), secondary winding current (magenta) and magnetizing current (black)



Therefore, setting the current ripple ΔI_L , the inductance is defined as:

$$L_{\text{pri}} = \frac{(V_{\text{IN}} - V_{\text{OUT_prim}}) \cdot V_{\text{OUT_prim}}}{V_{\text{IN}} \cdot f_{\text{SW}} \cdot \Delta I_L} \quad (19)$$

As an example, assuming $I_{\text{OUT_sec}} = 200 \text{ mA}$, $N = 4$, the current ripple can be set around 30% of the total current $N \cdot I_{\text{OUT_sec}} = 0.8 \text{ A}$, therefore 240 mA . If $V_{\text{IN}} = 24 \text{ V}$, $V_{\text{OUT_prim}} = 6 \text{ V}$ and $f_{\text{SW}} = 500 \text{ kHz}$, the inductor value should be around $40 \text{ } \mu\text{H}$.

Peak and RMS current

As with any inductor, the peak and RMS current for each winding must be calculated in order to define saturation and RMS currents that the transformer should fulfill.

For the primary winding, the equations below apply:

$$I_{\text{pri_pos_peak}} = \frac{I_{\text{OUT_sec}}}{N} + \frac{\Delta I_L}{2} \quad (20)$$

$$I_{\text{pri_RMS}} = \frac{I_{\text{OUT_sec}}}{N} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L \cdot N}{I_{\text{OUT_sec}}} \right)^2} \quad (21)$$

For the secondary winding, the peak current can change depending on the leakage inductance. In the picture below, secondary winding current waveforms with different leakage inductances are simulated. It is evident how the peak current can vary significantly. Considering the target leakage inductance value for an iso-buck (recommended up to 1% of the primary inductance), the waveform can be approximated with a sawtooth shape and the peak and RMS currents can hence be estimated as:

$$I_{\text{sec_pos_peak}} = \frac{2 \cdot I_{\text{OUT_sec}}}{1-D} \quad (22)$$

$$I_{\text{sec_RMS}} = I_{\text{sec_pos_peak}} \cdot \sqrt{\frac{1-D}{3}} \quad (23)$$

The equation gives an indication of the peak value. Nevertheless, the waveform can significantly change with the leakage. Therefore, the measured peak value can differ from the one provided by this equation.

A duty cycle higher than 50-60% significantly increases the peak current in the secondary winding, hence affecting the negative peak current at the primary side.

Windings resistance

Winding resistances should be minimized as much as possible since they affect the secondary output load regulations.

They also contribute to power losses, hence affecting the efficiency of the whole solution.

Leakage inductance

The leakage inductance of a transformer can be defined as an undesired inductive component due to the imperfect magnetic linking of the two windings. Leakage inductance is inherent to the transformer construction and can be only reduced but not eliminated. The typical recommendation is to keep the leakage inductance below 1% of the magnetizing inductance.

The leakage inductance affects the shape of the secondary winding current as well as the negative part of the primary winding current (which is affected by the reflected current from the secondary side). In general, a very low leakage inductance implies that the current in the secondary winding can quickly ramp up, allowing the charge of the secondary output capacitor and supporting the load current demand.

A high leakage inductance slows down the secondary winding current rise, limiting the charge delivery to the output. Comparing solutions with different values of transformer leakage inductance shows that higher leakage inductance transformers are characterized by poorer load regulation performances. On the other hand, the leakage inductance determines the slope of the rising edge of current in the primary winding (the lower is the leakage, the steeper is the slope) and the peak value it could reach. Therefore, under certain conditions (e.g. short-circuit at the secondary side) this peak can be significantly high.

A higher value of the leakage can help in these cases, jeopardizing however the load regulation performances. A similar effect can also be achieved by increasing the resistance of the secondary winding, keeping the optimized value of the inductance. In both cases, it is also possible to adjust the N value to improve the load regulation. Both higher leakage and higher secondary winding resistance have a slight negative impact on the efficiency.

Figure 24. Effect of the leakage inductance on the primary winding current

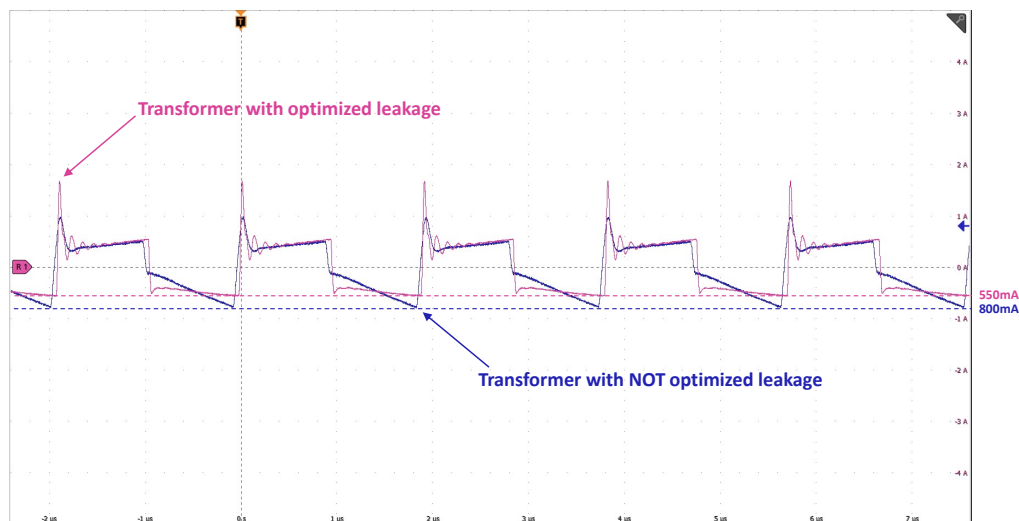
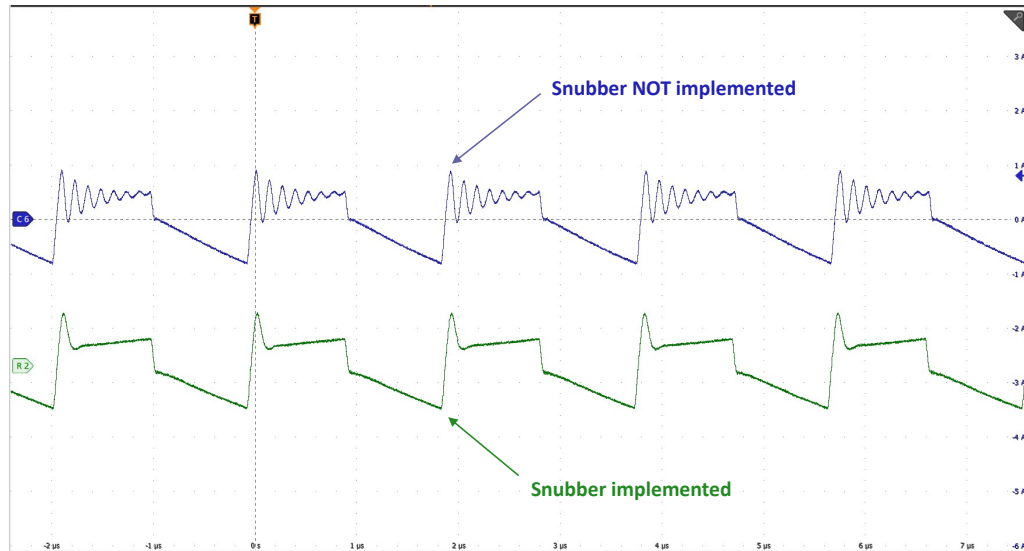


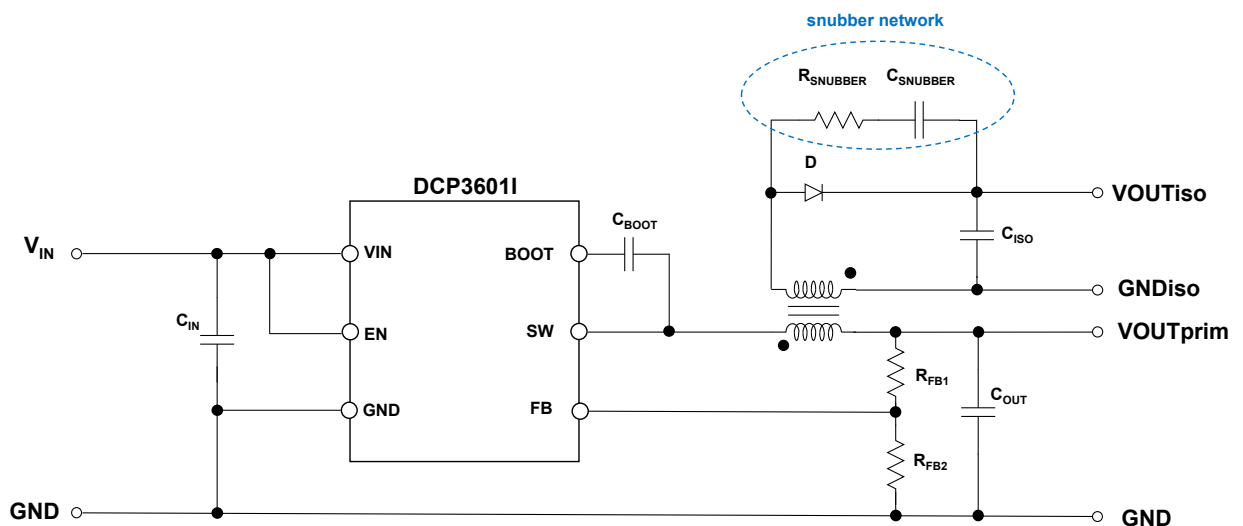
Figure 23 shows the effect of the leakage inductance looking at the primary winding current. A transformer with an optimized leakage inductance (between 0.5 and 1% of the magnetizing inductance) is compared with a transformer with a non-optimized leakage inductance (slightly above 2%). The main effect that can be observed is in the negative part of the waveform. A less optimized leakage causes the negative peak to reach a higher value (absolute value) and reduces the margin from the reverse current limit. This implies less power deliverable to the isolated output.

Another effect of the leakage inductance is the ringing observed when the transition from the off-phase to the on-phase occurs. These oscillations are due to the LC circuit represented by the leakage inductance and the total parasitic capacitance observed by the primary winding. This capacitance consists of several contributing factors:

- Primary winding capacitance
- Secondary winding capacitance, reflected to the primary side
- Reverse capacitance of the Schottky diode, reflected to the primary side

Figure 25. Filtering effect of the snubber network


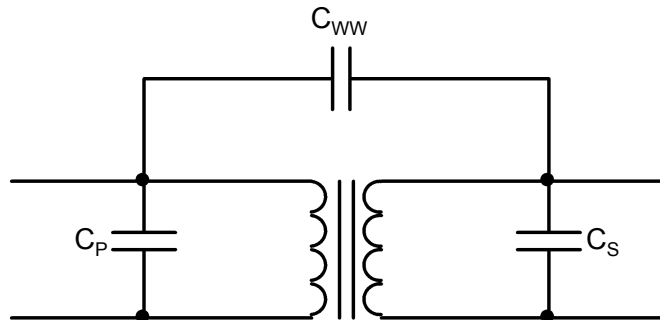
A proper masking time ($t_{ON\ MIN}$) filters these oscillations, so that in case of extreme oscillations, erroneous current limit exceeding can be avoided. Nevertheless, a RC snubber circuit (depicted in Figure 25) to dump this ringing is always recommended.

Figure 26. RC snubber network


Capacitance

The parasitic capacitance of a real transformer mainly consists of the following contributions:

- Capacitance across each winding (C_P and C_S , in the picture below) due to the capacitive coupling between the coil and the core. As already mentioned, the winding capacitances are involved in the ringing observed during transition from off to on-phase of the primary side.
- Interwinding capacitance (C_{WW}), that is the capacitance between windings. The interwinding capacitance should be reduced in order to limit disturbance on the primary side due to possible steep voltage transitions present in the load connected to the secondary output.

Figure 27. Transformer parasitic capacitances


9.4 Output capacitor selection

9.4.1 Primary output capacitor

The triangular-shaped current ripple (with an average value of zero) flowing into the output capacitor gives the output voltage ripple, which depends on the capacitor value and the equivalent resistive component (ESR). Therefore, the output capacitor should be selected in order to obtain a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as follows:

$$\Delta V_{OUT_pri} C_{OUT_pri} = ESR \cdot \Delta I_{pri} + \frac{\Delta I_{pri}}{8 \cdot f_{SW} \cdot C_{OUT_pri}} \quad (24)$$

For a multi-layer ceramic capacitor (MLCC), the capacitive component of the ripple dominates the resistive one, while the opposite is true for an electrolytic capacitor. Neglecting the ESR contribution the minimum value of the output capacitor is given by equation Eq. (25).

$$C_{OUT_pri} = \frac{\Delta I_{pri}}{8 \cdot f_{SW} \cdot \Delta V_{OUT_pri}} \quad (25)$$

The typical output ripple is set around 0.5% of output voltage. In the selection of the right value for C_{OUT_pri} , the derating of the capacitance with the voltage should be taken into account.

9.4.2 Secondary output capacitor

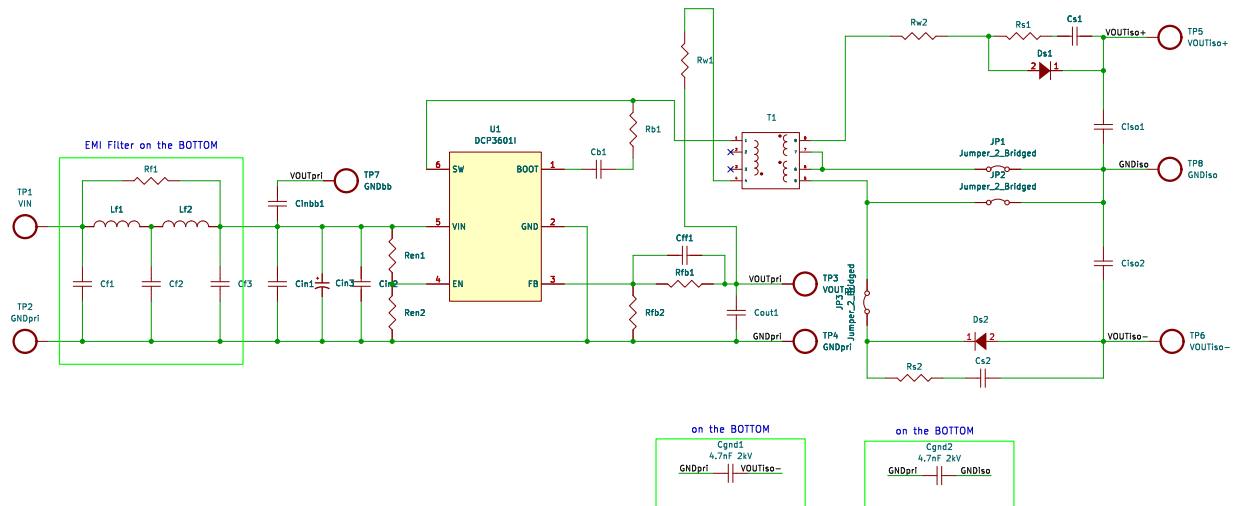
The secondary output capacitor supplies the secondary output load current during t_{ON} (when diode D1 is reverse biased) and its value defines the secondary output voltage ripple (ΔV_{OUT}).

$$C_{OUT_sec} = \frac{I_{OUT_sec} \cdot D}{\Delta V_{OUT_sec} \cdot f_{SW}} \quad (26)$$

10 Application board

The application board (STEVAL-360111L) schematic is shown below.

Figure 28. Schematic of the application board



The additional input filter (in the dotted box in Figure 28, on the bottom side of the board) limits the conducted emission on the power supply. In the case that the filter is not necessary or should be bypassed for any test, two 0 Ω resistors should be placed at Lf1 and Lf2 instead of the indicated inductor and ferrite.

The embedded transformer has two secondary windings that can be used separated (to generate a dual voltage) or in series (to generate a single voltage). The default configuration is in series.

The main advantage of an iso-buck is the possibility to use the primary voltage, which is well-regulated, as an auxiliary voltage, whenever it is required in the application. For that reason, the STEVAL-360111L has been designed so that the primary output voltage provides 12 V and the secondary isolated output voltage is around 24 V. The isolated output voltage varies slightly with the load. Nevertheless, a post-regulation circuit can be implemented when necessary. For further details, please refer to the AN6203.

Table 7. BOM of the application board

Reference	Part number	Description	Value	Manufacturer
U1	DCP3601I	Iso-buck		ST
T1	ZD2020-AE	Transformer	N = 2, 1.5 kV isolation	Coilcraft
Rs1		0805 SMD resistor	110 Ω	
Rs2		0805 SMD resistor	110 Ω	
Rb1		0603 SMD resistor	0 Ω	
Ren1		0603 SMD resistor	100 k Ω	
Ren2		0603 SMD resistor	Not mounted	
Rfb1		0603 SMD resistor	62 k Ω	
Rfb2		0603 SMD resistor	4.7 k Ω	
Rw1		0603/1206 SMD resistor	0 Ω	
Rw2		0603/1206 SMD resistor	0 Ω	
Cff1		0603 MLCC	Not mounted	
Cb1		0603 MLCC	100 nF, 50V	
Cs1		0603 MLCC	120 pF, 50 V	
Cs2		0603 MLCC	120 pF, 50 V	
Cin1		0805 MLCC	2.2 μ F, 50 V	Panasonic
Cin2		0603 MLCC	100 nF, 50 V	
Cin3		SMD Electrolytic capacitor, 6.3 mm	10 μ F, 100 V	
Cout1		1206 MLCC	22 μ F, 25 V	
Ciso1		1206 MLCC	10 μ F, 50 V	
Ciso2		1206 MLCC	10 μ F, 50 V	
C _{inbb1}		0603 MLCC	Not mounted	
C _{gnd1}		1812 MLCC	4.7 nF, 2 kV	Murata
C _{gnd2}		1812 MLCC	4.7 nF, 2 kV	Murata
Ds1	STPST1H100ZF	Schottky diode	V _{RRM} = 100 V, I _F = 1 A	ST
Ds2	STPST1H100ZF	Schottky diode	V _{RRM} = 100 V, I _F = 1 A	ST
EMC input filter				
Rf1		0603/0805 SMD resistor	Not mounted	
Cf1, Cf2, Cf3		1206 MLCC, 4.7 μ F, 50 V		
Lf1	MPZ2012S221A	220 Ω Ferrite bead, 100 MHz		
Lf2	XGL4030-473ME	4.7 μ H coil		Coilcraft

Table 8. ZD2020-AE main parameters

Parameter	Value
$N_{\text{PRIM}}:N_{\text{SEC1}}$	1:1.562 typ.
$N_{\text{PRIM}}:N_{\text{SEC2}}$	1:0.438 typ.
L_m	20 μH typ.
L_{LEAK}	250 nH max.
$R_{\text{WIND_PRIM}}$	120 m Ω max.
$R_{\text{WIND_SEC1}}$	370 m Ω max.
$R_{\text{WIND_SEC2}}$	160 m Ω max.
Isolation	1.5 kV

The performance of the application board is depicted in [Section 6](#).

The layout of the STEVAL-360111L is shown in [Figure 29](#) (top) and [Figure 30](#) (bottom).

Figure 29. Layout of the STEVAL-360111L (top side)

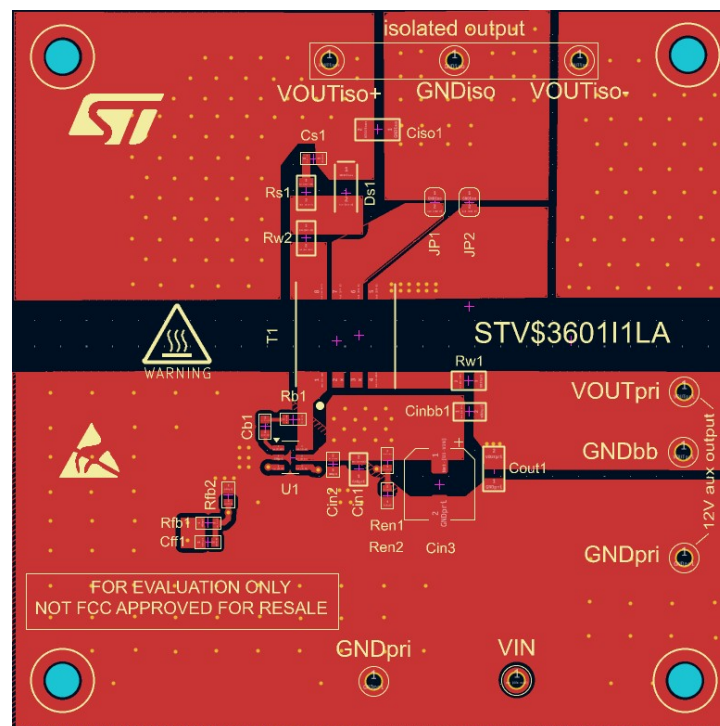
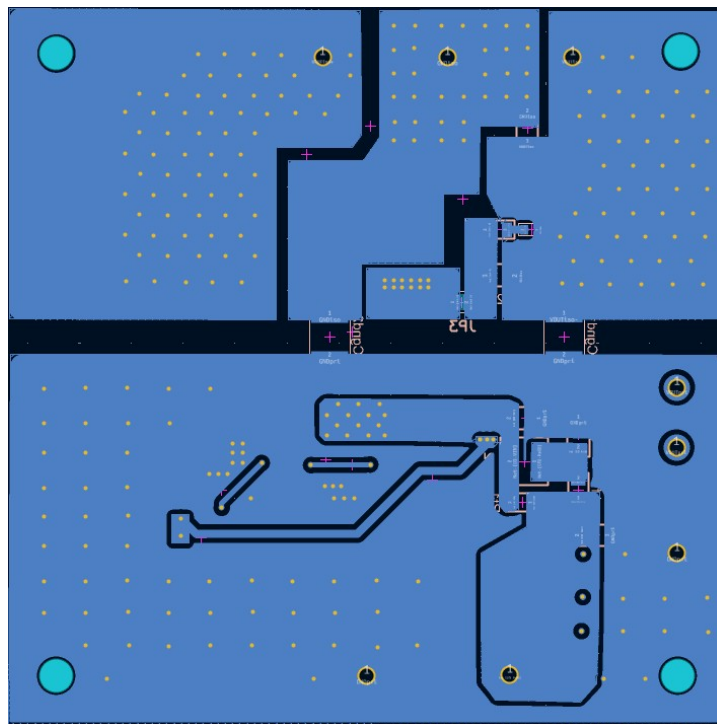


Figure 30. Layout of the STEVAL-3601I1L (bottom side)



10.1 Single or dual isolated output voltage

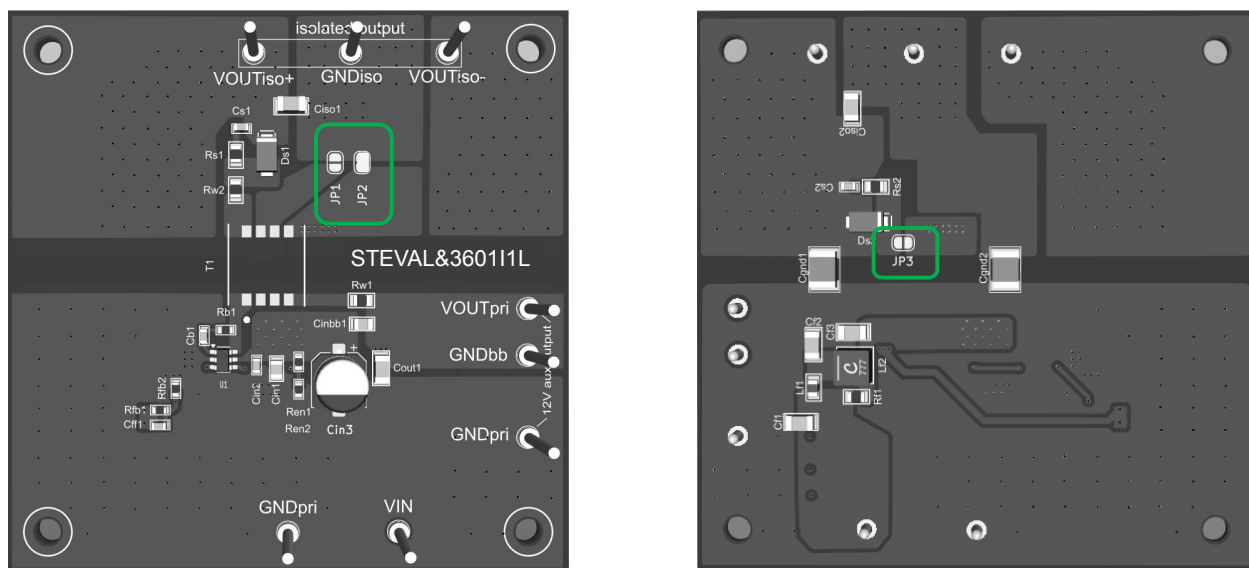
As described in the previous section, the embedded transformer allows for generating a single or dual isolated output voltage.

The selection of these two isolated output options can be done using the tin drop jumpers JP1, JP2 and JP3, according to the table shown below.

Table 9. Single or dual isolated output voltage

JP1	JP2	JP3	Isolated output voltage
open	shorted	open	single
shorted	open	shorted	dual

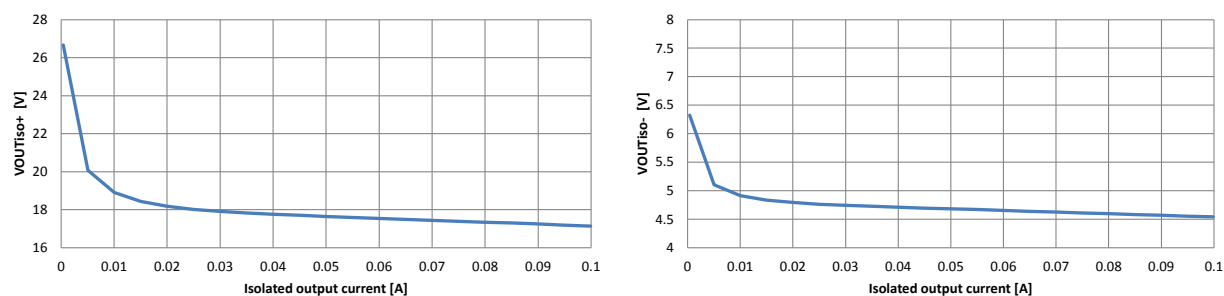
Figure 31. Position of the jumper for single/dual isolated output voltage



The dual voltage is by default around 18 V between VOUTiso+ and GNDiso and around -5 V between VOUTiso- and GNDiso, usually suitable for a SiC driver.

The load regulation performance is depicted below.

Figure 32. Load regulation for the dual output configuration (positive output on the left, negative output on the right)



11 Application ideas

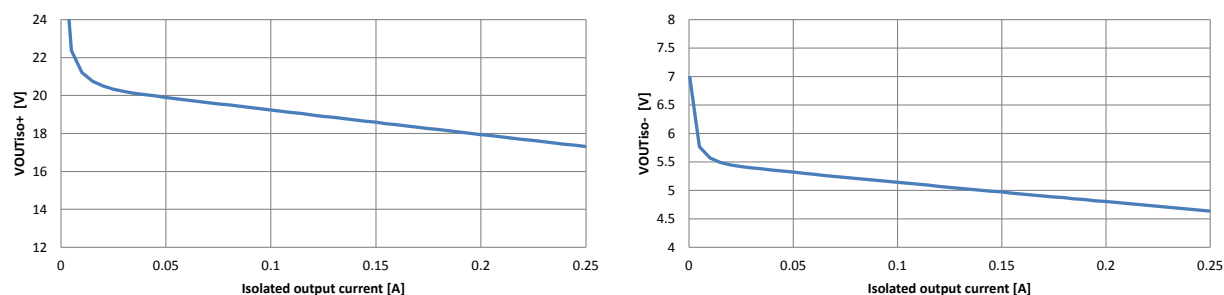
11.1 Maximizing the isolated output power

The STEVAL-3601I1L has been designed to provide a 12 V regulated voltage (not isolated) at the primary output, which can be used as an auxiliary voltage in a system where the DCP3601I is implemented.

Nevertheless, when the primary output voltage is not used, a different value of this voltage can be selected so that the deliverable power at the secondary output can be maximized.

In the example below, the primary output voltage is set to 13.6 V.

Figure 33. Load regulation for dual voltage application (18 V / -5 V), $V_{IN} = 24$ V, $V_{OUTprim} = 13.6$ V



11.2 Generating other isolated voltages

According to the final application, different values of the isolated voltage(s) can be required. Depending on the primary output voltage (if it should be used as auxiliary voltage or can be freely set), a different turn ratio might be required.

The table below summarizes some typical cases.

Table 10. Settings for generating other isolated voltages

Primary output voltage	Isolated output voltage	Transformer	RFB1	RFB2	Load regulation
13.6 V	6 V / -3 V (e.g. GaN)	ZE2774-BE	30 k Ω	2 k Ω	see Figure 33
13.6 V	12 V single	Any with N = 1	30 k Ω	2 k Ω	see Figure 34

Figure 34. Load regulation for a dual isolated voltage application (6 V / -3 V), transformer ZE2774-BE, $V_{OUTprim} = 13.6\text{ V}$

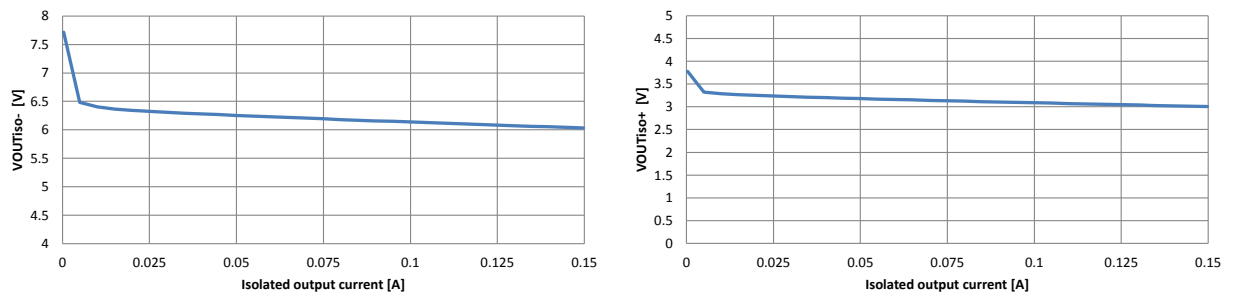


Figure 35. Load regulation for a single isolated voltage application (12 V), transformer MSD1038V-333, $V_{OUTprim} = 13.6\text{ V}$

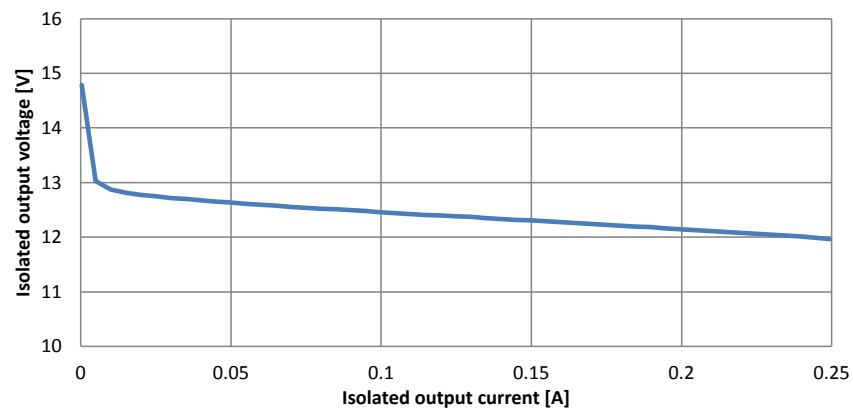


Table 11. ZE2774-BE main parameters

Parameter	Value
N _{PRIM} :N _{SEC}	1:0.5 typ.
N _{PRIM} :N _{SEC}	1:0.273 typ.
L _m	20 µH typ.
L _{LEAK}	410 nH max.
R _{WIND_PRIM}	170 mΩ max.
R _{WIND_SEC1}	430 mΩ max.
R _{WIND_SEC2}	300 mΩ max.
Isolation	1.5 kV

Table 12. MSD1038V-333 main parameters

Parameter	Value
N _{PRIM} :N _{SEC}	1:1
L _m	33 µH typ.
L _{LEAK}	800 nH typ.
R _{WIND_PRIM}	340 mΩ max.
R _{WIND_SEC1}	340 mΩ max.
Isolation	2.25 kV

11.3 Iso-buck-boost operation

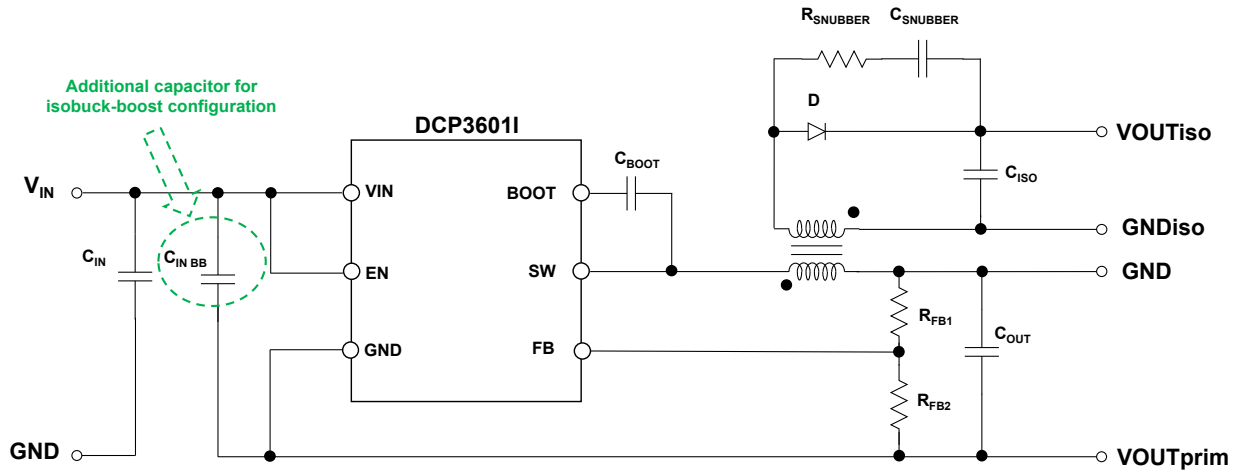
For lower values of input voltage (e.g. 5 V, 12 V), the primary output voltage should be further reduced and therefore regulating isolated voltages like 12 V, 24 V or higher implies a higher value of the turn ratio of the transformer. A higher value of the turn ratio affects the size and the parameters of the transformer, as well as leading to higher current peaks in the primary winding, limiting the deliverable current to the secondary side.

In case the primary output voltage is not used as an auxiliary voltage, a possible alternative would be to implement the iso-buck-boost configuration. This means that the primary side operates as an inverting buck-boost (hence the primary output voltage is negative), which implies that the primary output voltage can be higher than the input voltage (with the only limitation $V_{IN} + |V_{OUT_{prim}}| < 36$ V) and so the turn ratio can be reduced.

In terms of schematic, the iso-buck-boost slightly differs from the iso-buck (see [Figure 36](#)).

For the iso-buck-boost operation, it is recommended to solder the capacitor CINBB1 (e.g. 2.2 µF, 50 V MLCC).

Figure 36. Schematic for iso-buck-boost operation



The table below shows two possible examples of use for the iso-buck-boost configuration.

Example	V_{IN}	V_{OUTiso}	Transformer	$V_{OUTprim}$	R_{FB1}	R_{FB2}
#1	12 V	18 V / -5 V	ZD2020, two secondary windings separated	-12.6 V	18 k Ω	1.3 k Ω
#2	5 V	12 V	ZD2020, two secondary windings in series	-6.8 V	9.1 k Ω	1.3 k Ω

The load regulation performance of the two examples is shown in Figure 37 and Figure 38.

Figure 37. Load regulation for example #1

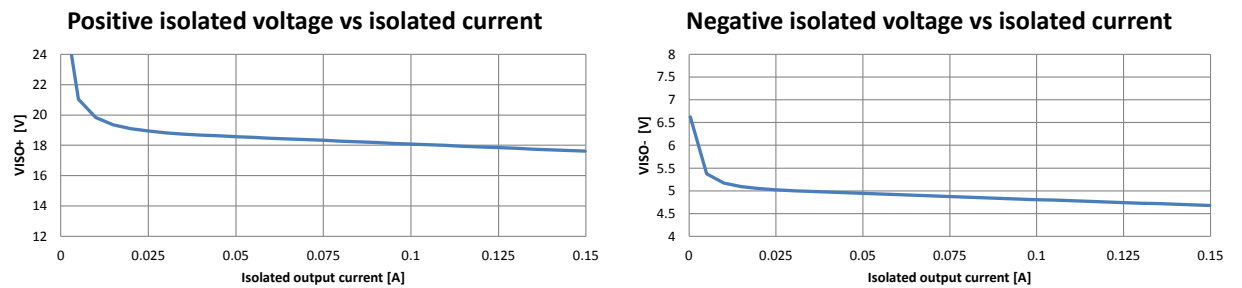
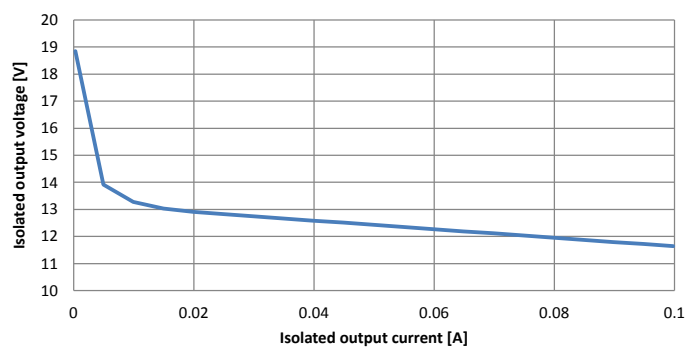


Figure 38. Load regulation for example #2



12 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

12.1 SOT23-6L package information

Figure 39. SOT23-6L package outline

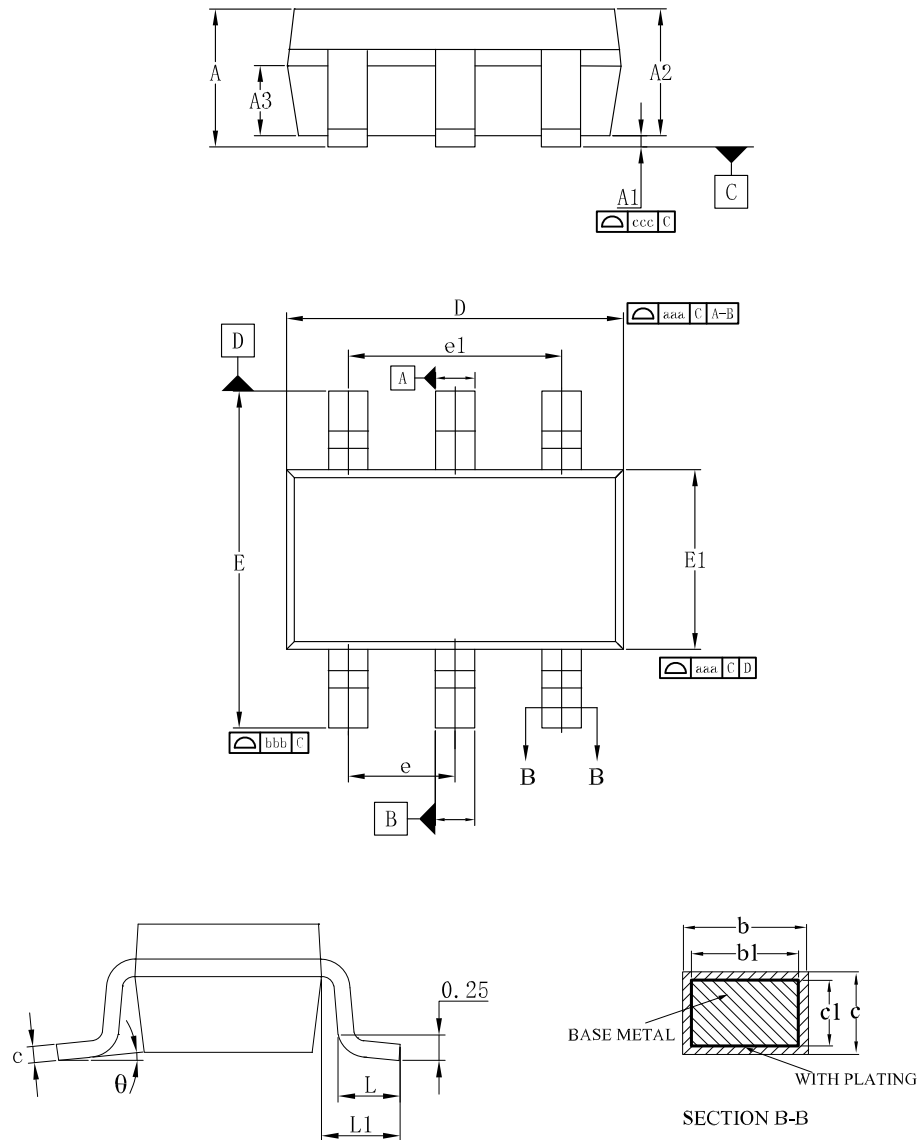
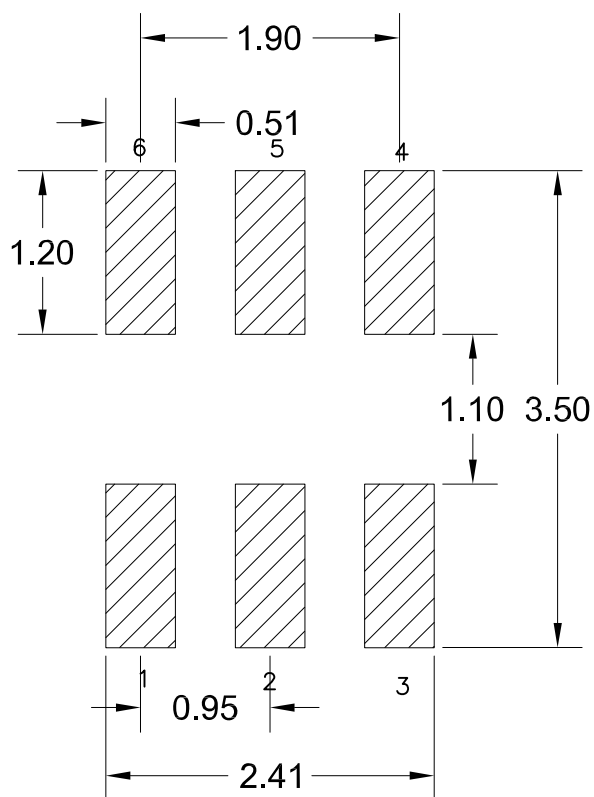


Table 13. SOT23-6L mechanical data

Dimensions			
Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.25
A1	0.02		0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33		0.41
b1	0.32	0.35	0.38
c	0.15		0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30		0.60
L1	0.60 REF		
α	0°		8°
Tolerance			
aaa	0.15		
bbb	0.20		
ccc	0.10		

Figure 40. SOT23-6L recommended footprint



12.2 SOT23-6L package information

Figure 41. SOT23-6L carrier tape outline

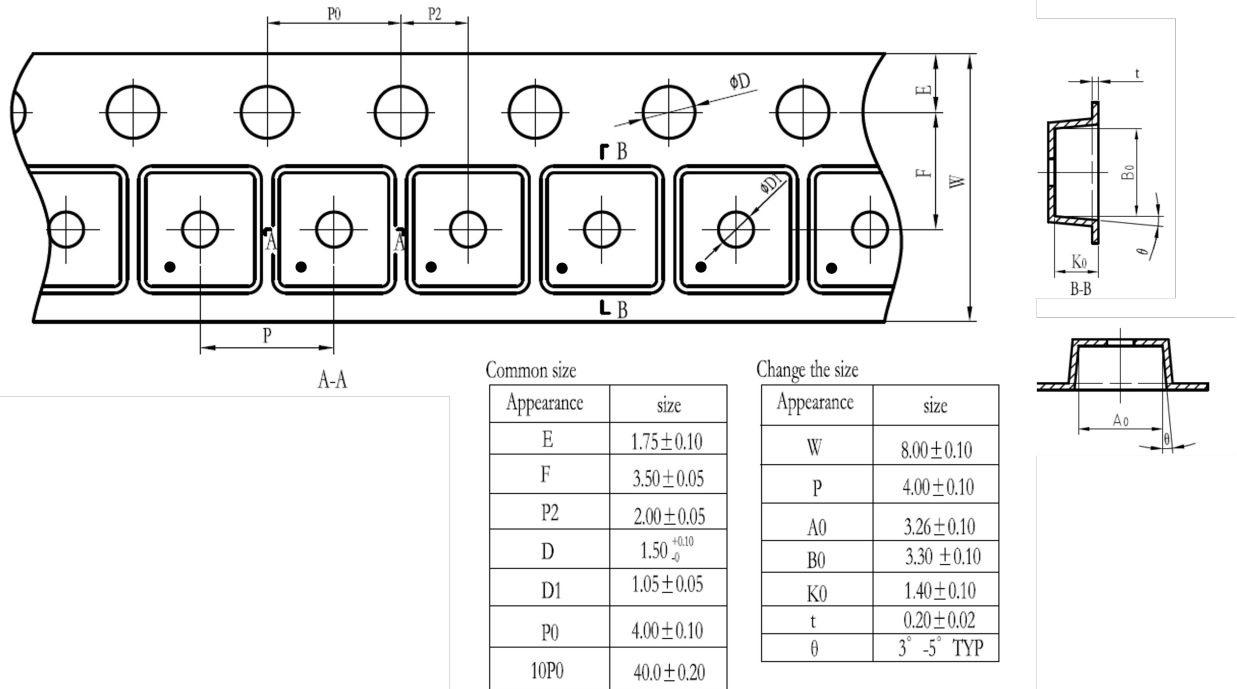
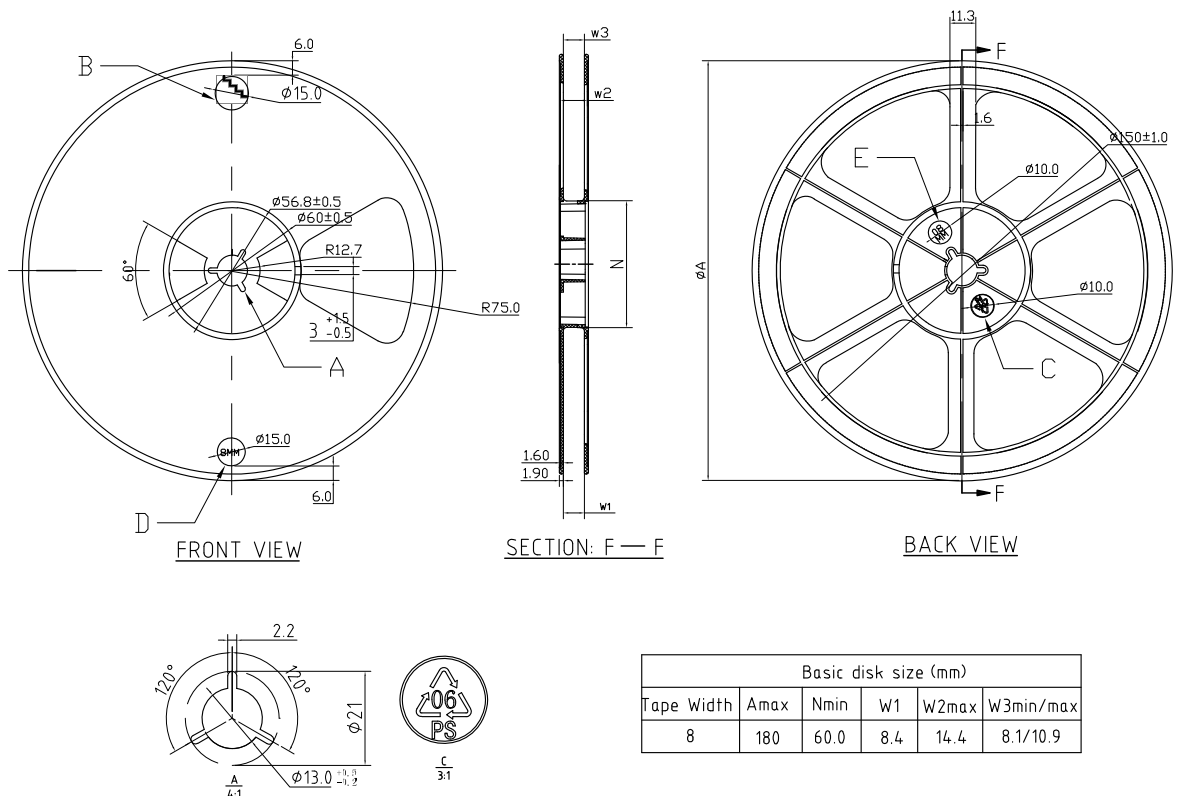


Figure 42. SOT23-6L reel outline



13 Ordering information

Table 14. Order codes

Order codes	Marking	Package	Packing
DCP3601IMR		SOT23-6L	Tape and reel

Revision history

Table 15. Document revision history

Date	Revision	Changes
13-Oct-2026	1	Initial release.

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