

Automotive 100 V, 10 W synchronous iso-buck converter for isolated applications



Maturity status link

[DCP10001IY](#)

Features

- AEC-Q100 Grade 1 qualified 
- Operating temperature range: -40 °C to 150 °C
- Designed for iso-buck topology
- 6 V to 100 V input voltage range
- Supports 36 V, 48 V, 60 V, 72 V electric battery packs
- Primary side regulation, no optocoupler required
- 1.5 A typical sink/source primary current capability
- Compliant with IPC-2221B requirements for clearance and creepage on both industrial and automotive versions
- Programmable switching frequency from 100 kHz to 1 MHz
- V²COT control mode architecture
- Fixed 3 ms internal soft-start timer
- Secondary-side short-circuit and overcurrent protection
- Overtemperature protection (OTP)

Applications

- Battery electric vehicle control supply
- EV GPS tracker
- Solar energy systems
- Industrial power supply
- Supply for GSM module

Description

The **DCP10001IY** is an automotive-grade synchronous monolithic converter specifically designed for the isolated buck topology (iso-buck).

The wide input voltage range (up to 100 V) makes the device suitable for a broad range of applications. The primary output voltage can be accurately adjusted, whereas the isolated secondary output is derived using a given transformer ratio. No optocoupler is required. The primary sink capability (typically up to 1.5 A) allows power delivery at the isolated output up to 10 W.

The **DCP10001IY** is based on a V²COT architecture that guarantees high load transient performance with a fixed switching frequency.

The **DCP10001IY** is available in HSOP8.

When the device is disabled, the consumption is 2 µA. As soon as the EN pin is pulled up, the device is enabled and the internal 3 ms soft-start takes place. Spread spectrum is set to reduce EMI. The device is provided with a full set of protections (overcurrent, short-circuit, and overtemperature protections) that ensure safe operation.

1 Pin configuration

Figure 1. Pin connection (top view)

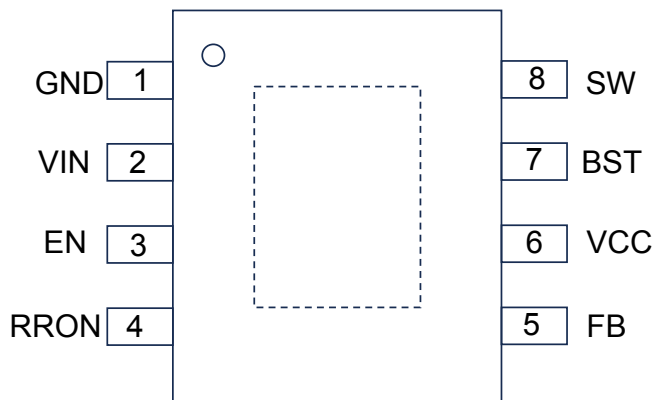


Table 1. Pin description

Pin #	Symbol	Function
1	GND	System ground. GND is the reference ground of the regulated output voltage. Therefore, care must be taken during PCB layout. Use wide PCB traces to make the connection.
2	VIN	Input voltage. VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
3	EN	Enable. Precision enable and undervoltage lockout (UVLO) programming pin. If the EN voltage is below 1.1 V, the converter is in shutdown mode with all functions disabled. If the EN voltage is above 1.1 V and below 1.5 V, the converter is in standby mode with the internal VCC regulator working, but without switching. If the EN voltage is above 1.5 V, the startup sequence begins.
4	RON	On-time programming. Connect an external resistor to program the switch-on time.
5	FB	Feedback. An external resistor divider from the output to GND tapped to FB sets the primary output voltage. It is recommended to place the resistor divider as close as possible to FB. Vias should be avoided on the FB traces.
6	VCC	Voltage bias. This pin supplies the embedded analog circuitry. Connect a ceramic capacitor ($\geq 1 \mu\text{F}$) to filter internal voltage reference.
7	BST	Bootstrap. Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
8	SW	Switch output. Connect SW to the primary winding of the transformer and to the bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.
-	EP	Exposed pad. No internal electrical connection. Connect the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

2 Typical application circuit

Figure 2. Typical application circuit

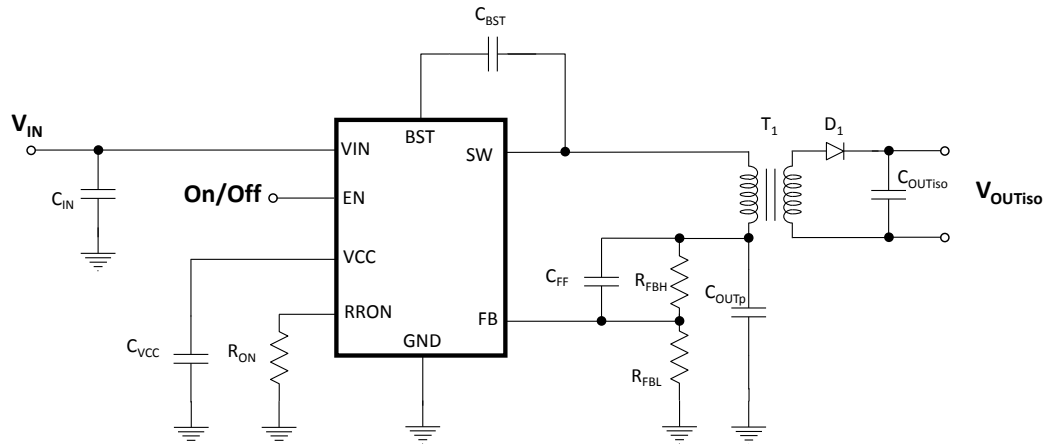


Table 2. Typical application components

Symbol	Description	Note
C_{IN}	Input capacitor	Normally 10 μ F, 100 V MLCC is enough
C_{VCC}	V_{CC} bypass capacitor	Recommended 1 μ F MLCC
C_{BST}	Bootstrap capacitor	Recommended 100 nF MLCC
C_{FF}	Feed Forward capacitor	To be placed if the loop requires it to achieve stability
C_{OUTp}	Primary output capacitor	Value and rated voltage dependent on the application conditions
C_{OUTiso}	Isolated output capacitor	Value and rated voltage dependent on the application conditions
R_{FBH}	V_{OUT} divider upper resistor	Value dependent on the application conditions
R_{FBL}	V_{OUT} divider lower resistor	Value dependent on the application conditions
R_{ON}	t_{ON} resistor	Value dependent on the application conditions
T1	Transformer	For transformer selection, see dedicated section
D1	Schottky diode	Max. reverse voltage should be carefully selected, depending on the input voltage, primary output voltage, isolated output voltage, and turn ratio.

3 Maximum ratings

3.1 Absolute maximum ratings

Stressing the device above the ratings listed in Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Input voltage	- 0.3	100	V
V_{EN}	Enable pin voltage	- 0.3	100	V
V_{FB}	Feedback pin voltage	- 0.3		V
V_{RON}	RON pin maximum voltage	-0.3	5.5	V
V_{CC}	Voltage bias pin	- 0.3	5.5	V
V_{SW}	DC voltage		100	V
V_{BST_GND}	BST to GND voltage	- 0.3	105.5	V
V_{BST_SW}	BST to SW voltage	- 0.3	5.5	V
T_{STG}	Storage temperature	-65	150	°C

3.2 ESD protection

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM non-corner pins	500	V
		CDM corner pins	750	

3.3 Thermal characteristics

Table 5. Thermal data

Symbol	HSOP8 Thermal resistance junction-ambient	Value	Unit
Rth JA	HSOP8 Thermal resistance junction-ambient	35	°C/W

3.4 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	6		100	V
V_{SW}	Switch node voltage range			100	V
$V_{EN/UVLO}$	Enable voltage range			100	V
C_{BST}	External BST to SW capacitance		100		nF

4 Electrical characteristics

V_{IN} = 6 V to 100 V, T_J = -40 °C to +150 °C, typical values are at T_J = 25 °C, V_{IN} = 24 V and V_{EN} = 2 V; unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{IN}	Operating input voltage		6		100	V
V _{IN-UVLO}	V _{IN} undervoltage lockout	Rising input voltage	5	5.55	5.7	V
		Falling input voltage	4.85			V
V _{EN-UVLO}	V _{EN} undervoltage lockout	Rising input voltage	1.1	1.2	1.3	V
		Falling input voltage	1	1.1	1.2	
V _{SD-UVLO}	V _{SD} undervoltage lockout	Rising input voltage			0.9	V
		Falling input voltage ⁽¹⁾	0.15			
I _{OFF}	Shutdown current	V _{EN} = GND		0.7	3	μA
R _{DS(ON)-H}	High-side MOSFET ON resistance	T _J = 25 °C		750		mΩ
R _{DS(ON)-L}	Low-side MOSFET ON resistance	T _J = 25 °C		300		mΩ
I _{LIM} ⁽²⁾	Peak current limit		1.3	1.5	1.75	A
I _{VY} ⁽²⁾	Valley current limit		1.05	1.3	1.5	A
I _{VY_SINK} ⁽²⁾	Reverse current limit		1.4	1.6	1.75	A
t _{ON_MIN}	Minimum on-time		150	220	300	ns
t _{ON_1}	On-time	V _{IN} = 24 V, R _{ON} = 20 kΩ	360	400	490	ns
t _{ON_2}	On-time	V _{IN} = 24 V, R _{ON} = 80 kΩ		1300		ns
t _{ON_3}	On-time	V _{IN} = 48V , R _{ON} = 20 kΩ		200		ns
t _{ON_4}	On-time	V _{IN} = 48 V, R _{ON} = 80 kΩ		820		ns
V _{BST}	Bootstrap voltage			2.8	3.5	V
V _{FB}	Feedback voltage	T _j = 25°C	0.792	0.8	0.808	V
			-1		+1	%
		T _J = -40 °C to 125 °C	0.788	0.8	0.812	V
			-1.5		+1.5	%
Soft-start						
t _{SS}	Internal soft-start timer		2.5	3.8	5.3	ms
Overvoltage protections						
V _{OVP}	Overvoltage trip (V _{OVP} /V _{REF})			120		%
V _{OVP_HYST}	Overvoltage hysteresis			6		%
Thermal shutdown						
T _{SHDWN}	Thermal shutdown temperature			175		°C
T _{Hys}	Thermal shutdown hysteresis			20		°C

1. *specified by design*
2. *Parameter tested in a static condition during the testing phase. The parameter value may change under a dynamic application condition.*

5 Datasheet parameters over the temperature range

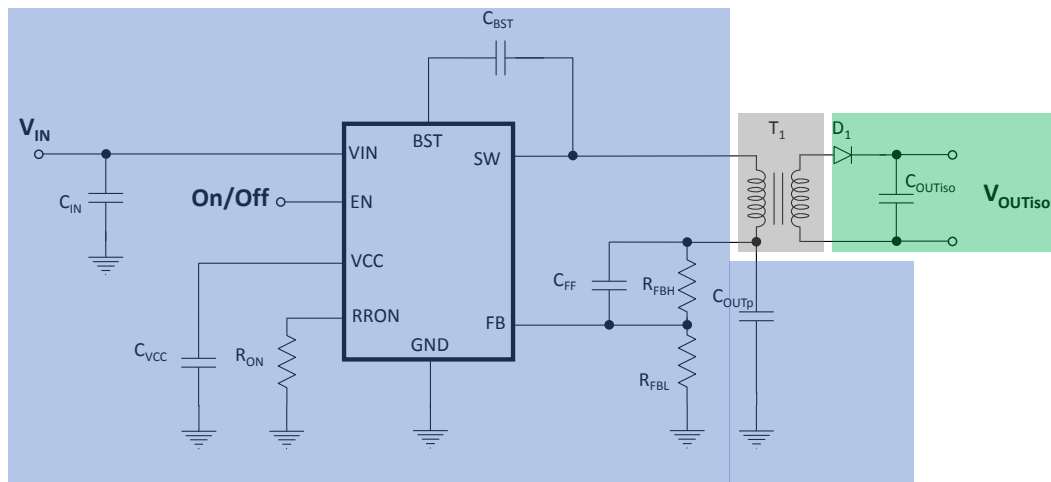
100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, +150 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C, +150 °C). Device operation is guaranteed when the junction temperature is within the temperature range (-40 °C, +150 °C). The designer can estimate the silicon temperature increase compared to the ambient temperature by evaluating the internal power losses generated during device operation. However, the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHDN} (+175 °C typ.) temperature. All the datasheet parameters can be guaranteed up to a maximum junction temperature of +150 °C, to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

6 Functional description

The iso-buck topology based on DCP10001IY consists of:

- Primary-side, the regulation loop of the V²COT architecture regulates the primary output voltage (in blue in the picture below)
- A two-windings transformer (in gray)
- The secondary side, which generates the isolated output voltage (in green) given the selected transformer ratio

Figure 3. Iso-buck general schematics



6.1 Power section

The DCP10001IY integrates N-channel power MOSFETs for synchronous operation. The high-side (HS) power MOSFET is optimized for rapid switching, while the low-side (LS) power MOSFET is designed with a low $R_{DS(ON)}$ to enhance conversion efficiency. Both MOSFETs are optimized to achieve high efficiency across the entire load range. The power stage is engineered to deliver a continuous output current of up to 1 A with a wide input voltage range of up to 100 V.

The HS MOSFET drain is internally connected to the VIN pin, while the LS MOSFET source is connected to the GND pin (power ground). The HS MOSFET source and LS MOSFET drain are connected to the SW pin (refer to the block diagram).

The DCP10001IY incorporates anti-shoot-through and adaptive deadtime control mechanisms to minimize low-side body diode conduction time, thereby reducing power losses. This feature is implemented by comparing the SW voltage with the HS and LS gate driving voltages. An anti-cross conduction system is also implemented to manage HS-LS gate stress.

The high-side MOSFET is effectively turned on using an integrated bootstrap network, requiring only an external capacitor between the BST and SW pins (100 nF typical). The bootstrap capacitor is recharged during the LS MOSFET on-time, with minimal impact on the maximum achievable duty cycle.

A minimum off-time (t_{OFF_min}) is implemented to ensure proper recharging of the BST capacitor.

The linear regulator sourced from VIN delivers a nominal output of 4.7 V at the VCC pin. This voltage supplies current to the gate drivers, internal circuit blocks, and logic components. To stabilize the linear regulator, it is recommended to incorporate a 1 μ F capacitor at the VCC pin.

6.1.1 Enable

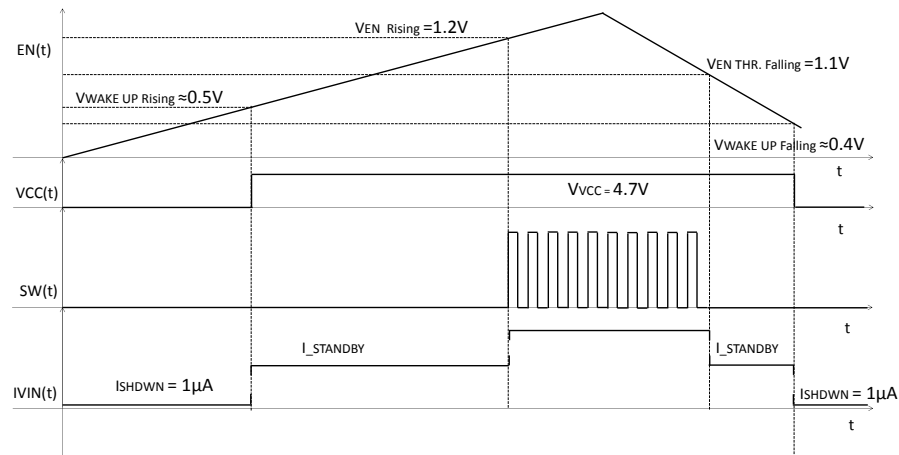
The EN pin is a digital input that turns the device on or off.

To maximize EN threshold accuracy and current consumption, the device implements two different thresholds:

- A wake-up threshold
- A start-up threshold

The following picture shows this behavior.

Figure 4. Enable power up/down



- If the voltage on the EN pin is below the $V_{SD-UVLO}$ falling, the internal circuitry is disabled to ensure very low power consumption in the off state ($I_{SHDWN} < 1\ \mu\text{A}$).
- Once the EN pin voltage exceeds the $V_{SD-UVLO}$ rising threshold, the device powers up the internal circuits, increasing current consumption.
- When the voltage surpasses the $V_{EN-UVLO}$ rising threshold, the device initiates switching activity as detailed in the Soft-start section (Section 6.1.2).

If the EN pin voltage drops below the $V_{EN-UVLO}$ falling threshold but remains above the $V_{SD-UVLO}$ falling threshold, the device halts switching activities while keeping internal blocks powered. Only when the voltage falls below the $V_{SD-UVLO}$ falling threshold does the device shut down internal circuits, reducing current consumption to the off-state level ($I_{SHDWN} < 1\ \mu\text{A}$).

The enable pin is VIN-compatible, allowing direct connection to the VIN pin if unused. A voltage divider can be designed on VIN to select the turn-on/off threshold for the start-up sequence. See Section 7.2 for more details.

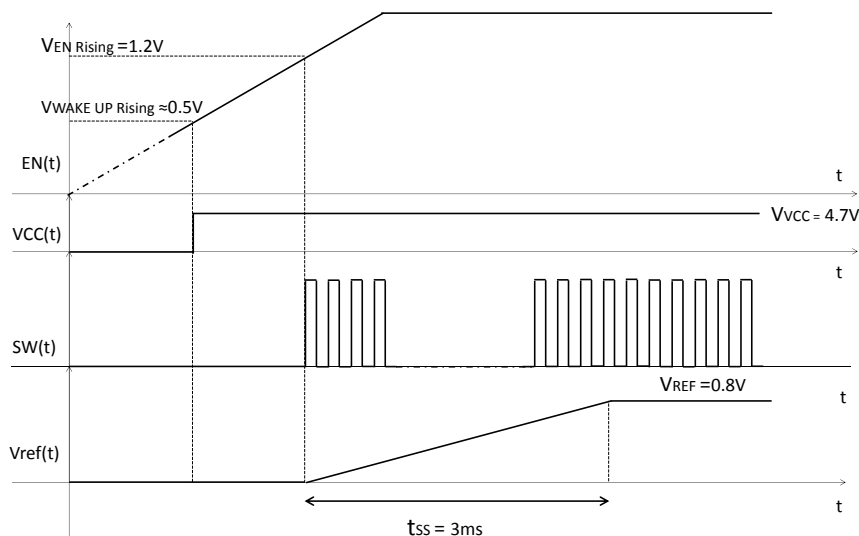
6.1.2 Soft-start

The device implements a soft-start phase, after a setup time delay of $3\ \mu\text{s}$, it ramps the FB pin to the internal reference with very small steps. This procedure minimizes the inrush current and decreases the stress of the power component at power up.

The soft-start ends when the FB pin voltage reaches the internal reference value of $0.8\ \text{V}$.

During the soft-start, a gradual limitation of the t_{ON} time is used to reduce initial V_{OUT} overvoltage (typical of a COT architecture). All available protections are enabled during this phase and OCP is limited on the very first part of the ramp ($< 100\ \text{mV}$) to avoid any inrush current.

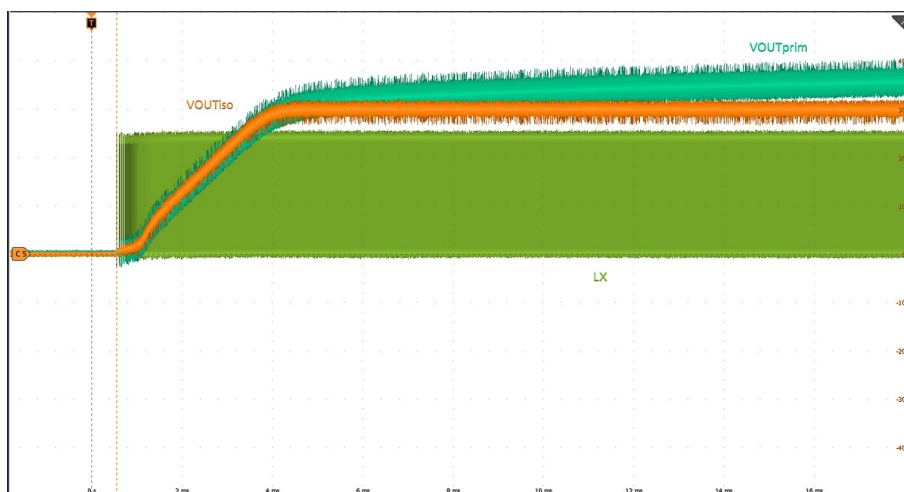
Figure 7 shows the soft-start procedure. Once the EN reaches the rising threshold, the switching activity starts and the error amplifier voltage increases linearly to the reference voltage.

Figure 5. Soft-start procedure


In case of an undesired event that may shut down the device during normal operation, the DCP10001IY can induce a new soft-start cycle to restore target working conditions. This takes place in case of:

1. Thermal shutdown event
2. UVLO event
3. EN pin rising over VEN threshold. Please refer to [Table 7](#).

The secondary output voltage tracks the primary output voltage rise, obviously with a different slope due to the turn ratio of the selected transformer.

Figure 6. Soft-start with primary and secondary output voltage rising up


6.1.3 Undervoltage lockout

If V_{IN} exceeds the V_{IN_UVLO} threshold, the internal blocks are turned on and a current charges the VCC capacitor. When V_{CC} exceeds V_{CC_UVLO} , the device is ready to turn on and is waiting only for the enable POR.

The device implements the undervoltage lockout (UVLO), continuously sensing the voltage on the VCC pin, if the UVLO lasts more than 10 μ s, the internal logic resets the device by turning off both LS and HS.

After the reset, if the EN pin is still high, the device repeats the soft-start procedure.

6.1.4 On-time generator

Considering that the DCP10001IY is based on a V²COT architecture, there is no clock generator, but an ON-time generator is embedded instead.

The ON-time can be programmed by connecting a resistor to the RON pin, as described later in [Section 9.2](#).

The ON-time circuitry is designed to generate a t_{ON} inversely proportional to the input voltage.

Consequently, the system works with a constant switching frequency even if V_{IN} variations occur.

The switching frequency should be in the range from 100 kHz to 1 MHz.

In the iso-buck, it is essential to extend the minimum on-time (t_{ON_min}) compared to a standard buck. The parameter t_{ON_min} can be found in the [Table 7](#).

Therefore, the selection of the on-time must comply with the following relation:

$$t_{ON} \geq t_{ON_MIN} \quad (1)$$

6.1.5 Dithering

To reduce the cost impact of the input filter for EMI reduction, the DCP10001IY implements the dithering function by default. This function is achieved by varying the t_{ON} time. The ramp current for the on-time generator is modulated within a specific percentage range of the nominal value according to a defined modulation pattern. As a result of t_{ON} variation, the switching frequency (f_{SW}) can fluctuate within a range of ± 5 kHz, with a modulation frequency of 9 kHz.

It is recommended to set the switching frequency in the middle of the 300-530 kHz range, where the CISPR25 EMI limits are more permissive.

6.2 Transformer

The transformer is the key component for the iso-buck, ensuring the desired isolation as well as allowing the energy transfer to the secondary side, hence generating the secondary isolated output voltage.

More details about the transformer selection are provided in the dedicated section (see [Section 10.2](#))

6.3 Secondary side

The secondary side includes an LC filter (secondary winding of the transformer and secondary output capacitor) and the rectifying element (Schottky diode).

6.4 Iso-buck operating principle

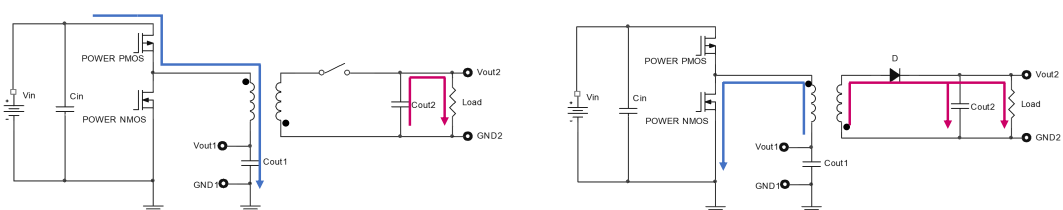
The diagram below describes the operation principle of the iso-buck converter.

When the high-side MOSFET is turned on, the current flows through the primary winding of the transformer and charges the primary output capacitor. Considering the dot convention of the transformer, the voltage at the anode of the Schottky diode is negative, hence the diode is reverse biased and no current flows in the secondary winding.

The load connected to the secondary output is supplied by COUT2.

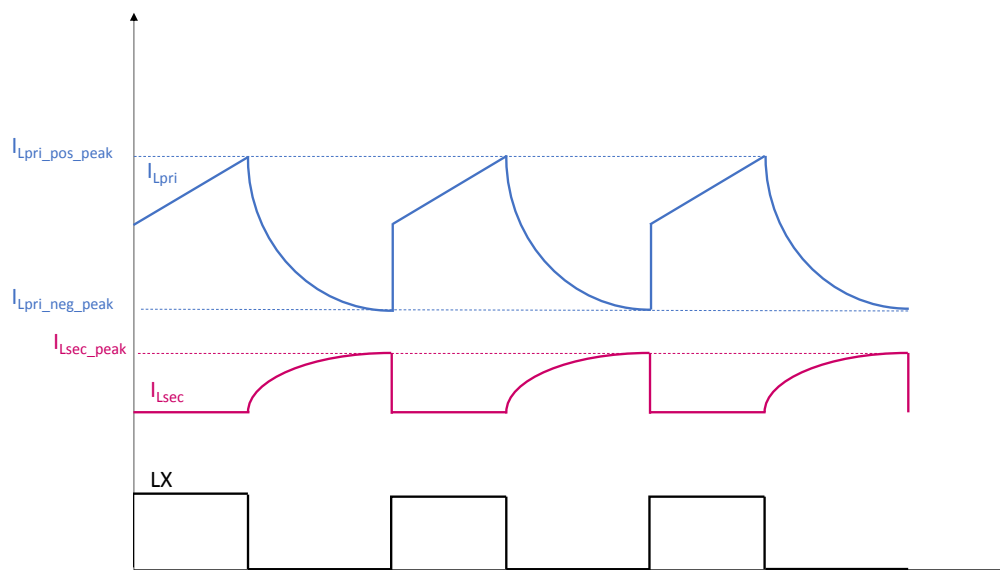
When the low-side MOSFET is turned on, the voltage applied at the transformer winding inverts its polarity. As a consequence, the Schottky diode is now forward biased and allows the current to flow from the secondary winding to COUT and the load. Under this condition, the energy transfer from primary to secondary side occurs.

Figure 7. Iso-buck basic operating principle



The waveforms in [Figure 15](#) reproduce the trend of the current in the two windings according to the switch node transitions.

Figure 8. Iso-buck primary and secondary current waveforms

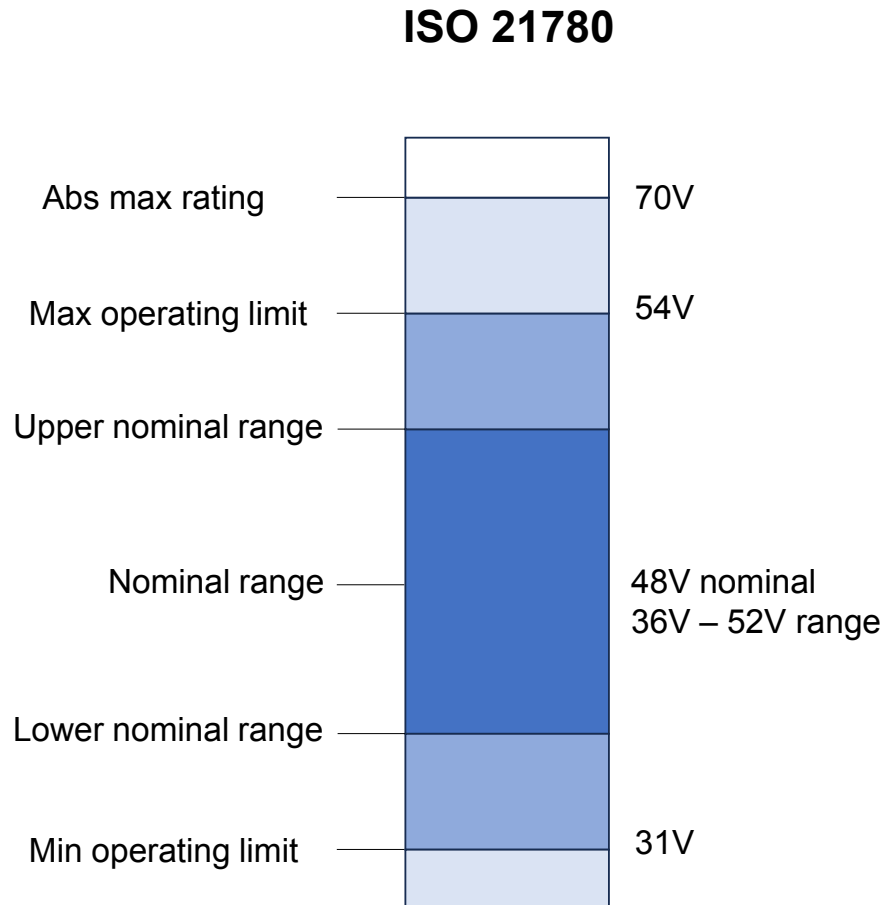


7 Isobuck performance

All results shown in this section come from measurements performed using the demoboard described in the dedicated section.

The input voltage range considered for these measurements assumes the maximum variation of the voltage when a 48V automotive battery is used, as depicted in the figure below (ISO 21780).

Figure 9. 48 V car battery voltage range according to ISO21780

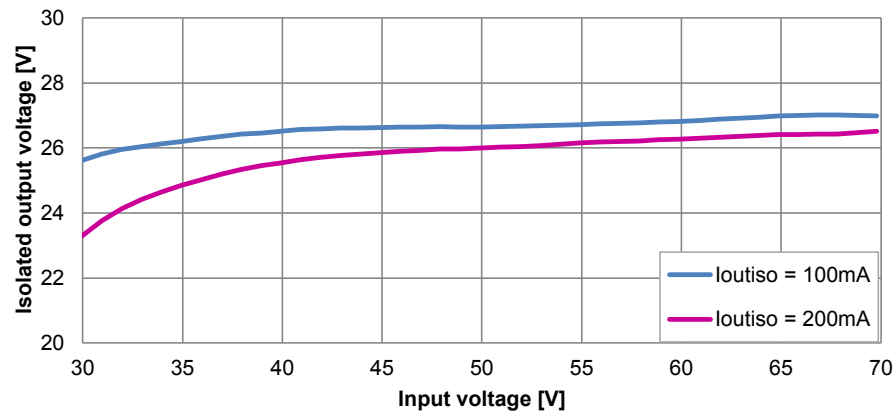


7.1 Secondary output line regulation

The secondary output line regulation is defined as the variation of the secondary output voltage due to the input voltage change at a specific current. The secondary output line regulation is mainly affected by the transformer and, in particular, by its leakage inductance.

Keeping the leakage inductance constant (that is, using the same transformer), a higher input voltage causes the isolated output voltage to slightly increase, as shown in [Figure 8.](#)

Figure 10. $V_{OUTprim} = 21\text{ V}$, $f_{SW} = 500\text{ kHz}$, transformer $N = 1.3$

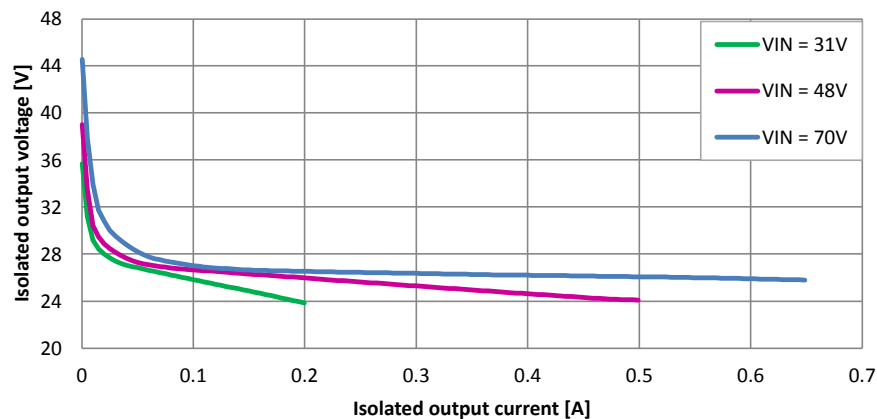


7.2 Secondary output load regulation

Since there is no regulation loop involving the secondary output, its load regulation depends, to some extent, on the primary load regulation and is affected by the leakage inductance of the transformer (see Figure 22), the voltage drops across the Schottky diode (diode forward voltage) and the DCR of the secondary coil, as indicated by Eq. (1) (where only the last two contributions are considered). Minimizing all the mentioned parameters leads to better load regulation.

As shown in Section 7.1, the input voltage also plays a role in the isolated output regulation, as depicted in Figure 11 and Figure 12.

Figure 11. Load regulation of the secondary isolated output, $f_{SW} = 500\text{ kHz}$, $V_{OUTprim} = 21\text{ V}$, transformer $N = 1.3$

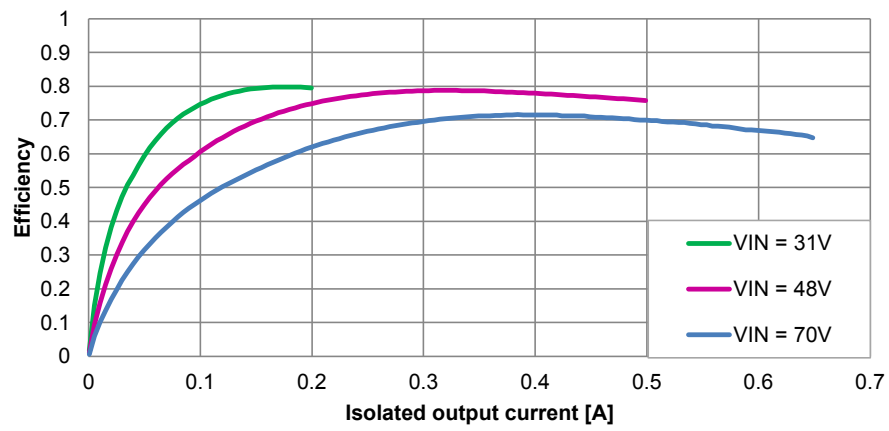


7.3 Efficiency

Figure 12 shows the efficiency referred to the secondary isolated output at different input voltages for two different application cases (different transformers and primary output voltage).

The effect of the input voltage on the efficiency is more evident at lower currents, especially for the application case of Figure 12.

Figure 12. Secondary output efficiency at different input voltages, $V_{OUTprim} = 21\text{ V}$, $f_{SW} = 500\text{ kHz}$, $N = 1.3$



8 Protections

The DCP10001IY implements a protection against overcurrent or short-circuit events of the secondary isolated output as well as a protection against an excessive increase of the temperature of the device (thermal shutdown).

8.1 Secondary output short-circuit protection

A short-circuit at the secondary isolated output normally causes a significant increase of both the positive and negative peaks of the primary winding current. This condition can be potentially dangerous for the device. A protection algorithm is therefore implemented to manage this event.

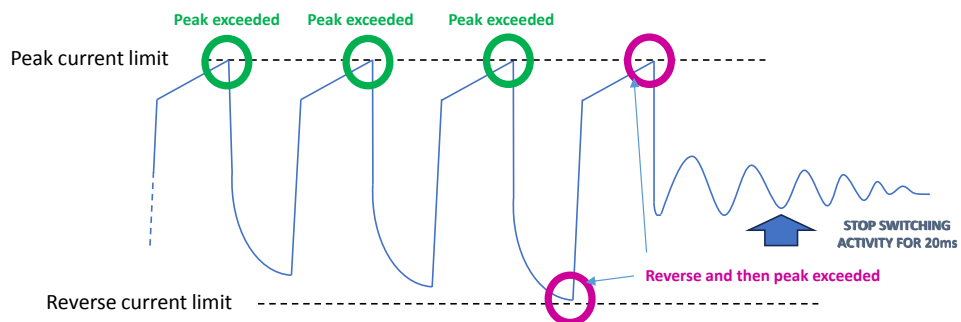
In case of short-circuit, the negative part of the primary current winding becomes more and more steep and get closer to the reverse current limit. Due to the short-circuit condition, also the positive peak rises until it exceeds the peak current limit threshold. Overcoming consecutively the reverse current limit threshold and then the peak current limit threshold is a clear indication that the isolated secondary output is in a short-circuit condition.

The device stops the switching activity for 20 ms. After that it re-starts implementing a new soft-start.

When the device re-starts, it normally discharges first the primary output capacitor. Especially in case of high regulated voltages at the primary output, the discharge of the output capacitor may give rise to very high currents. To avoid this potentially hazardous condition, an internal switch discharges the primary output within the 20 ms break. More details about this feature are provided in the dedicated section.

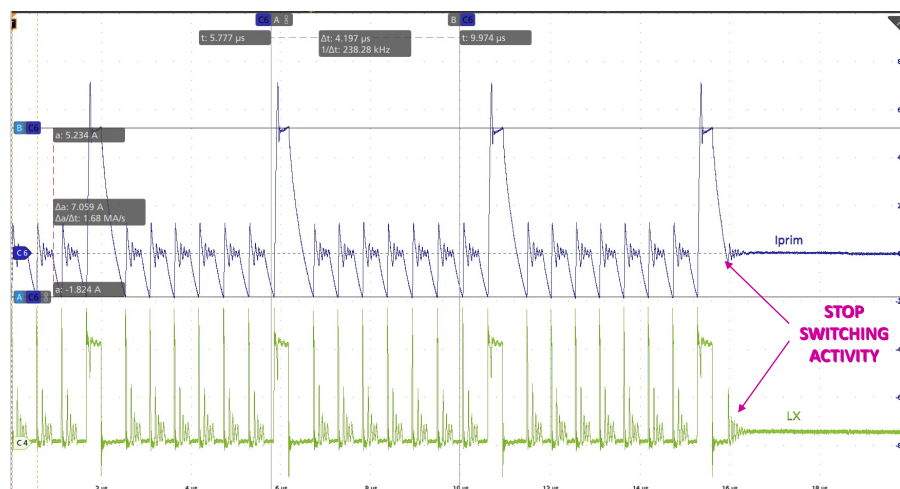
The Figure 13 depicts the implementation of the protection algorithm against short-circuits at the secondary output.

Figure 13. Implementation of the secondary output short-circuit protection



The Figure 12 shows the protection algorithm in a real case.

Figure 14. Short-circuit protection $V_{IN} = 48\text{ V}$, $V_{OUTprim} = 30\text{ V}$, $N = 1$



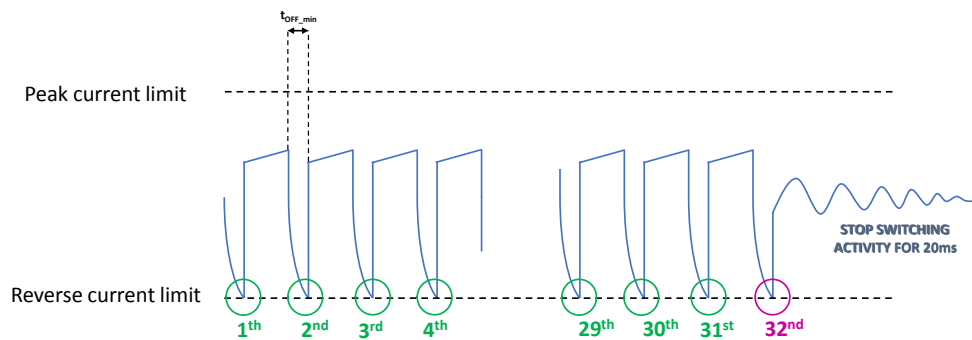
8.2 Secondary output overcurrent protection

The condition of overcurrent at the secondary output can be defined as a load that causes the primary winding current negative peak to exceed the reverse current limit threshold without triggering the peak current limit threshold. Since the condition of the short-circuit algorithm is not met in this case (only the reverse current limit is triggered), the device would continuously operate, exceeding the reverse current limit every cycle. The persistence of this conditions indicates a possible fault in the load.

Therefore, to prevent any damage for the load and the device, a further protection is provided.

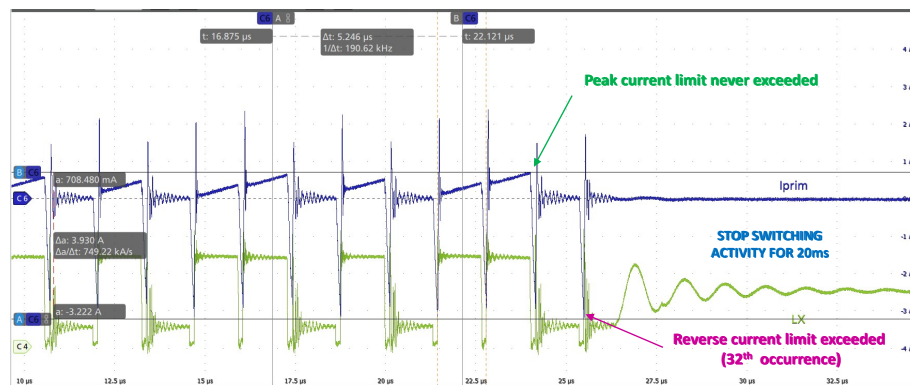
If the conditions “exceeding reverse current limit” and “off-time coincident with the t_{OFF_min} ” occur 32 times, the device reacts by stopping the switching activity for 20 ms. Then the device re-starts in the same way explained in the previous section. Before the device re-starts, the primary output capacitance is discharged by the embedded switch.

Figure 15. Implementation of the secondary output overcurrent protection



The effect of this protection on a real application is shown in Figure 14

Figure 16. Overcurrent protection, $V_{IN} = 48\text{ V}$, $V_{OUT_{prim}} = 30\text{ V}$, $N = 1$, $I_{OUT_{iso}} = 500\text{ mA}$



8.2.1 Current peaks estimate

Both protections described in the previous sections rely on exceeding the current peaks in the primary winding. A correct estimate of the current peaks is therefore necessary.

The positive and negative current peaks in the primary winding can be estimated using the following equations:

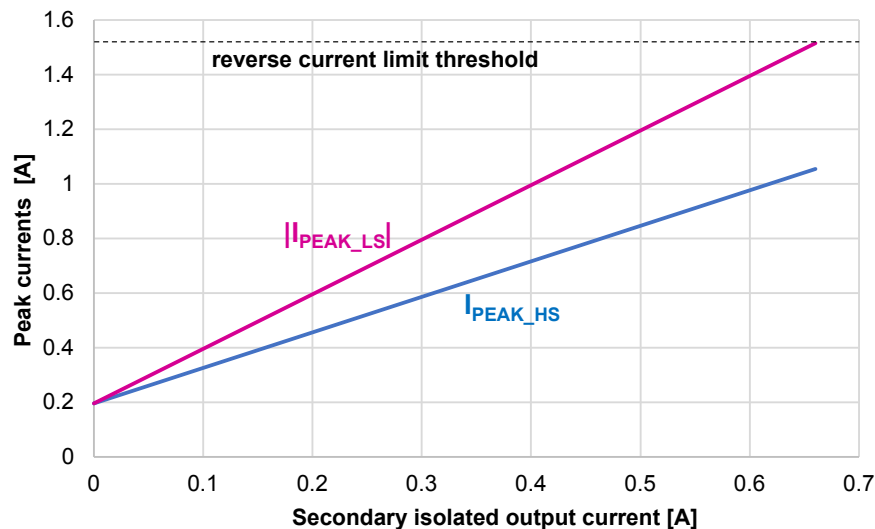
$$I_{PEAK_{HS}} = N \cdot I_{OUT_sec} + \frac{\Delta I_L}{2} \quad (2)$$

$$I_{PEAK_{LS}} = -N \cdot I_{OUT_sec} \left(\frac{2 \cdot D}{1 - D} \right) - \frac{\Delta I_L}{2} \quad (3)$$

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \cdot V_{IN}}{V_{OUT} \cdot f_{SW} \cdot L_m} \quad (4)$$

Eq. (3) and Eq. (4) are useful to determine the maximum current deliverable to the load. The Figure 15 shows how the current peaks (positive and negative) vary with the isolated output current in two different application conditions and the maximum value, defined by the reverse current limit threshold.

Figure 17. Current peaks in HS e LS MOSFETs depending on the isolated output current $V_{IN} = 48\text{ V}$, $V_{OUT_{prim}} = 21\text{ V}$, $f_{SW} = 500\text{ kHz}$



8.3 Thermal shutdown

The shutdown circuitry disables the switching activity if the junction temperature is higher than $175\text{ }^{\circ}\text{C}$ (T_{SHDWN} , refer to Section 4). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately $20\text{ }^{\circ}\text{C}$ prevents the device from turning ON and OFF too fast. After a thermal protection event has expired, the DCP10001IY restarts with a new soft-start. OTP is a not latching protection.

When the device stops the switching activity due to the thermal shutdown, an internal pull-down resistor discharges the primary output capacitance, just like after triggering the protections described in the Section 8.1 and Section 8.2.

8.4 Embedded discharge switch

As already mentioned in the previous sections, a 20 ms break of the switching activity occurs when:

- The event "exceeding the reverse current limit" is followed by the event "exceeding the peak current limit"
- The events "exceeding the reverse current limit" and "off-time coincident with the t_{OFF_min} " occur at least 32 times
- A thermal shutdown event occurs

After this break, the device re-starts. Prior to the soft-start, the primary output capacitance should be discharged. In 20ms the natural discharge of the capacitor is very limited. According to the voltage present at the primary output capacitance, the charge to dissipate can be very high and the current generated by the discharge, flowing through the low-side MOSFET, can be very high. To prevent the low-side MOSFET from being damaged by this current, an internal discharge switch has been embedded. This switch acts like a current sink. It starts drawing current at the beginning of the 20 ms break of the switching activity, discharging the primary output capacitance very rapidly.

Figure 16 shows that, even with 30 V across the primary output capacitance, the complete discharge occurs in less than 5 ms.

Figure 18. Effect of the embedded discharge switch

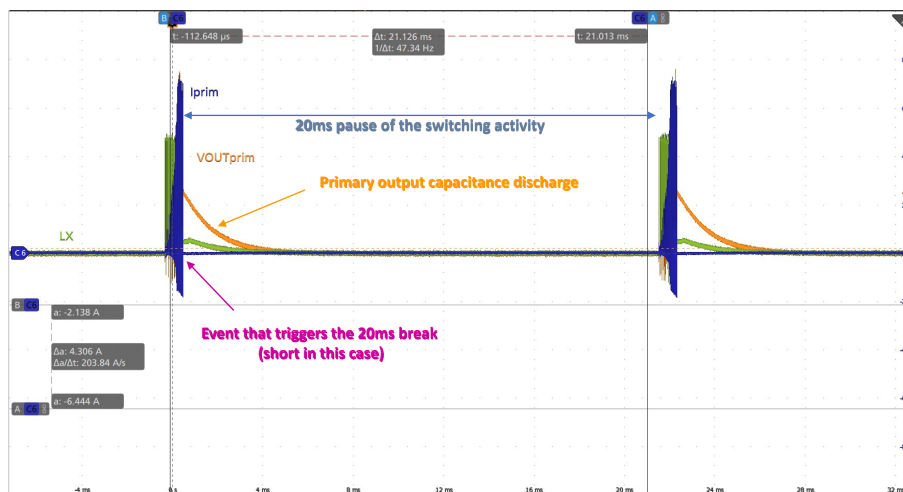
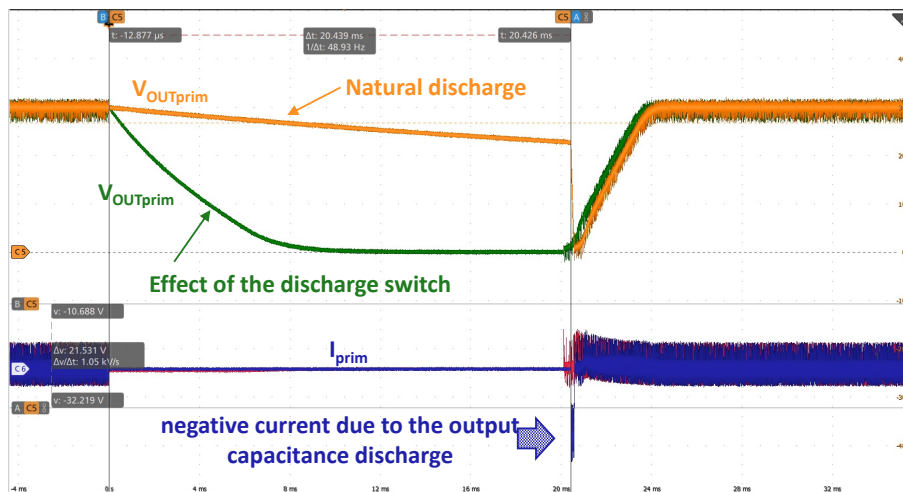


Figure 17 compares the effect of the discharge switch with the natural discharge of the primary output capacitance in case the internal discharge switch were not embedded.

The natural discharge in 20 ms would lower the voltage across the output capacitance down to 24 V (starting from 30 V in this example). The charge associated with this voltage causes a negative current peak at the re-start. The discharge switch brings the voltage across the primary output capacitance to zero quickly, so that no negative current peak is observed at the re-start.

Figure 19. Comparison between primary output capacitance voltage and primary winding current with and without the internal discharge switch



9 Application notes

9.1 Isolated output voltage adjustment

In the iso-buck converter, the secondary isolated output voltage is not included in the regulation loop. Nevertheless, a good regulation of the secondary output voltage is achieved by relying on the primary output voltage regulation, and the selection of a proper turn ratio of the transformer. Other influencing parameters are the voltage drops due to the secondary winding resistance and the Schottky diode, as well as the leakage inductance of the transformer.

This is summarized by the following equation:

$$V_{OUT_sec} = N \cdot V_{OUT_prim} \cdot \frac{L_m}{L_m + L_{LEAK}} - R_{wind_sec} \cdot I_{OUT_sec} - V_{FD1} \quad (5)$$

Where V_{OUT_prim} is the primary output voltage defined by the following equation:

$$V_{OUT_prim} = 0.8 \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \quad (6)$$

In Eq. (6), the 0.8 V represents the error amplifier reference voltage, whereas R_{FB1} and R_{FB2} are respectively the upper and lower resistor of the output divider.

A general recommendation for defining the V_{OUT_prim} is to keep the duty cycle below 70%. A higher duty cycle would limit off-time, limiting the time in which the energy transfer to the secondary side takes place.

Another restriction in the duty cycle selection derives from the minimum on-time (t_{ON_MIN}). Even though the DCP10001IY is based on a V^2COT loop, the frequency can be assumed almost constant and the minimum duty cycle can be defined as:

$$D \geq D_{MIN} = t_{ON_MIN} \cdot f_{SW} \quad (7)$$

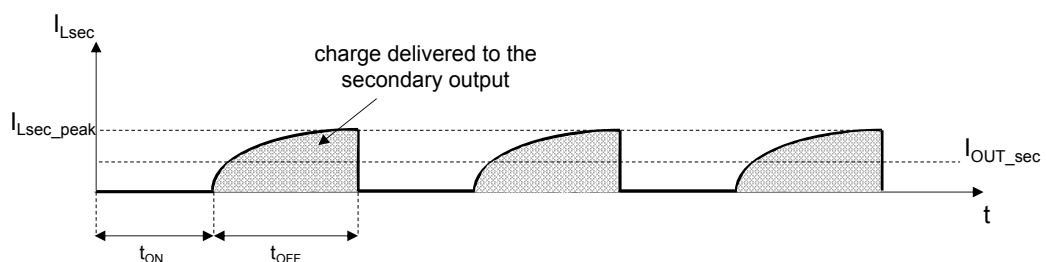
In Eq. (6), the other parameters can be described as:

- N is the turn ratio
- V_{FD1} is the forward voltage of the Schottky diode
- L_m is the magnetizing inductance of the transformer
- L_{LEAK} is the leakage inductance of the transformer.

Eq. (6) emphasizes how the selection of the transformer and, to some extent, the Schottky diode, play a crucial role in the accurate regulation of the secondary output voltage.

Another factor affecting the secondary output voltage regulation is the leakage inductance of the transformer. As described later, the leakage inductance determines the peak of the secondary winding current. This current peak defines the maximum current from the secondary isolated output by limiting the amount of charge delivered to the output. When the current demand from the secondary isolated output exceeds the maximum deliverable charge (limited by the peak current), the isolated output voltage drops

Figure 20. Secondary output current typical waveform



The effect of the leakage on the load regulation has already been shown in [Figure 22](#).

To some extent, the duty cycle can also affect the secondary output voltage. Since the energy transfer from primary to secondary occurs only during the t_{OFF} , a duty cycle that is too high could reduce the achievable peak current, hence limiting the deliverable current to the secondary output. Under this condition, the secondary output could drop.

9.2 On-time and switching frequency

Place a resistor between the RON pin to GND to select the on-time of the device, following [Eq. \(1\)](#).

$$t_{ON}(\mu s) = \frac{R_{ON}(k\Omega)}{2 \cdot V_{INPL}(V)} \quad (8)$$

$$R_{ON}(k\Omega) = V_{OUTprim}(V) \cdot \frac{2000}{f_{SW}(kHz)} \quad (9)$$

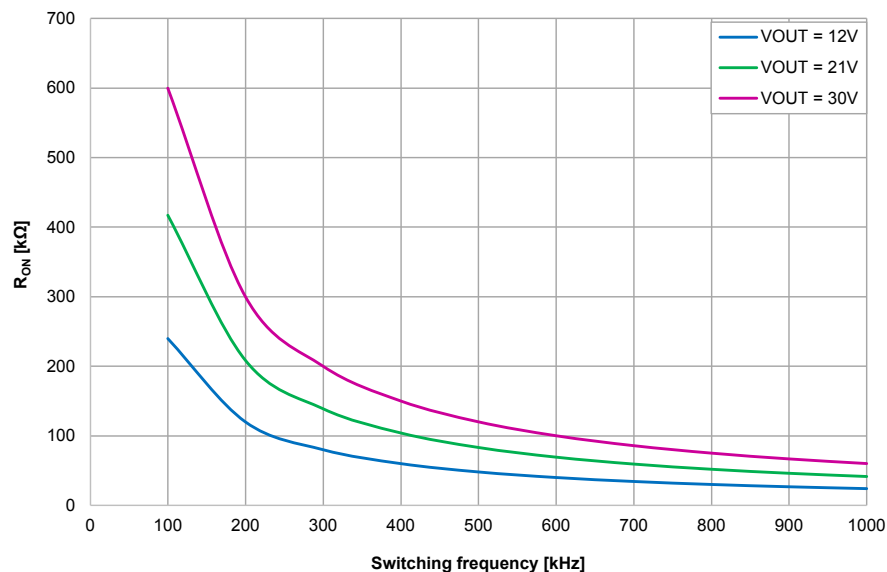
The relationship between the RON and the switching frequency is graphically depicted in [Figure 19](#).

The switching frequency should be in the range from 100 kHz to 1 MHz.

The selection of the ON-time should match the restriction shown by the equation (1) reported again below:

$$t_{ON} \geq t_{ON_MIN} \quad (10)$$

Figure 21. Switching frequency vs RON resistance

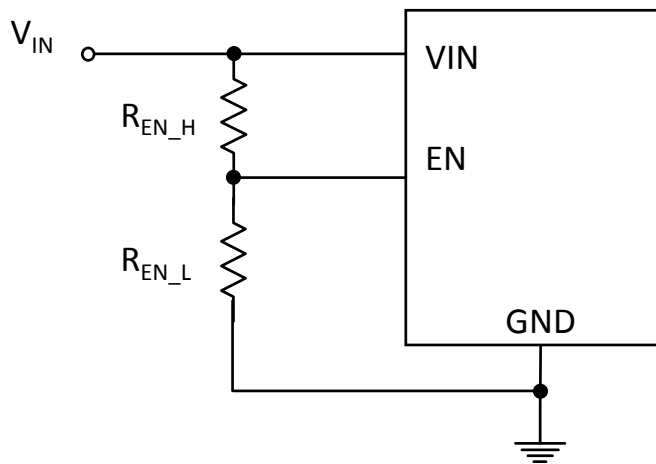


9.3 Enable resistor divider

The DCP10001IY EN pin is designed with two enable threshold levels (see [Section 6.1.1](#)).

The enable thresholds are characterized by 200 mV hysteresis to guarantee a good noise immunity and a programmable start up.

The VIN start-up can be easily programmed connecting a voltage divider to the EN pin between VIN pin and GND as shown in [Figure 21. Switching frequency vs RON resistance](#).

Figure 22. Connection of the enable resistor divider


The enable rising threshold is equal to 1.2 V. (refer to [Section 4](#)).

The power-up threshold is adjusted according to the formula reported in Eq. (11) :

$$V_{\text{POWER_UP}} = 1.2 \cdot \left(1 + \frac{R_{\text{EN_H}}}{R_{\text{EN_L}}} \right) \quad (11)$$

The enable falling threshold is equal to 1.1 V (refer to [Section 4](#)).

The turn-off threshold is obtained according to the formula reported in Eq. (12) :

$$V_{\text{POWER_DOWN}} = 1.1 \cdot \left(1 + \frac{R_{\text{EN_H}}}{R_{\text{EN_L}}} \right) \quad (12)$$

If EN pin is not used, it can be connected directly to the VIN pin. In this case, the device will start-up/switch off once V_{IN} reaches/falls below the $V_{\text{IN-UVLO}}$.

To maximize the overall system efficiency, it is suggested to use $R_{\text{EN_H}}$ and $R_{\text{EN_L}}$ between 10 kΩ and 1 MΩ.

10 Design of the external components

10.1 Input capacitor selection

The input capacitor, just like in a standard buck, should limit the input voltage ripple. Key parameters of the input capacitor are, together with its value, the maximum operating voltage and the RMS current capability.

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity, a pulsed current flows into the input capacitor and so its RMS current capability must be selected according to the application conditions. Internal losses of the input filter depends on the ESR value, so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, a lower ESR input filter has lower losses and thus contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$I_{RMS} = \left(\frac{I_{OUT_sec}}{N} \right) \cdot \sqrt{\left(1 - \frac{D}{\eta} \right) \cdot \frac{D}{\eta}} \quad (12)$$

In the ideal case of efficiency $\eta=1$, the RMS current reaches its maximum value when $D = 0.5$.

In general, the maximum and minimum duty cycles can be calculated as:

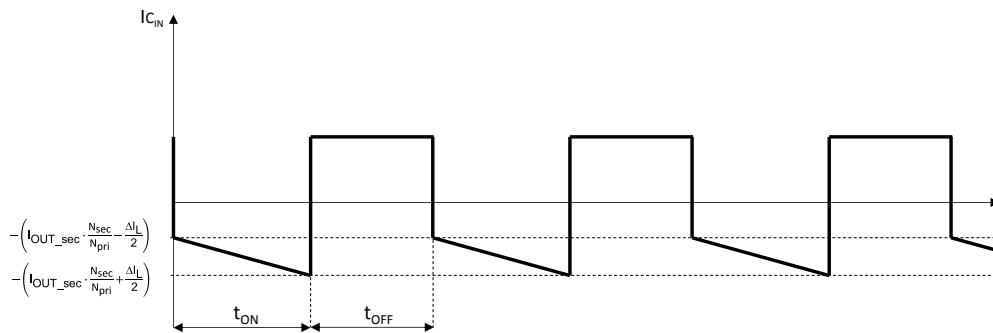
$$D_{MAX} = \frac{V_{OUT_pri} + \Delta V_{LS}}{V_{INmin} + \Delta V_{LS} - \Delta V_{HS}} \quad (13)$$

$$D_{MIN} = \frac{V_{OUT_pri} + \Delta V_{LS}}{V_{INmax} + \Delta V_{LS} - \Delta V_{HS}} \quad (14)$$

Where ΔV_{HS} and ΔV_{LS} are the voltage drop across the high-side and low-side MOSFET respectively.

The AC component of the input current (see Figure 20) flows in the input capacitor, generating the input voltage ripple.

Figure 23. Input capacitor AC current



The peak-to-peak voltage across the input capacitor can be calculated as follows:

$$V_{PP} = \left(\frac{I_{OUT_sec} \cdot \frac{N_{sec}}{N_{pri}}}{C_{IN} \cdot f_{SW}} \right) \cdot \frac{D}{\eta} \cdot \left(1 - \frac{D}{\eta} \right) + ESR \cdot \left(I_{OUT_sec} + \frac{\Delta I_L}{2} \right) \quad (15)$$

In case of negligible ESR (e.g. in case of MLCC capacitors), Eq. (15) can be simplified. The value of the input capacitor can thus be derived:

$$C_{IN} = \frac{I_{OUT_sec} \cdot \frac{N_{sec}}{N_{pri}} \cdot D}{V_{PP} \cdot f_{SW}} \cdot \left(1 - \frac{D}{\eta}\right) \quad (16)$$

Considering the ideal case of $\eta = 1$, the equation above reaches its maximum value when $D = 0.5$. Therefore, the minimum input capacitance value can be defined as follows:

$$C_{IN} \geq C_{INmin} = \frac{I_{OUT_sec} \cdot \frac{N_{sec}}{N_{pri}}}{4 \cdot V_{PP} \cdot f_{SW}} \quad (17)$$

Typically, C_{IN} is dimensioned to keep the maximum peak-to-peak voltage across the input filter in the order of 5 % of V_{INmax} .

10.2 Transformer selection

The transformer has two essential tasks:

- Providing isolation between the primary and secondary side in accordance with the application requirements
- Generating the necessary secondary output voltage from the regulated primary voltage with the most suitable turn ratio

The transformer selection implies defining the following parameters:

- Isolation voltage
- Turn ratio
- Primary inductance
- Peak and RMS currents
- Windings resistance
- Leakage inductance
- Parasitic capacitances

Isolation voltage

The isolation of the transformer in terms of voltage capability (1.5 kV, 4 kV, and so on) and type (functional basic, reinforced, etc.) is mainly driven by the application. Both parameters normally affect the size of the transformer as well as other electrical characteristics (e.g. winding resistance, leakage inductance, etc.).

Turn ratio

Naming the number of turns of the primary and secondary windings N_{prim} and N_{sec} respectively, the turn ratio is defined as:

$$N = \frac{N_{sec}}{N_{prim}} \quad (18)$$

Considering Eq. (18), the turn ratio must be defined so that the voltage at the secondary output is the desired one over the whole secondary output current range:

$$N \geq \frac{V_{OUT_sec} + R_{wind_sec} \cdot I_{OUT_sec} + V_{FD1}}{V_{OUT_pri}} \quad (19)$$

If no current is drawn from the primary output, the turn ratio should only be chosen to compensate the drops due to the secondary winding resistance and the Schottky diode.

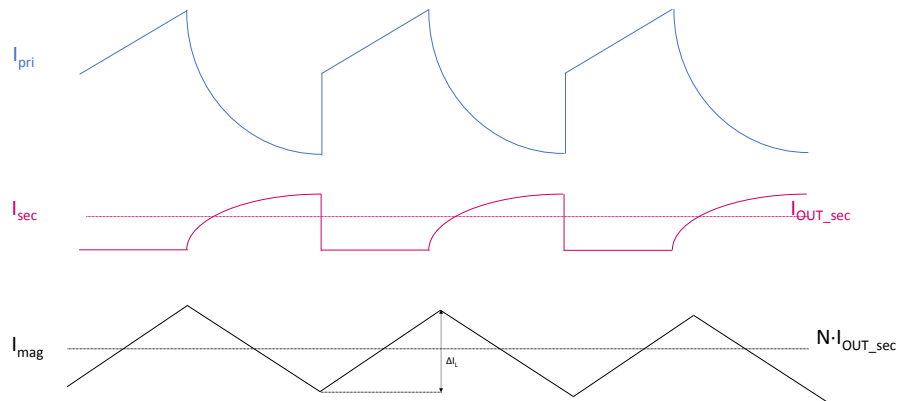
The effect of the leakage inductance on the secondary output voltage regulation (not included in the equation above) should also be taken into account. Figure 16 clearly shows how the secondary output voltage can drift due to the leakage inductance.

Primary inductance

The choice of the primary inductance does not differ much from a standard buck. The magnetizing current (see Figure 24), which combines the two winding currents, has the same shape of the buck inductor current and can be defined as:

$$I_{\text{mag}} = N \cdot I_{\text{sec}} \quad (20)$$

Figure 24. Primary winding current (blue), secondary winding current (magenta) and magnetizing current (black)



Therefore, setting the current ripple ΔI_L , the inductance is defined as:

$$L_{\text{pri}} = \frac{(V_{\text{IN}} - V_{\text{OUT_prim}}) \cdot V_{\text{OUT_prim}}}{V_{\text{IN}} \cdot f_{\text{SW}} \cdot \Delta I_L} \quad (21)$$

As example, assuming $I_{\text{OUT_sec}} = 100 \text{ mA}$, $N = 6$, the current ripple can be set around 30% of the total current $N \times I_{\text{OUT_sec}} = 0.6 \text{ A}$, therefore 180 mA. If $V_{\text{IN}} = 12 \text{ V}$, $V_{\text{OUT_prim}} = 5 \text{ V}$ and $f_{\text{SW}} = 400 \text{ kHz}$, the inductor value should be 40 μH .

Peak and RMS current

As with any inductor, the peak and RMS current for each winding must be calculated in order to define saturation and RMS currents that the transformer should fulfill.

For the primary winding, the equations below apply:

$$I_{\text{pri_pos_peak}} = \frac{I_{\text{OUT_sec}}}{N} + \frac{\Delta I_L}{2} \quad (22)$$

$$I_{\text{pri_RMS}} = \frac{I_{\text{OUT_sec}}}{N} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L \cdot N}{I_{\text{OUT_sec}}} \right)} \quad (23)$$

For the secondary winding, the peak current can change depending on the leakage inductance. In the picture below, secondary winding current waveforms with different leakage inductances are simulated. It is evident that the peak current can vary significantly. Considering the target leakage inductance value for an iso-buck (recommended up to 1% of the primary inductance), the waveform can be approximated with a sawtooth shape and the peak and RMS currents can hence be estimated as:

$$I_{\text{sec_pos_peak}} = \frac{2 \cdot I_{\text{OUT_sec}}}{1 - D} \quad (24)$$

$$I_{\text{sec_RMS}} = I_{\text{sec_pos_peak}} \sqrt{\frac{1-D}{3}} \quad (25)$$

Eq. (24) gives an indication of the peak value. Nevertheless, the waveform can significantly change with the leakage. Therefore, the measured peak value can differ from the one provided by this equation.

A duty cycle higher than 50-60% significantly increases the peak current in the secondary winding, hence affecting the negative peak current at the primary side.

Windings resistance

Winding resistances should be minimized as much as possible since they affect the secondary output load regulations.

They also contribute to power losses, hence affecting the efficiency of the whole solution.

Leakage inductance

The leakage inductance of a transformer can be defined as an undesired inductive component due to the imperfect magnetic linking of the two windings. Leakage inductance is inherent to the transformer construction and can be only reduced but not eliminated. The typical recommendation is to keep the leakage inductance below 1% of the magnetizing inductance.

The leakage inductance affects the shape of the secondary winding current as well as the negative part of the primary winding current (which is affected by the reflected current from the secondary side). In general, a very low leakage inductance implies that the current in the secondary winding can quickly ramp up, allowing the charge of the secondary output capacitor and supporting the load current demand.

A high leakage inductance slows down the secondary winding current rise, limiting the charge delivery to the output. Comparing solutions with different values of transformer leakage inductance shows that higher leakage inductance transformers are characterized by poorer load regulation performances. On the other hand, the leakage inductance determines the slope of the rising edge of current in the primary winding (the lower the leakage, the steeper the slope) and the peak value it could reach. Therefore, under certain conditions (e.g. short-circuit at the secondary side) this peak can be significantly high.

A higher value of the leakage can help in these cases, jeopardizing however the load regulation performance. A similar effect can also be achieved by increasing the resistance of the secondary winding, keeping the optimized value of the inductance. In both cases, it is also possible to adjust the N value to improve the load regulation. Both higher leakage and higher secondary winding resistance have a slight negative impact on the efficiency.

Figure 25. Effect of the leakage inductance on the primary winding current

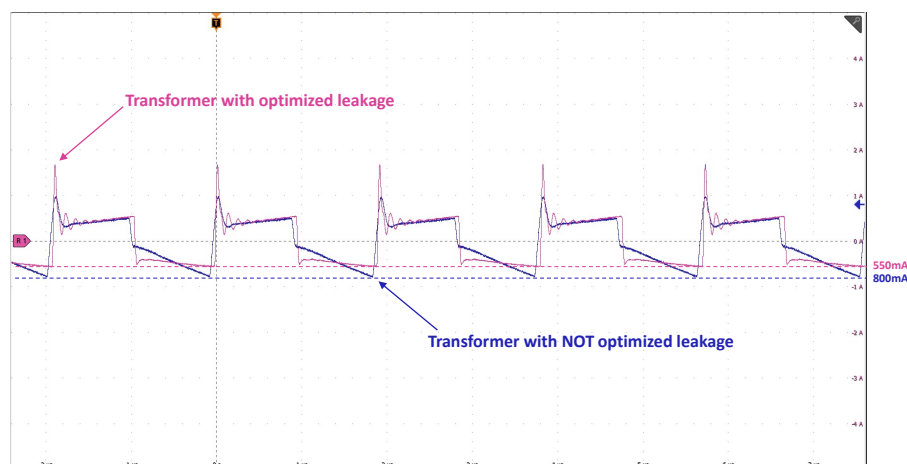
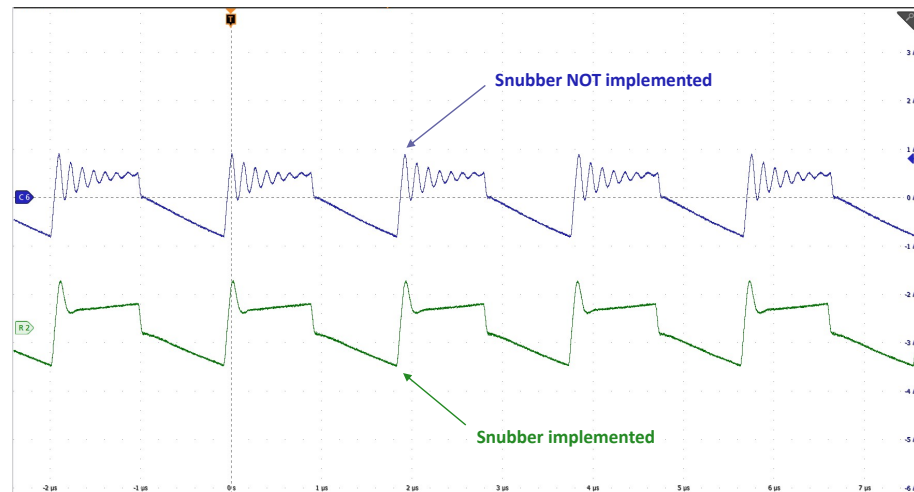


Figure 25 shows the effect of the leakage inductance looking at the primary winding current. A transformer with an optimal leakage inductance (between 0.5 and 1% of the magnetizing inductance) is compared with a transformer with suboptimal leakage inductance (slightly above 2%). The main effect that can be observed is in the negative part of the waveform. A less optimized leakage causes the negative peak to reach a higher value (absolute value) and reduces the margin from the reverse current limit. This implies less power deliverable to the isolated output.

Another effect of the leakage inductance is the ringing observed when the transition from the off-phase to the on-phase occurs. These oscillations are due to the LC circuit represented by the leakage inductance and the total parasitic capacitance observed by the primary winding. This capacitance consists of several contributing factors:

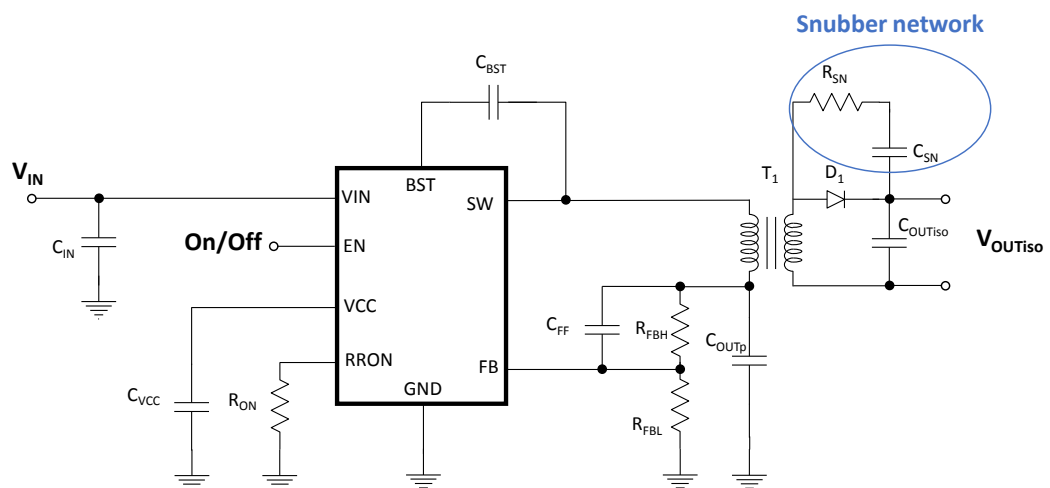
- Primary winding capacitance
- Secondary winding capacitance, reflected to the primary side
- Reverse capacitance of the Schottky diode, reflected to the primary side

Figure 26. Filtering effect of the snubber network



A proper masking time ($t_{ON\ MIN}$) filters these oscillations, so that in case of extreme oscillations, erroneous current limit exceeding can be avoided. Nevertheless, a RC snubber circuit (depicted in Figure 27) to dump this ringing is always recommended.

Figure 27. RC snubber network

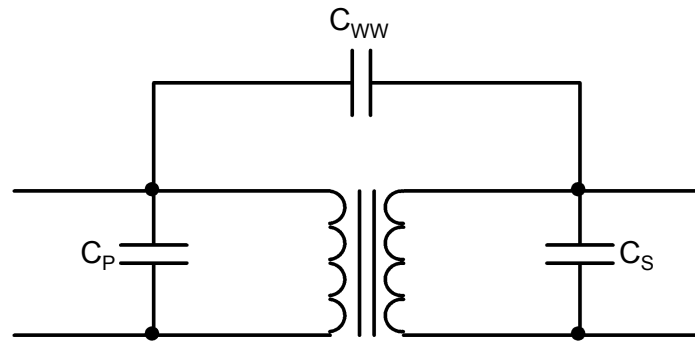


Capacitance

The parasitic capacitance of a real transformer mainly consists of the following contributions:

- Capacitance across each winding (C_P and C_S , in the picture below) due to the capacitive coupling between the coil and the core. As already mentioned, the winding capacitances are involved in the ringing observed during transition from off to on phase of the primary side
- Interwinding capacitance (C_{WW}), that is the capacitance between windings. The interwinding capacitance should be reduced in order to limit disturbance on the primary side due to possible steep voltage transitions present in the load connected to the secondary output.

Figure 28. Transformer parasitic capacitances



10.3 Schottky diode

The selection of the Schottky diode should consider the following parameters:

- Maximum forward current, mainly defined by the secondary output current demand
- Forward voltage drop, which affects the secondary output voltage regulation;
- Maximum peak reverse voltage. During the on-phase of the primary side, when no current flows in the secondary side, the diode is reverse biased and must withstand this voltage.

$$V_{D1_rev} = N \cdot (V_{INmax} - V_{OUT_pri}) + V_{OUT_sec} \quad (26)$$

- Junction capacitance, which should be as low as possible in order to reduce the ringing described in the previous section.

10.4 Output capacitor selection

10.4.1 Primary output capacitor

The triangular-shaped current ripple (with an average value of zero) flowing into the output capacitor gives the output voltage ripple, which depends on the capacitor value and the equivalent resistive component (ESR). Therefore, the output capacitor should be selected in order to obtain a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as follows:

$$\Delta V_{OUT_pri} C_{OUT_pri} = ESR \cdot \Delta I_{pri} + \frac{\Delta I_{pri}}{8 \cdot f_{SW} \cdot C_{OUT_pri}} \quad (27)$$

For a multi-layer ceramic capacitor (MLCC), the capacitive component of the ripple dominates the resistive one, while the opposite is true for an electrolytic capacitor. Neglecting the ESR contribution the minimum value of the output capacitor is given by Eq. (29) :

$$C_{OUT_pri} = \frac{\Delta I_{pri}}{8 \cdot f_{SW} \cdot \Delta V_{OUT_pri}} \quad (28)$$

The typical output ripple is set at around 0.5% of the output voltage. In the selection of the right value for C_{OUT_prim} , the derating of the capacitance with the voltage should be taken into account.

10.4.2 Secondary output capacitor

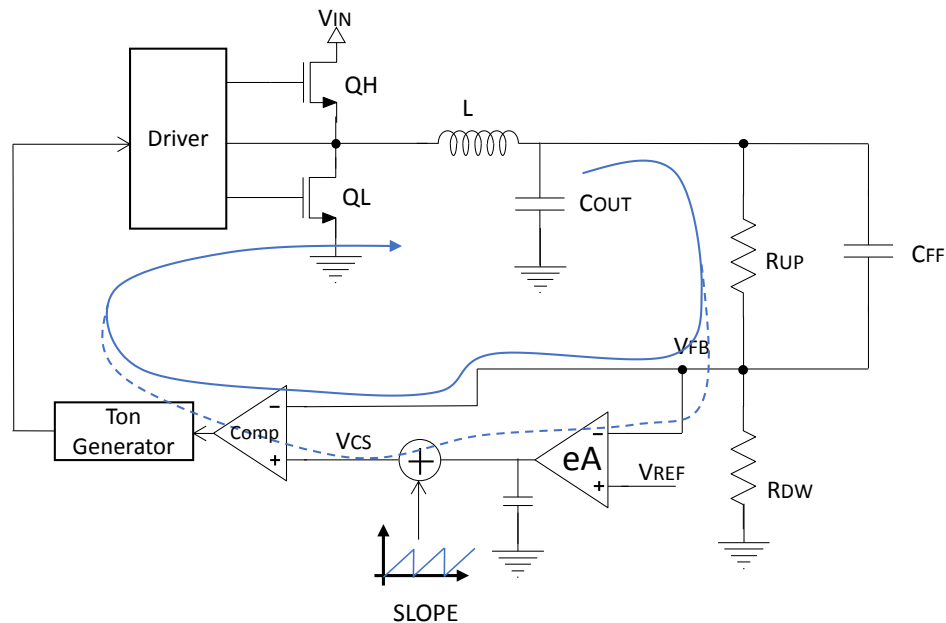
The secondary output capacitor supplies the secondary output load current during the t_{ON} (when diode D1 is reverse biased) and its value defines the secondary output voltage ripple (ΔV_{OUT}).

$$C_{OUT_sec} = \frac{I_{OUT_sec} \cdot D}{\Delta V_{OUT_sec} \cdot f_{SW}} \quad (29)$$

10.5 Compensation network

The primary side of the DCP10001IY is based on a V²COT control loop which combines the advantage of a COT loop (fast response with load transient) with the advantage of frequency clock loops. The main structure of the loop is shown in Figure 29.

Figure 29. V²COT loop



The V²COT is composed of double feedback paths:

- Dotted line loop: A compensator with high DC gain and low bandwidth is put on the slow feedback path to improve accuracy performances. A slope during the time period is added to the compensator output node to ensure stability also in low ESR conditions (using the MLCC case).
- Linear line loop: fast loop. The V_{OUT} variation is sensed directly on the comparator with a fast response. As a result, the load transient the system behaves like a COT system loop.

The PWM comparator matches the error amplifier output node with the feedback voltage to generate the main PWM request. Once the V_{FB} goes below the error amplifier voltage (V_{CS}) a t_{ON} pulse is turned on.

Figure 30. V²COT waveforms

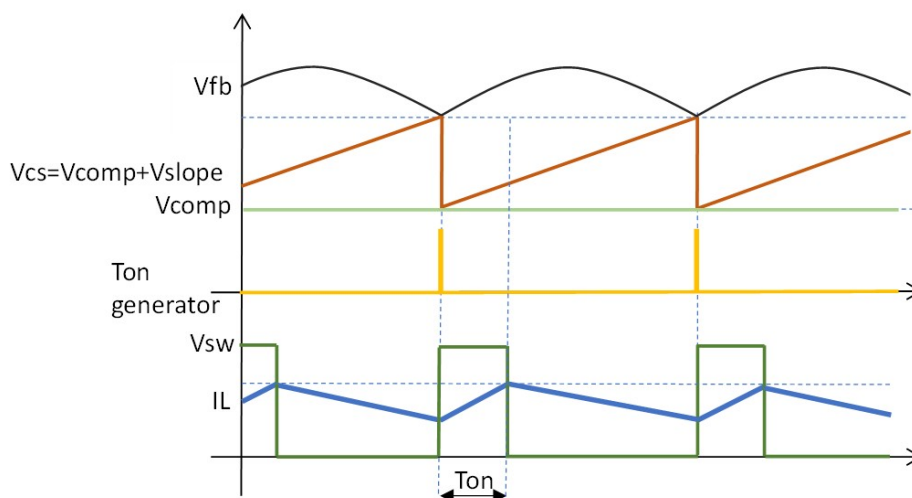
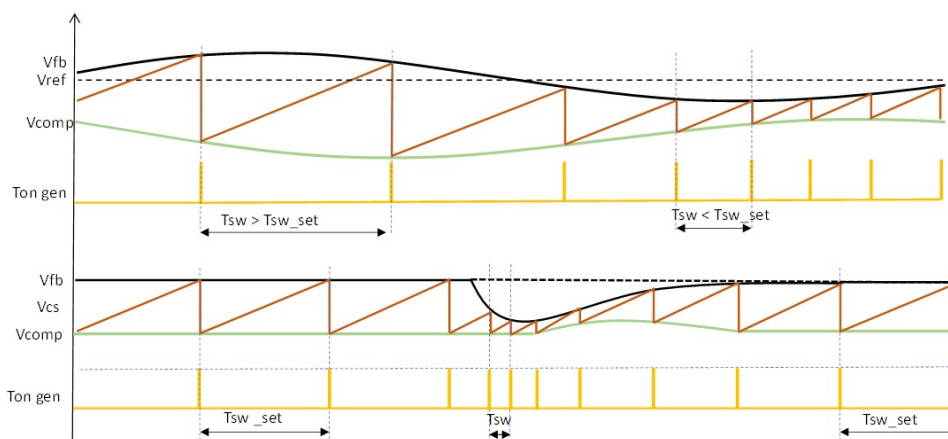


Figure 31 shows an example of system response of the two loops:

Example 1: V_{OUT} changes slowly ($<$ bandwidth of dotted line loop) and therefore V_{FB} , partition of V_{OUT} , follows the same behavior. The embedded V_{COMP} follows with the integral signal of the error amplifier inverting input. Once V_{FB} is over the reference V_{REF} , the V_{COMP} pulse sawtooth signal (V_{CS}) needs more time to reach the V_{FB} value and the f_{SW} decreases. Vice versa, when V_{FB} is below the reference, the V_{CS} signal needs less time to reach the V_{FB} value and f_{SW} is higher than the f_{SW} set.

Example 2: Once V_{OUT} drops immediately, like in load transient event, the V_{COMP} is not able to follow the abrupt V_{OUT} transition in a short time. However, the V_{CS} reaches the V_{FB} faster and f_{SW} increases quickly to avoid an extra V_{OUT} drop. In this case, the system behaves like a normal COT.

Figure 31. V_{OUT} variation example



C_{FF} capacitance is used to improve the stability condition and to inject an extra ripple on the feedback node, bypassing the effect of the resistor divider.

The C_{FF} suggested to best match the bandwidth (of the slow loop) and phase margin is calculated by Eq. 20 :

$$C_{FF} = \frac{5 \cdot \sqrt{V_{OUT}/V_{REF}}}{2 \cdot \pi \cdot R_{UP} \cdot f_{SW}} \quad (30)$$

It is recommended to use a $C_{FF} > 10$ pF.

Since the system V^2COT is COT-based with 2 loops, modeling is not possible.

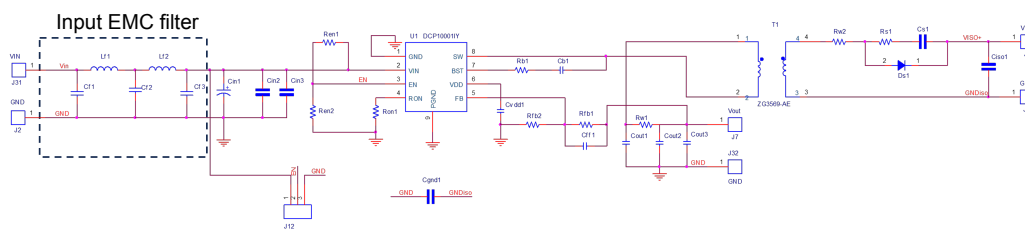
Besides, it is possible to study the slower loop compensation network and follow the stability good rules to select C_{FF} for stability.

ST provides (on the ST web eDesignSuite) a proprietary tool to design and tailor any applications, and eDSim, an online simulation tool based on SIMetrix SIMPLIS to evaluate start-up, stability and load/line transient of the system.

11 Application board

The application board (STEVAL-10001IY1M) schematic is shown in [Figure 32](#).

Figure 32. Schematic of the application board



The additional input filter (in the dotted box in [Figure 32](#), on the bottom side of the board) limits the conducted emission on the power supply. In the case that the filter is not necessary or should be bypassed for any test, two 0 Ω resistors should be placed at Lf1 and Lf2 instead of the indicated inductor and ferrite.

The isolated output supplied by the board is unregulated. Nevertheless, a post-regulation circuit can be implemented when necessary. For further details, please refer to the [AN6203](#).

Table 8. BOM of the application board

Reference	Part number	Description	Value	Manufacturer
U1	DCP10001IY			ST
T1	ZG3569	Transformer	N = 1.3, 2.25 kV isolation	Coilcraft
Rs1		0805 SMD resistor	300 Ω	
Rb1		0603 SMD resistor	0 Ω	
Ren1		0603 SMD resistor	100 k Ω	
Ren2		0603 SMD resistor	Not mounted	
Rfb1		0603 SMD resistor	30 k Ω	
Rfb2		0603 SMD resistor	1.2 k Ω	
Rw1		0603/1206 SMD resistor	Not mounted	
Rw2		0603/1206 SMD resistor	Not mounted	
C _{GND1}	GR443DR73D472KW01L	1812 MLCC	4.7nF, 2kV	Murata
Cvdd1		0603 MLCC	1 μ F, 100 V	
Cff1		0603 MLCC	Not mounted	
Cb1		0603 MLCC	100 nF, 100 V	
Cs1		0603 MLCC	Not mounted	
Cin1		SMD electrolytic capacitor, 10x10mm	100 μ F, 100 V	Panasonic
Cin2		0603 MLCC	100 nF, 100 V	
Cin3		1206 MLCC	4.7 μ F, 100 V	
Cout1		1206 MLCC		
Cout2		1206 MLCC		
Cout3		1206 MLCC		
Ciso1		1206 MLCC	22 μ F, 50 V	
R _{ON1}		0603 MLCC	82 k Ω	Murata

Reference	Part number	Description	Value	Manufacturer
Ds1	STPS1150-Y	Schottky diode	$V_{RRM} = 150\text{ V}$, $I_F = 1\text{ A}$	ST
Reference	Part number	Description	Value	Manufacturer
EMC input filter				
Cf1, Cf2, Cf3		1206 MLCC, 4.7 μ F, 50V		
Lf1	MPZ2012S221A	220 Ω Ferrite bead, 100MHz		
Lf2	XAL4030-682ME	6.8 μ H coil		Coilcraft

The performances of the application board are depicted in [Section 7](#).

The layout of the STEVAL-10001IY1M is shown in [Figure 33](#) (top) and [Figure 34](#) (bottom).

Figure 33. Layout of the STEVAL-10001IY1M (top side)

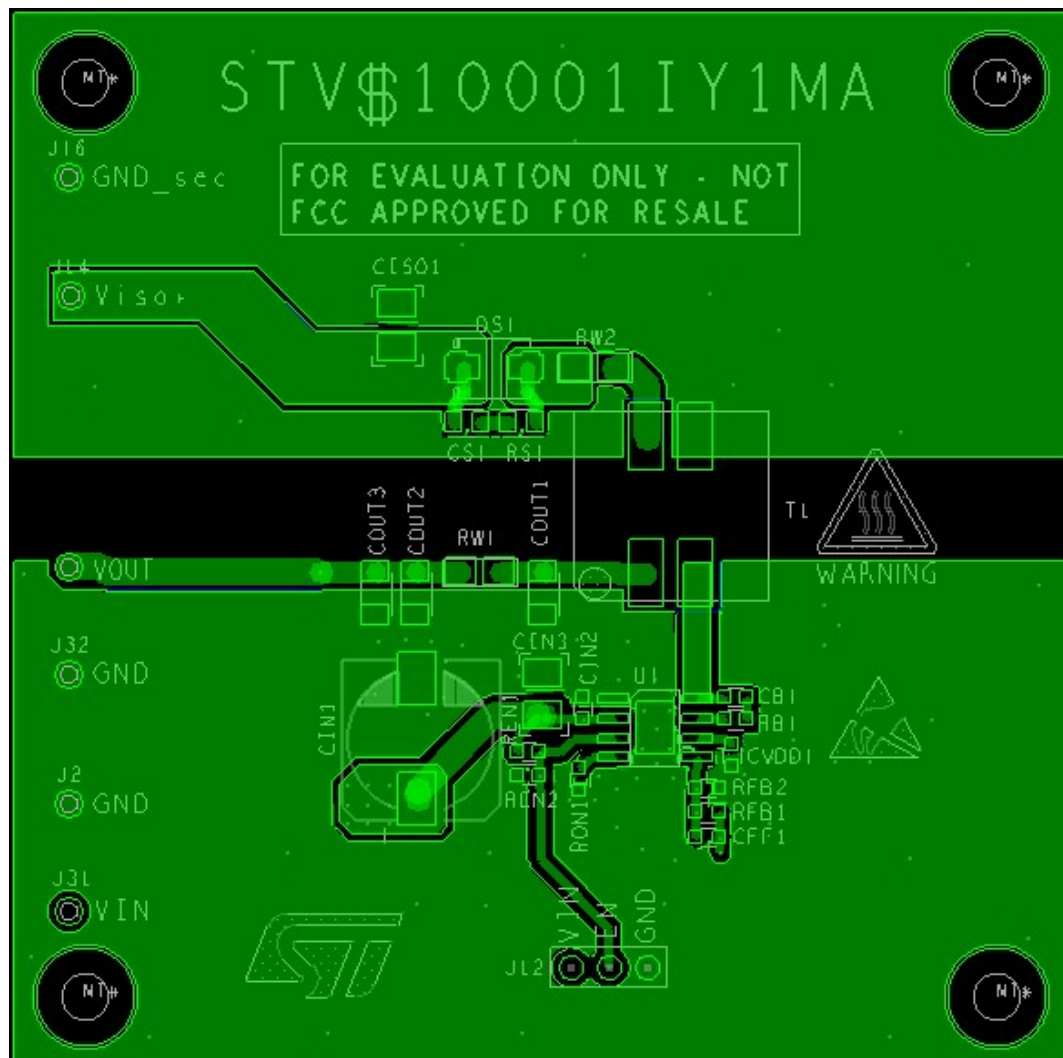
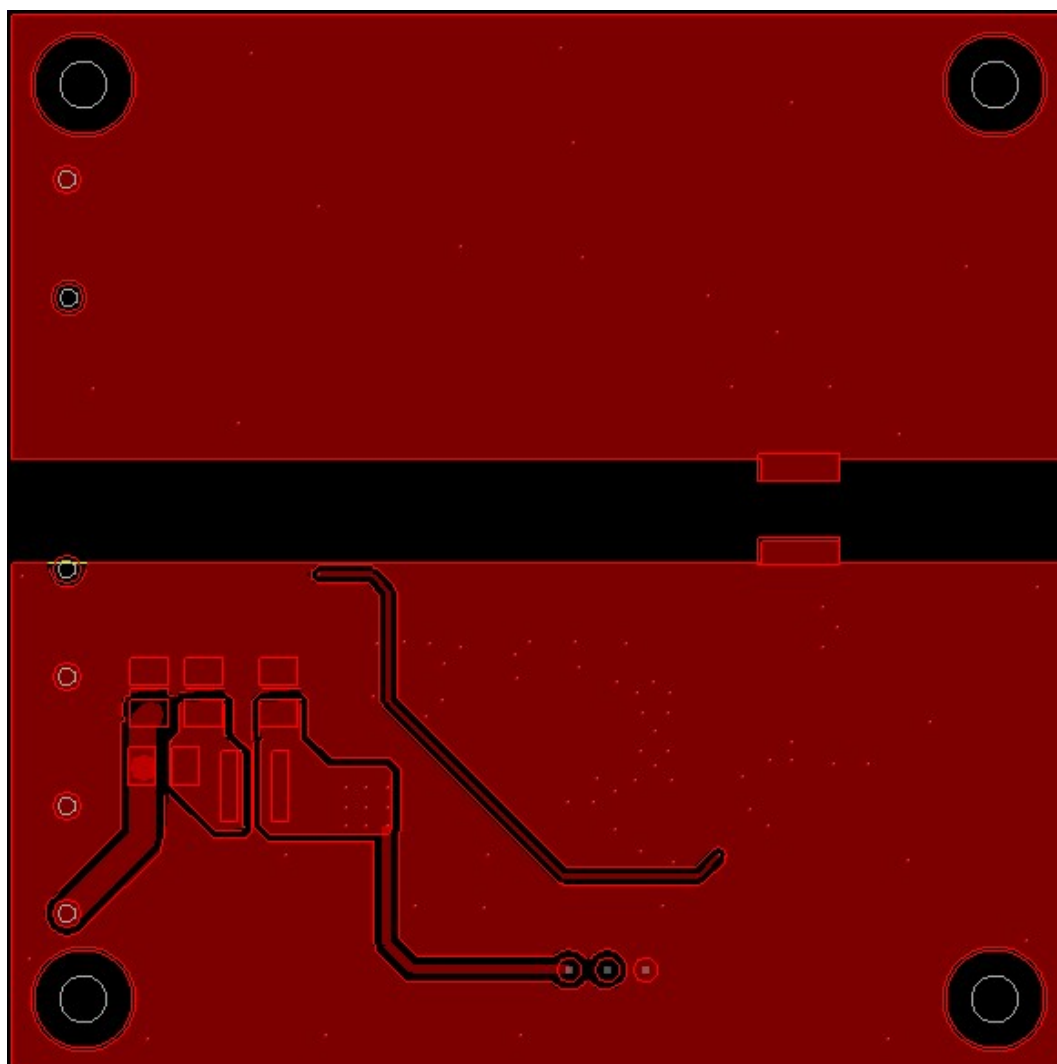


Figure 34. Layout of the STEVAL-10001Y1M (bottom side)



12 Application ideas

12.1 Other applications with ZG3569-AE

The application board described in the previous section is defined to generate an isolated voltage suitable for driving SiC (typ. 18/20 V and -5 V) or IGBT (typ. 15 V/ -8 V). The load regulation curves in Figure 11 clearly show that the isolated voltage is at least 24 V, even at higher loads. The 24 V minimum voltage has been defined to provide a sufficient margin in case a post-regulation (e.g. linear regulator + TL431) is expected.

For different isolated output voltages and/or for increasing or reducing this margin, the output resistor dividers Rfb1 and Rfb2 should be adjusted (see Eq. (6)).

The table below summarizes the values of Rfb1 and Rfb2 to be used in case voltages for GaN drivers (e.g. 6V/-3V) or standard MOSFETs (e.g. single 12 V isolated voltage).

Application	Required isolated voltage (s)	Rfb1	Rfb2
GaN drivers	+6 V/-3 V	22 k Ω	2 k Ω
MOSFETs	12 V	27 k Ω	2 k Ω

Load regulation performances are shown in Figure 35 and Figure 36.

Figure 35. Load regulation for GaN driver applications with the transformer ZG3569-AE

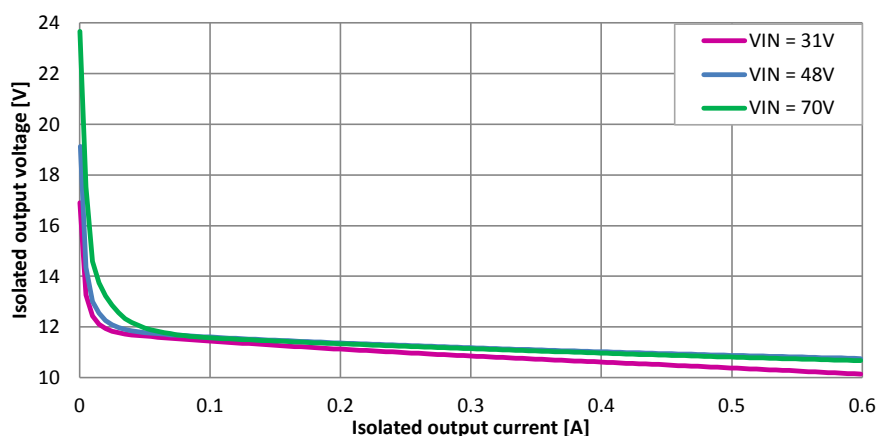
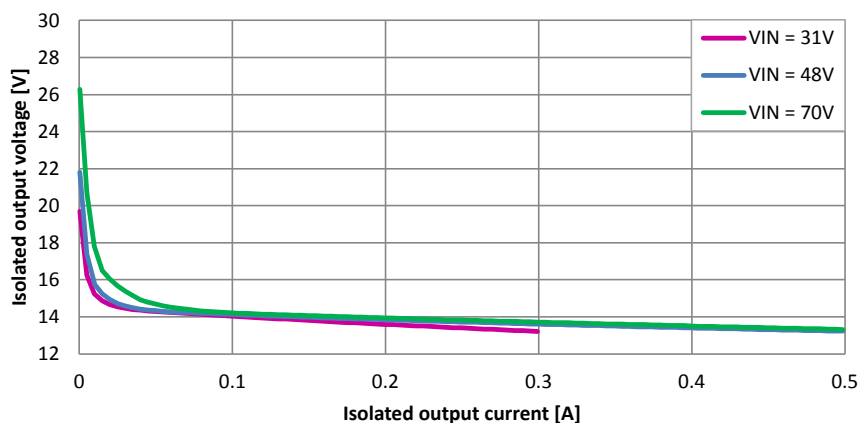


Figure 36. Load regulation for 12 V isolated driver applications with the transformer ZG3569-AE



12.2 Applications with other transformers or coupled inductors

As an alternative to the ZG3569-AE, other transformers or coupled inductors might be selected.

Different solutions for T1 are possible due to different reasons:

- Using an off-the-shelf component (availability and cost can be convenient)
- Need for a multi secondary windings transformer
- Different requirements for isolation
- Etc.

In this section, some application ideas with two selected off-the-shelf coupled inductors are presented. The selected components are:

Part number	Manufacturer	Turn ratio	Magnetizing inductance	Isolation
MSD1038V-683	Coilcraft	1:1	68 μ H	2.25 kV (functional)
750315811	Würth Elektronik	1:1	60 μ H	1.5 kV (functional)

With regard to the possible target applications, this highly depends on the input voltage range. Considering the voltage range illustrated in Figure 9 (48 V car battery), the use of a transformer with a 1:1 turn ratio does not make it possible to support applications with isolated voltages above 24 V (e.g. SiC and IGBT). For different (or narrower) input voltage ranges, it is definitely possible, but for this section, the same range of Figure 9 will be considered.

Therefore, the following applications can be supported:

- GaN drivers (typ. 6 V/-3 V)
- Single isolated voltages (e.g. 12 V, for standard MOSFETs)

12.3 Applications with 750315811

12.3.1 Example for GaN drivers

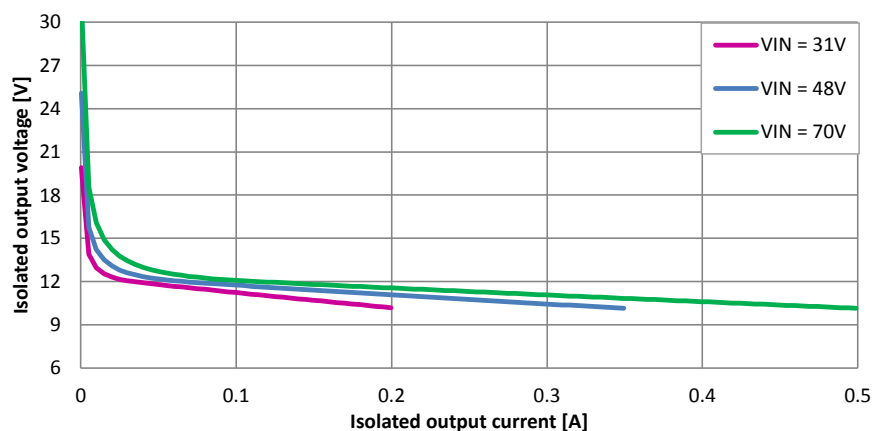
The output resistor divider should be adjusted as follows:

$R_{fb1} = 30 \text{ k}\Omega$

$R_{fb2} = 2 \text{ k}\Omega$

The load regulation performances at different input voltages are depicted in Figure 37.

Figure 37. Load regulation for GaN driver applications with 750315811



12.3.2 Example for MOSFET drivers

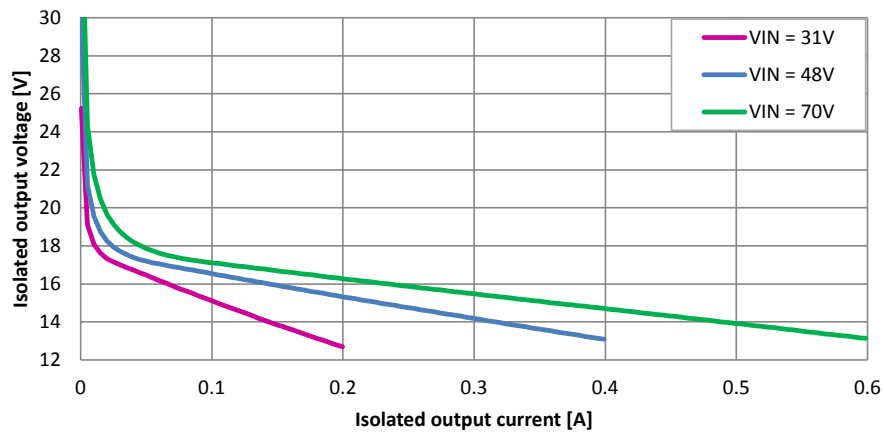
The output resistor divider should be adjusted as follows:

$$R_{fb1} = 43 \text{ k}\Omega$$

$$R_{fb2} = 2 \text{ k}\Omega$$

The load regulation performance at different input voltages are depicted in Figure 38.

Figure 38. Load regulation for MOSFET driver applications with 750315811



12.4 Applications with MSD1038V-683

12.4.1 Example for GaN drivers

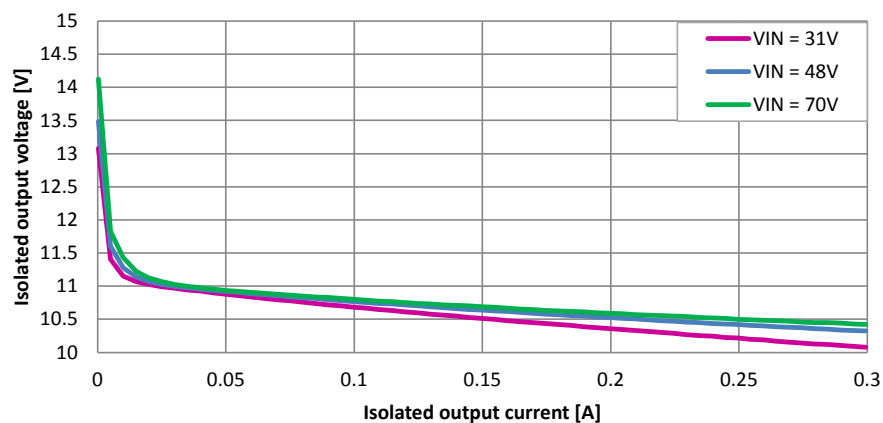
The output resistor divider should be adjusted as follows:

$$R_{fb1} = 27 \text{ k}\Omega$$

$$R_{fb2} = 2 \text{ k}\Omega$$

The load regulation performance at different input voltages are depicted in Figure 39.

Figure 39. Load regulation for GaN driver applications with MSD1038V-683



12.4.2 Example for MOSFET drivers

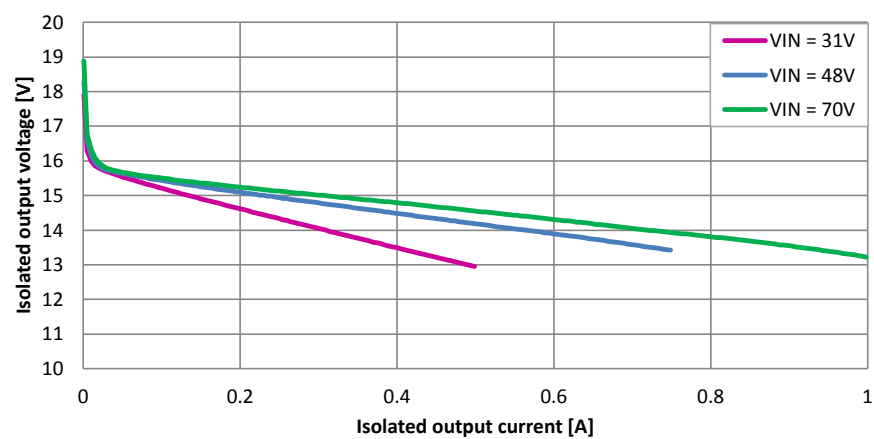
The output resistor divider should be adjusted as follows:

$$R_{fb1} = 39 \text{ k}\Omega$$

$$R_{fb2} = 2 \text{ k}\Omega$$

The load regulation performances at different input voltages are depicted in Figure 40.

Figure 40. Load regulation for MOSFET driver applications with MSD1038V-683



13 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

13.1 HSOP8 package information

Figure 41. HSOP8 package outline BOTTOM View

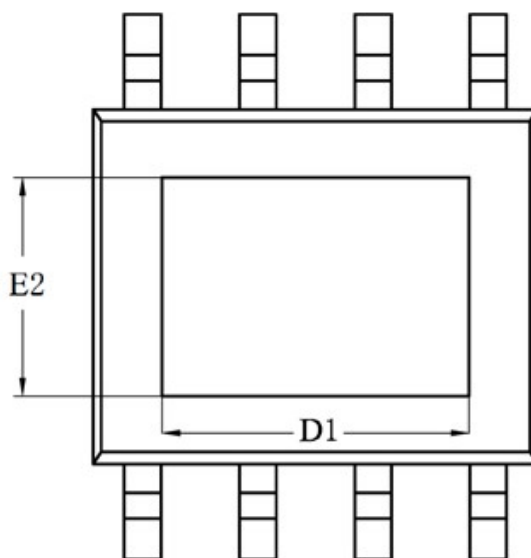


Figure 42. HSOP8 Package outline SIDE View

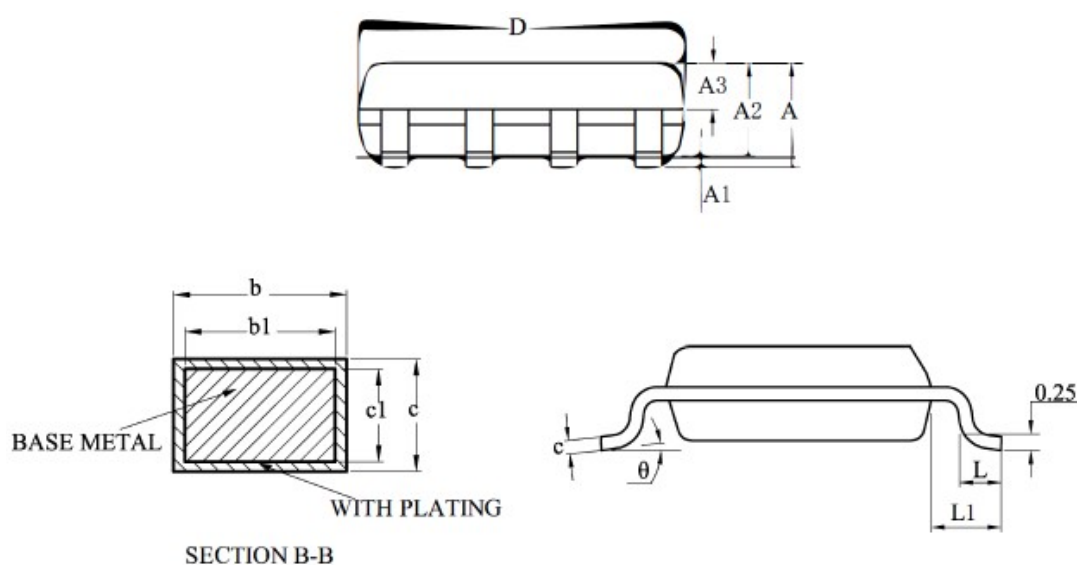
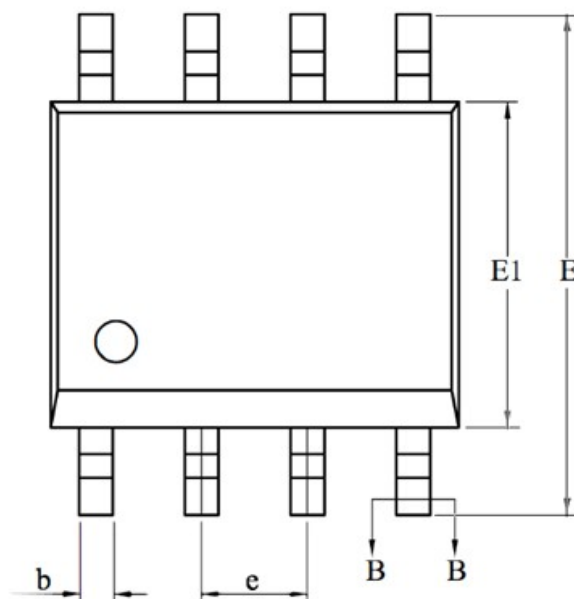
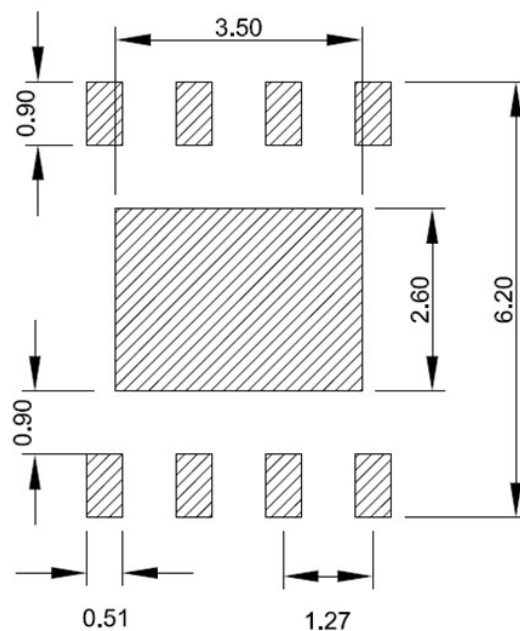


Figure 43. HSOP8 Package outline TOP View

Table 9. HSOP8 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	- 5	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
B1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
D1	3.1 REF		
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	0.60	0.80
L1	1.05REF		
O	0	-	8°

Figure 44. HSOP8 Recommended Footprint (Dimensions in mm)



13.2 Package information

Figure 45. Carrier type

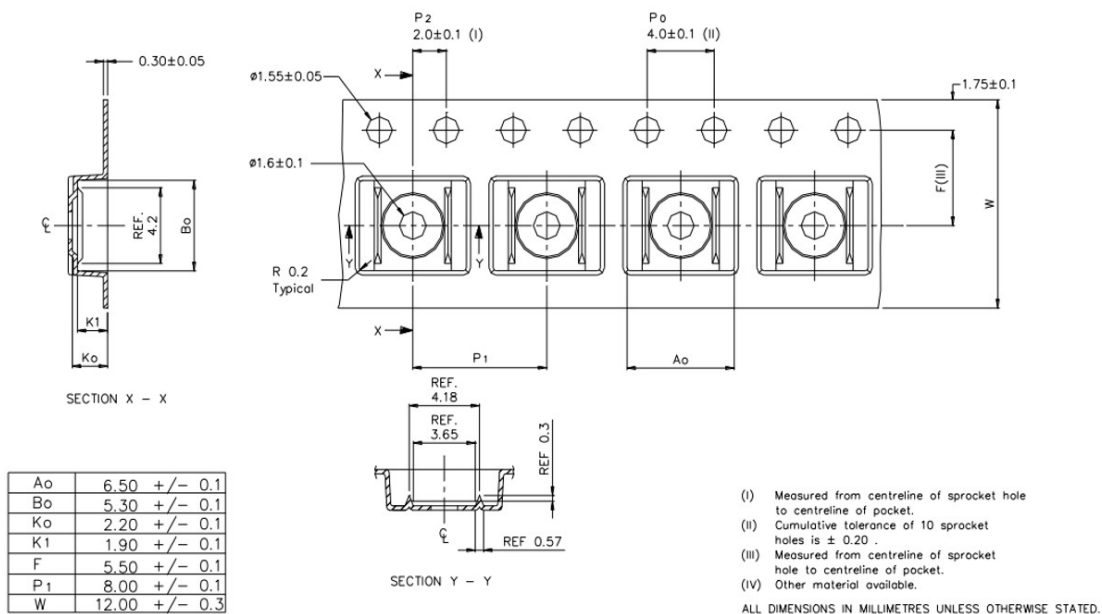
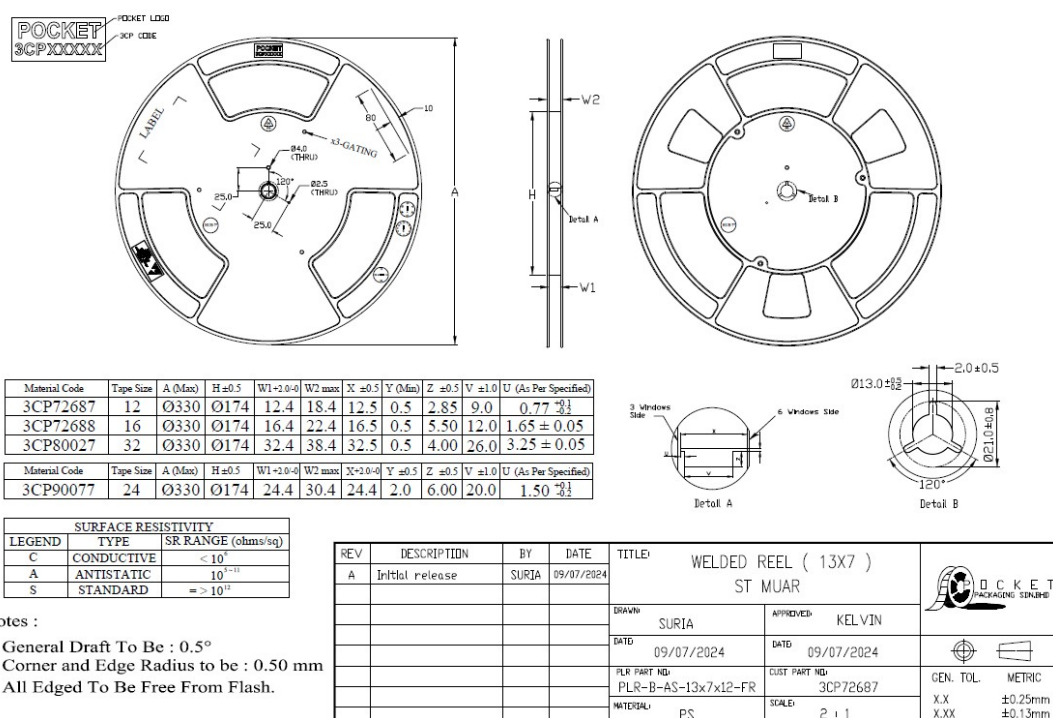


Figure 46. Plastic reel



14 Ordering Information

Table 10. Order codes

Part number	Package	Packaging
DCP10001IPHRY	HSOP8	Tape and reel

Revision history

Table 11. Revision history

Date	Revision	Changes
13-Oct-2026	1	Initial release.

Contents

1	Pin configuration	2
2	Typical application circuit	3
3	Maximum ratings	4
3.1	Absolute maximum ratings	4
3.2	ESD protection	4
3.3	Thermal characteristics	4
3.4	Recommended operating conditions	4
4	Electrical characteristics	5
5	Datasheet parameters over the temperature range	7
6	Functional description	8
6.1	Power section	8
6.1.1	Enable	8
6.1.2	Soft-start	9
6.1.3	Undervoltage lockout	10
6.1.4	On-time generator	11
6.1.5	Dithering	11
6.2	Transformer	11
6.3	Secondary side	11
6.4	Iso-buck operating principle	11
7	Isobuck performance	13
7.1	Secondary output line regulation	13
7.2	Secondary output load regulation	14
7.3	Efficiency	14
8	Protections	16
8.1	Secondary output short-circuit protection	16
8.2	Secondary output overcurrent protection	17
8.2.1	Current peaks estimate	17
8.3	Thermal shutdown	18
8.4	Embedded discharge switch	18
9	Application notes	20
9.1	Isolated output voltage adjustment	20
9.2	On-time and switching frequency	21
9.3	Enable resistor divider	21
10	Design of the external components	23

10.1	Input capacitor selection	23
10.2	Transformer selection	24
10.3	Schottky diode	28
10.4	Output capacitor selection	28
10.4.1	Primary output capacitor	28
10.4.2	Secondary output capacitor	28
10.5	Compensation network	29
11	Application board	32
12	Application ideas	35
12.1	Other applications with ZG3569-AE	35
12.2	Applications with other transformers or coupled inductors	36
12.3	Applications with 750315811	36
12.3.1	Example for GaN drivers	36
12.3.2	Example for MOSFET drivers	37
12.4	Applications with MSD1038V-683	37
12.4.1	Example for GaN drivers	37
12.4.2	Example for MOSFET drivers	37
13	Package information	39
13.1	HSOP8 package information	39
13.2	Package information	41
14	Ordering Information	43
	Revision history	44

List of tables

Table 1.	Pin description	2
Table 2.	Typical application components	3
Table 3.	Absolute maximum ratings	4
Table 4.	ESD performance	4
Table 5.	Thermal data	4
Table 6.	Recommended operating conditions	4
Table 7.	Electrical characteristics	5
Table 8.	BOM of the application board	32
Table 9.	HSOP8 package mechanical data	40
Table 10.	Order codes	43
Table 11.	Revision history	44

List of figures

Figure 1.	Pin connection (top view)	2
Figure 2.	Typical application circuit	3
Figure 3.	Iso-buck general schematics	8
Figure 4.	Enable power up/down	9
Figure 5.	Soft-start procedure	10
Figure 6.	Soft-start with primary and secondary output voltage rising up	10
Figure 7.	Iso-buck basic operating principle	11
Figure 8.	Iso-buck primary and secondary current waveforms	12
Figure 9.	48 V car battery voltage range according to ISO21780	13
Figure 10.	$V_{OUTprim} = 21\text{ V}$, $f_{SW} = 500\text{ kHz}$, transformer $N = 1.3$	14
Figure 11.	Load regulation of the secondary isolated output, $f_{SW} = 500\text{ kHz}$, $V_{OUTprim} = 21\text{ V}$, transformer $N = 1.3$	14
Figure 12.	Secondary output efficiency at different input voltages, $V_{OUTprim} = 21\text{ V}$, $f_{SW} = 500\text{ kHz}$, $N = 1.3$	15
Figure 13.	Implementation of the secondary output short-circuit protection	16
Figure 14.	Short-circuit protection $V_{IN} = 48\text{ V}$, $V_{OUTprim} = 30\text{ V}$, $N = 1$	16
Figure 15.	Implementation of the secondary output overcurrent protection	17
Figure 16.	Overcurrent protection, $V_{IN} = 48\text{ V}$, $V_{OUTprim} = 30\text{ V}$, $N = 1$, $I_{OUTiso} = 500\text{ mA}$	17
Figure 17.	Current peaks in HS e LS MOSFETs depending on the isolated output current $V_{IN} = 48\text{ V}$, $V_{OUTprim} = 21\text{ V}$, $f_{SW} = 500\text{ kHz}$	18
Figure 18.	Effect of the embedded discharge switch	19
Figure 19.	Comparison between primary output capacitance voltage and primary winding current with and without the internal discharge switch	19
Figure 20.	Secondary output current typical waveform	20
Figure 21.	Switching frequency vs R_{ON} resistance	21
Figure 22.	Connection of the enable resistor divider	22
Figure 23.	Input capacitor AC current	23
Figure 24.	Primary winding current (blue), secondary winding current (magenta) and magnetizing current (black).	25
Figure 25.	Effect of the leakage inductance on the primary winding current	26
Figure 26.	Filtering effect of the snubber network	27
Figure 27.	RC snubber network	27
Figure 28.	Transformer parasitic capacitances	28
Figure 29.	V^2COT loop	29
Figure 30.	V^2COT waveforms	30
Figure 31.	V_{OUT} variation example	30
Figure 32.	Schematic of the application board	32
Figure 33.	Layout of the STEVAL-10001IY1M (top side)	33
Figure 34.	Layout of the STEVAL-10001IY1M (bottom side).	34
Figure 35.	Load regulation for GaN driver applications with the transformer ZG3569-AE	35
Figure 36.	Load regulation for 12 V isolated driver applications with the transformer ZG3569-AE	35
Figure 37.	Load regulation for GaN driver applications with 750315811	36
Figure 38.	Load regulation for MOSFET driver applications with 750315811	37
Figure 39.	Load regulation for GaN driver applications with MSD1038V-683	37
Figure 40.	Load regulation for MOSFET driver applications with MSD1038V-683	38
Figure 41.	HSOP8 package outline BOTTOM View	39
Figure 42.	HSOP8 Package outline SIDE View	39
Figure 43.	HSOP8 Package outline TOP View	40
Figure 44.	HSOP8 Recommended Footprint (Dimensions in mm).	41
Figure 45.	Carrier type	41
Figure 46.	Plastic reel	42

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