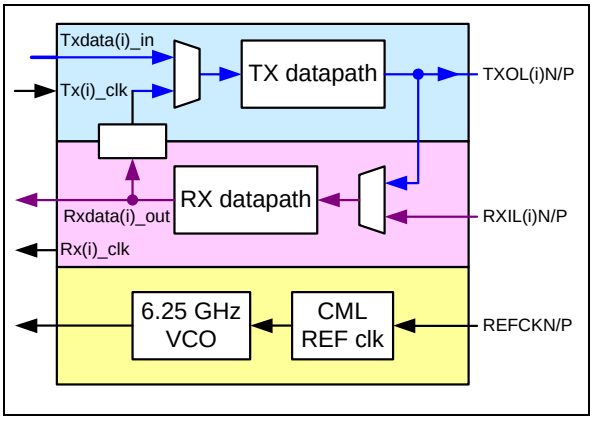
C65SPACE-HSSL

6.25 Gbps multi-rate, multi-lane, SerDes macro IP

Datasheet - preliminary data



Features

- ST CMOS065LP low-power 65 nm CMOS technology
- 1.5625, 3.125 and 6.25 Gbps operation
- BER < 10^{-14}
- 20 bit TX and RX parallel data interface width / sub-rate mode
- Global power down and per link TX & RX power downs
- Compact form factor: 3040u x 1600u (tbc)
- Flip chip only layout
- Full immunity to single event latch-up (SEL) failures with a LET up to 60MeVcm2/mg
- No single event functional interrupts (SEFIs), up to 60MeVcm2/mg
- 1.2V power supply

Description

The ST 65 nm HSSL IP is a radiation hardened high-performance SERDES developed in ST CMOS065LP Low Power 65 nanometer CMOS technology and is provided as Flip chip only layout with build-in 2KV ESD protection. It features 8 channels (4Tx + 4 Rx) and is supplied by 1.2 volt.

It embeds a PLL and four identical data slices. Each data slice is composed of a data transmission lane and a data reception lane. The PLL provides very stable 6.25 GHz internal bit clock which is synthesized from a lower frequency input reference clock. This bit clock is used to generate each transmission bit clock and to recover each received bit clock.

Each data slice is running independently to each other. In each data slice, the transmitter and receiver are running independently to each other and may have different bit rate.

A +/-100ppm plesiochronous operation is guaranteed by design in each data lane individually and independently (Tx data lane and Rx data lane).

Each data slice embeds one BIST which contains: a PRBS generator, a BER monitor, an internal data lane loopback TX -> RX (in each data slice) and a TX clock jitter generator.

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1 Overview

The ST 65 nm HSSL IP is a radiation hardened high-performance SERDES developed in ST CMOS065LP low power 65 nanometer CMOS technology and is provided as Flip chip only layout with build-in 2KV ESD protection. It features 8 serial channels (4Tx + 4 Rx) and is supplied by 1.2 volt.

It embeds a clock slice including a PLL and four identical data slices. Each data slice is composed of a data transmission lane and a data reception lane. The PLL provides a very stable 6.25 GHz internal bit clock which is synthesized from a lower frequency input reference clock. This bit clock is used to generate each data transmission lane bit clock and to recover each received bit clock.

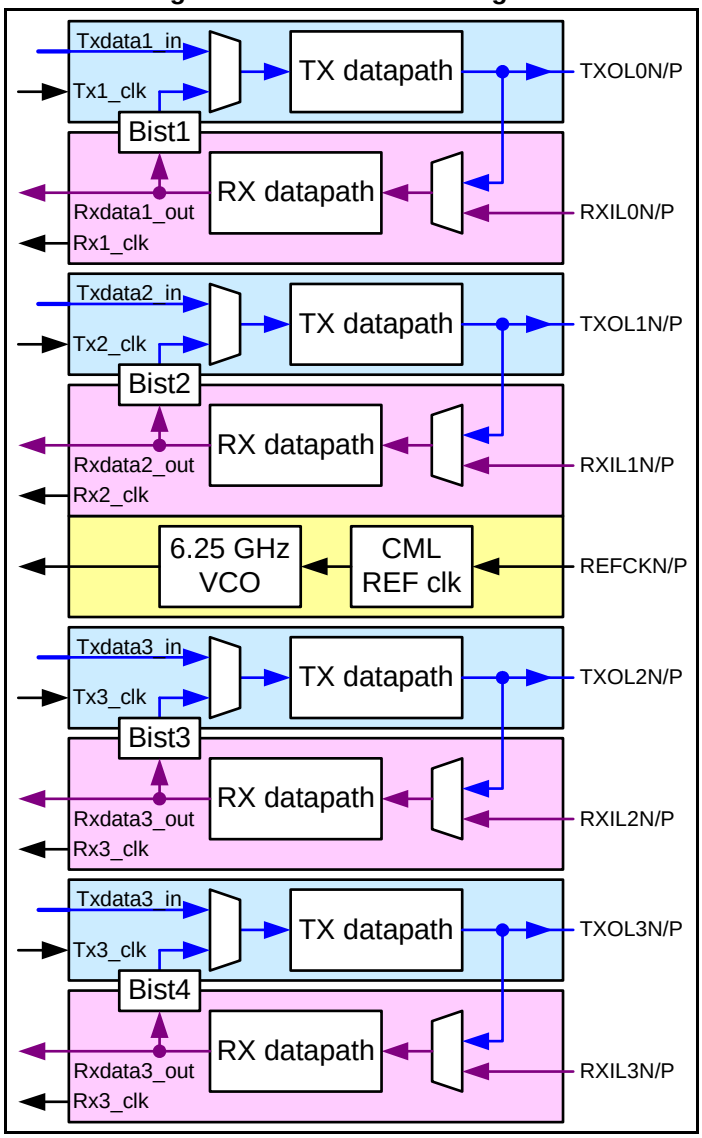
Each data slice is running independently to each other. In each data slice, the transmitter and receiver are running independently to each other and may have different bit rate. Each transmitter and receiver can sustain one of three possible data rate: 6.25 Gbit/s (full rate), 3.125 Gbit/s (half rate) and 1.5625 Gbit/s (quarter rate).

A +/-100ppm plesiochronous operation is guaranteed by design in each data lane individually and independently (Tx data lane and Rx data lane).

Each data slice embeds one BIST (So, 4 BIST in total in the HSSL IP) which contains: a PRBS generator, a BER monitor, an internal data lane loopback TX -> RX (in each data slice) and a TX clock jitter generator.

Note: The HSSL IP implements a SERDES PHY layer only. Any transmission encoding (like 8B10b), any elastic buffer or any synchronization between any data lane for link aggregation purpose is part of the link layer of any communication protocol and have to be developed in Soc core logic driving the HSSL by the user.

Figure 1. HSSL IP block diagram



2 Control bus

Control registers are accessible via a parallel, memory-like control bus located in the clock-slice. It is based on a 16 bit write data bus (“WRITE_DATA”), a 16 bit read data bus (“READ_DATA”) and a 10 bit address bus (“RW_ADDRESS”). All HSSL settings are written and are read via the control bus.

Each registers has a 16 bits width but there are 2 separate upper byte and lower byte enables so the bus supports single byte access and is compatible with 8-bit bus interfaces.

For test purpose, an “intercept” mode and 3 special pins on the clock-slice allow full access to the HSSL registers at any time via the JTAG port.

The clock-slice has four 16-bit control registers and one 16-bit status register.

Each data slice has its own set of registers which is independent of the other data slices.

In each data slice, each Tx lane and each Rx lane has five 16-bit control registers. The Eye monitor and a few bits for BIST and other features are assigned in three 16-bit control registers and six 16-bit “status and measurement results” registers.

Control bus consists of:

- 4 control signals (SELECT, WRITE, BE_MSB and BE_LSB).
- 10 binary coded Address lines: upper 5 for channel, lower 5 for register (RW_ADDRESS [9:0]).
- 16 Data-In bits (WRITE_DATA[15:0]).
- 16 Data-Out bits (READ_DATA[15:0])

Control bus timing

Even if the control bus is clocked internally with MCLK, it can be used as an asynchronous interface.

So, there are no phase relationship requirements between any control bus input and MCLK (as all required retiming is included internally). The only influence of MCLK is to limit how fast the interface can run, which is no faster than one command per 10 MCLK cycles (but there are no limitations on the phase relation between the commands and MCLK).

In *Figure 2* MCLK is indicated in grey for reference only (as not needed).

Note: MCLK is like the high speed clock of a computer system: it controls internal processes but is not used or needed for the interfaces.

Figure 2. Control bus write timing requirements

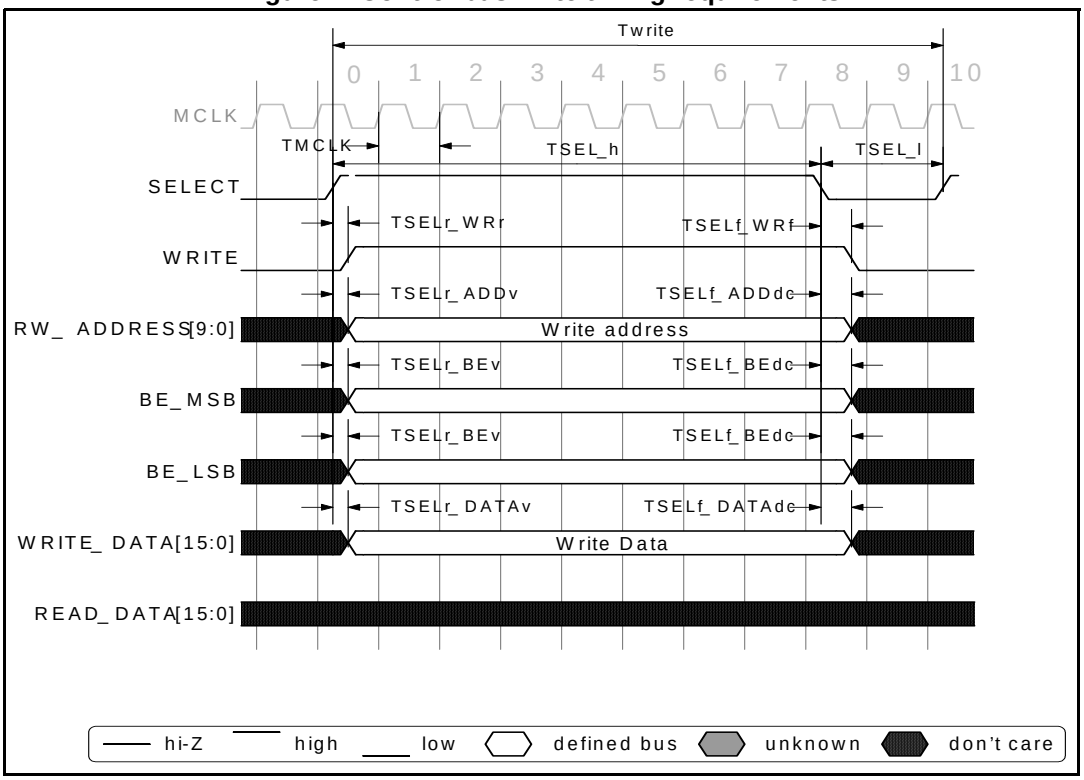
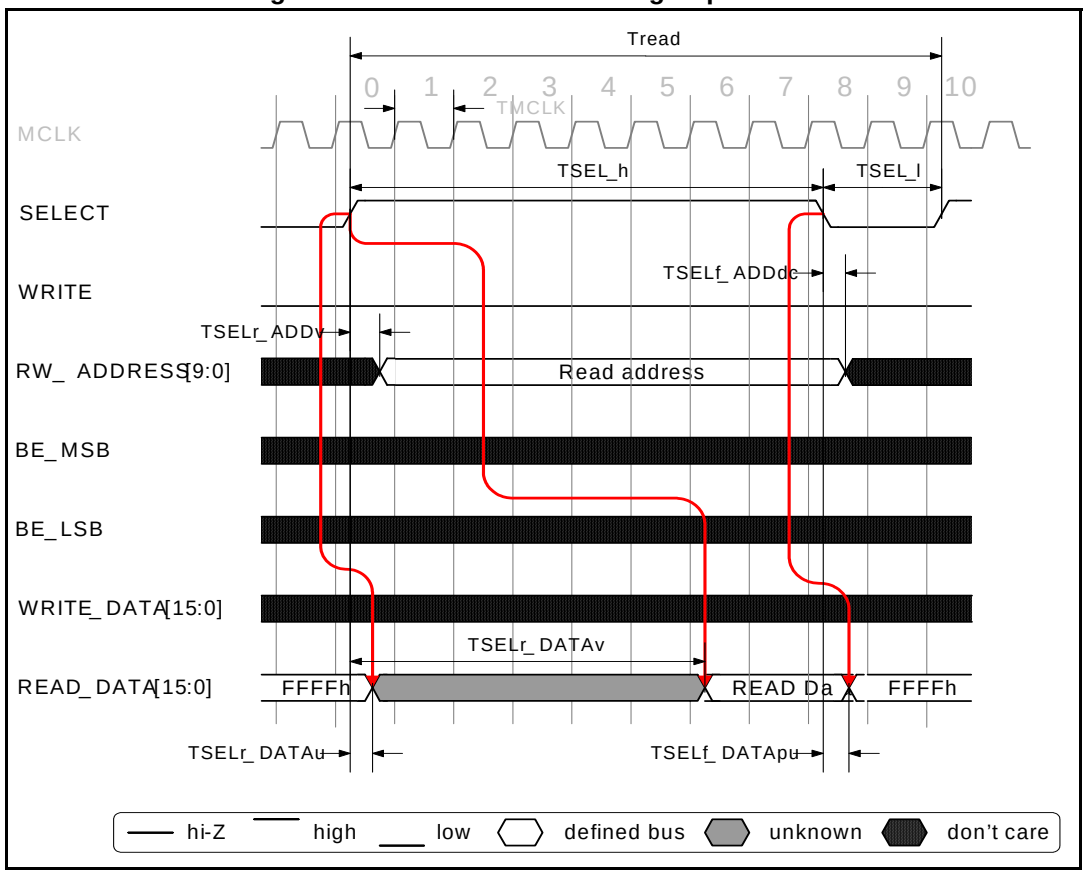


Figure 3. Control bus read timing requirements



3 Clocking system and reference clocks

3.1 Feature

- Supports 156.25 MHz CML or AC coupled input differential reference clock (without pre-divider). Suppresses jitter above 1 MHz at -20dB / decade.
- Very stable LC tank oscillator calibrated by hardware state machine.
- Internal loss of clock and loss of lock detectors status available by register reading.
- Loss of clock and loss of lock detectors “ored” status result available on PLLOUTOFLOCK output pin.

Note: The HSSL requires a 100 nF capacitor to be connected to the CAPP and CAPN bumps and a 500 ohm resistor to be connected on REXT.
Usually the capacitor is located in the SOC package.

3.2 Reference clock and derived clock specification

Table 1 defines the specification of REFCLK, the 6.25 GHz VCO range and MCLK.

Table 1. REFCLK, the 6.25 GHz VCO range and MCLK specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes(1)
F_{REF}	REFCLK frequency	156.248	156.25	156.252	MHz	For min jitter with input divide ratio = 1
DC_{REF}	REFCLK duty cycle	40	50	60	%	Duty cycle of the input Ref clock
J_{REF}	Ref clock jitter			0.5	ps rms	Jitter meas.> 1MHz will be cut @ 20 dB/decade. Copied directly to all outputs.
J_{REFCC}	Jitter cycle to cycle			10	ps p-p	J_{REF} spec must also be met
V_{REF}	Ref clock input peak differential voltage	300	400	600	mVp	Reasonably large amplitude helps to minimize jitter from cross-talk. A.C. coupling is assumed.
F_{CORE}	MCLK frequency	F_{REF}	312.5	2x F_{REFmax}	MHz	Bus and system master clock

1. The PLL random jitter amplitude varies relatively with PFD clock period. M is the reference clock divider ratio, N is the feedback divider ratio, K is the MCLK divider ratio.

4 TX lane description

4.1 Tx lane features

- Differential CML outputs with polarity and/or bit order inversion.
- Programmable differential terminations of 100 ohms.
- 5 tap programmable pre-emphasis (1 precursor,1 cursor, 3 post-cursor).
- Programmable output amplitude with level boost mode.
- 20 bit parallel Interface running at 312.5 MHz with a possible frequency offset up to ±100ppm relative to the 6.25 GHz internal reference clock divided by 20.
- Clock aligner for Rx to Tx loop-back.
- Partial standby mode controlled by register.
- Test features:
  - IEEE 1149.1 (DC) and 1149.6 (AC) JTAG boundary scan support.
  - TX – RX full speed serial loop-back (in analog at pin level or internally in digital).
  - TX – RX and RX –TX parallel loop-back.
  - Five standard PRBS patterns generation.
  - Programmable 20 bit fixed transmission pattern generation.
  - Programmable triangular phase jitter generation for BER measurement.
  - Additional programmable bit rate frequency offset versus the 6.25 GHz reference clock for BER measurement.

4.2 Tx parallel interface timing

The parallel interfaces of each HSSL transmitter consists of 20 data pins TXD[19:0]<n>, and two clock pins TXDCLK<n> and TXOCLK<n>. In every case the intention is for data to change roughly on one edge of the clock and to be captured roughly on the other edge of the clock to allow sizeable skews between the clocks and data of either polarity.

Normally, TXDCLK<n> is driven by a clock be provided by the ASIC derivate from the clock slice MCLK.

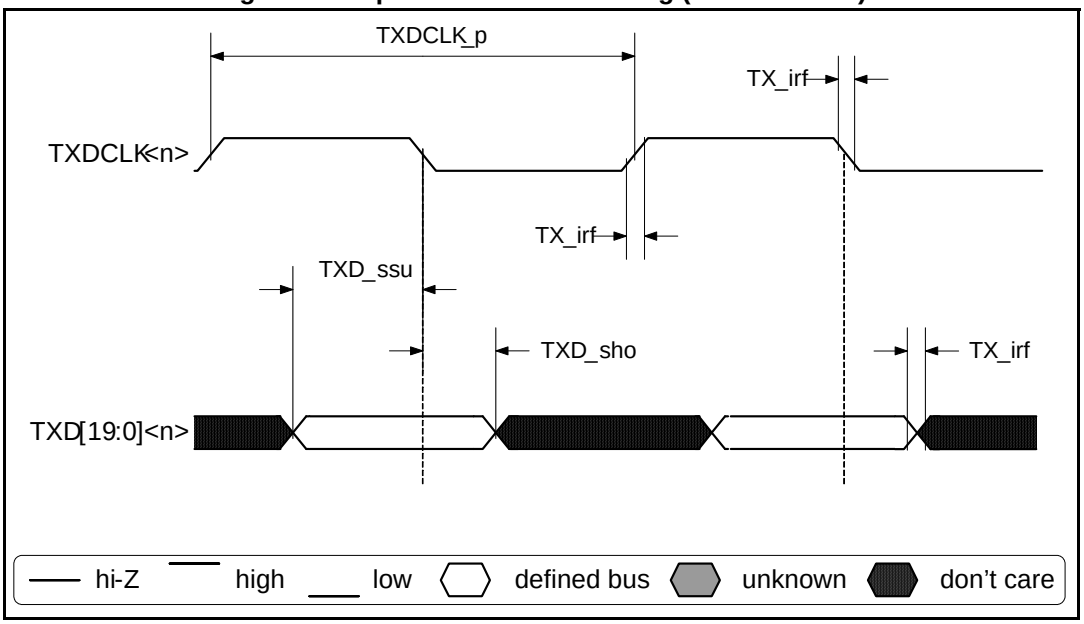
Each core interface to each transmit channel can independently use one of 3 different rate modes. The parallel word rate is 1/20 of the Tx_bit_clock<n>. 20, 10 or 5 bit words can be provided on TXD[19:0]<n> by selecting full-rate, ½-rate, or ¼-rate respectively.

The parallel interfaces always justify the bits to the LSB side of the 20 data pins, and can map them such that the serial bit stream has either the LSB or the MSB end first.

There is no option to operate the parallel interface at twice the rate and ½ the width as such functionality can be directly implemented outside the HSSL in an application-specific manner when required.

The Tx parallel interface timing in normal mode is described in *Figure 4*.

Figure 4. TX parallel interface timing (normal mode)



4.3 TX driver analog characteristics

Table 2 defines the specification of TX analog driver.

Table 2. Transmitter analog characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{OCM}	Output common mode voltage	800	1000	1200	mV	DC coupled, all terminations to 1.2V
		N.A.				AC coupled
V_{OD}	Output peak differential voltage		300	600	mVp	DC coupled
			300	600		AC coupled
S_{22}	Output return loss			10	dB	Measured @ 4GHz
Z_{OD}	Differential output impedance	90		110	Ohm	Not included S_{22} effects > 1 GHz
Z_{OCM1}	Common mode OP impedance	24	28	32	Ohm	Common mode term. sw. closed
R_J	Random jitter with RefClk as specified			0.8	ps rms	Integrated from 12 to 100kHz
				1.0		Integrated from Fbaud/1667 to Nyquist
D_J	Deterministic jitter			0.125	UI pp	With 0 ppm frequency offset
D_{JP}	Jitter from freq. offset (Pleisiochronous)			0.032	UI pp	With 300 ppm frequency offset
F_{OFF}	Allowed freq.offset from PLL			100	ppm	"STEPSIZE" must be 1, 2, 4 for full, ½, ¼ rate modes respectively
J_T	Jitter transfer(1)		-40		dB	From input clock TXDCLK

Table 2. Transmitter analog characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{RF}	Output rise/fall times 20_80%(2)	20		60	ps	At die bumps with nominal load
T_{TPL}	TX pipeline latency	34		49	UI	UI refers to full rate for all modes Min for 1st bit, max for last bit
T_{TAL}	TX analog latency in all modes	0		1.0	ns	
$T_{TCCS}K$	TX channel to channel skew	-2	0	+2	full-rate UI	Assumes self-align mode, identical TXDCLK inputs to all channels.

1. Clock aligner dead band of~2 full-rate UI normally inhibits jitter transfer below ~1.5 full-rate UI p-p but allows similar sized skews
2. Does not include package and board impedance irregularities and high frequency losses if they significantly affect external waveform.

4.4 TX eye mask

Figure 5 describes the transmission eye mask. It displays two successive bits: the first one is a bit due to a transition and the second one is the same repeated bit which includes the de-emphasis due to one or several FIR activated coefficients.

Figure 5. Transmitter eye mask: Repeat bit with de-emphasis following a transition bit

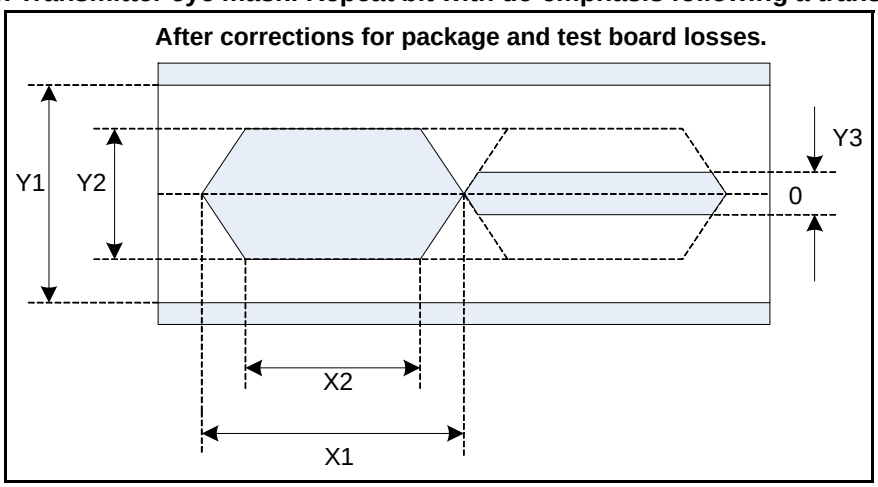


Table 3. Transmitter eye mask values

Symbol	Parameter	Value	Unit	Notes
X1	Min horizontal eye opening	0.75	UI	Measured @ 1e-12 BER
X2	Min horizontal eye width @ Y2	0.4	UI	Measured @ 1e-12 BER
Y1	max eye hight	1200	mVpp	20mA drive setting
Y2	Min vertical eye opening @ X2	Function of mA setting	mVpp	Drive settings: 8 values from 8 to 20mA
Y3	minimum vertical eye opening for bits with de-emphasis	Y2*(1- de emphasis)	mV	De-emphasis = 90, 80, ..., 0 % With pre-emphasis = 1/(1 - de-emphasis)

5 RX lane description

5.1 Rx lane features

- Differential CML signaling with polarity and order inversion.
- Programmable differential terminations of 100 ohms.
- 20 bit parallel Interface running at 312.5 MHz.
- Up to ± 100ppm data rate offset tracking capability relative to 6.25 GHz internal reference clock.
- Up to ± 100ppm additional CDR tracking capability for received bit frequency swing.
- 4 tap adaptive Decision Feedback Equalizer (DFE).
- Linear Equalizer and gain control.
- Separate sampler for eye mapping & extraction of ISI coefficients for equalizer adaptation.
- Independently configurable per link multi-rate digital Clock and Data Recovery (CDR).
- Bit-Slip / phase control via the control bus.
- Test features:
  - IEEE 1149.1 (DC) and 1149.6 (AC) JTAG boundary scan support.
  - RX –TX parallel loop-back.
  - BER with Five standard PRBS patterns.
  - In-service eye mapping and spot measurement (vertical and horizontal).
  - Programmable RX sampling position within the data eye.

5.2 Receiver input characteristics

Table 4 defines the specification of Receiver input.

Table 4. Receiver input characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{ICM}	Input common mode voltage	700	1000	AVCC	mV	Internally compensated
		N.A.				AC coupled
V_{IDP}	Input peak differential voltage	62.5		600	mVp	DC coupled
		62.5		600		AC coupled
V_{IDPP}	Input peak to peak differential voltage	125		1200	mVpp	DC coupled
		125		1200		AC coupled
S_{11}	Input return loss			12	dB	Measured @ 4GHz
Z_{ID}	Differential input impedance	93		107	Ohm	At frequencies < 1 GHz With proper trimming settings
Z_{ICM1}	Common mode input impedance	24	28	32	Ohm	Termination sw. closed

Table 4. Receiver input characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Z_{ICM2}	Common mode DC input impedance	2		4	kOhm	Includes leakage of the RX input pins. Termination sw. open CMV = AVCC-200mV
V_{IOFF}	Input referred offset voltage			25	mV	Includes leakage of the RX input pins. 5 sigma value, offset compensation off
J_{TD}	Deterministic jitter tolerance				UI pp	Meets IEEE802.3 XAUI and similar standards
J_{TT}	Total jitter tolerance				UI pp	
F_{OFF1}	Frequency tracking capability of CDR	-100		100	ppm	Frequency offset capability disabled. Normalized relative the actual ref. clock frequency.
F_{OFF2}	Additional frequency tracking capability of CDR	-100		100	ppm	Provided by the frequency offset capability enabled. Normalized relative the actual ref. clock frequency
T_{ODC}	RXDCLK output clock duty cycle	40		60	%	Measured at 50% points
T_{RPL}	RX pipeline latency	28		43	UI	UI refers to full rate for all modes Min for last bit, max for 1^{st} bit
T_{RAL}	RX analog latency in all modes	0		1.0	ns	

5.3 50 ohm RX pull-p line termination

The 100 ohm differential impedance is implemented as two 50 ohm variable resistors connected to AVCC and is programmable in the range of +/- 20% (5 values with step of 10%): it can be adjusted to compensate resistor fabrication process variation or eventually to try to help in the transmission media characteristic impedance matching. The chosen value of the differential impedance is common for all the Tx lanes and the Rx lanes of all the data slices.

5.4 Receiver eye mask

Figure 6 and *Table 5* define the receiver internal eye mask. These mask and values refer to the internal eye which can only be seen by the eye monitor as equalization and DFE are not included in the eye seen at the input pins.

Figure 6. Receiver internal eye mask

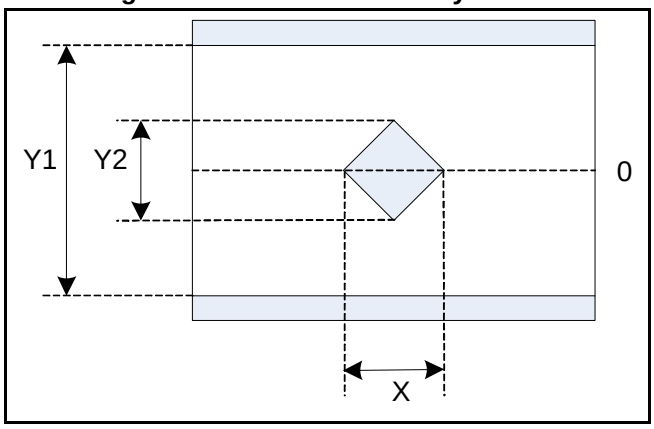


Table 5. Receiver eye mask values (indicative)

Symbol	Parameter	Value	Unit
X	Min horizontal eye opening	0.35	UI
Y1	max eye hight	1000	mVpp
Y2	Min vertical eye opening	125	mVpp

Note: All voltages are measured differentially peak to peak.

5.5 BER measurement in HSSL

The eye monitor and the BER block are both used to measure a Bit Error Rate (BER) but they are not used for the same purpose and they are not running with the same error detection criteria:

- The eye monitor is used to optimize the Rx equalizer and DFE. It compares the eye sampled data (with a timing or/and a voltage offset) versus the center sampled data. If a mismatch is found then an error is detected. The eye monitor has no hint on the received bit sequence like the BER block.
- The BER block is used to check a Tx to Rx transmission quality on a quite long period. It detects and calculates the bit error rate of a Tx lane connected to a Rx lane from the same data slice (in loopback mode) or from another HSSL data slice connected by a transmission media (line bit error rate). It compares the center sample data versus a defined bit sequence defined in the emitter (in the TX PRBS) and in the receiver (in the Rx BER block). The BER measurement is achieved by simultaneously counting two items: the detected transmission errors in a 26 bit counter named “BISTCNT” (located in the BER block) and the time elapsing in a resettable 42 bit counter named “TIMECOUNT” (clocked by MCLK).

One BER block, one TIMECOUNT counter and one eye monitor is available in each Rx lane.

6 BIST

6.1 Tx to Rx, Rx to Tx loopback

There are 4 possible loopbacks between the Tx lane and the Rx lane of the same data slice:

- Digital serial Tx to Rx loopback (for manufacturing field test and for HSSL debug): the digital serial data available on the Tx driver input is loopback at the Rx analog equalizer input. The Tx loopback amplitude is programmable through register.
- Analog serial Tx to Rx bump loopback (for manufacturing field test only): the analog serial data available on the Tx bump is loopback to the Rx input bump.
- Parallel Tx to Rx loopback: RXD<n>[19:0] is a copy of the data provided on TXD<n>[19:0] (for Soc integration test).
- Parallel Rx to Tx loopback: the 20 bit received Rx data is input to the Tx lane to be transmitted serially (for application far end loopback full duplex line transmission test (or validation) or BER transmission line characterisation).

Note: The power-down control signals should be set appropriately.

Caution: The “Tx to Rx loopback” and “Rx to Tx loopback” is only possible with Tx lane and Rx lane in the same data slice.

6.2 Boundary scan

HSSL supports IEEE 1149.1 (DC) and 1149.6 (AC) JTAG boundary scan. Boundary Scan Mode (IEEE 1149.6) is a mode allowing use of receiver’s special functionality to check and detect the connectivity conditions of the external components on board.

The HSSL includes standard JTAG scan testing capability for all of the low to medium speed internal logic circuitry, and boundary scan capability for all I/O pins and bumps. This includes the accurately terminated high-speed differential serial input and output pins, which, however, maintain their ~100 ohm termination load between the two pins of each differential pair even when in boundary scan mode. This allows these interfaces to achieve the best possible matching with the lowest possible return reflections, and allows boundary scan to use the true mission mode conditions. The common-mode point on the 100 ohm termination in the receiver does have a low impedance switch to the AVCC termination supply rail to allow it to be disconnected if wanted for special testing, start-up, or power-down.

7 General electrical performance and requirements

Table 6 provides power consumption numbers for several cases for data-slice and for the clock-slice.

Table 6. Worst case HSSL power dissipation

Full rate (Gb/s)	Full HSSL (mW)	Clock slice only (mW)	One data slice (mW)(1)
6.25	960 (TBC)	160 (TBC)	200 (TBC)

1. Averaged per HSSL for a macro of 4 SerDes and one clock slice 20mA transmitter drive current.

Table 7. Absolute maximum and operating conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{MAX}	Maximum temperature			150	°C	Maximum without damage.
$AVCC_{MAX}$	Sustained maximum AVCC			1.32	V	Maximum without damage.
VDD_{MAX}	Sustained maximum VDD			1.32	V	Maximum without damage.
AVCC	Operating analog supply	1.14	1.2	1.26	V	Supplied via internal bumps.
VDD	Operating digital supply	1.14	1.2	1.26	V	Supplied from the ASIC core.
V_{CMLMAX}	Sustained I/O voltage	-0.6		1.8	V	Sustained peak for CML pins. Not to be used long term.
I_{PINMAX}	Current into any I/O pins	-100		+100	mA	Peak pin current excluding ESD
V_{ASN}	Analog supply noise (AC)			30	mVpp	At the package pin. Note: Each mV of supply ripple will add ~0.5 ps of deterministic jitter to the Tx outputs.
T_J	Operating temperature	-40	+85	+125	°C	Operating junction temperature
VESD	ESD protection limit			2	kV	Assumes human body model
	Latch up and hot-plugs limits					Same as V_{CMLMAX} and I_{PINMAX}

8 Radiation target performance

This high performance SERDES IP architecture was originally designed for communication networking market. Its intrinsic high robustness to terrestrials environment perturbations made it selected to be adapted to Space applications.

Intensive analysis of the sensitivity to radiations of all the blocks/cells was conducted and the design was significantly reworked while keeping original architecture and speed performance.

Specific layout precautions, fully compatible with SoC design practices, were applied to insure Single Event Latch-up (SEL) immunity up to 60 MeVcm2/mg Heavy Ions at 125°C Tj and Max voltage supply (ECSS-Q-60-15C standard).

Systematic usage of ST hardened cells library in combination with Triple Mode Redundancy (TMR) techniques were also implemented to ensure that no Single Event Functional Interrupt (SEFI) can occur up to 60 Mev/cm2/mg.

A BER < 10E-14 is obtained under terrestrial conditions, BER minimized degradations under different radiations (protons, heavy ions) have been characterized allowing users to determine the global system performance versus the space mission profile.

9 Revision history

Table 8. Document revision history

Date	Revision	Changes
22-May-2015	1	Initial release.
28-Oct-2015	2	Update document properties