150 V half-bridge gate driver for automotive applications

SO-8

Product status link
A2387

Product label
SUSTAINABLE TECHNOLOGY

Features

- AEC-Q100 qualified
- High voltage rail up to 150 V
- dV/dt transient immunity ±50 V/ns in full temperature range
- Driver current capability:
  - 400 mA source
  - 650 mA sink
- Switching times 50/30 ns rise/fall with 1 nF load
- CMOS/TTL Schmitt-trigger inputs with hysteresis and pull down
- Internal bootstrap diode
- Outputs in phase with inputs
- Interlocking function

Application

- HID ballasts
- DC-DC converters
- On-board charger (OBC)
- Automotive HVAC compressor modules
- Fans and pumps

Description

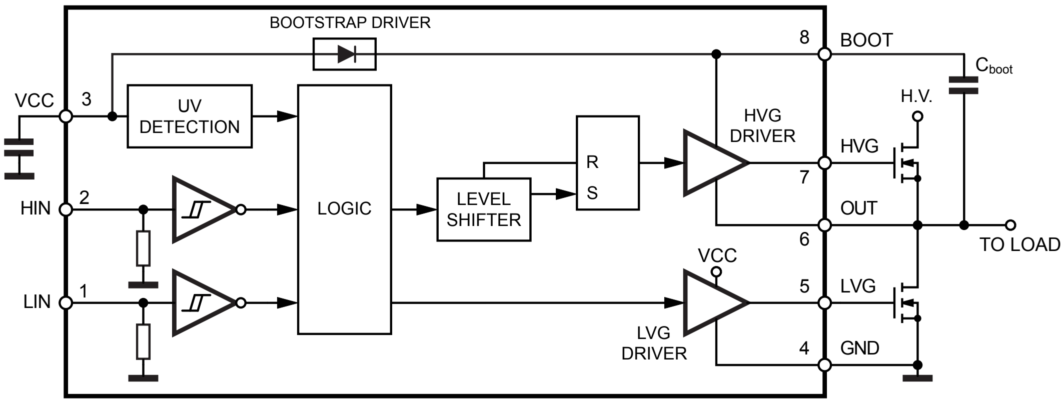
The A2387 is a single chip half-bridge gate driver for N-channel power MOSFETs or IGBTs.

The high-side (floating) section is designed to stand a voltage rail of up to 150 V. The logic inputs are CMOS/TTL compatible for easy interfacing of the microcontroller or DSP.

The A2387 features supply UVLOprotection and interlocking to avoid cross-conduction conditions. It operates in the temperature range -40 °C to 125 °C.

1 Block diagram

Figure 1. A2387 block diagram



2 Pin description

Figure 2. Pin connection

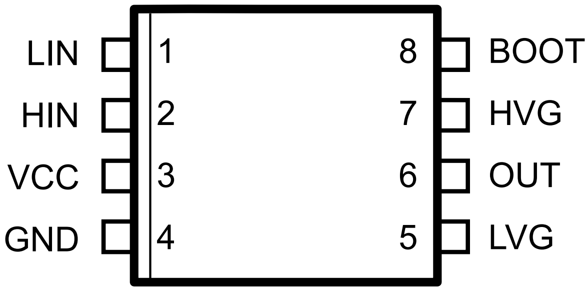


Table 1. Pin descritpion

Pin N.	Name	Type	Function
1	LIN	I	Low-side driver logic input
2	HIN	I	High-side driver logic input
3	VCC	P	Low voltage power supply
4	GND	P	Ground
5	LVG (1)	O	Low-side driver output
6	OUT	P	High-side driver floating reference
7	HVG (1)	O	High-side driver output
8	BOOT	P	Bootstrap supply voltage

1. *The circuit provides less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA). This allows the omitting of the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.*

3 Electrical data

3.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 2 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages referred to ground pins unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage	-0.3 to 18	V
V_{OUT}	Output voltage	V_{BOOT}-18 to V_{BOOT}+0.3	V
V_{BOOT}	Bootstrap voltage	-0.3 to 168	V
V_{HVG}	High-side gate output voltage	V_{OUT}-0.3 to V_{BOOT}+0.3	V
V_{LVG}	Low-side gate output voltage	-0.3 to VCC+0.3	V
V_i	Logic input voltage	-0.3 to VCC+0.3	V
dV_{OUT}/dt	Allowed output slew rate	50	V/ns
P_{tot}	Total power dissipation (T_{amb} = 85 °C)	750	mW
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-50 to 150	°C
ESD	Human body model	2	kV

3.2 Recommended operating conditions

All voltages referred to ground pins unless otherwise specified. The junction temperature must be maintained within recommended operating conditions with proper thermal design.

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
VCC	3	Supply voltage		6.3	17	V
V_{BO} (1)	8 - 6	Floating supply voltage			17	V
V_{OUT}		Output voltage		-6 (2)	150	V
f_{SW}		Switching frequency	HVG, LVG load C_L = 1 nF		400	kHz
T_j		Junction temperature		-40	125	°C

1. *$V_{BO} = V_{BOOT} - V_{OUT}$*
2. *LVG off. VCC = 12 V*

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(J-A)}$	Thermal resistance junction-to-ambient	150	°C/W

4 Electrical characteristics

Testing conditions: , VCC = 15 V; T_j = -40 °C to +125 °C, unless otherwise specified.

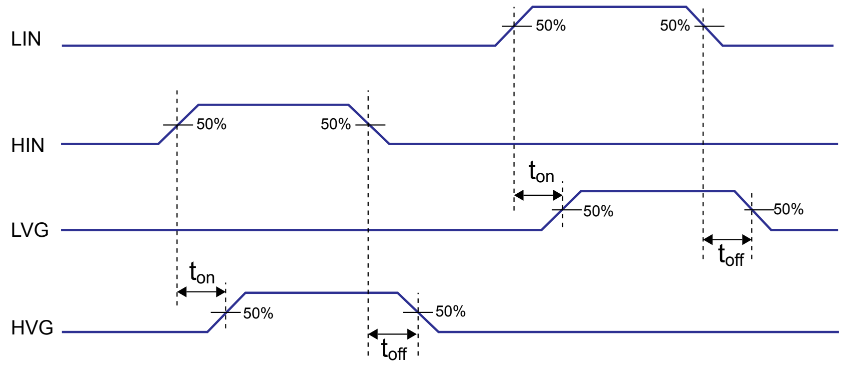
Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Logic section supply						
VCC_{thON}	VCC UVLO turn-ON threshold		5.5	6.0	6.3	V
VCC_{thOFF}	VCC UVLO turn-OFF threshold		5.0	5.5	6.0	V
VCC_{hys}	VCC UVLO hysteresis		0.3	0.5	0.7	V
I_{QCC}	VCC quiescent supply current			250	320	µA
I_{QCCU}	VCC undervoltage supply current	VCC ≤ 5.0 V		150	220	µA
Bootstrapped supply voltage section (1)						
I_{QBO}	V_{BO} quiescent current	HVG ON			100	µA
I_{LK}	High voltage leakage current	$V_{HVG} = V_{OUT} = V_{BOOT}$ = 150 V			10	µA
R_{DBOOT}	Bootstrap diode on-resistance (2)	LVG ON		125		Ω
Output driving buffers						
I_{SO}	High/low-side source short circuit current	$V_{IN} = V_{ih}$ (t_p < 10 µs)	300	400		mA
I_{SI}	High/low-side sink short circuit current	$V_{IN} = V_{ih}$ (t_p < 10 µs)	450	650		mA
Logic inputs						
V_{ih}	High level logic threshold voltage		3.2			V
V_{il}	Low level logic threshold voltage				1.4	V
I_{ih}	High level logic input current	V_{IN} = 15 V	8	20	40	µA
I_{il}	Low level logic input current	V_{IN} = 0 V			1	µA
Dynamic characteristics (see Figure 3)						
t_{on}	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V, V_{BOOT} = VCC C_L = 1 nF	40	120	240	ns
t_{off}	High/low-side driver turn-off propagation delay		40	110	210	ns
t_r	Rise time	C_L= 1 nF		50	100	ns
t_f	Fall time			30	80	ns

1. *$V_{BO} = V_{BOOT} - V_{OUT}$*
2. *R_{DBOOT} is tested in the following way:*

$$R_{DBOOT} = \frac{(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})}{I_1(V_{CC},\ V_{BOOT1}) - I_2(V_{CC},\ V_{BOOT2})}$$

Figure 3. Timing of input-output signals; turn-on and off propagation delays



5 Input logic

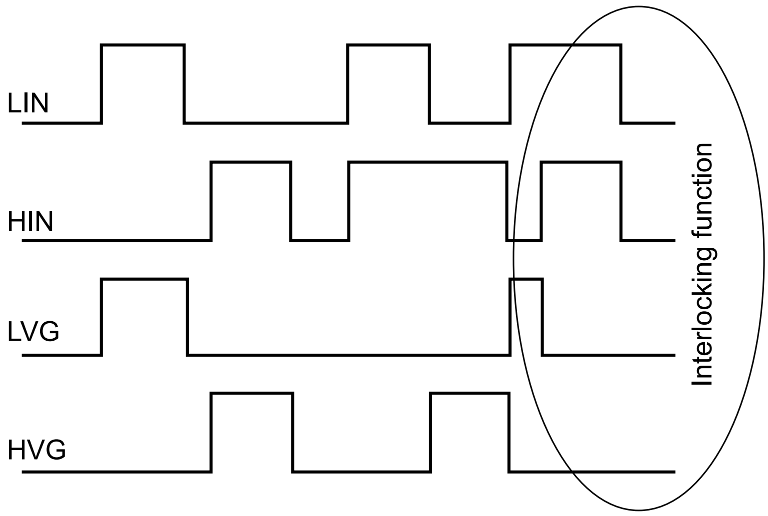
The A2387 input logic is VCC (17 V) compatible.

An interlocking feature is offered (see Table 6) to avoid undesired simultaneous turn-on of both power switches.

Table 6. Truth table

INPUT		OUTPUT	
HIN	LIN	HVG	LVG
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

Figure 4. Timing of input/output signals; interlocking waveforms definition

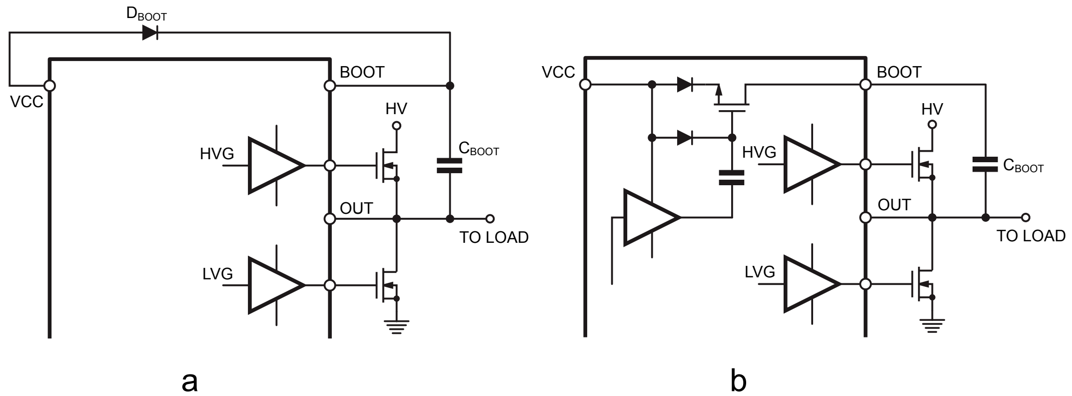


6 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high-voltage fast recovery diode (Figure 5 a).

In the A2387 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in Figure 5 b. An internal charge pump (Figure 5 b) provides the DMOS driving voltage.

Figure 5. Bootstrap driver



6.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}} \tag{1}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It must be: $C_{BOOT} >> C_{EXT}$.

For example: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG must be supplied for a long period, the C_{BOOT} selection must take into account also the leakage and quiescent losses.

For example: HVG steady-state consumption is lower than 100 µA, therefore, if HVG t_{on} is 5 ms, C_{BOOT} must supply 0.5 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 0.5 V.

The internal bootstrap driver offers a big advantage: the external fast recovery diode can be avoided (it usually has very high leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and, in the meantime, the LVG is on. The charging time (t_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it must be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DBOOT} (typical value: 125 Ω). This drop can be neglected at low switching frequency, but it should be taken into account when operating at high switching frequency.

Eq. (2) is useful to compute the drop on the bootstrap DMOS:

Equation 2

$$V_{drop} = I_{charge} \cdot R_{DBOOT} \rightarrow V_{drop} = \frac{Q_{gate}}{t_{charge}} \cdot R_{DBOOT} \tag{2}$$

where Q_{gate} is the gate charge of the external power MOS, R_{DBOOT} is the ON-resistance of the bootstrap DMOS, and t_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the t_{charge} is 5 µs. In fact:

Equation 3

$$V_{drop} = \frac{30\ nC}{5 \mu s} \cdot\ 125\ \Omega \sim 0.8\ V \tag{3}$$

V_{drop} should be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

7 Typical characteristics

Figure 6. Typical rise and fall times vs load capacitance

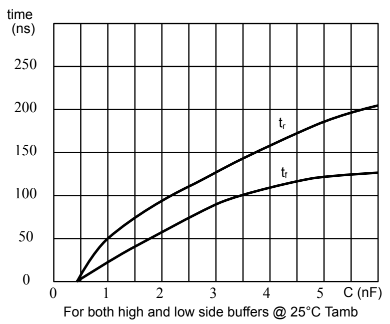


Figure 7. Quiescent current vs supply voltage

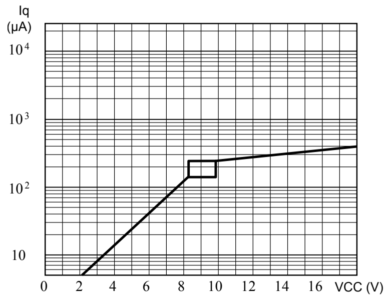


Figure 8. Turn-on time vs temperature

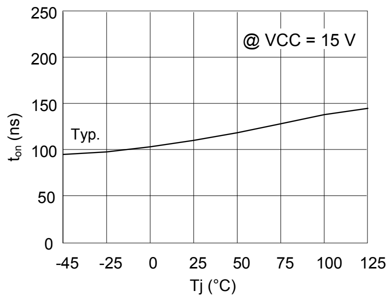


Figure 9. Turn-off time vs. temperature

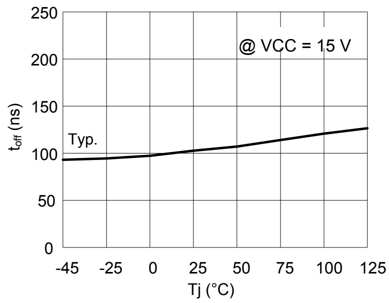


Figure 10. Output source current vs temperature

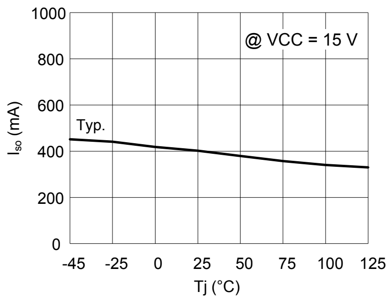
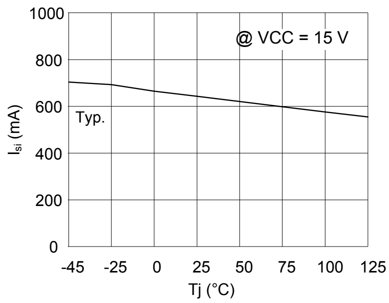


Figure 11. Output sink current vs temperature



8 Package information

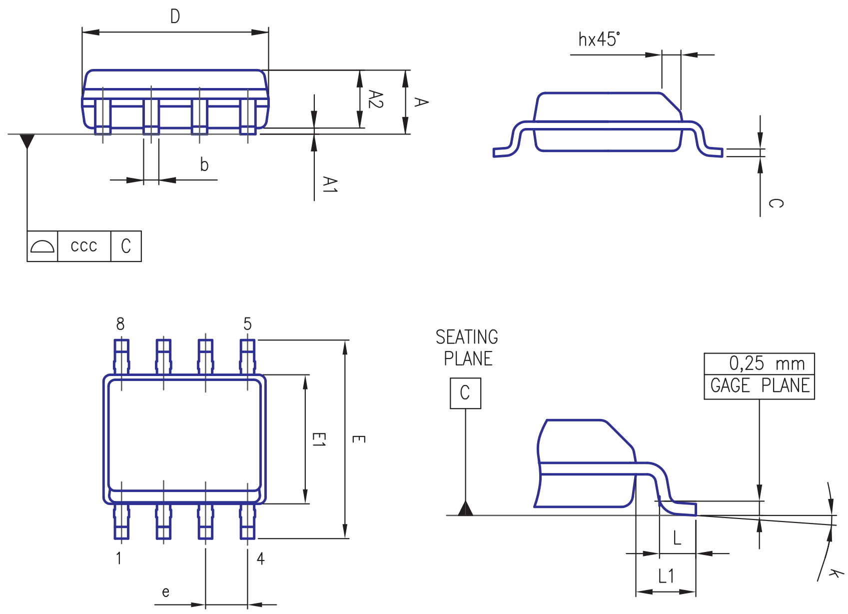
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 SO-8 package information

Table 7. **SO-8 package dimensions**

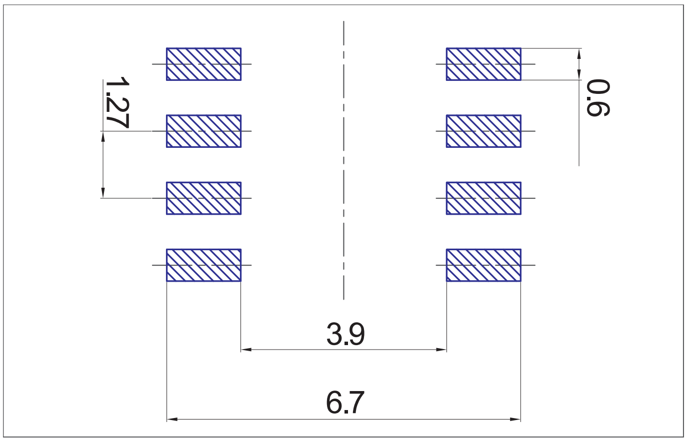
Symbol	Dimensions [mm]		
	Min	Typ	Max
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Figure 12. **SO-8 package outline**



8.2 Suggested footprint

Figure 13. **SO-8 suggested footprint**



9 Ordering information

Table 8. Order code

Order Code	Package	Package marking	Packaging
A2387D	SO-8	A2387D	Tube
A2387DTR	SO-8	A2387D	Tape and reel

Revision history

Table 9. **Document revision history**

Date	Version	Changes
05-Mar-2024	1	Initial release.

Contents

List of tables

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