

Rad hard low voltage CMOS 16-bit d-type latch (3-state) with 3.6 V tolerant inputs and outputs

Datasheet - production data



Description

The 54VCXH162374 is a low voltage CMOS 16 bit d-type flip-flop with 3 state outputs non inverting fabricated with sub-micron silicon gate and five-layer metal wiring C²MOS technology. It is ideal for low power and very high speed 1.8 to 3.6 V applications; it can be interfaced to 3.6 V signal environment for both inputs and outputs. These 16 bit d-type flip-flops are controlled by two clock inputs (nCK) and two output enable inputs (nOE). On the positive transition of the (nCK), the nQ outputs will be set to the logic state that were setup at the nD inputs. While the (nOE) input is low, the 8 outputs (nQ) will be in a normal state (HIGH or LOW logic level) and while high level the outputs will be in a high impedance state. Any output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are OFF.

Features

- 1.8 to 3.6 V operating voltage
- High speed outputs:
 - $t_{PD} = 3.4 \text{ ns}$ at $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
 - $t_{PD} = 4.8 \text{ ns}$ at $V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$
- Symmetrical impedance outputs:
 - $|I_{OH}| = I_{OL} = 12 \text{ mA (min.)}$ at $V_{CC} = 3.0 \text{ V}$
 - $|I_{OH}| = I_{OL} = 8 \text{ mA (min.)}$ at $V_{CC} = 2.3 \text{ V}$
- Power down protection on inputs and outputs
- 26Ω series resistors in outputs
- Bus hold provided on both sides
- Cold spare function
- 300 krad(Si) Total ionizing dose (TID)
- No SEL, no SEU and no SET at 110 MeV.cm²/mg LET
- QML-V qualified
- SMD 5962F05212

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1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

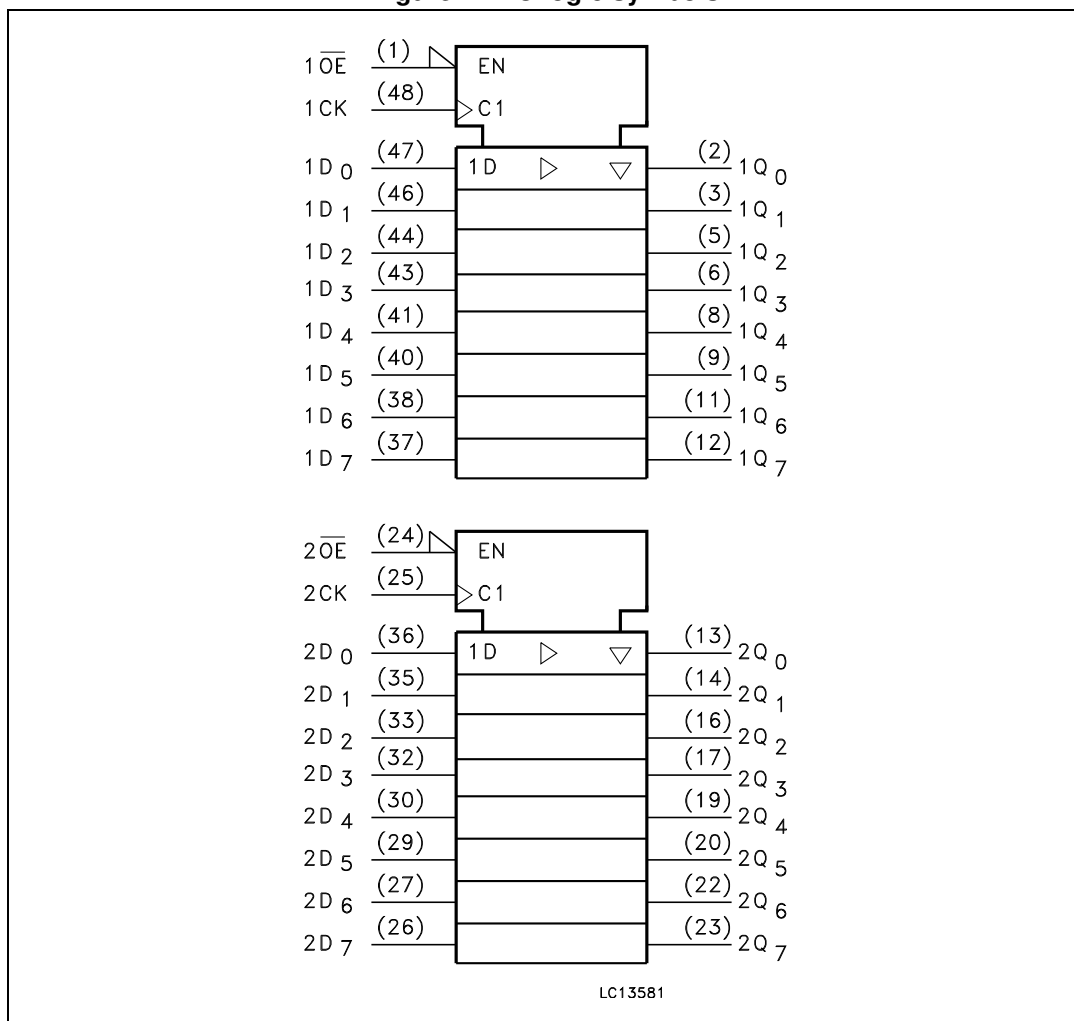


Figure 2. Input and output equivalent circuit

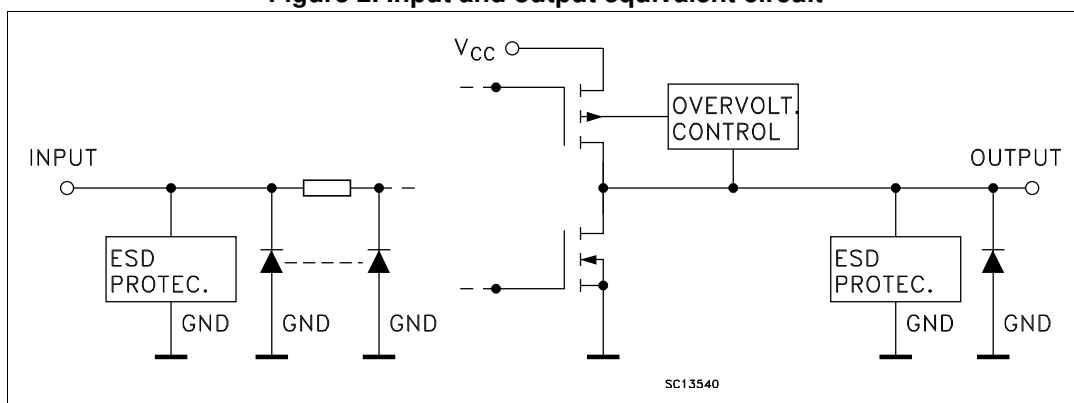
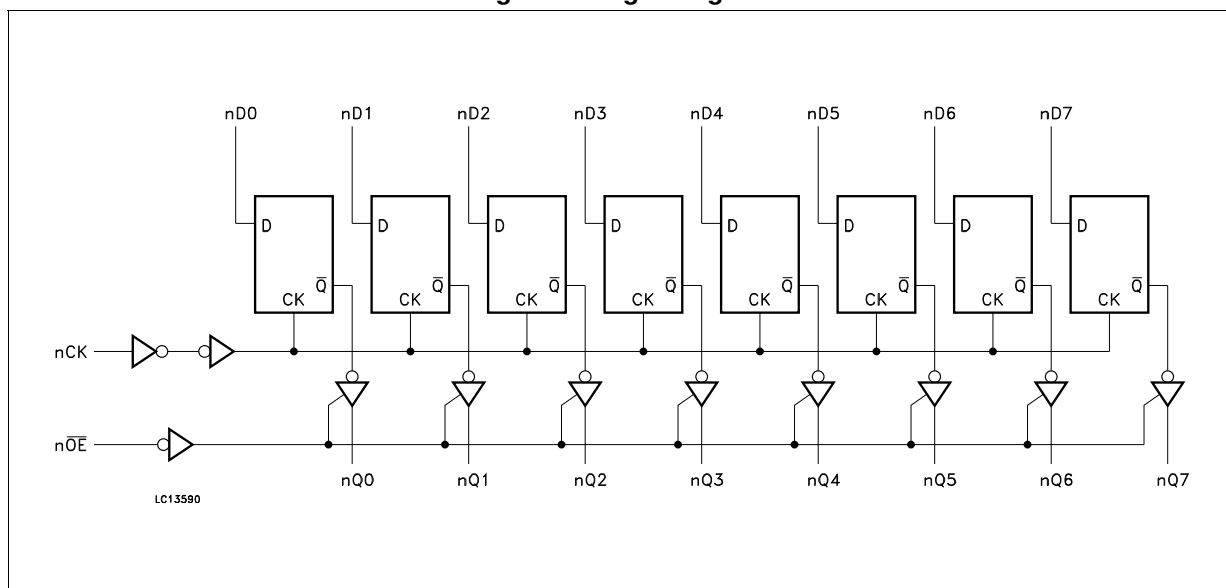


Figure 3. Logic diagram

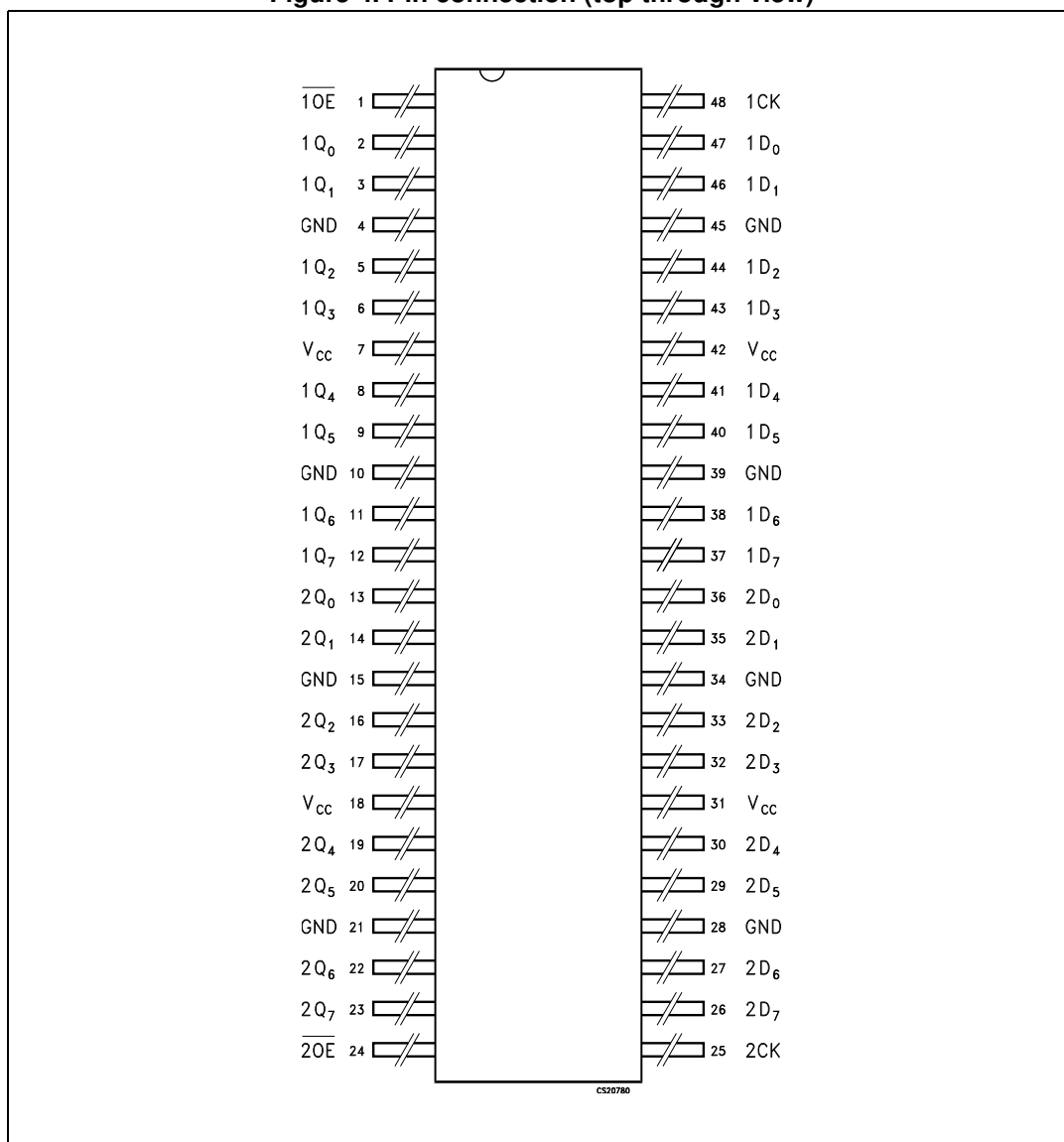


Note: This logic diagram has not to be used to estimate propagation delays

2 Pin settings

2.1 Pin connection

Figure 4. Pin connection (top through view)



2.2 Pin description

Table 1. Pin description

Pin n°	Symbol	Name and function
1	$1\overline{OE}$	3 state output enable input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-state outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-state outputs
24	$2\overline{OE}$	3 state output enable input (Active LOW)
25	2CK	Clock input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1CK	Clock input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	V _{CC}	Positive supply voltage

2.3 Truth table

Table 2. Truth table

Inputs			Output
OE	LE	D	Q
H	X	X	Z
L	$\overline{\text{L}}$	X	No change ⁽¹⁾
L	$\overline{\text{L}}$	L	L
L	$\overline{\text{L}}$	H	H

1. Q outputs are latched at the time when the LE input is taken low logic level.

Note: X = Do not care; Z = High impedance

3 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +4.6	V
V_I	DC input voltage	-0.5 to +4.6	V
V_O	DC output voltage (OFF state)	-0.5 to +4.6	V
V_O	DC output voltage (high or low state) ⁽¹⁾	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	- 50	mA
I_{OK}	DC output diode current ⁽²⁾	- 50	mA
I_O	DC output current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current per supply pin	± 100	mA
P_D	Power dissipation	400	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	260	°C
R_{thjc}	Thermal resistance junction-to-case ⁽³⁾	22	°C/W
ESD	HBM ⁽⁴⁾ as MIL STD 883 method 3015	2	kV

1. I_O absolute maximum rating must be observed
2. $V_O < GND$, $V_O > V_{CC}$
3. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
4. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

3.1 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.8 to 3.6	V
V_I	Input voltage	-0.3 to 3.6	V
V_O	Output voltage (OFF state)	0 to 3.6	V
V_O	Output voltage (high or low state)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or low level output current ($V_{CC} = 3.0$ to 3.6 V)	± 12	mA
I_{OH}, I_{OL}	High or low level output current ($V_{CC} = 2.3$ to 2.7 V)	± 8	mA
T_{op}	Operating temperature	-55 to 125	°C
dt/dv	Input rise and fall time ⁽¹⁾	0 to 10	ns/V

1. V_{IN} from 0.8 V to 2 V at $V_{CC} = 3.0$ V

4 Electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test condition		Value		Unit
		V _{CC} (V)		-55 to 125°C		
				Min.	Max.	
V _{IC}	Negative input clamp voltage	1.8 to 3.6	I _{IN} = -1 mA	-0.4	-1.5	V
	Functional tests	3.6	V _{IN} = V _{IH} min or V _{IL} max, verify output V _{OUT}	L	H	
		2.7		L	H	
		2.3		L	H	
		1.8		L	H	
V _{IH}	High level input voltage	3.6		2		V
		3		2		
		2.7		2		
		2.3		1.6		
		1.8		1.2		
V _{IL}	Low level input voltage	3.6			0.8	V
		3			0.8	
		2.7			0.8	
		2.3			0.7	
		1.8			0.4	
V _{OH}	High level output voltage	3.6	I _O = -100 μA	3.4		V
		3	I _O = -8 mA	2.4		
			I _O = -12 mA	2.2		
		2.7	I _O = -100 μA	2.5		
			I _O = -6 mA	2.2		
		2.3	I _O = -6 mA	1.8		
			I _O = -8 mA	1.7		
	1.8	I _O = -4 mA	1.4			

Table 5. DC specifications

Symbol	Parameter	Test condition		Value		Unit
		V _{CC} (V)		-55 to 125°C		
				Min.	Max.	
V _{OL}	Low level output voltage	3.6	I _O = 100 μA		0.2	V
		3	I _O = 8 mA		0.55	
			I _O = 12 mA		0.8	
		2.7	I _O = 100 μA		0.2	
			I _O = 6 mA		0.4	
		2.3	I _O = 6 mA		0.4	
			I _O = 8 mA		0.6	
1.8	I _O = 4 mA		0.3			
I _I	Input leakage current	3.6	V _{IN} = 0 V for input under test, V _{IN} = V _{CC} or 0 V for all other input		± 5	μA
I _{CC}	Quiescent supply current, output high or low	3.6	V _{IN} = V _{CC} or 0V		100	μA
I _{CCZ}	Quiescent supply current, output three-state	3.6	V _{IN} = V _{CC} or 0V		100	μA
ΔI _{CC}	Quiescent supply current delta, TTL input level	3.6	input under test: V _{IN} = V _{CC} - 0.6 V for all other inputs: V _{IN} = V _{CC} or 0 V		750	μA
I _{I(HOLD)}	Input hold current	3	V _{IN} = V _{IL} = 0.8 V	75		μA
			V _{IN} = V _{IH} = 2.0 V	-75		
I _{OFF}	Power off leakage current	0	V _{IN} or V _O = 0 to 3.6 V		10	μA
I _{OZ}	High impedance output leakage current	3.6	V _{IN} = V _{IH} or V _{IL} V _O = 0 or 3.6 V		± 10	μA

Table 6. Dynamic switching characteristics

Symbol	Parameter	Test condition		Value		Unit
		V _{CC} (V)		T _A = 25 °C		
				Min.	Max.	
V _{OLP}	Low level ground bounce noise ⁽¹⁾	3.3	V _{IL} = 0 V, V _{IH} = V _{CC} C _L = 30pF, R _L = 500 Ω 25 °C	4	600	mV
V _{OLV}				4	-300	
V _{OHP}	High level ground bounce noise ⁽¹⁾	3.3		4	1000	mV
V _{OHV}				4	-1250	

1. Guaranteed by design.

$$C_L = 30 \text{ pF}, R_L = 500 \Omega$$

Table 7. AC electrical characteristics

Symbol	Parameter	Test conditions	Value		Unit
		V _{CC} (V)	-55 to 125 °C		
			Min.	Max.	
F _{max}	Maximum clock frequency	3.6	235		MHz
		2.3	190		
		1.8	110		
t _{PLH} t _{PHL}	Propagation delay time, mCLK to mQn	3.6	0.8	4.5	ns
		2.3	1.0	5.5	
		1.8	1.0	10.2	
t _{PZL} t _{PZH}	Output enable time, mOE/ to mQn	3.6	0.8	4.5	
		2.3	1.0	6.2	
		1.8	1.0	11	
t _{PLZ} t _{PHZ}	Output disable time mOE/ to mQn	3.6	0.8	4.6	
		2.3	1.0	5.1	
		1.8	1.0	8.7	

Table 7. AC electrical characteristics

t_s	Setup time, high or low, mDn to mCLK ⁽¹⁾	3.6	1.0		ns
		2.3	1.0		
		1.8	2.5		
t_h	Hold time, high or low, mDn to mCLK ⁽¹⁾	3.6	1.5		
		2.3	1.5		
		1.8	2.5		
t_w	mLE pulse width, high ⁽¹⁾	3.6	1.5		
		2.3	1.5		
		1.8	4.0		
t_{OSLH} t_{OSHL}	Output to output skew time ⁽¹⁾ ⁽²⁾	2.3 to 2.7		0.5	ns
		3.0 to 3.6		0.5	

1. Parameter guaranteed by design

2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

Table 8. Capacitive characteristics

Symbol	Parameter	Test condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input capacitance	0		4		10	pF
C _{OUT}	Output capacitance	3.3		4		12	pF
C _{PD}	Power dissipation capacitance (1)	3.3	f _{IN} = 1 MHz	4		80	pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation.
 $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)

5 Test circuit

Figure 5. Test circuit

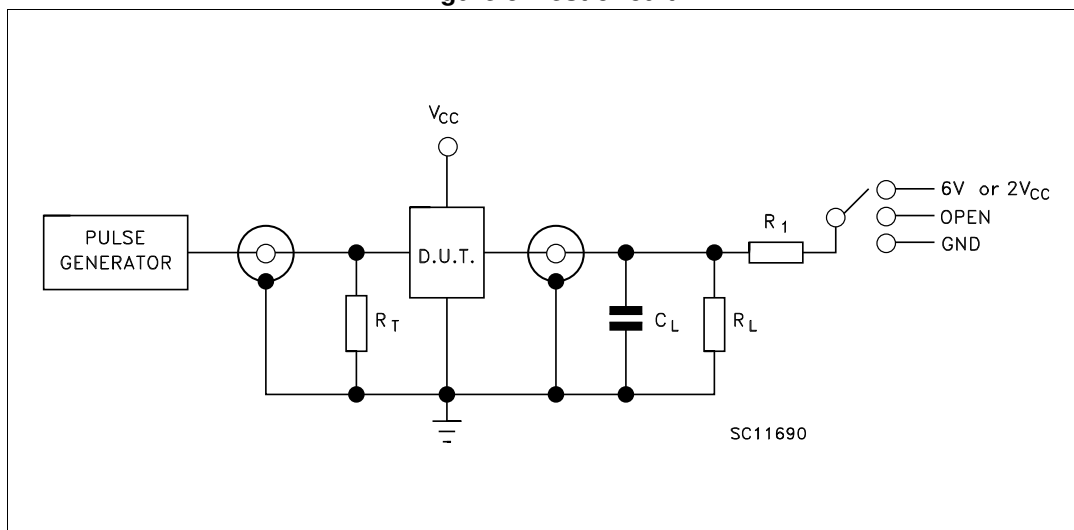


Table 9. Test circuit

Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ} ($V_{CC} = 3.0$ to 3.6 V)	6 V
t_{PZL} , t_{PLZ} ($V_{CC} = 1.8$ to 2.7 V)	$2 V_{CC}$
t_{PZH} , t_{PHZ}	GND

$C_L = 30$ pF or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

6 Waveforms

Table 10. Waveform symbol value

Symbol	V_{CC}	
	3.0 to 3.6 V	1.8 V and 2.3 to 2.7 V
V_{IH}	2.7 V	V_{CC}
V_M	1.5 V	$V_{CC}/2$
V_X	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V
V_Y	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V

Figure 6. Waveform - nCK TO Qn propagation delays, nCK maximum frequency, Dn TO nCK setup and hold times ($f = 1$ MHz; 50% duty cycle)

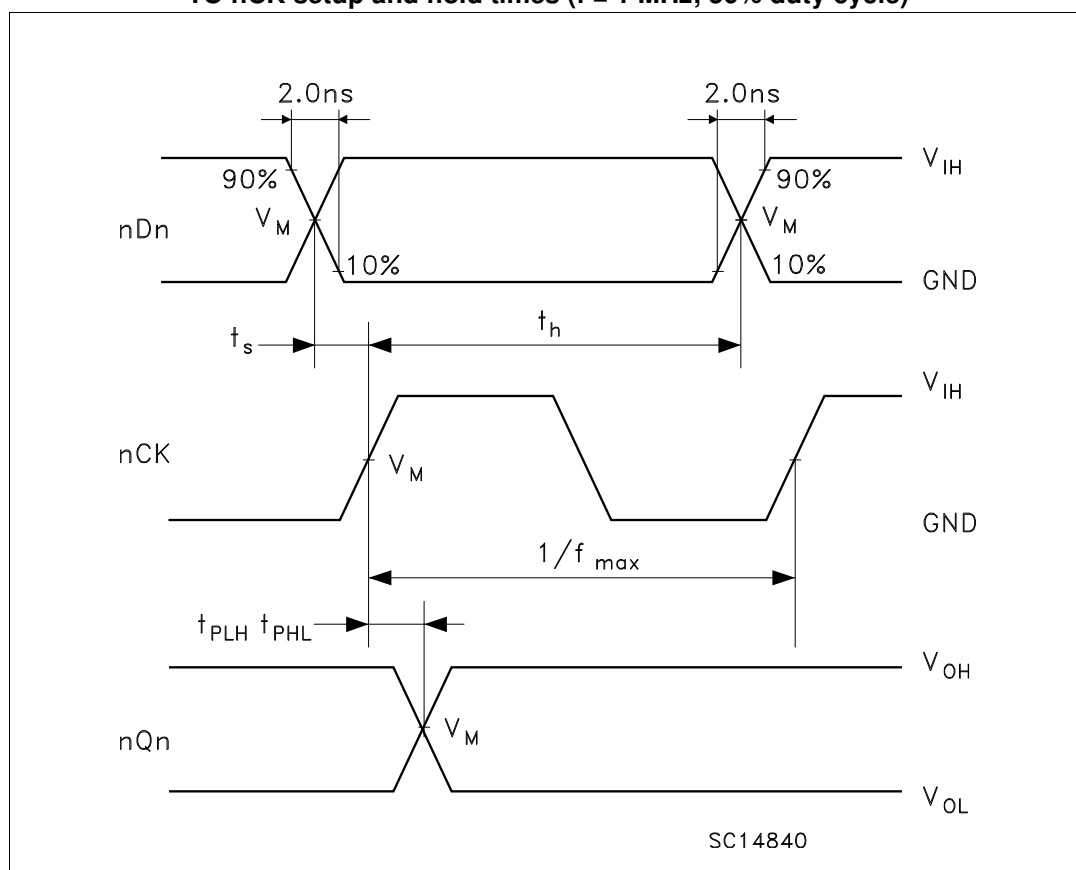
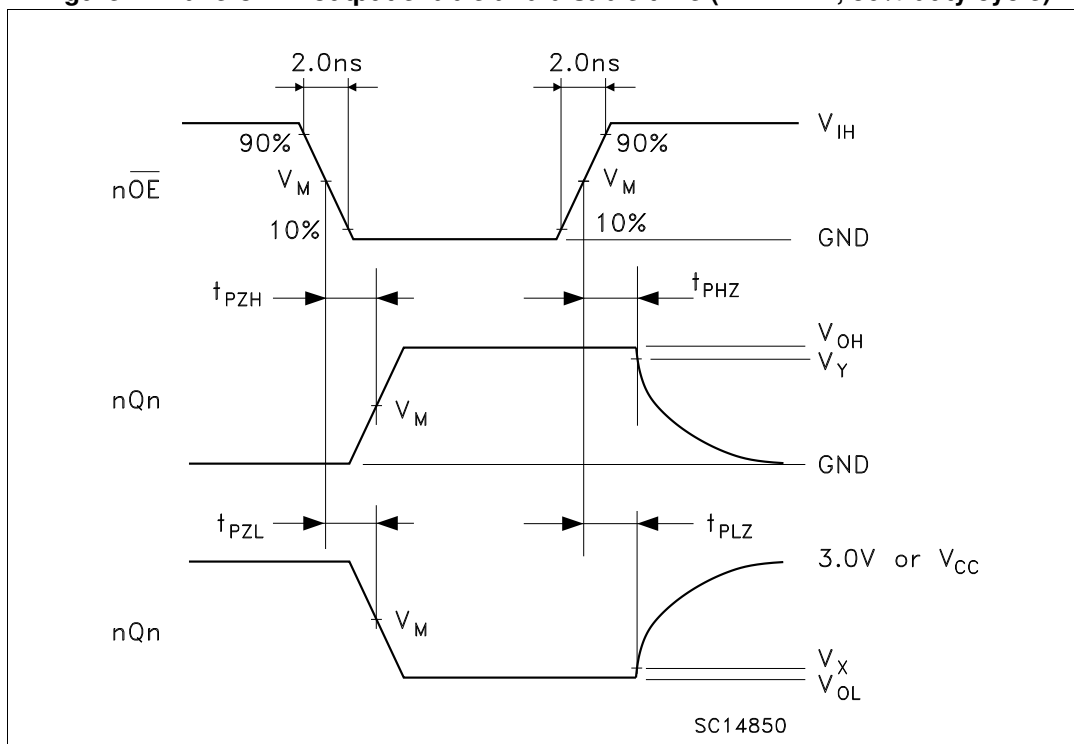
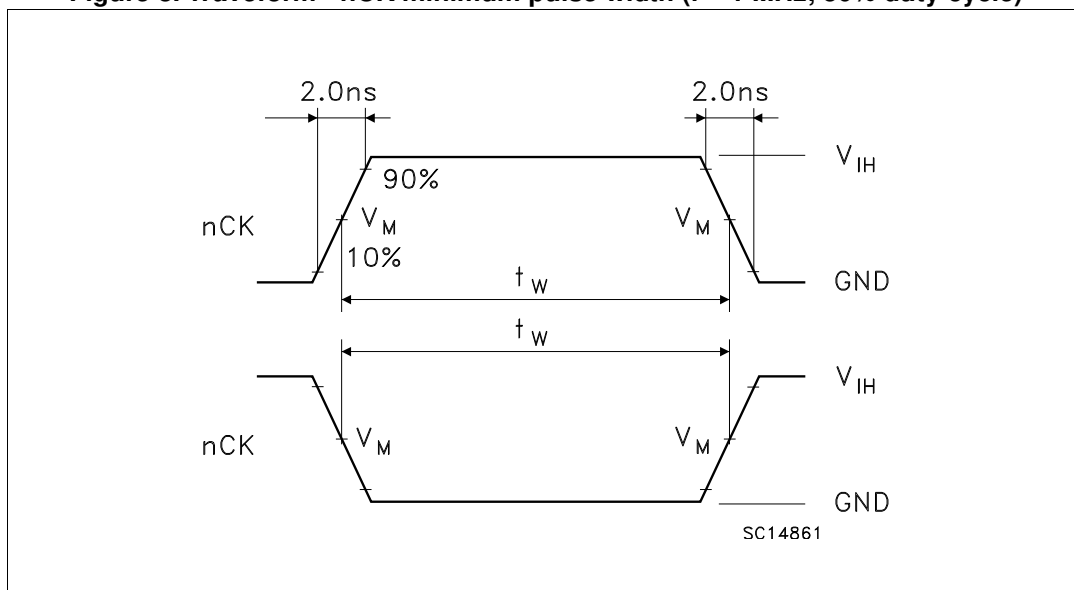


Figure 7. Waveform - output enable and disable time ($f = 1\text{ MHz}$; 50% duty cycle)Figure 8. Waveform - nCK minimum pulse width ($f = 1\text{ MHz}$; 50% duty cycle)

7 Package mechanical data

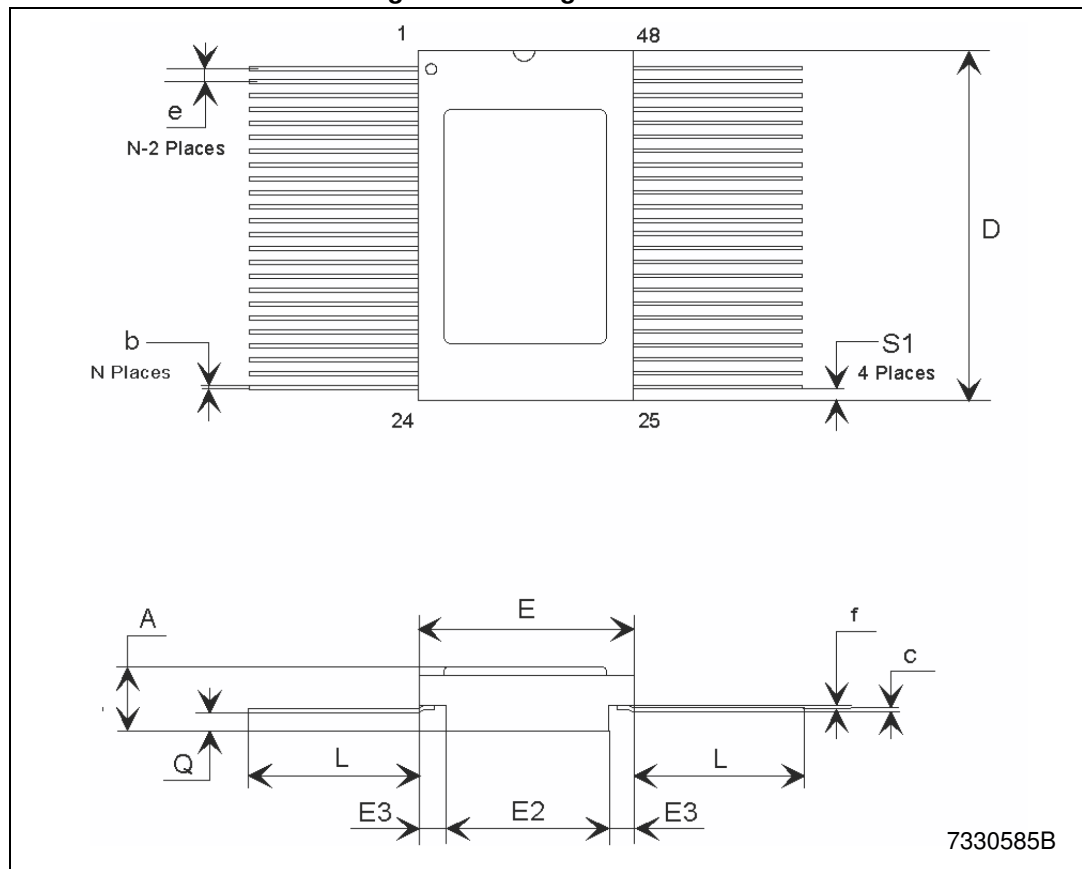
54VCXH162374 products are supplied into ceramic body / metal lid hermetic Flat 48-pin space package.

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 11. Flat-48 (MIL-STD-1835) mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	6.85	8.38	9.40	0.270	0.330	0.370
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

Figure 9. Package dimension



Note: The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

8 Order codes

Table 12. Ordering information

Order code	SMD ⁽¹⁾	Quality level	Package	Marking ⁽²⁾	Finishing	Packing
RHRXH162374K1	-	Engineering Model	Flat-48	RHRXH162374K1	Gold	Strip Pack
RHFXH162374K03V	5962F05212	QML-V Flight	Flat-48	5962F0521202VXC		
RHFXH162374K05V	5962F05212	QML-V Flight	Flat-48 with grounded lid	5962F0521202VYC		

1. Standard microcircuit drawing.
2. Specific marking only. Complete marking includes the following:
 - ST logo
 - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
 - Country of origin (FR = France)

Other information

Date code:

The date code is structured as engineering model: EM xyywwz

where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 13. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID
QML-V flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

9 Revision history

Table 14. Document revision history

Date	Revision	Changes
09-Jul-2004	1	First release
17-May-2005	2	SMD qualified
19-Jun-2006	3	300 Krad bullet updated, new template, mechanical data updated
25-Jul-2007	4	Typo in Table 12 on page 14
17-Sep-2008	5	Updated cover page
23-Sep-2009	6	Updated Table 13 on page 16
02-Aug-2011	7	Added Note: on page 15 and in the "Pin connections" diagram on the coverpage
04-Jun-2024	8	Updated figure, features and description on the cover page, Table 3 , Table 5 , Table 6 , Table 7 , Table 8 and Table 12

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