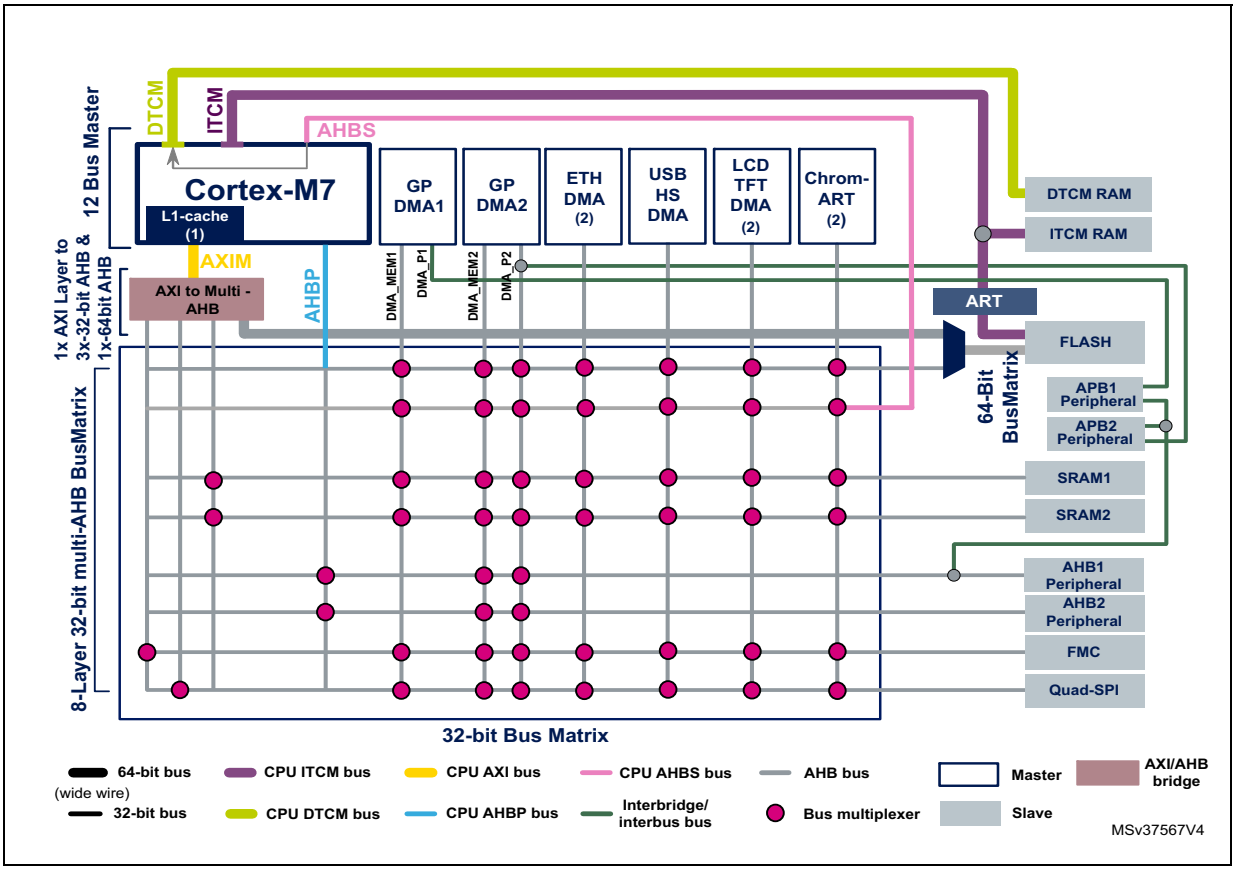
X-CUBE-32F7PERF

STM32F7 performance software expansion for STM32Cube

Data brief

Features

- STM32F7 Series performance demonstrator
- Code execution and data storage in different memory locations
- Instruction cache (I-Cache)
- Data cache (D-Cache)
- ST ART Accelerator™ performances in multi-master configuration



1. I-Cache and D-cache size for:
   - STM32F74xxx/STM32F75xxx devices: 4 Kbytes
   - STM32F72xxx/STM32F73xxx devices: 8 Kbytes
   - STM32F76xxx/STM32F77xxx devices: 16 Kbytes
2. Masters not available in STM32F72xxx and STM32F73xxx devices.

Description

This firmware, called X-CUBE-32F7PERF, aims to demonstrate the performance of the STM32F7 Series architecture (see figure on the first page), including the Cortex® -M7, the CPU caches (instruction and data caches) and its memory interfaces.

The ST ART Accelerator™ is provided to unleash the Cortex® -M7 core performance and to allow 0-wait-state-like execution from the Flash memory at the CPU frequency up to 216 MHz.

The Bus Matrix and the AXI-to-AHB bridge, running at the same CPU frequency, interconnect the core, the masters and the slaves, minimizing the latency.

The firmware is provided with two projects for STM32756G-EVAL, STM32F769I-EVAL and STM32F723E-DISCO boards: stm32f7_performances and stm32f7_performances_DMAs.

The first project comes with several sub-project configurations. Each of them allows the execution of the application code and the data storage in different memory locations, that is, internal memories as well as external memories.

In the case of the stm32f7_performances project, there are different combinations of enabling or disabling for I-Cache, D-Cache and ST ART Accelerator™ in each subproject configuration.

The different combinations present in the project are there to show in which case the user should enable/disable the I-Cache, the D-Cache and the ST ART Accelerator™.

The memory location, internal or external, does not impact the performance. The proposed use case is the FFT (fast Fourier transform) example, provided in the CMSIS library.

The second project comes with three subproject configurations. They are based on the same skeleton than the first project as well as in the FFT computation and they give the possibility to activate some DMA (direct memory access) transfers, to evaluate the STM32F7 Series architecture performances in several scenarios.

The two examples are provided with Keil® MDK-ARM, IAR Embedded Workbench® for ARM (EWARM) and System Workbench for STM32 (SW4STM32) toolchains and can easily be ported to any other toolchain.

For more details refer to the *STM32F7 Series system architecture and performance* application note (AN4667).

Ordering information

X-CUBE-32F7PERF is available for free download from the *www.st.com* website.

Revision history

Table 1. Document revision history

Date	Revision	Changes
23-Jun-2015	1	Initial release.
02-Dec-2015	2	Updated *Features* and *Description*.
30-Sep-2016	3	Updated figure and *Description* section.
21-Feb-2017	4	Updated figure and *Description*.