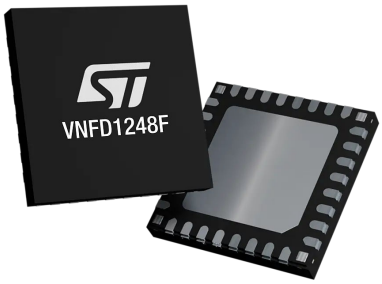
VNFD1248F

Data brief

High-side dual switch controller with intelligent fuse protection for 12 V, 24 V and 48 V automotive



QFN 5x5x0.9 mm 32+4L WF

Product summary	
Order code	VNFD1248FTR
Package	QFN 5x5x0.9 mm 32+4L wettable flanks
Packing	Tape and reel

Features

Maximum transient supply voltage	V_S	70 V
Operating voltage range	V_S	6 V to 60 V
Operating voltage range (extended)	V_S	6 V to 70 V
Standby current (max.)	I_{S_Q}	80 µA
Deep standby current (max.)	$I_{S\_Q\_DS}$	1 µA
SPI I/O supply voltage	V_{SPI}	3 V to 5.5 V
SPI standby current (max.)	I_{SPI_STBY}	5 µA

- Designed for automotive applications
- General
  - Dual independent channel high-side switch control IC with eFuse protection for automotive 12 V, 24 V, and 48 V applications
  - SPI slave interface for host control
  - 32-bit ST-SPI interface compatible with 3.3 V and 5 V CMOS level
  - 2-stage charge pump
  - Dual gate drive for an external MOSFET in high-side configuration
  - Back to back configuration
  - High precision bidirectional digital current sense for each channel via SPI through an external high-side shunt resistor
  - Input for an NTC resistor to monitor the external MOSFET temperature
  - Very low standby current: 25 µA in standby mode per channel, 0 µA in deep standby mode
  - Emergency stop and limp-home pins for advanced safety features
  - Device configuration lockout by a dedicated digital input pin
  - Integrated ADC for TJ, VNTC, VOUT, VSENSEP1, 2 and VDS conversion
  - Fast ADC for VDS, VSENSE conversion
  - CCM: capacitive charging mode
  - Few times programmable non-volatile memory (FTP NVM) embedded for customer sector program/erase/read
  - Direct input pin for hardware control of external MOSFET gate pin
  - BIST (current sense, VDS monitor and stuck on)
  - QFN 5x5x0.9 mm 32+4L package with wettable flanks

- Protections
  - Battery undervoltage shut-down configurable via SPI
  - External MOSFET desaturation shutdown configurable via SPI
  - Hard short circuit latch-off configurable via SPI
  - Bidirectional OVL shutdown (over-load current) with a delay configurable via SPI
  - I2t protection (current vs time latch-off) configurable via SPI (fuse-emulation)
  - Device overtemperature shutdown
  - Current sense undervoltage
  - External battery (protection with external component) MOSFET overtemperature shutdown
  - Reverse battery protection with external component
  - Battery µcut protection with external component (compliant to LV124)
  - Loss of GND

Application

- Specially intended for automotive power distribution applications
- Intelligent high current fuse replacement for automotive applications

Description

The device is an advanced controller for a power MOSFET in high-side configuration, designed for the implementation of two intelligent high-side switches for 12 V, 24 V, and 48 V automotive applications. The control IC is interfaced to a host microcontroller through a 3.3 V and 5 V CMOS-compatible SPI interface and provides protection and diagnostics to the system.

1 Block diagram and pin description

Figure 1. Block diagram

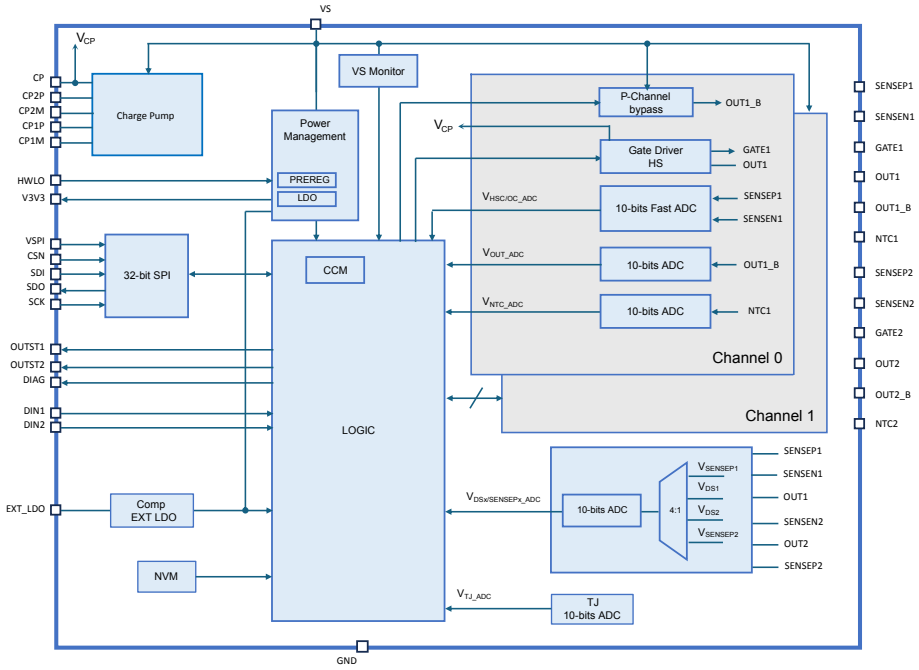
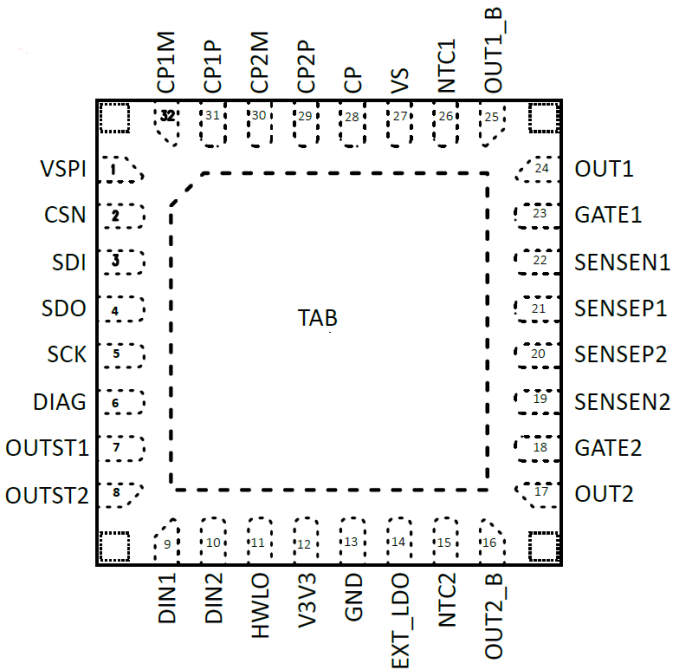


Figure 2. Configuration diagram (top through view)



Note: Although the TAB is not intended as the device reference ground, it can be connected to the PCB GND layer. The four corner leads (internally connected to the TAB) are intended for thermo-mechanical purpose only: they must be soldered on PCB copper areas (not necessarily directly connected to the PCB GND layer).

Table 1. Pin functions

Pin #	Name	Function
TAB		Connected to internal ground through high resistive path. To be connect to GND.
1	VSPI	DC supply input for the SPI interface. 3.3 V and 5 V are compatible.
2	CSN	Chip select (active low) for SPI communication. It is the selection pin of the device. CMOS compatible input.
3	SDI	Serial data input for SPI communication. Data is transferred serially into the device and sampled on SCK rising edge.
4	SDO	Serial data output for SPI communication. Data is transferred serially out of the device on the SCK falling edge.
5	SCK	Serial clock for SPI communication. It is a CMOS compatible input.
6	DIAG	Open drain active low logic output. Diagnostic feedback.
7	OUTST1	Open drain active high. GATE1 status monitor. This pin reports in digital format the status of the GATE1 pin: OUTST1 = H or L accordingly to GATE1 status high or low.
8	OUTST2	Open drain active high. GATE2 status monitor. This pin reports in digital format the status of the GATE2 pin: OUTST2 = H or L accordingly to GATE2 status high or low.
9	DIN1	Direct input to wake up device from standby and to control directly GATE1 turn-on/turn-off. If not used, must be connected to the ground through a 1 kΩ resistor.
10	DIN2	Direct input to wake up device from standby and to control directly GATE2 turn-on/turn-off. If not used, must be connected to the ground through a 1 kΩ resistor.
11	HWLO	Active high input pin compatible with 3.3 V and 5 V CMOS; it allows moving the device into states with default or locked configurations, with optional output control. It wakes up the device from deep standby. If not used, must be connected to the ground through a 1 kΩ resistor.
12	V3V3	Output of the 3.3 V internal LDO voltage regulator (logic and I/O supply). Connect a low ESR capacitor (1 µF) close to this pin.
13	GND	Ground connection.
14	EXT_LDO	External V3V3 supply. If not used, must be connected to the ground through a 1 kΩ resistor.
15	NTC2	Positive input pin for external NTC2 resistor.
16	OUT2_B	Out of P-channel bypass 2 connection.
17	OUT2	External FET source 2 connection.
18	GATE2	Output of the gate driver 2 for the external FET.
19	SENSEN2	Current sense amplifier 2 negative input.
20	SENSEP2	Current sense amplifier 2 positive input.
21	SENSEP1	Current sense amplifier 1 positive input.
22	SENSEN1	Current sense amplifier 1 negative input.
23	GATE1	Output of the gate driver 1 for the external FET.
24	OUT1	External FET source 1 connection.
25	OUT1_B	Out of P-channel bypass 1 connection.
26	NTC1	Positive input pin for external NTC1 resistor.
27	VS	Input supply pin. Connect to the 12 V, 24 V, 48 V battery voltage.
28	CP	Charge pump output.
29	CP2P	Charge pump–Positive terminal of the flying capacitor C_{P2}.
30	CP2M	Charge pump–Positive terminal of the flying capacitor C_{P2}.
31	CP1P	Charge pump–Positive terminal of the flying capacitor C_{P1}.
32	CP1M	Charge pump–Negative terminal of the flying capacitor C_{P1}.

2 Application information

Figure 3. **Application diagram per-channel back-to-back configuration**

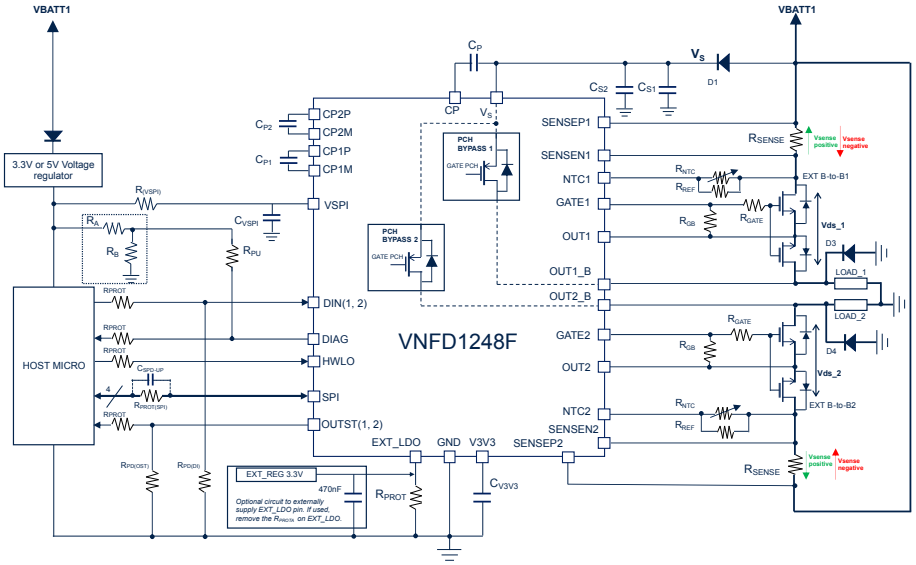


Figure 4. **Application diagram back-to-back configuration**

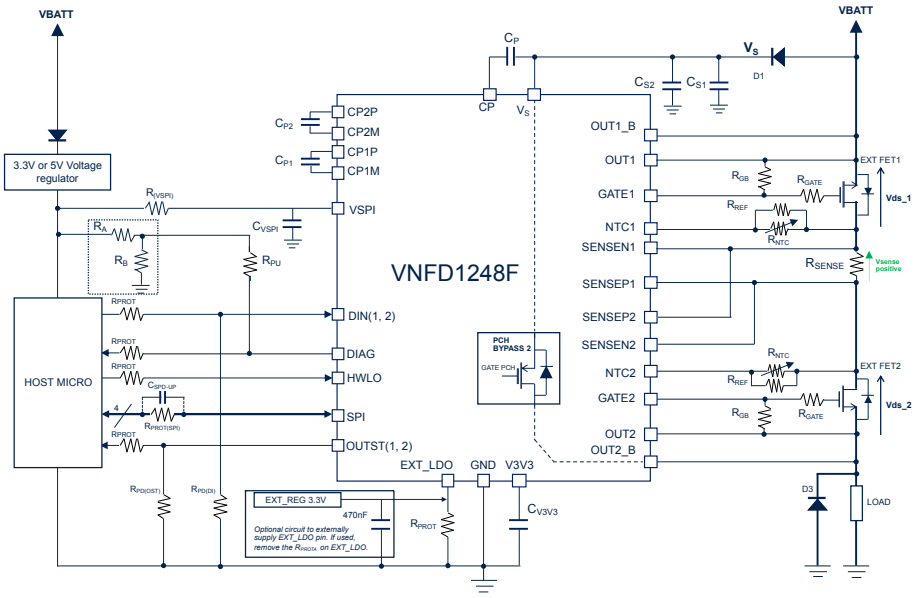


Figure 5. Application diagram independent channels configuration

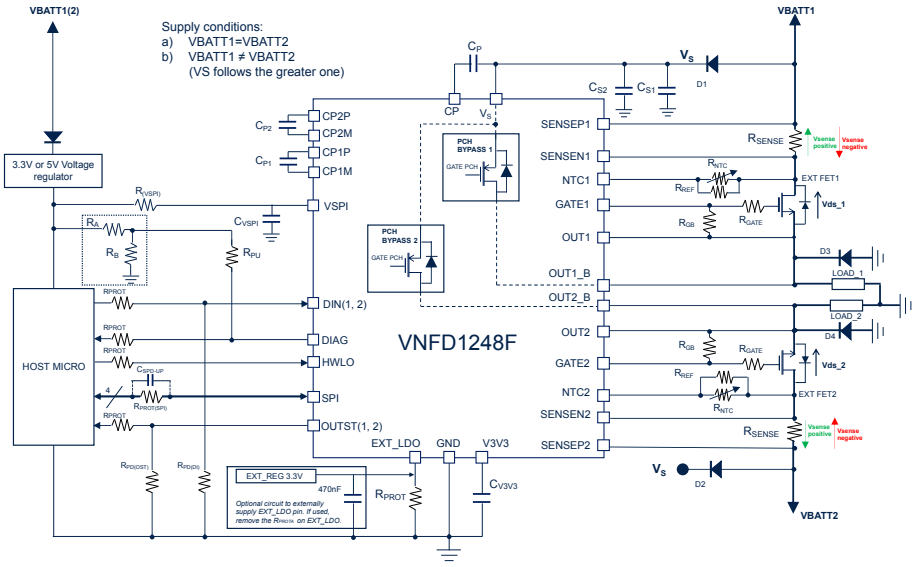


Figure 6. Application diagram with shared load configuration

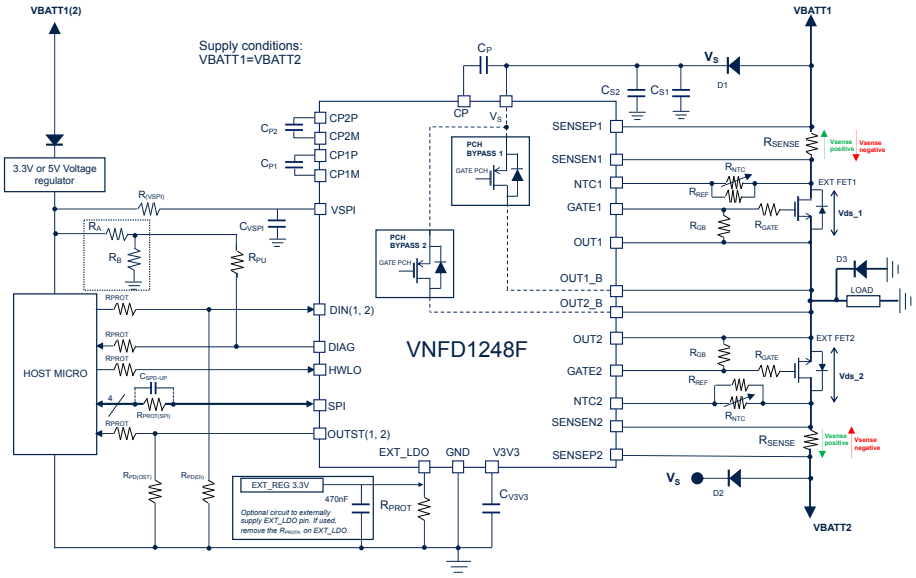


Table 2. Components value

Reference		Value	Notes
C_{S1}		3x(22 uF)	100 V rated for 48 V applications
		2x(47 uF)(1)	50 V rated for ≤ 24 V applications
C_{S2}		100 nF	50 V rated for ≤ 24 V applications
			100 V rated for 48 V applications
C_{P1}, C_{P2}		220 nF	50 V rated
C_P		390 nF	50 V rated
C_{VSPI}		330 nF	10 V rated
C_{V3V3}		1 uF	6.3 V rated
C_{SPD-UP}(2)		100 pF	10 V rated
R_{PU}		5.6 kΩ	-
R_A		8.2 kΩ	Mounted only in case of VREG at 5 V
R_B		15 kΩ	Mounted only in case of VREG at 5 V
$R_{PD(OST)}$		4.7 kΩ	-
$R_{PD(DI)}$		47 kΩ	-
$R_{(VSPI)}$		300 Ω	-
R_{PROT}		2.2 kΩ	-
$R_{PROT(SPI)}$(2)	R_{CS}	0 to 2.2 kΩ	-
	R_{CLK}	0 to 2.2 kΩ	-
	R_{SDI}	0 to 2.2 kΩ	-
	R_{SDO}	100 Ω	-
R_{GATE}		1 Ω to 10 Ω	In case of multiple external MSFET in parallel,
			use an R_{GATE} for each
R_{GB}		47 kΩ	-
R_{REF}		12 kΩ	±1%
R_{NTC}		10 kΩ	Example: B57232V5103F360
R_{SENSE}		1 mΩ	Power rating according to load current
D_1, D_2		IF and VRRM according to application requirements	Examples: STPS2H100ZFY and STPS2L60ZFY for 48 V and ≤ 24 V applications, respectively
D_3, D_4		IF, IFSM, and VRRM according to application requirements	These free-wheeling diodes deenergize the inductive component of the load. VRRM, IF, and IFSM are selected according to voltage and output rating, as well as to load inductance.

1. *In case of usage at 12 V, the device can withstand the severe cold-start pulse test defined by the VW80000 LV124 E-11 without turning OFF the OUT.*
2. *In case of single device on the SPI bus, then the protection resistors are not strictly necessary. In case of shared SPI bus with other devices, the protection resistor may result necessary to improve application robustness against fault events on the shared bus. The presence of the protection resistor may impact the maximum speed of the SPI; if necessary, a small (100 pF) capacitor in parallel to the protection resistor can be used.*

3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: http://www.st.com. ECOPACK is an ST trademark.

3.1 QFN 5x5x0.9 mm 32+4L wettable flanks package information

Figure 7. QFN 5x5x0.9 mm 32+4L wettable flanks package outline

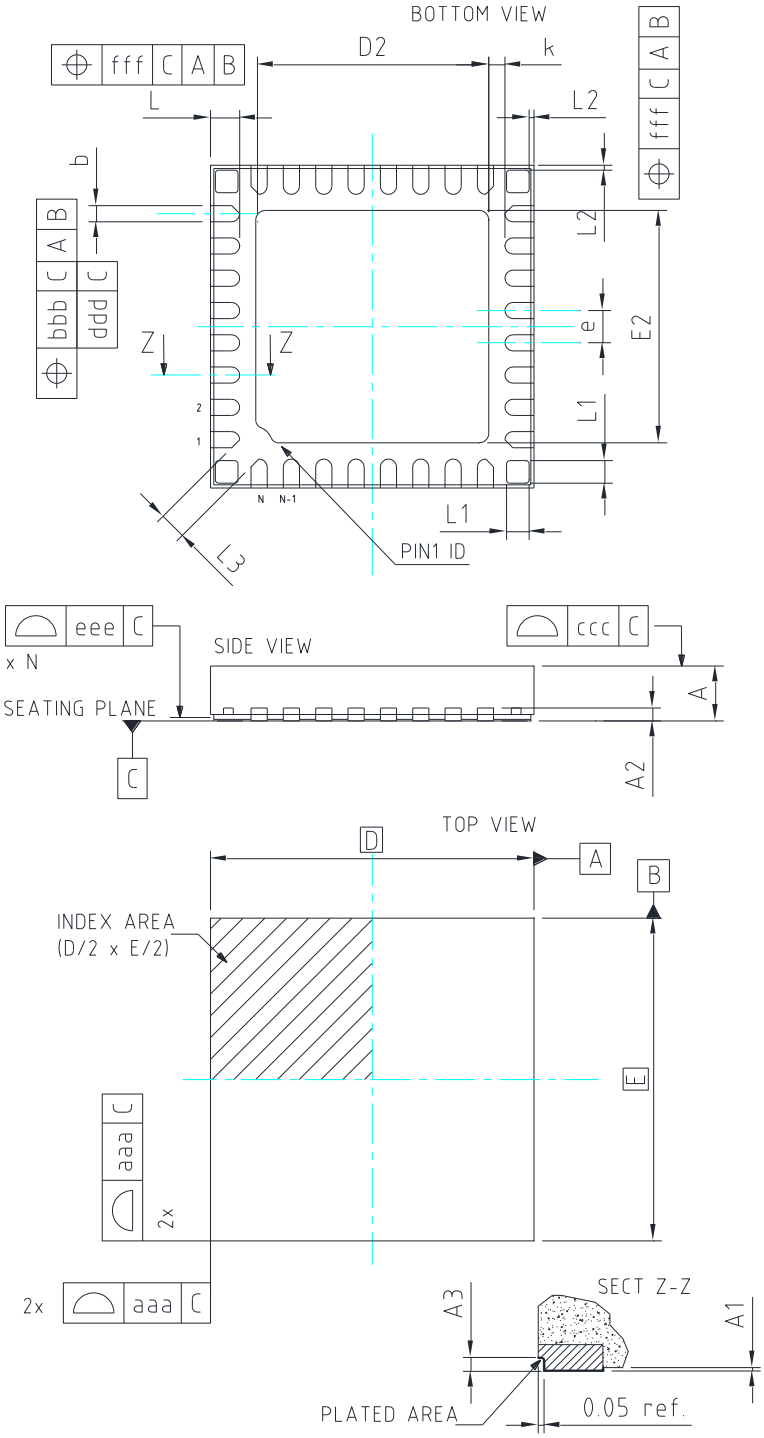


Table 3. QFN 5x5x0.9 mm 32+4L wettable flanks mechanical data

	Dimension [mm]		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.2 REF	
A3	0.10		
b	0.20	0.25	0.30
D		5.00	
e		0.50	
E		5.00	
L	0.35	0.45	0.55
L1		0.35	
L2		0.075	
L3		0.42	
k	0.20		
N		32 + 4	

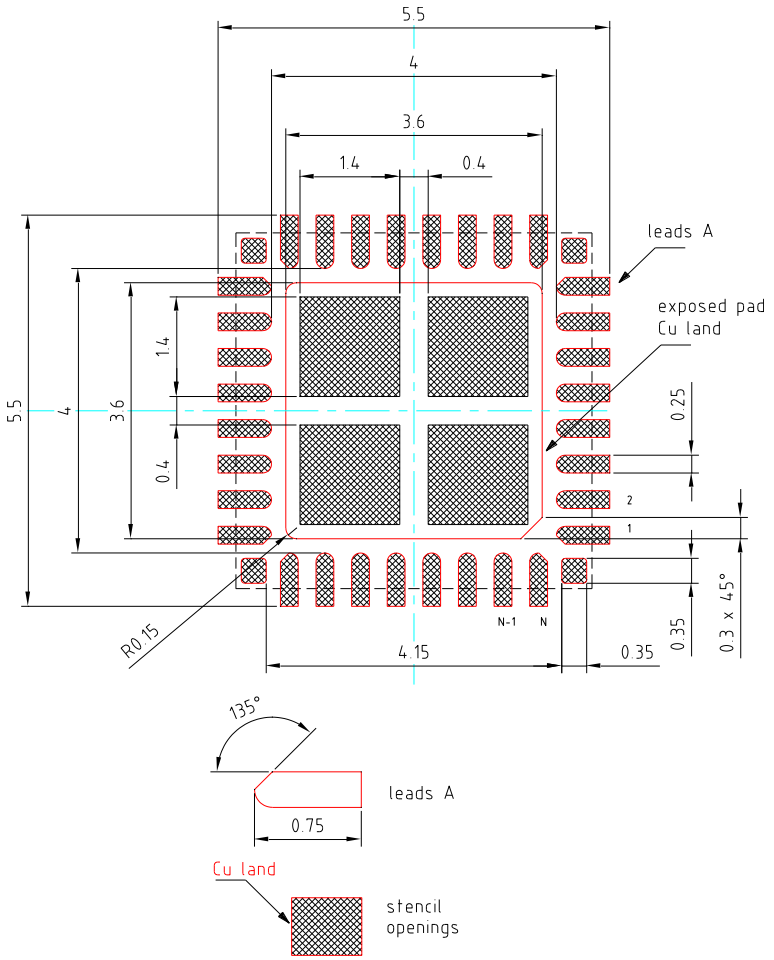
Table 4. Tolerance of form and position

Symbol	Tolerance
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Table 5. Exposed pad variation

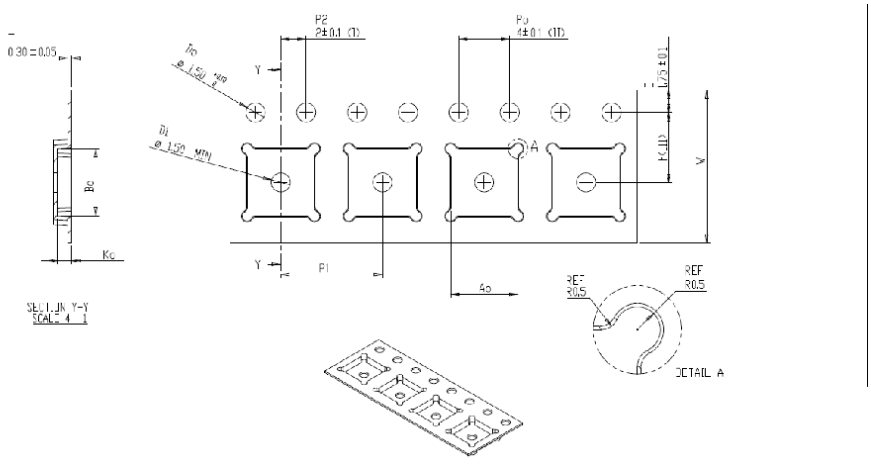
	Dimension [mm]		
	Min.	Typ.	Max.
D2	3.55	3.60	3.65
E2	3.55	3.60	3.65

Figure 8. **QFN 5x5x0.9 mm 32+4L wettable flanks suggested footprint**



3.2 QFN 5x5x0.9 mm 32+4L wettable flanks packing information

Figure 9. **QFN 5x5x0.9 mm 32+4L wettable flanks carrier tape**



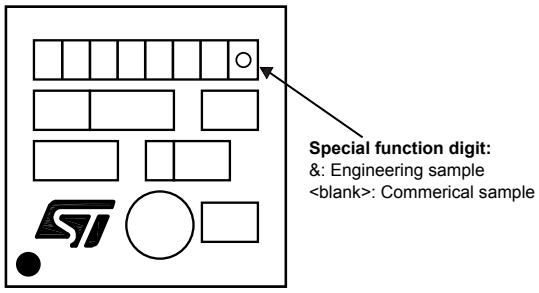
Note: (I) (III) Measured from the centreline of the sprocket hole to the centreline of the pocket.
(II) Cumulative tolerance of sprocket holes is ± 020.

Table 6. **QFN 5x5x0.9 mm 32+4L wettable flanks mm carrier tape**

Description	Value [mm]
A0	5.30 ± 0.1
B0	5.30 ± 0.1
K0	1.10 ± 0.1
F	5.50 ± 0.1
P1	8.00 ± 0.1
W	12.00 ± 0.1

3.3 QFN 5x5x0.9 mm 32+4L wettable flanks marking information

Figure 10. **QFN 5x5x0.9 mm 32+4L wettable flanks marking information**



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Revision history

Table 7. **Document revision history**

Date	Version	Changes
05-Feb-2026	1	Initial release.

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