VIPER31

Data brief

Energy saving offline high voltage converter

Features

- 800 V avalanche-rugged power MOSFET (4.5 Ω max. $R_{DS(on)}$)
- Embedded HV startup and sense FET
- Current mode PWM controller
- Drain current limit protection (OCP)
  - 710 mA (VIPER317)
  - 850 mA (VIPER318)
  - 990 mA (VIPER319)
- Wide supply voltage range: 4.5 V to 30 V
- Ultra-low input power consumption:
  - < 10 mW @ 230 VAC in no-load;
  - < 400 mW @ 230 VAC, 250mW output load
- Jittered switching frequency reduces the EMI filter cost:
  - 30 kHz ±7% (type X)
  - 60 kHz ±7% (type L)
  - 132 kHz ±7% (type H)
- Embedded E/A with 1.2 V reference
- Built-in soft-start for improved system reliability
- Embedded protections with automatic restart

Product status link

VIPER31

Product label

SUSTAINABLE TECHNOLOGY

Application

- **SMPS for**:
  - home appliances
  - home automation
  - smart metering
  - industrial
  - consumer
  - lighting
- **SMPS Topologies:**
  - Isolated flyback (secondary side and primary-side regulation)
  - non-isolated flyback
  - buck
  - buck-boost

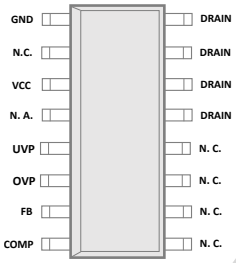
Description

The VIPER31 device is a high-voltage converter that smartly integrates an 800 V avalanche rugged power MOSFET with PWM current-mode control.

The 800 V breakdown allows extended input voltage range to be applied, as well as to reduce the size of the DRAIN snubber circuit. The IC can meet the most stringent energy-saving standards as it has very low consumption and operates in pulse frequency modulation at light load. Overvoltage and undervoltage protections with separate and settable intervention thresholds are available at OVP and UVP pins respectively. UVP can also be used as a disabling input for the entire SMPS, with ultra-low residual input power consumption. Integrated HV startup, sense FET, error amplifier and oscillator with frequency jitter allow a complete application to be designed with a minimum component count.

1 Connection diagram

Figure 1. Connection diagram



Note: A PCB copper area has to be provided under DRAIN pins to heat dissipation.

Table 1. Pin description

Pin number	Name	Function
1	GND	**Ground and MOSFET source.** Connection of both the source of the internal MOSFET and the return of the bias current of the device. All of the groundings of bias components must be tied to a trace going to this pin and kept separate from the pulsed current return.
2	N. C.	**Not connected.** When designing the PCB, this pin can be soldered to GND.
3	VCC	**Controller Supply**. An external storage capacitor has to be connected across this pin and GND. The pin, internally connected to the high-voltage current source, provides the VCC capacitor charging current at startup. A small bypass capacitor (0.1 µF typ.) in parallel, placed as close as possible to the IC, is also recommended, for noise filtering purposes.
4	N.A.	**Not available for user.** This pin is mechanically connected to the controller die pad of the frame. In order to improve noise immunity, it is highly recommended to connect it to GND.
5	UVP	**Undervoltage Protection.** If V_{UVP} falls below the internal threshold V_{UVP_th} (0.4 V typ.) for more than t_{UVP_DEB} time (30 ms, typ.), the IC is disabled, and its consumption reduced to ultra-low values. When V_{UVP} rises above V_{UVP_th}, the device waits for a t_{UVP_REST} time interval (30 ms, typ.) then resumes switching. The pin can be used to realize an input undervoltage protection or as a disabling input for the entire SMPS, with ultra-low residual input power consumption. If the feature is not required, the pin must be left open, which excludes the function.
6	OVP	**Overvoltage Protection**. If VOVP exceeds the internal threshold V_{OVP_th} (4 V typ.) for more than t_{OVP_DEB} time (250 µsec, typ.), the PWM is disabled in auto-restart for t_{OVP_REST} (500 msec, typ.) until the OVP condition is removed, after that it restarts switching with soft-start phase. OVP pin can be used to realize an input overvoltage protection (or, in non-isolated topologies, an output overvoltage protection). If the feature is not required, the pin must be connected to GND, which excludes the function.
7	FB	**Direct feedback**. It is the inverting input of the internal transconductance E/A, internally referenced to 1.2 V with respect to GND. In non-isolated converter, the output voltage information is directly fed into the pin through a voltage divider. In primary regulation, the FB voltage divider is connected to the VCC. The E/A is disabled if FB is connected to GND pin.
8	COMP	**Compensation**. It is the output of the internal E/A. A compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the control loop. In case of secondary feedback, the internal E/A must be disabled and the COMP directly driven by the optocoupler to control the DRAIN peak current setpoint.
9 to 12	N.C.	**Not connected.** These pins must be left floating in order to get a safe clearance distance.
13 to 16	DRAIN	**MOSFET drain**. The internal high-voltage current source sources current from these pins to charge the VCC capacitor at startup. The pins are mechanically connected to the internal metal PAD of the MOSFET in order to facilitate heat dissipation. On the PCB, some copper area under these pins decreases the total junction-to-ambient thermal resistance thus facilitating the power dissipation.

2 Electrical and thermal characteristics

Table 2. Electrical and thermal characteristics

Symbol	Parameter	Value
$V_{(BR)DSS}$	Breakdown voltage	800 V
$R_{DS(on)}$	Drain-source ON state resistance (max.@25C)	4.5 Ω
V_{START}	Drain-source start voltage	30 V (max.)
V_{DD}	Operating voltage range	4.5 – 30 V
V_{REF_FB}	E/A Input Voltage	1.2 V (typ.)
I_{DLIM}	Drain current limitation	710 mA (VIPER317) 850 mA (VIPER318) 990 mA (VIPER319)
F_{OSC}	Switching frequency	30 kHz ±7% (type X) 60 kHz ±7% (type L) 132 kHz ±7% (type H)
T_{SD}	Thermal shutdown temperature	160 °C (typ.)
R_{thJA}	Thermal resistance junction ambient (Dissipated power = 1 W)	80 °C/W

1. *When mounted on a standard single side FR4 board with 100 mm2 (0.155 sq in) of Cu (35 im thick)*

Figure 2. Typical isolated flyback configuration

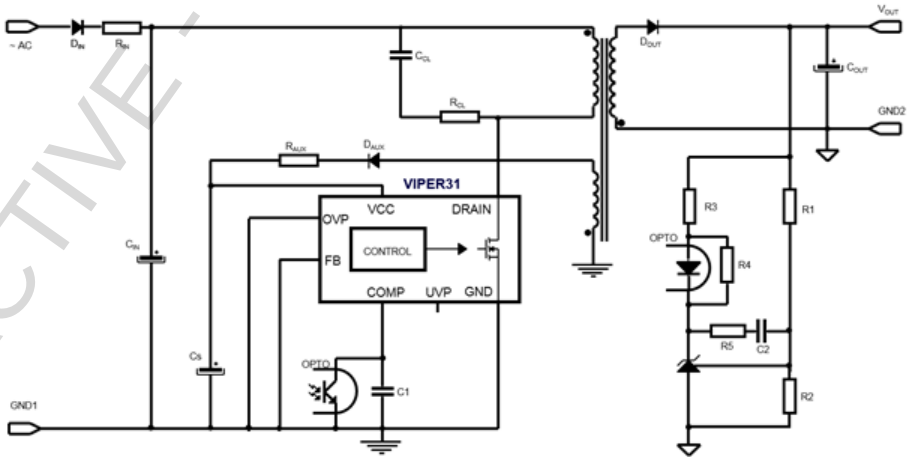


Figure 3. Typical isolated flyback configuration with primary regulation

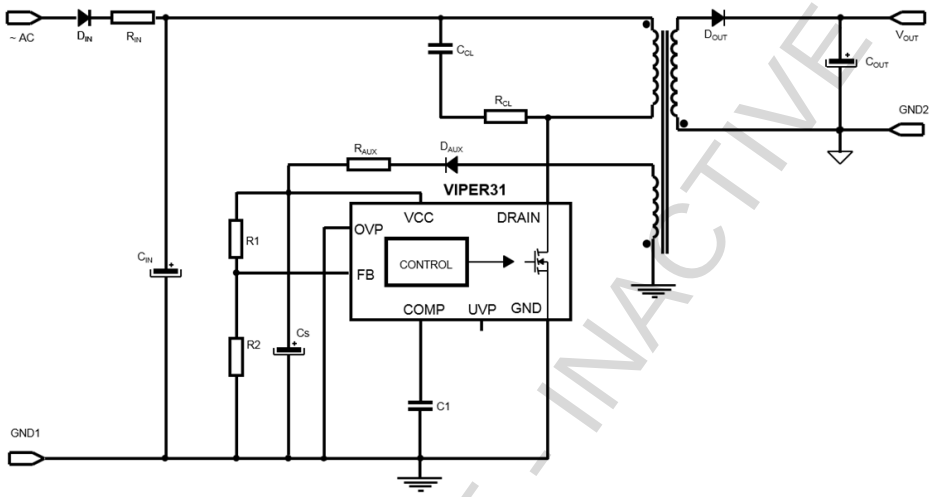


Figure 4. Typical non-isolated flyback configuration with direct feedback

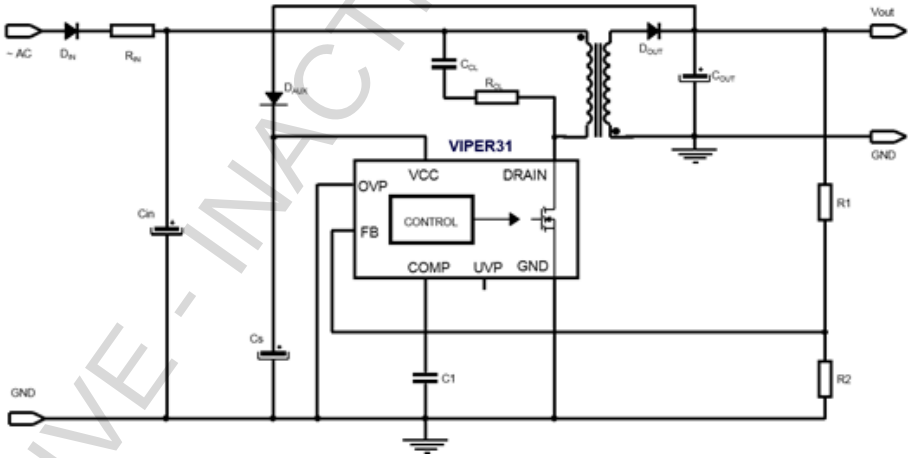
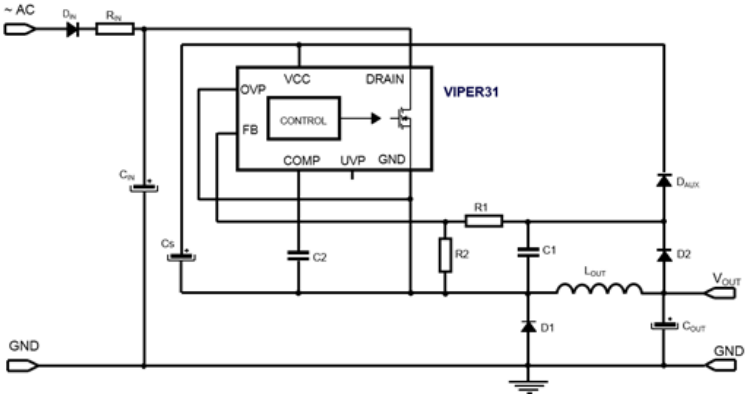


Figure 5. Typical buck configuration



3 Order codes

Table 3. **Order codes**

Order code	I_{DLIM} (OCP) typ	FOSC ± jitter	Package
VIPER318XD(TR)	850 mA	30 kHz ± 7%	SO16N tube (tape and reel)
VIPER319XD(TR)	990 mA		
VIPER317LD(TR)	990 mA	60 kHz ± 7%	
VIPER318LD(TR)	850 mA		
VIPER319LD(TR)	990 mA		
VIPER317HD(TR)	710 mA	132 kHz ± 7%	
VIPER318HD(TR)	850 mA		
VIPER319HD(TR)	990 mA		

Revision history

Table 4. **Document revision history**

Date	Version	Changes
3-Mar-2020	1	Initial release.

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