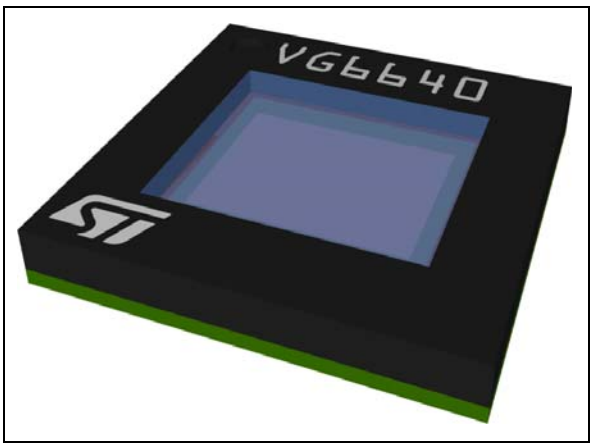
VG5640, VG6640, VG8640, VD5640, VD6640, VD8640

1.3 megapixel high dynamic range image sensor

Data brief



Features

- 1.3 megapixel resolution sensor (1304 x 980) in 1/2.7 inch optical format
- High dynamic range (HDR) pixel architecture, up to 132 dB dynamic range
- Best in class FSI high pixel sensitivity with 3.75 µm pixel size
- 45 frames per second at full resolution, 60 frames per second at 720p resolution
- Small physical size of 9.0 mm x 9.3 mm in automotive qualified package Im2BGA
- Synchronization for multiple cameras
- Highly configurable HDR image pre-processing
- Motion and flicker tolerant HDR options including flicker flag to denote affected pixels
- Comprehensive inline pixel defect correction
- Fast+ I^2C control interface
- MIPI CSI-2[(a)] version 1.01 serial and/or 12-bit parallel video data interface

a. Copyright© 2005-2010 MIPI Alliance, Inc. Standard for Camera Serial Interface 2 (CSI-2) version 1.01, limited to 1 Gbps per lane

- Automotive Safety Integrity Level (ASIL) data included as part of each frame
- Automotive qualification: AEC-Q100 grade 2
- Operating junction temperature: -40°C to +125°C

Description

This is a high performance, high dynamic range 1.3 megapixel image sensor. Designed for automotive, security and other demanding outdoor applications, the device offers supreme low light performance and numerous safety integrity features.

An embedded Bayer data pre-processor integrates a wide range of image enhancement functions, designed to ensure high image quality.

An advanced synchronization facility allows multi-camera systems to work with minimal latency and motion temporal mismatch artifacts.

This sensor targets the market for mono and stereo forward facing, mirror replacement, multi purpose cameras in cars, parking assist and all round view camera systems and is a good match for the needs of HD security applications.

Table 1. Device variants

Device	Color filter	Package
VG5640	CCCC	Im2BGA
VG6640	RGB Bayer	Im2BGA
VG8640	RCCC	Im2BGA
VD5640	CCCC	None(bare die)
VD6640	RGB Bayer	None(bare die)
VD8640	RCCC	None(bare die)

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Technical specifications

Table 2. Technical specifications

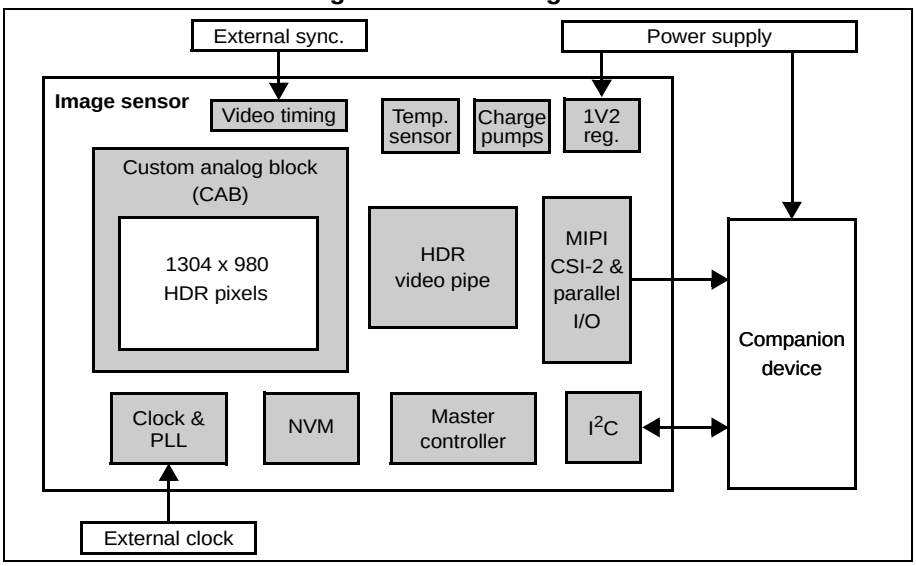
Feature	Detail
Pixel resolution	1304 x 980
Sensor technology	65 nm, CMOS imager process
Pixel size	3.75 µm x 3.75 µm
HDR characteristics	3 integration times with real-time data merging
Pixel gain	+13 dB (x5) maximum
Analog gain	+12 dB (maximum)
Dynamic range (linear mode)	72 dB
Dynamic range (in scene)	132 dB
Peak signal to noise ratio (on pixel)	42 dB @ 12 lux
Minimum illumination (on pixel)	1.0 mlux @ SNR 1 (no color filter, 30ms Integration)
Pixel sensitivity (without colour filter)	>=32V/lxsec @3200K
Power consumption	400 mW @ 30 fps
Junction Temperature range (Tj)	-40°C to +125°C functional (-40°C to +105°C for acceptable images)
Shutter	Electrical rolling
Peak quantum efficiency	>60% @ 520 nm
NIR cut-off wavelength	>=10% QE @ <900 nm
Fixed pattern noise (FPN)	<0.01% @ 20°C
Temporal read noise	<0.025% @ full swing
Image lag	<0.1%
Package option	Exposed glass BGA 9.0 mm x 9.3 mm
Frame rate at full resolution	45 fps
Frame rate at HD video (720p) resolution	60 fps
Parallel interface data rate	66 Mpixel/s (12 bits per pixel)
CSI-2 serial interface data rate	2 x 550 Mbit/s
Supply voltages	2.8V analog supply 1.8V or 2.8V digital I/O supply 1.2V digital core supply (on-board regulator available)
Temperature sensor accuracy	±3°C over the operating range
External clock frequency range	12-50 MHz, AC or DC coupled
Oscillator frequency range	12-27 MHz, quartz crystal
Frame synchronization	±1 line through an I^2C command or through dedicated signal

Functional description

The VG6640 block diagram is shown in *Figure 1*. The main blocks are as follows:

- Master controller
  - clock and reset management
  - I2C bus control interface and transaction routing
  - safe control of system state changes from Standby to Streaming
  - device reinitialization to default mode (software Reset)
  - management of integration times across the three captures
  - Non Volatile Memory (NVM) management
- Custom Analog Block (CAB)
- Video timing block
- HDR video pipe
  - responsible for real time image data processing at pixel clock rate, Processes the RAW pixel data from the ADCs in the CAB. The HDR video pipe contains a set of defect correction and data coding blocks.
- Image data interfaces
  - video data coders and transmitters for the serial (MIPI CSI-2) and parallel interfaces
- On chip regulators
  - to supply the analog block and, optionally, the digital core
- Clock and PLL
  - to provide all the clocks required for data capture through to output interfaces from a single frequency source
- Non volatile memory (NVM)
  - to store production and part to part variance data
- Temperature sensors
  - to allow the host application to monitor sensor temperature

Figure 1. Block Diagram



Interfaces

The VGx640 is ready to connect via one of two interfacing options. The sensor supports a 12bit (ITU) parallel interface with frame and line sync signals and a pixel clock, or a dual lane MIPI CSI-2 serial interface. Before transmission the 22bit HDR image data is compressed down to 12bits using a piece wise linear (PWL) compression algorithm to minimize perceptible losses.

The 12bit ITU parallel interface is capable of 66Mpixel/s.

The dual lane MIPI CSI-2 serial interface supports 1.1Gbit/s and is the industry standard for low EMI and excellent EMC high speed interfacing.

The sensor is configured and controlled via a I2C (Inter Integrated Circuit) interface operating in either Fast (up to 400KHz) or Fast+(up to 1MHz) modes.

Power supplies

Power supplies required by the sensor are:

- 2.8V for the analogue blocks
- 2.8V or 1.8V for the digital I/Os
- The digital core operates at 1.2V. This can be supplied via an internal regulator or from an external 1.2V supply.

Clock

An input clock is required which can be supplied from an external clock in the range of 12MHz to 50MHz or from a quartz crystal of between 12MHz to 27MHz.

Image enhancement, status and test features

The device contains an embedded video processor and delivers uncolored images up to 60 frames/s at 720p resolution, or 45 frames/s at 1304x980 resolution. The video processor integrates a wide range of image enhancements, designed to ensure a high image quality. These enhancements include:

- External frame synchronization
- Windowing/image cropping
- Subsampling
- Dark calibration
- Fixed pattern noise correction
- Frame cropping
- Defective pixel correction
- Test pattern generation
- Statistics generation
- Embedded sensor data

HDR Merge modes

The on chip video processor implements and manages one of five different merge schemes with each of the key parameters user configurable by the host to give a fully flexible HDR scheme to maximise in scene dynamic range and maximise SNR. There are also IP blocks included to manage and minimise ‘flicker’, such as indicators and PWM controlled lighting, and ‘ghosting’, caused by motion of sensor or in scene movement at the maximum frame

rates. Many of the configuration parameters for the HDR image capture are duplicated in a second register bank. These two banks can be toggled at the maximum frame rates to provide images from two distinct configurations to, for example, optimise for machine vision and for driver display.

External frame synchronization

The external frame synchronization offers two methods for control synchronization of the frame start of multiple cameras.

- A common Frame Sync signal from the host or a ‘principal’ camera.
- An I2C bus command sent by the host to set an offset to the current frame start.

Using one of these techniques each camera sync can be corrected to an accuracy of less than 1 line period.

Safety integrity

A set of self diagnostic features allow the device to support the automotive safety integrity level (ASIL) system requirements. These include the following:

- Cyclic redundancy checking (CRC) on image data through the parallel or serial interface
- Error correction codes (ECC) for sensor critical memories
- Analog in line test information
- Digital in line test information
- Two temperature sensors
- Access to diagnostic information via embedded data lines in the image

Ordering Information

Table 3. Ordering information

Ordering code(1)	Color filter	Device package	Packing
VG5640xB1M/1	CCCC	Im2BGA	Tape & reel(2)
VG6640xB1M/1	RGB Bayer	Im2BGA	Tape & reel(2)
VG8640xB1M/1	RCCC	Im2BGA	Tape & reel(2)
VG5640xB1M	CCCC	Im2BGA	Tray(3)
VG6640xB1M	RGB Bayer	Im2BGA	Tray(3)
VG8640xB1M	RCCC	Im2BGA	Tray(3)
VD5640xzSB/RW	CCCC	None (bare die)	Reconstructed wafer
VD6640xzSB/RW	RGB Bayer	None (bare die)	Reconstructed wafer
VD8640xzSB/RW	RCCC	None (bare die)	Reconstructed wafer

1. Substitute x with A for automotive grade; C for industrial grade parts. For bare die substitute z for wafer thickness.
2. For volume orders.
3. For sample orders.

ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark

Revision history

Table 4. Document revision history

Date	Revision	Changes
20-Aug-2014	1	Initial version
06-Nov-2014	2	Update *Features* and *Functional description* sections
01-Oct-2015	3	Updated to align with v7 of the datasheet

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