

STSW-RFSOL001

STWPLLSIM_v5.2 simulation tool for STW81200/STuW81300

Data brief

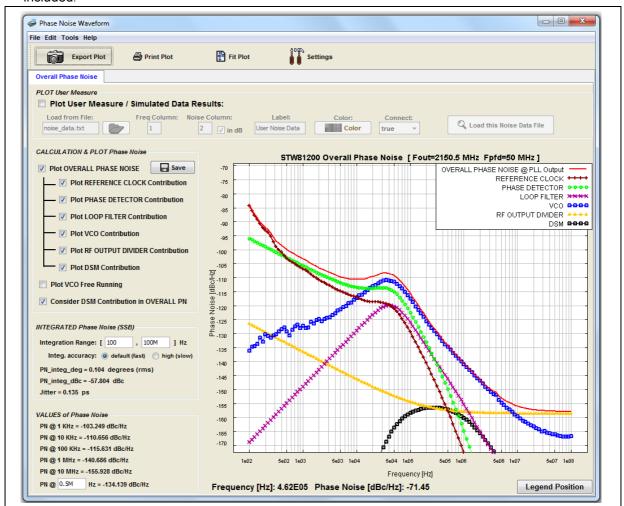
Features

Embedded model of the PLL synthesizer integrated in the STW81200 product (46.875-6000 MHz Wideband RF Fractional/Integer Synthesizer) and in the new STuW81300 (1.925-16GHz Wideband RF/Microwave Fractional/Integer Synthesizer.

The environment for design and simulation using STW8110x family product is also included.

Description

STWPLLSim software (STSW-RFSOL001) is a powerful tool developed to allow the end-user of ST PLL Synthesizer products to optimize the PLL design and accurately simulate both phase-noise and transient performance.



Revision history STSW-RFSOL001

1 Revision history

Table 1. Document revision history

Date	Revision	Changes
15-Jul-2015	1	Initial release.
12-Jan-2016	2	Updated to scope STW81200/STuW81300 and STWPLLSIM_v5.2.

IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics - All rights reserved

