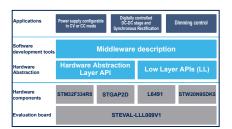




Firmware for STEVAL-LLL009V1 based on STM32F334R8T6



Features

- Based on libraries generated by STM32CubeMX
- Control of the DC-DC half bridge LCC resonant converter by PI regulator
- · Control of secondary side synchronous rectification

Description

The STSW-LLL009FW firmware runs on the STEVAL-LLL009V1 evaluation kit control board.

The firmware is based on libraries generated from STM32CubeMX on the STM32F334R8T6 high performance 32-bit ARM® Cortex®-M4 microcontroller and controls the DC-DC half bridge LCC resonant converter and the output synchronous rectification.

The power supply can be either configured in constant voltage (CV) or constant current (CC) mode.

In CV mode, the PI control loop executed at 50 kHz provides the PWM switching period of primary side MOSFETs, changing the gain of the resonant tank and regulating the output voltage at the desired value. The primary devices are driven by 50% duty cycle PWM signals, with a proper dead time for each leg to ensure ZVS operation and avoid input voltage shot-through.

In CC mode, the firmware detects 0-10 V input signals and manages the dimming (with a resolution of 1%) by changing the current through the LED lighting application.

| Product summary | | |
|--|---------------------------|--|
| Firmware for STEVAL-LLL009V1 based on STM32F334R8 MCU | STSW-LLL009FW | |
| 300 W output digitally controlled HV AC Input HB LED driver | STEVAL-LLL009V1 | |
| Mainstream mixed signal MCU with ARM Cortex-M4 core | STM32F334R8T6 | |
| Applications | LED Lighting and Controls | |



1 Block diagram

ISOLATION 750 ±2.5% DC-BUS Bridge Rectifier Sync. Filter PFC **HB-LCC** Rect. 275 –480V AC Mains STW20N95DK5 L6562AT STP100N10F7 STW20N95K5 **Gate Driver** Output Operation Mode: ii CV (SW1: 1-2) CC (SW1: 2-3) Auxiliary Supply Flyback GATE DRIVE STGAP2D Gate Driver CONTROL VIPer26K LOGIC ISOLATION II п П п П MCU 0-10V Optically Isolated DC-BUS Sense STM32F334 ij ii

Figure 1. STEVAL-LLL009V1 functional block diagram

DB4279 - Rev 1 page 2/5



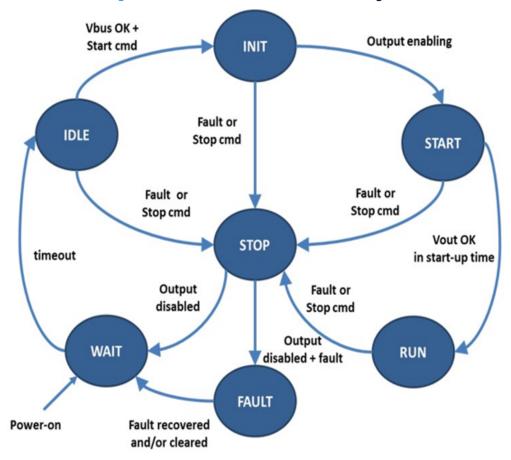


Figure 2. STSW-LLL009FW functional block diagram

The STSW-LLL009FW workflow can be summarized as follows:

- 50 kHz PI voltage control loop
- PWM generation with 217 ps resolution (HRTIM)
- Startup with linear frequency decreasing to avoid current spikes
- Startup protection on mismatch of output voltage
- SR based on embedded comparators and voltage sensing
- · Automatic SR activation depending on output load
- Fast overcurrent protection with internal comparator
- Analog watchdog on output voltage for overvoltage protection

DB4279 - Rev 1 page 3/5



Revision history

Table 1. Document revision history

| Date | Version | Changes |
|-------------|---------|------------------|
| 16-Nov-2020 | 1 | Initial release. |

DB4279 - Rev 1 page 4/5



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DB4279 - Rev 1 page 5/5