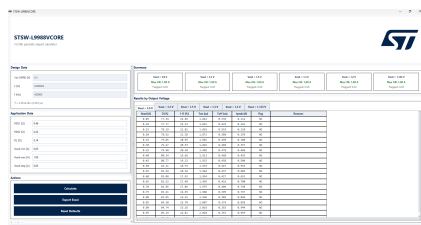


VCORE parasitic estimator for L9988 12 V BMS IC



Product status link

[STSW-L9988VCORE](#)

Features

- Calculation utility for evaluating the impact of **parasitic resistances** on **VCORE buck regulator performance**
- Supports analysis across multiple VCORE output voltages
- Evaluation of maximum load current that can be supported without performance degradation of VCORE regulator
- Provides a compact summary of maximum supported load current per output voltage
- Export the calculated results for documentation or design review
- Fast assessment of regulator robustness
- Useful for design reviews and PCB layout reviews

Applications

- **STSW-L9988VCORE tool** is ideal for evaluating the effect of PCB parasitic and inductor losses during power supply design and layout optimization.
- It supports schematic definition, component selection, and design validation by quickly identifying operating points that may degrade regulator performance

Description

The **STSW-L9988VCORE** tool is a calculation utility developed to help users evaluate the impact of parasitic resistances on the VCORE buck regulator performance.

In a real application, the regulator performance is affected by the resistive parasitic introduced by:

- internal switches,
- PCB copper paths,
- ground return paths,
- output inductor series resistance.

The tool is intended to provide a simple and practical way to evaluate whether the selected parasitic resistances degrade the VCORE regulator performance.

1 Overview

The **STSW-L9988VCORE tool** is a practical calculation utility developed to help users assess how parasitic resistances affect the performance of the VCORE buck regulator. It enables fast evaluation of whether a selected resistance combination remains acceptable over the required load current range, helping engineers make informed design decisions early in the development flow.

The tool supports both design review and sensitivity analysis, with results organized by output voltage and load current. It is intended as a useful aid during:

- schematic definition,
- PCB layout review,
- inductor selection,
- regulator performance verification.

The tool calculates, for each operating point:

- duty cycle
- ON and OFF time
- peak current
- limit violation conditions

Results are highlighted with visual flags to quickly identify critical operating points.

The user can set:

- RDS1: total resistance between VIN and SW
- RDS2: total resistance between SW and GND
- RL: total resistance between SW and VOUT
- load current range:
 - Iload min
 - Iload max
 - Iload step

Figure 1. STSW-L9988VCORE TOOL

The screenshot displays the STSW-L9988VCORE tool interface. It includes a 'Design Data' section with input fields for Vin (V), I [A], f [Hz], and T. Below this is the 'Application Data' section with fields for RDS1 [Ω], RDS2 [Ω], RL [Ω], Iload min [A], Iload max [A], and Iload step [A]. The 'Actions' section contains buttons for 'Calculate', 'Export Excel', and 'Reset Defaults'. The 'Summary' section shows a grid of output voltage buttons (5.0V, 3.3V, 1.5V, 1.2V, 1.1V, 1.0V) with their respective max current and flag status. The 'Results by Output Voltage' section displays a table with columns for Iload [A], D [%], f-D [%], Ton [ns], Toff [ns], Ipeak [A], Flag, and Remarks. The table contains 24 rows of data for various load currents and output voltages.

Iload [A]	D [%]	f-D [%]	Ton [ns]	Toff [ns]	Ipeak [A]	Flag	Remarks
0.05	77.54	22.46	1.042	0.550	0.112	NO	
0.10	77.77	22.23	1.052	0.552	0.143	NO	
0.15	78.19	21.81	1.062	0.553	0.170	NO	
0.20	78.64	21.36	1.072	0.550	0.200	NO	
0.25	79.05	20.95	1.082	0.495	0.200	NO	
0.30	79.45	20.55	1.092	0.460	0.200	NO	
0.35	79.58	20.42	1.092	0.475	0.200	NO	
0.40	80.34	19.66	1.113	0.460	0.200	NO	
0.45	80.77	19.23	1.123	0.450	0.200	NO	
0.50	81.21	18.79	1.133	0.437	0.200	NO	
0.55	81.64	18.36	1.144	0.431	0.200	NO	
0.60	82.08	17.92	1.154	0.427	0.200	NO	
0.65	82.51	17.49	1.165	0.423	0.200	NO	
0.70	82.95	17.04	1.175	0.400	0.200	NO	
0.75	83.41	16.59	1.186	0.395	0.200	NO	
0.80	83.88	16.12	1.196	0.391	0.200	NO	
0.85	84.39	15.61	1.207	0.374	0.200	NO	
0.90	84.74	15.26	1.218	0.363	0.200	NO	
0.95	85.19	14.81	1.229	0.353	0.200	NO	

Revision history

Table 1. Document revision history

Date	Version	Changes
14-Sep-2026	1	Initial release.



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Figure 1. STSW-L9988VCORE TOOL. 2

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