STHV749

Quad ±90 V, ±2 A, ±4 A, 3-, 5-, 7-level RTZ, high-speed ultrasound pulser

Data brief

LGA-48 (8x8x0.9 mm)
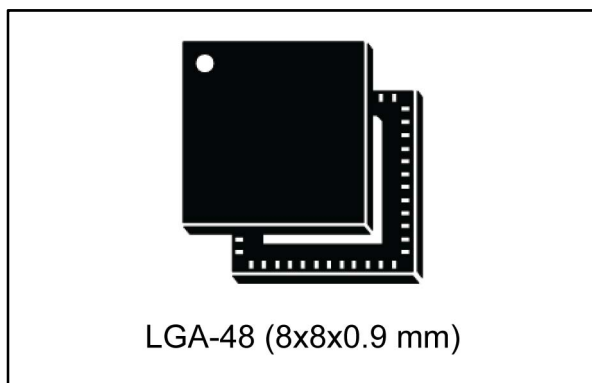
Features

- 0 to ±90 V output voltage
- 3 levels ±4 A or 5 levels ±2 A user-selectable operation
- 7 levels also using CW bridge
- Up to 40 MHz operating frequency (3 level option)
- Power-up/down sequence free
- Low-power, high-voltage, high-speed PW, CW drivers
- Gate drivers self-biased architecture, no filtering capacitors required
- Optional input signal synchronization by external clock
- Three independently-supplied half bridges (TX0 and TX1 for pulsed wave/ CW for continuous wave)
- Pulsed wave (PW) mode operations (TX0 and TX1):
  - 5-level output waveforms
  - TX0 and TX1 fully independent
  - ±2 A source and sink current (each half bridge)
  - ±4 A source and sink current with 3 level option
  - Down to 20 ps jitter
  - Anti-cross conduction
  - Low 2nd harmonic distortion

- Continuous wave (CW) mode operations:
  - 130 mW/200 mW max. power consumption/channel
  - ±0.3 A/±0.6 A source and sink current
  - Down to 10 ps jitter
  - Low power consumption
- Fully integrated real clamping-to-ground functionality
  - 4 Ω synchronous active clamp
  - Anti-leakage on output node
  - ±4 A source and sink current
- Fully integrated TR switch
  - 8 Ω ON resistance
  - Up to 300 MHz BW
  - Receiver multiplexing function
  - Low DC consumption (High impedance/standby state)
- 1.8 V to 3.6 V CMOS logic interface
- Auxiliary integrated circuits
  - Noise blocking diodes
  - Anti-memory effect for all internal HV nodes
  - Thermal protection
- Latch-up free due to HV SOI technology
- Very few external passive components needed

Applications

- Medical ultrasound imaging
- Pulse waveform generators
- NDT ultrasound transmission
- Piezoelectric transducer drivers

Table 1: Device summary

Order code	Package	Packing
STHV749L	VFLGA-48LD	Tape and reel

Description

This monolithic, high-voltage, high-speed pulse generator features four independent channels. It is designed for medical ultrasound applications, but can also be used for driving other piezoelectric, capacitive, or MEMS transducers. The STHV749 is made up of a controller logic interface circuit (compatible with both 1.8 V and 3.3 V input signals), level translators, self-biased high-voltage MOSFET gate drivers, noise blocking diodes, three high power P-channel and three N-channel MOSFETs as the output stage for each channel (TX0, TX1 and CW), clamping-to-ground circuitry [RTZ], anti-leakage, anti-memory effect block, thermal sensor, and a T/R switch which guarantees effective decoupling during the transmission phase. Moreover, the STHV749 includes self-biasing and thermal shutdown blocks.

Each channel can support up to seven active output levels with two main half bridge and a half bridge dedicated for the CW waveforms. It is comprised of three independently supplied output stages, respectively: two TX0 and TX1 used for pulsed wave (PW), and one for continuous wave (CW) operation. TX0 and TX1 are able to provide up to ±2 A peak output current each, while to reduce power dissipation and jitter during continuous wave mode, the fully optimized CW output stage delivers up to ±0.3 A. The current capability for CW mode is also selectable to 0.6 A.

Each channel can be used with TX0 and TX1 in parallel obtaining up to ±4 A peak output current. This is to support short pulse waveforms and to increase the maximum output frequency. This option is selectable by a dedicated input pin (SEL).

The four independent T/R switches can be used in both a dedicated RX chain per-channel or in a multiplexing configuration.

The clamp circuit, used to carry the output pin XDCR down to GND, has a current capability in excess of 4 A.

The STHV749 internal self-biasing circuitry prevents the need to use dedicated external high voltage rails to drive all the gates of the TX0, TX1 and CW bridges. Moreover, it allows very low power consumption during the RX phase.

The STHV749 requires very few external components. The reference voltage supplies for the gate drivers of the TX0, TX1 and CW bridges do not require any dedicated external pins.

Each channel is independently controlled by means of 3 digital bits in the 5 levels option, and 2 bits in the 3 levels option. An external clock can be used to synchronize all the control input signals, allowing the optimization of both the jitter and the HD2 performance of the device. This feature is, however, optional: if the CK pin is tied to ground the device works in asynchronous mode.

The STHV749 is fully power-up and power-down sequence free.

1   Typical application circuit

Figure 1: STHV749 internal block diagram
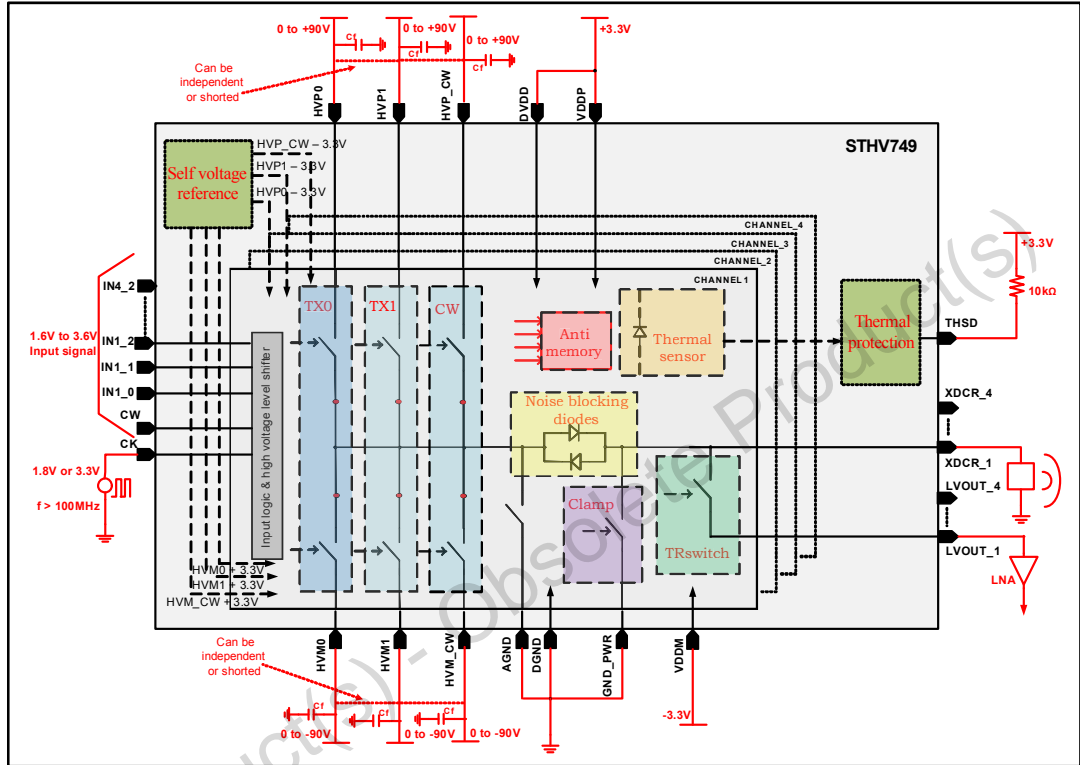
2   XDCR output waveforms

Figure 2: XDCR output in TRIPLEX mode from single channel - PWs and CW composition example
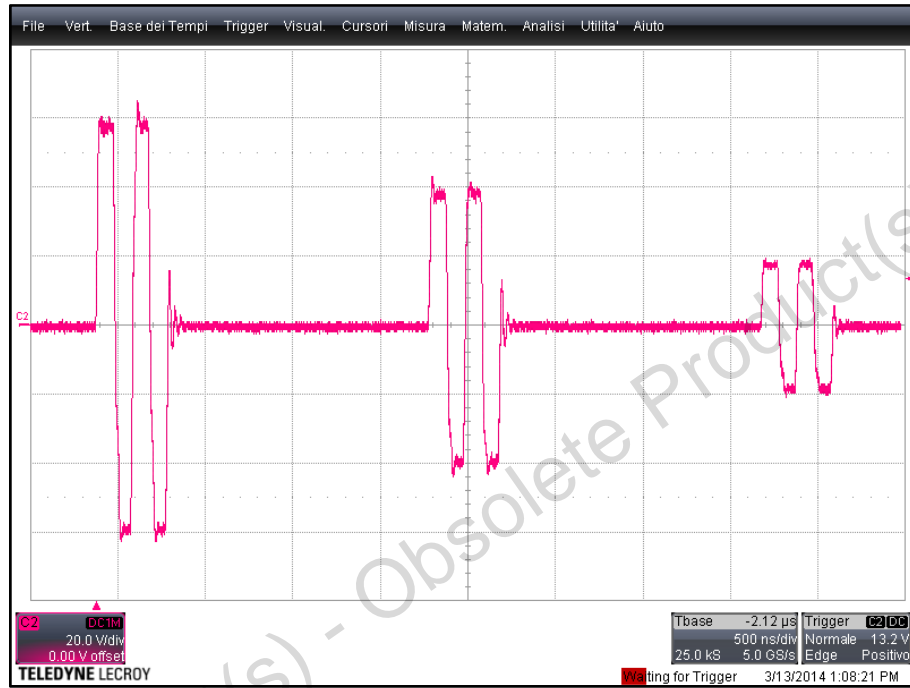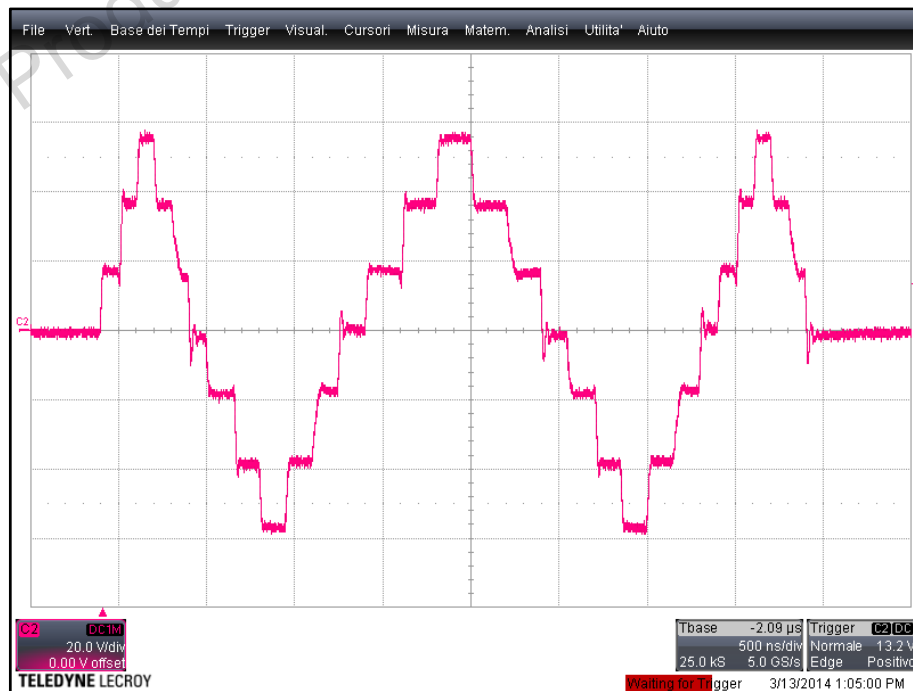

Figure 3: XDCR output sine-like waveform approximation example from single channel - 7 levels HV steps setting

3   Revision history

Table 2: Document revision history

Date	Revision	Changes
29-Apr-2014	1	Initial release.

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